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MX29VS128F

MULTIPLEXED, Burst Mode

Read While Write Flash Memory

Contents

1. FEATURES

Characteristics

Burst Length

- Burst Mode - Continuous linear
- Linear burst length - 8/16 word with wrap around

Sector Architecture

- Multi-bank Architecture (8 banks)
- Read while write operation
- Four 16 Kword sectors on top/ bottom of address range
- 127 sectors are 64 KWord sectors

Power Supply Operations

- 1.8V for read, program and erase operations (1.70V to 1.95V)
- Deep power down mode

Performance

High Performance

- 30 µs - Word programming time
- 7.5 µs - Effective word programming time utilizing a 32 word Write Buffer at VCC level
- 2.5 µs - Effective word programming time of utilizing a 32 word Write Buffer at ACC level

Sector Erase Time

- 500 ms for 16 Kword sectors
- 1000 ms for 64 Kword sectors

Read Access Time

- Burst access time: 7 ns (at industrial temperature range)
- Asynchronous random access time: 80 ns
- Synchronous random access time: 75 ns

Secure Silicon Sector Region

- 128 words for the factory & customer secure silicon sector

Power Dissipation

- Typical values: 8 bits switching,
  CL = 10 pF at 108 MHz, CIN excluded
- 20 mA for Continuous burst read mode
- 30 mA for Program/Erase Operations (max.)
- 30 uA for Standby mode

Program/Erase Cycles

- 100,000 cycles typical

Data Retention

- 20 years

Hardware Features

- Supports multiplexing data and address for reduced I/O count.
- A15–A0 multiplexed as Q15–Q0 Sector Architecture

Hardware Sector Protection

- All sectors locked when WP#/ACC = VIL

Package

- 56-Ball Thin FBGA (Fine-Pitch Ball Grid Array)
- All packaged devices are RoHS Compliant and Halogen-free.

Handshaking Feature

- Allows system to determine the read operation of burst data with minimum possible latency by monitoring RDY.

Software Features

Advanced Security Features

- Volatile Sector Protection
- A command sector protection method that protects individual sectors from being programmed or erased.
- Secured Silicon Sectors can be locked or in-system at VCC level.

Electronic Identification

- Software command set compatible with JEDEC 42.4 standards
- Common Flash Interface (CFI) supported

Erase Suspend/Erase Resume

- Erase operation will be halted when the bank receives an Erase Suspend command. And will be restarted when the bank receives the Erase Resume command.

Program Suspend/Program Resume

- Program operation will be halted when the bank receives a Program Suspend command. It will be restarted when the bank receives the Program Resume command.

Write Condition Bits

- Provides a software method of providing write condition bits to indicate the status of program and erase operations.

2. GENERAL INFORMATION

2-1. Operating Speeds

Clock Speed	Burst Access (ns)	Synch. Initial Access (ns)	Asynch. Initial Access (ns)	Output Loading
108 MHz	7	75	80	10 pF

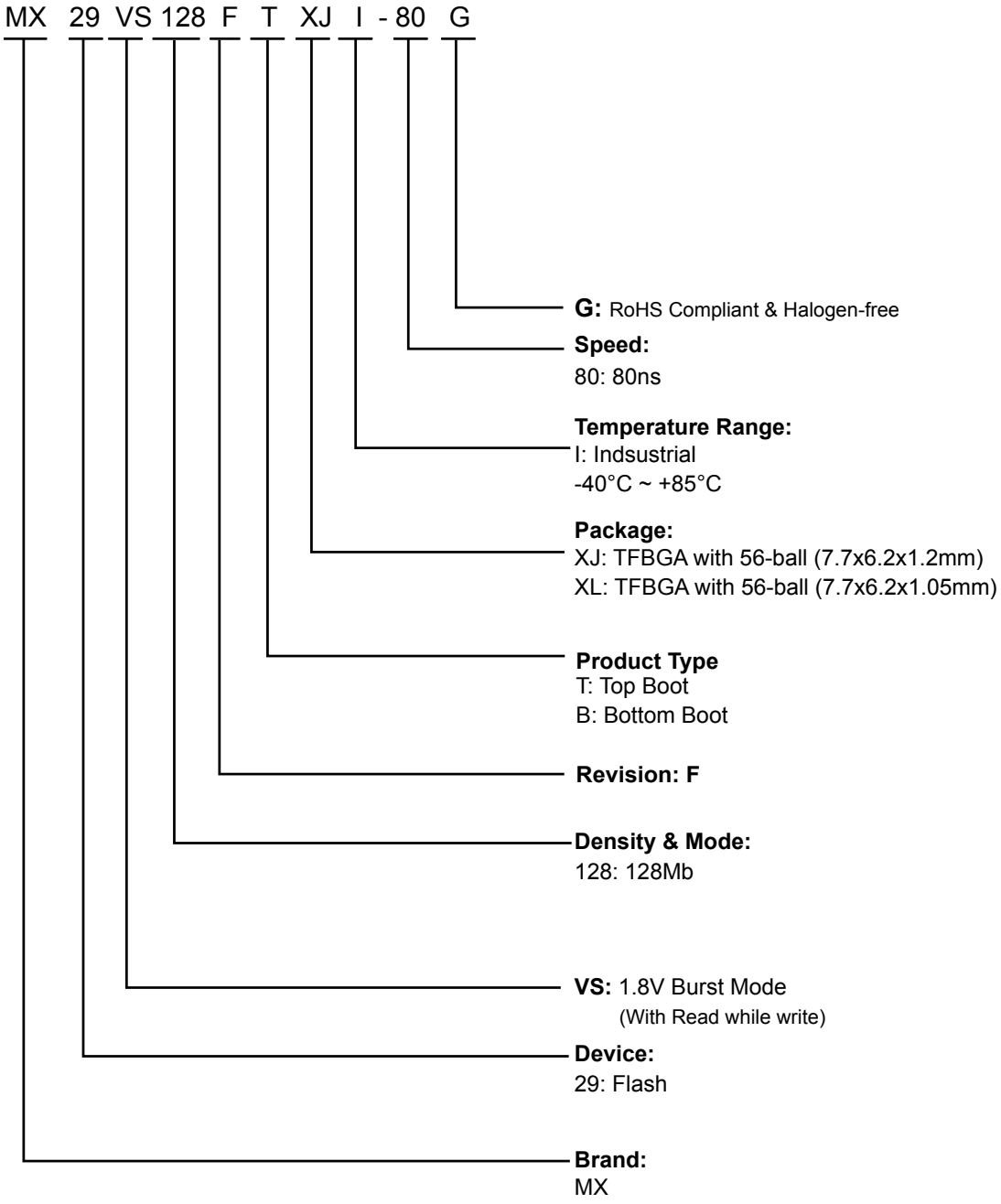
The operating temperature range is from -40°C to +85°C.

2-2. Ordering Information

Part Number	Access Time (ns)	Package	Remark
MX29VS128FTXJI-80G	80	56 TFBGA	VI/O=VCC
MX29VS128FBXJI-80G	80	56 TFBGA	VI/O=VCC
MX29VS128FTXLI-80G*	80	56 TFBGA	VI/O=VCC
MX29VS128FBXLI-80G*	80	56 TFBGA	VI/O=VCC

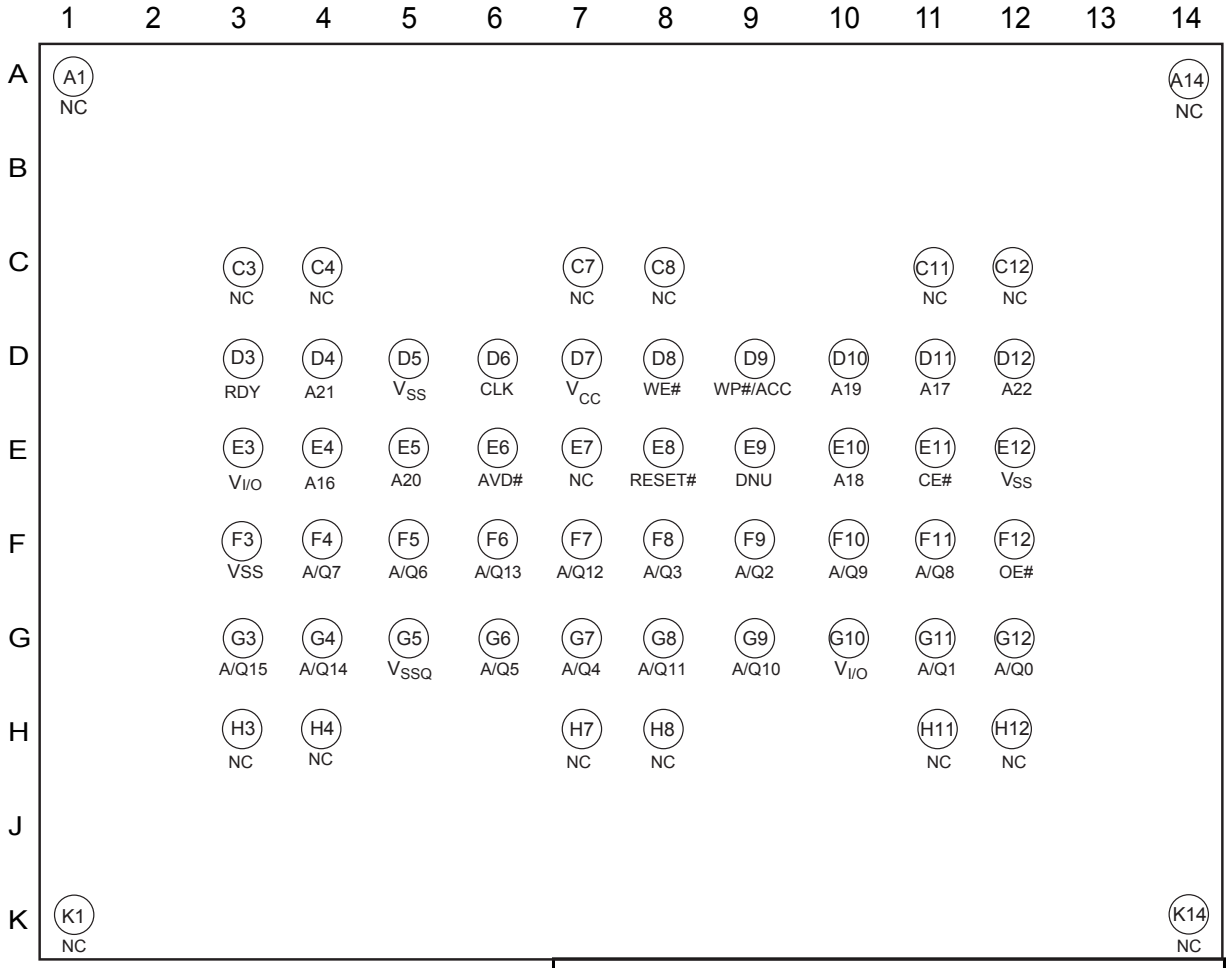
***NOTE**: * = Advanced Information*

2-3. Part Name Description

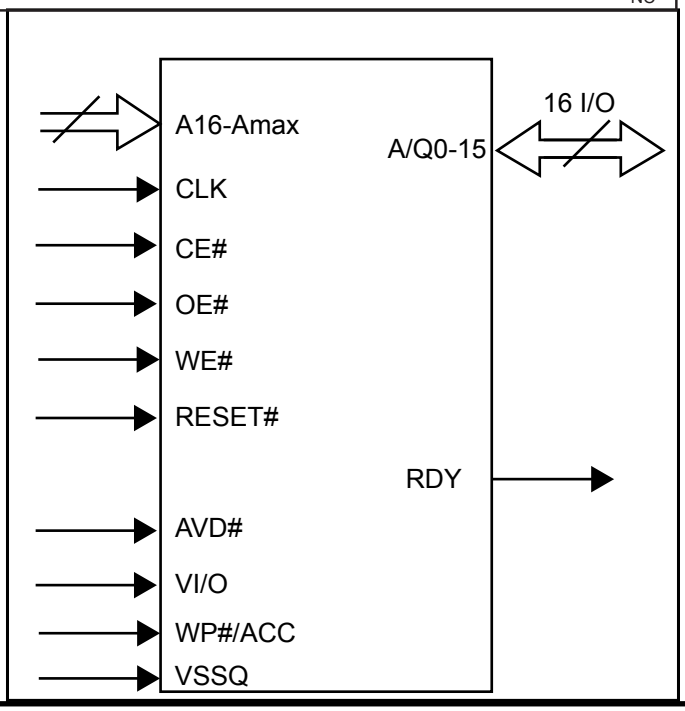


3. PIN CONFIGURATION / SYMBOL DESCRIPTION

56-Ball Thin FBGA



3-1. Logic Symbol



3-2. Pin Descriptions

SYMBOL	DESCRIPTIONS		
A22-A16	Input pins for Address		
A/Q15-A/Q0	Input pins for Address and Multiplex Input/Output pins for Data		
WP#/ACC	Write Protect/Input pin for Programming Acceleration		
AVD#	An Input pin for Address Valid, to indicate the following input are address information or data information. (A/Q15-A/Q0 are multiplex pins and A22-A16 are address pins only)		
	VIL	Asynchronous Mode	To indicate valid address
		Burst Mode	To latch starting address on rising edge of CLK
	VIH	Data will be inputted from A/Q15-A/Q0, A22-A16 will be ignored by device.	
CE#	Input pin for Chip Enable		
CLK	The first rising edge of CLK pin will start when both AVD# low latches address input and activates burst mode operation.		
NC	No Connection		
OE#	Input pin for Output Enable		
RESET#	Input pin for Hardware Reset, reset operation starts when voltage goes low.		
RDY	Output pin for Ready signal. For further information please refer to Configuration Register Table.		
VCC	Power Supply pin (1.70V-1.95V) for Device		
VI/O	Power Supply pin (1.70V-1.95V) for Input/Output		
WE#	Input pin for Write Enable		
VSS	Ground pin for Device		
VSSQ	Ground pin for Input/Output		
DNU	Do Not Use (DNU pin can be connected to VCC, Ground, Floating, but cannot connect to voltage > 1.5Vcc)		

***NOTES**:*

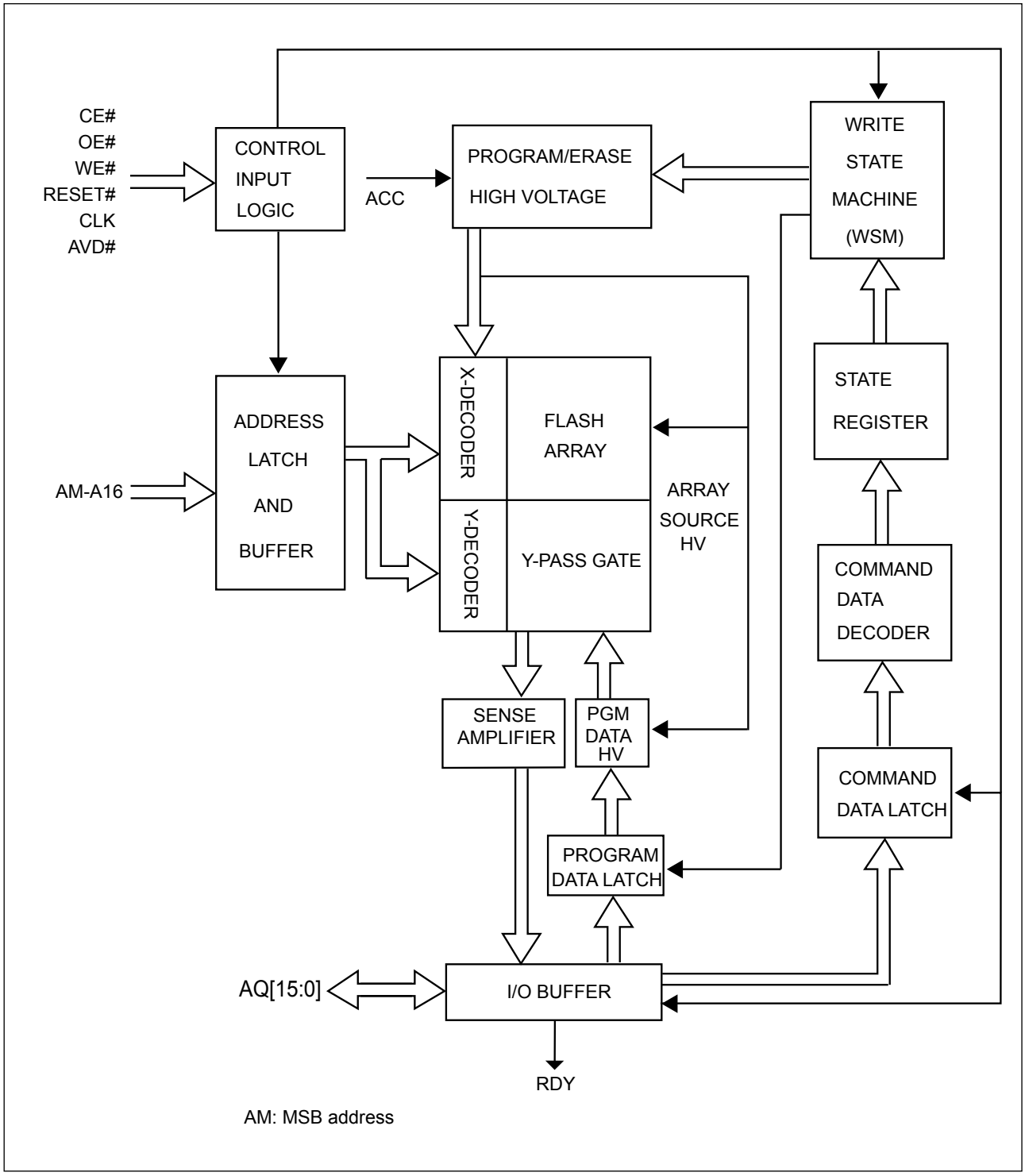
1. *WP#/ACC=Vhv enters into the ACC programming mode. WP#/ACC=VIL, erase/program function disabled.*

   WP#/ACC should keep VIH for all other cases. It must not be left floated or unconnected; inconsistent behavior of the device may result.

2. *VI/O Voltage must tight up with VCC.*

   VI/O = VCC = 1.70V to 1.95V

4. BLOCK DIAGRAM



4-1. Block & Address Structure

The main flash memory array is organized as Word mode (x16). The details of the address ranges and the corresponding sector addresses are shown in Table 1.

The device is consisted of five memory address areas as below:

- Main Flash Array area
- Secured Silicon Sector area
- Device ID & CFI area
- Configuration Register area
- SSS (Secured Silicon Sector) Lock Bit

To facilitate the data read flexibility, this device enables the "Address Mapping" feature that could have user to define the non-main array areas to be read as the main array area by mapping the address into the intended main array.

For address range being marked as mapping area but not defined will output invalid data.

Each bank can be operated in the following three modes:

- Normal Read Mode

- Program/Erase (PE) Mode

- Address Mapping (AM) Mode

First two modes can be operated in any bank, but AM mode can only be operated in bank0. In addition, at any time, only one bank is available to use the PE or AM mode.

- **Normal Read Mode:** The device will be in Normal Read Mode in following status: Hardware Reset, Power on, command reset, Exit from PE mode.
- **PE Mode:** The Program & Erase operation can be conducted in the bank, however, in the same bank, no read is allowed. Other non-PE-mode banks are available for Read operation at the same time. This is the "Read-While-Write" operation.
- **AM Mode:** One of the non-main-aray address is mapped in a bank. Only one bank may be in AM mode, all other banks may not be in AM or PE mode. Before entering AM mode, all P/E operation should be finished. The attempt of entering PE mode or AM mode when the other bank is in PE or AM mode will be ignored.

Simultaneous operation of one bank in AM mode, the other bank for Normal Read mode is allowed.

The AM mode can only be operated in lowest address bank. The mapping address of AM mode should be within the assigned lowest address bank address area.

- The Secured Silicon Sector, SSS Lock bit, and Configuration Register can be programmed in AM mode per the mapped address. During above operation, it switches from AM mode to PE mode. Device ID/ CFI is factory programming only.

Table 1-1. Sector Address Table (Top Boot)

Bank	Sector Size (Kwords)	Sector	Address Range
0	64	SA0	000000h-00FFFFh
	64	SA1	010000h-01FFFFh
	64	SA2	020000h-02FFFFh
	64	SA3	030000h-03FFFFh
	64	SA4	040000h-04FFFFh
	64	SA5	050000h-05FFFFh
	64	SA6	060000h-06FFFFh
	64	SA7	070000h-07FFFFh
	64	SA8	080000h-08FFFFh
	64	SA9	090000h-09FFFFh
	64	SA10	0A0000h-0AFFFFh
	64	SA11	0B0000h-0BFFFFh
	64	SA12	0C0000h-0CFFFFh
	64	SA13	0D0000h-0DFFFFh
	64	SA14	0E0000h-0EFFFFh
	64	SA15	0F0000h-0FFFFFh
1	64	SA16	100000h-10FFFFh
	64	SA17	110000h-11FFFFh
	64	SA18	120000h-12FFFFh
	64	SA19	130000h-13FFFFh
	64	SA20	140000h-14FFFFh
	64	SA21	150000h-15FFFFh
	64	SA22	160000h-16FFFFh
	64	SA23	170000h-17FFFFh
	64	SA24	180000h-18FFFFh
	64	SA25	190000h-19FFFFh
	64	SA26	1A0000h-1AFFFFh
	64	SA27	1B0000h-1BFFFFh
	64	SA28	1C0000h-1CFFFFh
	64	SA29	1D0000h-1DFFFFh
	64	SA30	1E0000h-1EFFFFh
	64	SA31	1F0000h-1FFFFFh
2	64	SA32	200000h-20FFFFh
	64	SA33	210000h-21FFFFh
	64	SA34	220000h-22FFFFh
	64	SA35	230000h-23FFFFh
	64	SA36	240000h-24FFFFh
	64	SA37	250000h-25FFFFh
	64	SA38	260000h-26FFFFh
	64	SA39	270000h-27FFFFh
	64	SA40	280000h-28FFFFh
	64	SA41	290000h-29FFFFh
2	64	SA42	2A0000h-2AFFFFh
	64	SA43	2B0000h-2BFFFFh
	64	SA44	2C0000h-2CFFFFh
	64	SA45	2D0000h-2DFFFFh
	64	SA46	2E0000h-2EFFFFh
	64	SA47	2F0000h-2FFFFFh
3	64	SA48	300000h-30FFFFh
	64	SA49	310000h-31FFFFh
	64	SA50	320000h-32FFFFh
	64	SA51	330000h-33FFFFh
	64	SA52	340000h-34FFFFh
	64	SA53	350000h-35FFFFh
	64	SA54	360000h-36FFFFh
	64	SA55	370000h-37FFFFh
	64	SA56	380000h-38FFFFh
	64	SA57	390000h-39FFFFh
	64	SA58	3A0000h-3AFFFFh
	64	SA59	3B0000h-3BFFFFh
	64	SA60	3C0000h-3CFFFFh
	64	SA61	3D0000h-3DFFFFh
	64	SA62	3E0000h-3EFFFFh
	64	SA63	3F0000h-3FFFFFh
4	64	SA64	400000h-40FFFFh
	64	SA65	410000h-41FFFFh
	64	SA66	420000h-42FFFFh
	64	SA67	430000h-43FFFFh
	64	SA68	440000h-44FFFFh
	64	SA69	450000h-45FFFFh
	64	SA70	460000h-46FFFFh
	64	SA71	470000h-47FFFFh
	64	SA72	480000h-48FFFFh
	64	SA73	490000h-49FFFFh
	64	SA74	4A0000h-4AFFFFh
	64	SA75	4B0000h-4BFFFFh
	64	SA76	4C0000h-4CFFFFh
	64	SA77	4D0000h-4DFFFFh
	64	SA78	4E0000h-4EFFFFh
	64	SA79	4F0000h-4FFFFFh
5	64	SA80	500000h-50FFFFh
	64	SA81	510000h-51FFFFh
	64	SA82	520000h-52FFFFh
	64	SA83	530000h-53FFFFh
	64	SA84	540000h-54FFFFh

Bank	Sector Size Kwords	Sector	Address Range
5	64	SA85	550000h-55FFFFh
	64	SA86	560000h-56FFFFh
	64	SA87	570000h-57FFFFh
	64	SA88	580000h-58FFFFh
	64	SA89	590000h-59FFFFh
	64	SA90	5A0000h-5AFFFFh
	64	SA91	5B0000h-5BFFFFh
	64	SA92	5C0000h-5CFFFFh
	64	SA93	5D0000h-5DFFFFh
	64	SA94	5E0000h-5EFFFFh
	64	SA95	5F0000h-5FFFFFh
6	64	SA96	600000h-60FFFFh
	64	SA97	610000h-61FFFFh
	64	SA98	620000h-62FFFFh
	64	SA99	630000h-63FFFFh
	64	SA100	640000h-64FFFFh
	64	SA101	650000h-65FFFFh
	64	SA102	660000h-66FFFFh
	64	SA103	670000h-67FFFFh
	64	SA104	680000h-68FFFFh
	64	SA105	690000h-69FFFFh
	64	SA106	6A0000h-6AFFFFh
	64	SA107	6B0000h-6BFFFFh
	64	SA108	6C0000h-6CFFFFh
	64	SA109	6D0000h-6DFFFFh
	64	SA110	6E0000h-6EFFFFh
	64	SA111	6F0000h-6FFFFFh
7	64	SA112	700000h-70FFFFh
	64	SA113	710000h-71FFFFh
	64	SA114	720000h-72FFFFh
	64	SA115	730000h-73FFFFh
	64	SA116	740000h-74FFFFh
	64	SA117	750000h-75FFFFh
	64	SA118	760000h-76FFFFh
	64	SA119	770000h-77FFFFh
	64	SA120	780000h-78FFFFh
	64	SA121	790000h-79FFFFh
	64	SA122	7A0000h-7AFFFFh
	64	SA123	7B0000h-7BFFFFh
	64	SA124	7C0000h-7CFFFFh
	64	SA125	7D0000h-7DFFFFh
	64	SA126	7E0000h-7EFFFFh
	16	SA127	7F0000h-7F3FFFh
	16	SA128	7F4000h-7F7FFFh
	16	SA129	7F8000h-7FBFFFh
	16	SA130	7FC000h-7FFFFFh

Table 1-2. Sector Address Table (Bottom Boot)

Bank	Sector Size (Kwords)	Sector	Address Range
0	16	SA0	000000h-003FFFh
	16	SA1	004000h-007FFFh
	16	SA2	008000H-00BFFFh
	16	SA3	00C000h-00FFFFh
	64	SA4	010000h-01FFFFh
	64	SA5	020000h-02FFFFh
	64	SA6	030000h-03FFFFh
	64	SA7	040000h-04FFFFh
	64	SA8	050000h-05FFFFh
	64	SA9	060000h-06FFFFh
	64	SA10	070000h-07FFFFh
	64	SA11	080000h-08FFFFh
	64	SA12	090000h-09FFFFh
	64	SA13	0A0000h-0AFFFFh
	64	SA14	0B0000h-0BFFFFh
	64	SA15	0C0000h-0CFFFFh
	64	SA16	0D0000h-0DFFFFh
	64	SA17	0E0000h-0EFFFFh
	64	SA18	0F0000h-0FFFFFh
1	64	SA19	100000h-10FFFFh
	64	SA20	110000h-11FFFFh
	64	SA21	120000h-12FFFFh
	64	SA22	130000h-13FFFFh
	64	SA23	140000h-14FFFFh
	64	SA24	150000h-15FFFFh
	64	SA25	160000h-16FFFFh
	64	SA26	170000h-17FFFFh
	64	SA27	180000h-18FFFFh
	64	SA28	190000h-19FFFFh
	64	SA29	1A0000h-1AFFFFh
	64	SA30	1B0000h-1BFFFFh
	64	SA31	1C0000h-1CFFFFh
	64	SA32	1D0000h-1DFFFFh
	64	SA33	1E0000h-1EFFFFh
	64	SA34	1F0000h-1FFFFFh
2	64	SA35	200000h-20FFFFh
	64	SA36	210000h-21FFFFh
	64	SA37	220000h-22FFFFh
	64	SA38	230000h-23FFFFh
	64	SA39	240000h-24FFFFh
	64	SA40	250000h-25FFFFh
	64	SA41	260000h-26FFFFh
	64	SA42	270000h-27FFFFh
	64	SA43	280000h-28FFFFh
	64	SA44	290000h-29FFFFh
	64	SA45	2A0000h-2AFFFFh
2	64	SA46	2B0000h-2BFFFFh
	64	SA47	2C0000h-2CFFFFh
	64	SA48	2D0000h-2DFFFFh
	64	SA49	2E0000h-2EFFFFh
	64	SA50	2F0000h-2FFFFFh
3	64	SA51	300000h-30FFFFh
	64	SA52	310000h-31FFFFh
	64	SA53	320000h-32FFFFh
	64	SA54	330000h-33FFFFh
	64	SA55	340000h-34FFFFh
	64	SA56	350000h-35FFFFh
	64	SA57	360000h-36FFFFh
	64	SA58	370000h-37FFFFh
	64	SA59	380000h-38FFFFh
	64	SA60	390000h-39FFFFh
	64	SA61	3A0000h-3AFFFFh
	64	SA62	3B0000h-3BFFFFh
	64	SA63	3C0000h-3CFFFFh
	64	SA64	3D0000h-3DFFFFh
	64	SA65	3E0000h-3EFFFFh
	64	SA66	3F0000h-3FFFFFh
4	64	SA67	400000h-40FFFFh
	64	SA68	410000h-41FFFFh
	64	SA69	420000h-42FFFFh
	64	SA70	430000h-43FFFFh
	64	SA71	440000h-44FFFFh
	64	SA72	450000h-45FFFFh
	64	SA73	460000h-46FFFFh
	64	SA74	470000h-47FFFFh
	64	SA75	480000h-48FFFFh
	64	SA76	490000h-49FFFFh
	64	SA77	4A0000h-4AFFFFh
	64	SA78	4B0000h-4BFFFFh
	64	SA79	4C0000h-4CFFFFh
	64	SA80	4D0000h-4DFFFFh
	64	SA81	4E0000h-4EFFFFh
	64	SA82	4F0000h-4FFFFFh
5	64	SA83	500000h-50FFFFh
	64	SA84	510000h-51FFFFh
	64	SA85	520000h-52FFFFh
	64	SA86	530000h-53FFFFh
	64	SA87	540000h-54FFFFh
	64	SA88	550000h-55FFFFh

Bank	Sector Size Kwords	Sector	Address Range
5	64	SA89	560000h-56FFFFh
	64	SA90	570000h-57FFFFh
	64	SA91	580000h-58FFFFh
	64	SA92	590000h-59FFFFh
	64	SA93	5A0000h-5AFFFFh
	64	SA94	5B0000h-5BFFFFh
	64	SA95	5C0000h-5CFFFFh
	64	SA96	5D0000h-5DFFFFh
	64	SA97	5E0000h-5EFFFFh
	64	SA98	5F0000h-5FFFFFh
6	64	SA99	600000h-60FFFFh
	64	SA100	610000h-61FFFFh
	64	SA101	620000h-62FFFFh
	64	SA102	630000h-63FFFFh
	64	SA103	640000h-64FFFFh
	64	SA104	650000h-65FFFFh
	64	SA105	660000h-66FFFFh
	64	SA106	670000h-67FFFFh
	64	SA107	680000h-68FFFFh
	64	SA108	690000h-69FFFFh
	64	SA109	6A0000h-6AFFFFh
	64	SA110	6B0000h-6BFFFFh
	64	SA111	6C0000h-6CFFFFh
	64	SA112	6D0000h-6DFFFFh
	64	SA113	6E0000h-6EFFFFh
	64	SA114	6F0000h-6FFFFFh
7	64	SA115	700000h-70FFFFh
	64	SA116	710000h-71FFFFh
	64	SA117	720000h-72FFFFh
	64	SA118	730000h-73FFFFh
	64	SA119	740000h-74FFFFh
	64	SA120	750000h-75FFFFh
	64	SA121	760000h-76FFFFh
	64	SA122	770000h-77FFFFh
	64	SA123	780000h-78FFFFh
	64	SA124	790000h-79FFFFh
	64	SA125	7A0000h-7AFFFFh
	64	SA126	7B0000h-7BFFFFh
	64	SA127	7C0000h-7CFFFFh
	64	SA128	7D0000h-7DFFFFh
	64	SA129	7E0000h-7EFFFFh
	64	SA130	7F0000h-7FFFFFh

5. BUS OPERATIONS

This chapter indicates the functions and utilizations of Bus Operations. Bus operations are started by the internal command register and executed by a bus interface or similar logic circuitry. The Command register does not occupy any memory addresses. It is stored in the format of latches and independent to the address and data information when executing the command.

The contents of the register acts as it is input to internal state machine. In addition, the state machine outputs determine the function of the device.

Table 2. shows all inputs, control level requirement, and resulting output for all the bus operations. Please read it for further information.

***NOTE**: Falling edge of AVD# determines when to disable the current burst cycle while a new burst read cycle is started by the rising edge of CLK.*

Table 2. Bus Operations

Operation	CE#	OE#	WE#	CLK	AVD#	Address	Data	RESET#
Synchronous Operations								
Latch Starting Burst Address by CLK	L	H	H	R	L	Addr In	Addr In	H
Advance Burst Read to Next Address	L	L	H	R	H	X	Output Valid	H
Terminate Current Burst Read Cycle	H	X	X	X	X	X	HighZ	H
Terminate Current Burst Read Cycle through RESET#	X	X	X	X	X	X	HighZ	L
Asynchronous Operations								
Asynchronous Read - Addresses Latched	L	H	H	L	R	Addr In	Addr In	H
Asynchronous Read - Data on Bus	L	L	H	L	H	X	Output Data	H
Asynchronous Program (AVD# Latched Addresses)	L	H	X	L	R	Addr In	Addr In	H
Asynchronous Program (WE# Latched Data)	L	H	R	L	H	X	Input Valid	H
Non-Operations								
Standby (CE#)	H	X	X	X	X	X	HighZ	H
Hardware Reset	X	X	X	X	X	X	HighZ	L

Legend:

L = 0; H = 1; X = VIL or VIH; R = Rising edge; h-l = High to low.

NOTES:

1. *WP#/ACC low protects all sectors.*
2. *A/Q0~A/Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection.*
3. *In Word Mode, the addresses are AM to A0, AM: MSB of address.*

5-1. Status Register

Bits in Status Register can offer users to identify the state in device right now. For more details, please see the following tables:

Table 3-1.Status Register

Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Device Ready	Erase Suspend	Erase Status	Program Status	RFU	Program Suspend	Sector Protect	Bank Status
Device Ready	1	0: Default	0: Default	0: Default	DC	0: Default	0: Default	0: Default
Device Busy	0	DC	DC	DC	DC	DC	DC	0: Busy in this bank
Device Busy	0	DC	DC	DC	DC	DC	DC	1: Busy in other bank
Invalid	1	DC	DC	DC	DC	DC	DC	1

NOTES:

1. *DC=Don't Care*
2. *Bit 0 will show which bank is busy if and only if Bit 7 is 0. Otherwise, Bit 0 can only become 0.*
3. *Bit 3 is RFU*

Table 3-2.Status Register - Erase Suspend

Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Device Ready	Erase Suspend	Erase Status	Program Status	RFU	Program Suspend	Sector Protect	Bank Status
No Sector in Erase Suspend	1	0	DC	DC	DC	DC	DC	DC
One sector in Erase Suspend	1	1	DC	DC	DC	DC	DC	DC

NOTES:

1. *DC=Don't Care*
2. *After issuing Erase Suspend command, user should check Bit 7 to make sure the value is 1 before accessing other sectors in the same bank.*
3. *Bit 3 is RFU*

Table 3-3.Status Register - Erase Status

Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Device Ready	Erase Suspend	Erase Status	Program Status	RFU	Program Suspend	Sector Protect	Bank Status
Erase Success	1	DC	0	DC	DC	DC	DC	DC
Erase Fail	1	DC	1	DC	DC	DC	DC	DC

NOTES:

1. DC=Don't Care

2. Bit 5 will show the erase status of last erase operation. User may input "Clear Status Register" or "Hardware Reset" to return to the default value.

3. Bit 3 is RFU

Table 3-4.Status Register - Program Status

Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Device Ready	Erase Suspend	Erase Status	Program Status	RFU	Program Suspend	Sector Protect	Bank Status
Program Success	1	DC	DC	0	DC	DC	DC	DC
Program Fail	1	DC	DC	1	DC	DC	DC	DC

NOTES:

1. DC=Don't Care

2. Bit 4 will show the program status of last program operation. User may input "Clear Status Register" or "Hardware Reset" to return to the default value.

3. Bit 3 is RFU

Table 3-5.Status Register - Program Suspend

Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Device Ready	Erase Suspend	Erase Status	Program Status	RFU	Program Suspend	Sector Protect	Bank Status
No Sector in Program Suspend	1	DC	DC	DC	DC	0	DC	DC
One Sector in Program Suspend	1	DC	DC	DC	DC	1	DC	DC

NOTES:

1. DC=Don't Care

2. After issuing Program Suspend command, user should check Bit 7 to make sure the value is 1 before accessing other sectors in the same bank.

3. Bit 3 is RFU

Table 3-6.Status Register - Protect Status

Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Device Ready	Erase Suspend	Erase Status	Program Status	RFU	Program Suspend	Sector Protect	Bank Status
Unprotected Sector during Operation	1	DC	DC	DC	DC	DC	0	DC
Protected Sector during Operation	1	DC	DC	DC	DC	DC	1	DC

NOTES:

1. *DC=Don't Care*
2. *If last operation is failed due to the sector is protected Bit 1 will become 1. User may input "Clear Status Register" or "Hardware Reset" to return to the default value.*
3. *Bit 3 is RFU.*

5-2. Blank Check

Users can use Blank Check command to confirm the selected sector is erased.

It is not allowed for users to read the array while the Blank Check command is being executed in the same array. This will return unknown data.

Blank Check command is only valid in Asynchronous Read mode, which means the Configuration Register Bit 15(CR [15]) is 1. This command may not conduct if the device is in operations.

The operation process of Blank Check command is as follows: Command will be issued (Address 555h and Data 33h) on Sector X, while the device is in the Idle State (neither during program suspend nor erase suspend operations.) After the operation is completed, the device will return to the Idle State.

User may use the Read Status Register to confirm if the device is still busy and when compete if the sector is blank or not. Bit 5 in the Status Register will be zero if the sector is erased and will become one if it is not erased. In addition, Bit 7 & Bit 0 in the Status Register will show if the device is performing a Blank Check. The device will halt the operation and report the results immediately, if any bit is found has not been erased.

5-3. Non-Burst (Asynchronous) Read Operation

Upon device's power-up, non-burst mode read is as the default state. To perform a read operation, the system addresses the desired memory array or status register location by providing its address on the address pins and simultaneously enabling the chip by driving AVD# & CE# LOW, and WE# HIGH. The CLK keeps low during asynchronous read operation. The address is latched on the rising edge of AVD#; OE# will be driven low afterwards. A/Q15-A/Q0 output the data after previous operations is complete.

5-4. Burst (Synchronous) Read Operation

The device supports the following burst read modes:

- Burst Mode - Continuous linear

- Linear burst mode - 8/16 word with wrap around

5-4-1. Burst Mode - Continuous Linear

Burst read mode is enabled when configuration register bit 15 is set to 0.

The number of dummy cycles should be set (for tIACC for each burst session) before the clock signal is being activated. Before the burst read mode is activated, the number of dummy cycle will be determined by the setting configuration register command. See Configuration Register Chapter for details.

The process of the continuous burst read operation is as follows:

The rising edge of a CLK cycle while AVD# = VIL--> Initial word output tIACC --> Wait for dummy cycle --> Rising edge of each consecutive clock, following words output (tBACC) (Automatically increase the internal address counter)

1. For address boundary every 128 words, the first boundary starts with 00007Fh, next with 0000FFh by adding 128 words address; and etc.
2. Additional dummy cycles are needed if the start address for the output cannot be divided by 8.

   RDY status indicates the condition of the device by de-asserting.

There is a permanent internal address boundary in the device that occurs every 128 words. 1 or 2 dummy cycles are required while crossing boundary. Additional dummy cycles needed when starting burst address cannot be divided by 8.

Table 4-1. Address Latency for 10-13 Dummy Cycles

(+2dc only occures when crossing 128 words boundary)

Dummy Cycles	Word	Subsequent Clock Cycles After Initial Dummy Cycles									
10-13 Dummy Cycles	0	D0	D1	D2	D3	D4	D5	D6	D7	+2dc	D8
	1	D1	D2	D3	D4	D5	D6	D7	1dc	+2dc	D8
	2	D2	D3	D4	D5	D6	D7	1dc	1dc	+2dc	D8
	3	D3	D4	D5	D6	D7	1dc	1dc	1dc	+2dc	D8
	4	D4	D5	D6	D7	1dc	1dc	1dc	1dc	+2dc	D8
	5	D5	D6	D7	1dc	1dc	1dc	1dc	1dc	+2dc	D8
	6	D6	D7	1dc	1dc	1dc	1dc	1dc	1dc	+2dc	D8
	7	D7	1dc	1dc	1dc	1dc	1dc	1dc	1dc	+2dc	D8

Table 4-2. Address Latency for 9 Dummy Cycles

(+1dc only occures when crossing 128 words boundary)

Dummy Cycles	Word	Subsequent Clock Cycles After Initial Dummy Cycles									
9 Dummy Cycles	0	D0	D1	D2	D3	D4	D5	D6	D7	+1dc	D8
	1	D1	D2	D3	D4	D5	D6	D7	1dc	+1dc	D8
	2	D2	D3	D4	D5	D6	D7	1dc	1dc	+1dc	D8
	3	D3	D4	D5	D6	D7	1dc	1dc	1dc	+1dc	D8
	4	D4	D5	D6	D7	1dc	1dc	1dc	1dc	+1dc	D8
	5	D5	D6	D7	1dc	1dc	1dc	1dc	1dc	+1dc	D8
	6	D6	D7	1dc	1dc	1dc	1dc	1dc	1dc	+1dc	D8
	7	D7	1dc	1dc	1dc	1dc	1dc	1dc	1dc	+1dc	D8

Table 4-3. Address Latency for 8 Dummy Cycles

Dummy Cycles	Word	Subsequent Clock Cycles After Initial Dummy Cycles								
8 Dummy Cycles	0	D0	D1	D2	D3	D4	D5	D6	D7	D8
	1	D1	D2	D3	D4	D5	D6	D7	1dc	D8
	2	D2	D3	D4	D5	D6	D7	1dc	1dc	D8
	3	D3	D4	D5	D6	D7	1dc	1dc	1dc	D8
	4	D4	D5	D6	D7	1dc	1dc	1dc	1dc	D8
	5	D5	D6	D7	1dc	1dc	1dc	1dc	1dc	D8
	6	D6	D7	1dc	1dc	1dc	1dc	1dc	1dc	D8
	7	D7	1dc	1dc	1dc	1dc	1dc	1dc	1dc	D8

Table 4-4. Address Latency for 7 Dummy Cycles

Dummy Cycles	Word	Subsequent Clock Cycles After Initial Dummy Cycles								
7 Dummy Cycles	0	D0	D1	D2	D3	D4	D5	D6	D7	D8
	1	D1	D2	D3	D4	D5	D6	D7	D8	D9
	2	D2	D3	D4	D5	D6	D7	1dc	D8	D9
	3	D3	D4	D5	D6	D7	1dc	1dc	D8	D9
	4	D4	D5	D6	D7	1dc	1dc	1dc	D8	D9
	5	D5	D6	D7	1dc	1dc	1dc	1dc	D8	D9
	6	D6	D7	1dc	1dc	1dc	1dc	1dc	D8	D9
	7	D7	1dc	1dc	1dc	1dc	1dc	1dc	D8	D9

Table 4-5. Address Latency for 6 Dummy Cycles

Dummy Cycles	Word	Subsequent Clock Cycles After Initial Dummy Cycles								
6 Dummy Cycles	0	D0	D1	D2	D3	D4	D5	D6	D7	D8
	1	D1	D2	D3	D4	D5	D6	D7	D8	D9
	2	D2	D3	D4	D5	D6	D7	D8	D9	D10
	3	D3	D4	D5	D6	D7	1dc	D8	D9	D10
	4	D4	D5	D6	D7	1dc	1dc	D8	D9	D10
	5	D5	D6	D7	1dc	1dc	1dc	D8	D9	D10
	6	D6	D7	1dc	1dc	1dc	1dc	D8	D9	D10
	7	D7	1dc	1dc	1dc	1dc	1dc	D8	D9	D10

Table 4-6. Address Latency for 5 Dummy Cycles

Dummy Cycles	Word	Subsequent Clock Cycles After Initial Dummy Cycles								
5 Dummy Cycles	0	D0	D1	D2	D3	D4	D5	D6	D7	D8
	1	D1	D2	D3	D4	D5	D6	D7	D8	D9
	2	D2	D3	D4	D5	D6	D7	D8	D9	D10
	3	D3	D4	D5	D6	D7	D8	D9	D10	D11
	4	D4	D5	D6	D7	1dc	D8	D9	D10	D11
	5	D5	D6	D7	1dc	1dc	D8	D9	D10	D11
	6	D6	D7	1dc	1dc	1dc	D8	D9	D10	D11
	7	D7	1dc	1dc	1dc	1dc	D8	D9	D10	D11

Table 4-7. Address Latency for 4 Dummy Cycles

Dummy Cycles	Word	Subsequent Clock Cycles After Initial Dummy Cycles								
4 Dummy Cycles	0	D0	D1	D2	D3	D4	D5	D6	D7	D8
	1	D1	D2	D3	D4	D5	D6	D7	D8	D9
	2	D2	D3	D4	D5	D6	D7	D8	D9	D10
	3	D3	D4	D5	D6	D7	D8	D9	D10	D11
	4	D4	D5	D6	D7	D8	D9	D10	D11	D12
	5	D5	D6	D7	1dc	D8	D9	D10	D11	D12
	6	D6	D7	1dc	1dc	D8	D9	D10	D11	D12
	7	D7	1dc	1dc	1dc	D8	D9	D10	D11	D12

Table 4-8. Address Latency for 3 Dummy Cycles

Dummy Cycles	Word	Subsequent Clock Cycles After Initial Dummy Cycles								
3 Dummy Cycles	0	D0	D1	D2	D3	D4	D5	D6	D7	D8
	1	D1	D2	D3	D4	D5	D6	D7	D8	D9
	2	D2	D3	D4	D5	D6	D7	D8	D9	D10
	3	D3	D4	D5	D6	D7	D8	D9	D10	D11
	4	D4	D5	D6	D7	D8	D9	D10	D11	D12
	5	D5	D6	D7	D8	D9	D10	D11	D12	D13
	6	D6	D7	1dc	D8	D9	D10	D11	D12	D13
	7	D7	1dc	1dc	D8	D9	D10	D11	D12	D13

5-4-2. Linear Burst Mode - 8/16 Word with Wrap Around

Fixed amount of data (8 or 16 words) is output from continuous address for the linear wrap around mode. (in the unit of words). The origin burst read address is decided by the group where the origin address falls. The definition of groups is as illustrated in **Table 5** below.

If the system is in 16-Word Mode, the Subsequent Clock Cycles are needed. The detailed number of Subsequent Clock Cycles please see the table above. There is no need to have Subsequent Clock Cycles in 8-Word Mode.

8-, 16-Word Modes will be determined by the setting configuration register command. See **Configuration Register** Chapter for details.

Table 5. Burst Address Groups

Mode	Word Group Size	Word Group Address Ranges
8-Word Mode	8 words per group	0-7h, 8-Fh, 10-17,…
16-Word Mode	16 words per group	0-Fh, 10-1Fh, 20-2Fh,…

5-4-3. Reading Memory Array

Read mode is the default state after a power-up or a reset operation.

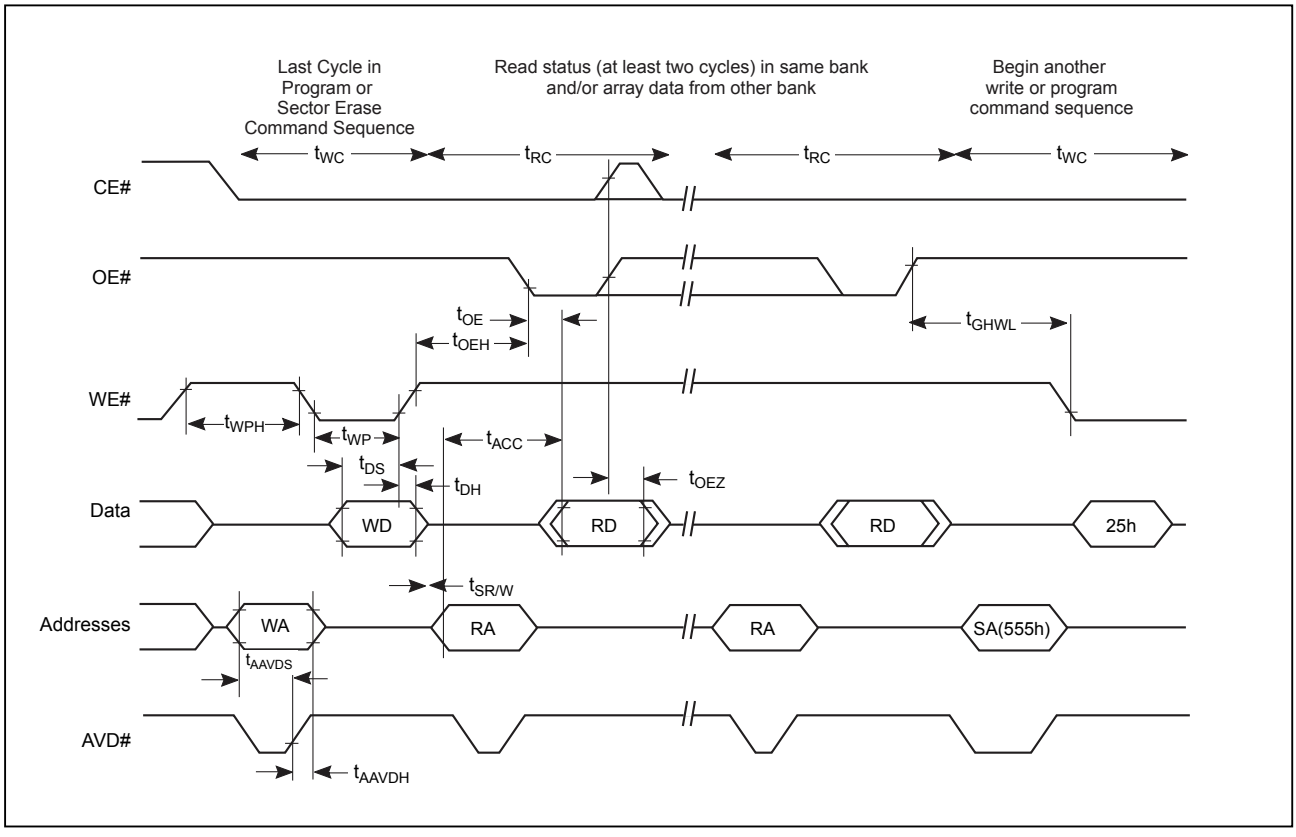
An erase operation will be paused (after a time delay less than tESL) and the bank will enter Erase-Suspended Read mode if the bank receives an Erase Suspend command while in the Sector Erase state. While in the Erase-Suspended Read mode, data can be programmed or read from any sector which is not being erased. Reading from addresses within sector (s) being erased is invalid.

If a program command is issued to any inactive (not currently being erased) sector during Erase-Suspended Read mode, the bank will perform the program operation and automatically return to Erase-Suspended Read mode after the program operation completes successfully.

While in Erase-Suspended Read mode, an Erase Resume command must be issued by the system to reactivate the erase operation. The erase operation will resume from where it was suspended and will continue the operation until it completely finishes or another Erase Suspend command is received.

After the memory bank completes an embedded operation (Chip Erase, Sector Erase, or Program) successfully, it will automatically return to idle state. If the embedded operation fails to complete, Bit 5 (Erase fail) or Bit 4(Program fail) in Status Register will become 1. The system may perform a "Clear Status Register" operation before the next operation.

Figure 1. Back-to-Back Read/Write Cycle Timings



NOTE:

Breakpoints in waveforms indicate that system may alternately read array data from the non-busy bank while checking the status of the program or erase operation in the busy bank. The system should read status twice to ensure valid information.

5-5. Program Operation

The program operation is combined by two parts,"Program to Buffer" and "Program Buffer to Flash". For further operation detail, please refer to 5-5-1. Write Buffer Programming Operation.

After the program command sequence has been executed, the internal write state machine (WSM) automatically executes the algorithms and timings necessary for programming and verification, which includes generating suitable program pulses, checking cell threshold voltage margins, and repeating the program pulse if any cells do not pass verification or have low margins. The internal controller protects cells that do pass verification and margin tests from being over-programmed by inhibiting further program pulses to these passing cells as weaker cells continue to be programmed.

With the internal WSM automatically controlling the programming process, users only need to enter the program command and data once.

Programming will only change the bit status from "1" to "0". It is not possible to change the bit status from "0" to "1" by programming. This can only be done with an erase operation. Furthermore, the internal write verification only checks and detects errors in cases where a "1" is not successfully programmed to "0".

Any commands written to the bank during programming will be ignored except, Read Status Register, hardware reset or program suspend. Hardware reset will terminate the program operation after a period of time not more than tPSL. When the program is complete or the program operation is terminated by a hardware reset, the bank will return to idle state. When program suspend is ready, the bank will enter program suspend read mode.

After the embedded program operation has begun, users can check for completion by reading the following bits in the status register table (Please refer to **Section 5-1. Status Register, Table 3-1 and 3-4).**