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MX30LF1G08AA

1G-bit NAND Flash Memory

Contents

1G-bit (128 M x 8 bit) NAND Flash Memory

1. FEATURES

- **1 Gbit SLC NAND Flash**
  - 128 M x 8 bit
  - 64 K pages of (2,048+64) bytes each
  - 1K blocks of 64 pages each
- **Multiplexed Command/Address/Data**
- **4 MByte User Redundancy**
  - 64 bytes attached to each page
- **Fast Read Access**
  - First-byte latency: 25us
  - Sequential read: 30ns/byte
- **Cache Read Support**
- **Page Program Operation**
- **Cache Program**
  - Internal cache of (2,048+64) bytes
- **Program Time:** Page program 250us (typ.)
- **Single Voltage Operation:** 3.3V
- **Low Power Dissipation** - Max. 30mA active current (RD/PGM/ERS)
- **Automatic Sleep Mode**
  - 50uA (Max) standby current
- **Block Erase Architecture**
  - Block size: (128K+4K) bytes per block
  - 1K blocks, 64 pages each
  - Block Erase Time: 2ms (Typ.)
- **Hardware Data Protection:** WP# pin
- **Multiple Device Status Indicators**
  - Ready/Busy (R/B#) pin
  - Status Register
- **Chip Enable Don't Care**
  - Simplify System Interface
- **Status Register**
- **Electronic Signature (Four Cycles)**
- **High Reliability**
  - Endurance: 100K cycles (with 1-bit ECC per 528-byte)
  - Data Retention: 10 years
- **Wide Temperature Operating Range:**
  -40°C to +85°C
- **Package:**
  - 48-TSOP(I) (12mm x 20mm),
  - 63-ball 9mmx11mm VFBGA
  - All packaged devices are RoHS Compliant & Halogen-free.

2. GENERAL DESCRIPTIONS

The MX30LF1G08AA is a 1Gb SLC NAND Flash memory device. Its standard NAND Flash features and reliable quality make it most suitable for embedded system code and data storage usage.

The MX30LF1G08AA is typically accessed in pages of 2,112 bytes, both for read and for program operations.

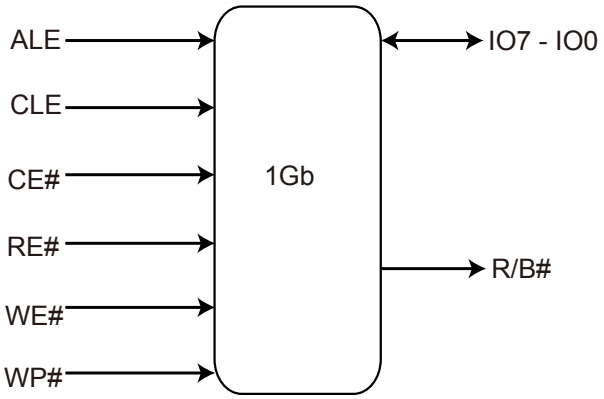
The MX30LF1G08AA array is organized as 1024 blocks, which is composed by 64 pages of (2,048+64) byte in two NAND strings structure with 32 serial connected cells in each string. Each page has an additional 64 bytes for ECC and other purposes. The device has an on-chip buffer of 2,112 bytes for data load and access.

The Cache Read Operation of the MX30LF1G08AA enable first-byte read-access latency of 25us and sequential read of 30ns per byte.

Fast programming is supported, enabling page programming at a rate of 8MB/sec (approx.)

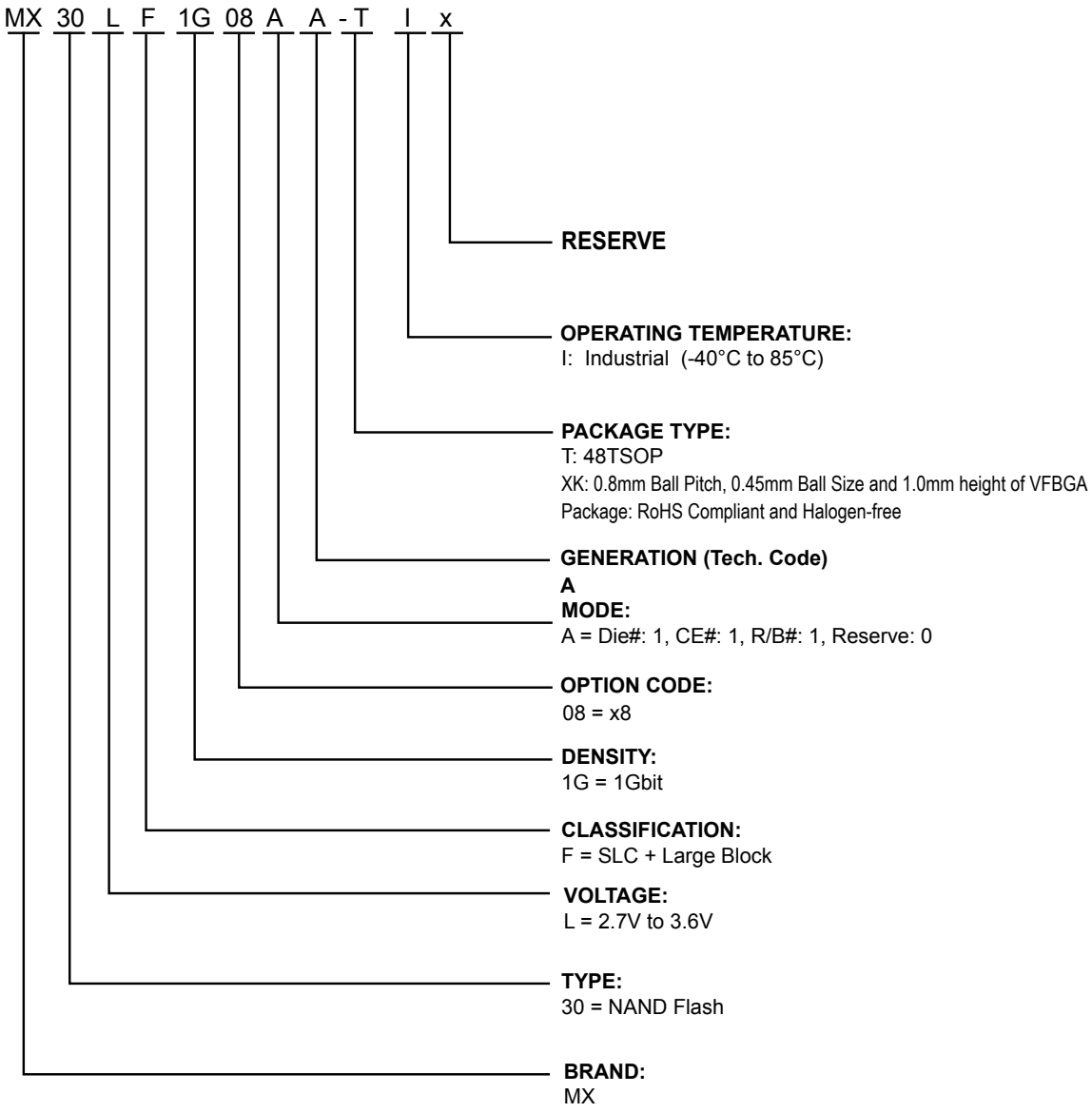
The MX30LF1G08AA power consumption is 30 mA during all modes of operations (Read/ Program/Erase), and 50uA in standby mode.

Figure 1. Logic Diagram



2-1. ORDERING INFORMATION

Part Name Description

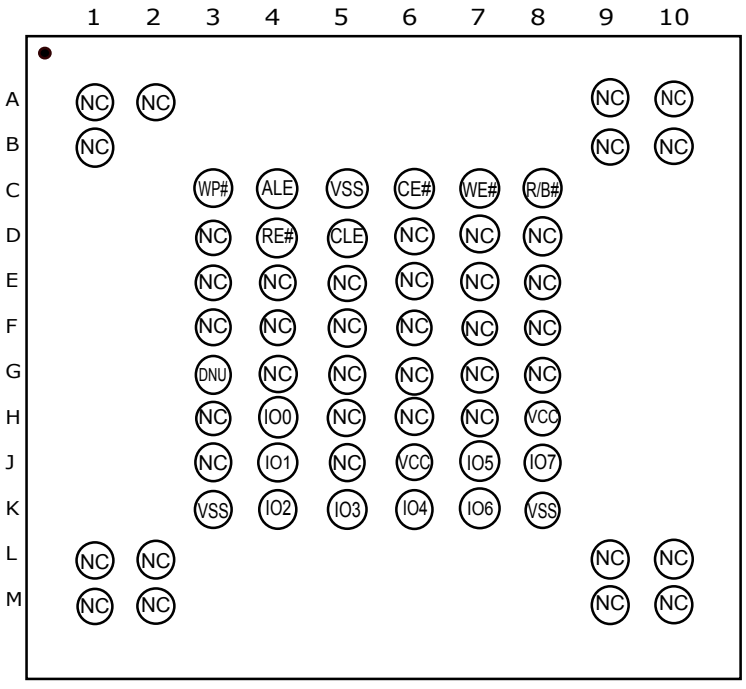


PART NUMBER	ORGANIZATION	VCC RANGE	PACKAGE	TEMPERATUR GRADE
MX30LF1G08AA-TI	x8	2.7V - 3.6 Volt	48-TSOP	Industrial (-40° to 85°C)
MX30LF1G08AA-XKI	x8	2.7V - 3.6 Volt	63-VFBGA	Industrial (-40° to 85°C)

3. PIN CONFIGURATIONS

48-TSOP

63-ball 9mmx11mm VFBGA



3-1. PIN DESCRIPTIONS

SYMBOL	PIN NAME
IO7 - IO0	Data I/O port
CE#	Chip Enable (Active Low)
RE#	Read Enable (Active Low)
WE#	Write Enable (Active Low)
CLE	Command Latch Enable
ALE	Address Latch Enable
WP#	Write Protect (Active Low)
R/B#	Ready/Busy (Open Drain)
VSS	Ground
VCC	Power Supply for Device Operation
NC	Not Connected Internally
DNU	Do Not Use (Do Not Connect)

4. PIN FUNCTIONS

The MX30LF1G08AA device is a sequential access memory that utilizes multiplexing input of Command/Address/Data.

I/O PORT: IO7 - IO0

The IO7 to IO0 pins are for address/command input and data output to and from the device.

CHIP ENABLE: CE#

The device goes into low-power Standby Mode when CE# goes High during a Read operation and not at busy stage.

The CE# goes low to enable the device to be ready for standard operation. When the CE# goes high, the device is deselected. However, when the device is at busy stage, the device will not go to standby mode when CE# pin goes high.

READ ENABLE: RE#

The RE# (Read Enable) allows the data to be output by a tREA time after the falling edge of RE#. The internal address counter is automatically increased by one at the falling edge of RE#.

WRITE ENABLE: WE#

When the WE# goes low, the address/data/command are latched at the rising edge of WE#.

COMMAND LATCH ENABLE: CLE

The CLE controls the command input. When the CLE goes high, the command data is latched at the rising edge of the WE#.

ADDRESS LATCH ENABLE: ALE

The ALE controls the address input. when the ALE goes high, the address is latched at the rising edge of WE#.

WRITE PROTECT: WP#

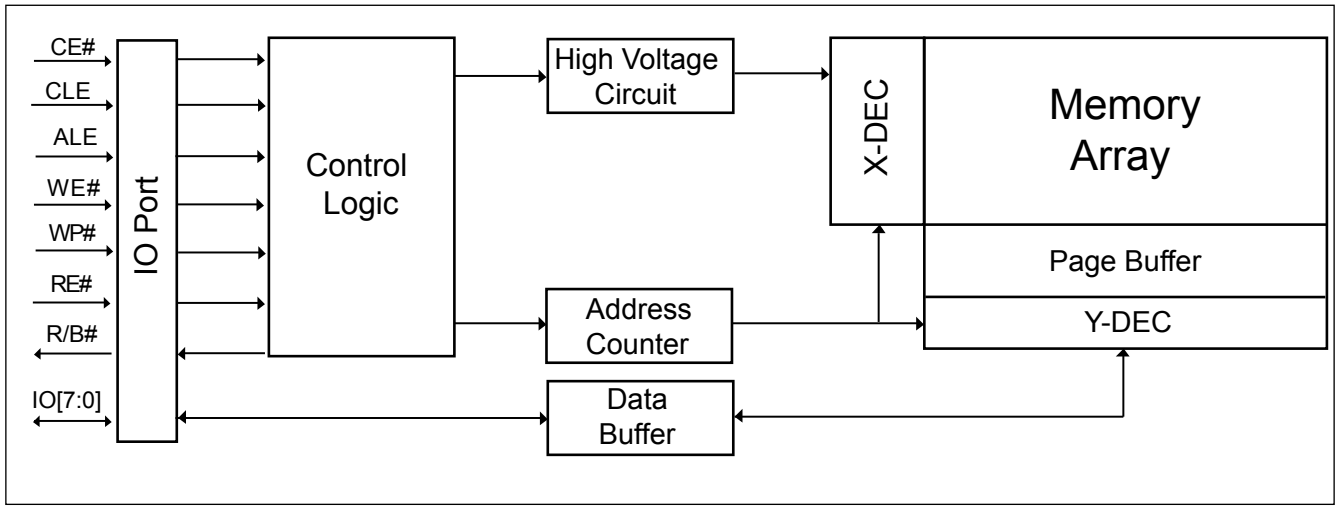
The WP# signal keeps low and then the memory will not accept the program/erase operation. The WP# pin is not latched by WE# for ensuring of the data can be protected during power-on. It is recommended to keep WP# pin low during power on/off sequence. Please refer to the waveform of "Power On/Off Sequence".

READY/Busy: R/B#

The R/B# is an open-drain output pin. The R/B# outputs the ready/busy status of read/program/erase operation of the device. When the R/B# is at low, the device is busy for read or program or erase operation. When the R/B# is at high, the read/program/erase operation is finished.

Please refer to **Section 9.1** for details.

5. BLOCK DIAGRAM



6. DEVICE OPERATIONS

ADDRESS INPUT / COMMAND INPUT / DATA INPUT

Address input bus operation is for address input to select the memory address. The command input bus operation is for giving command to the memory. The data input bus is for data input to the memory device.

Figure 2. AC Waveform for Command / Address / Data Latch Timing

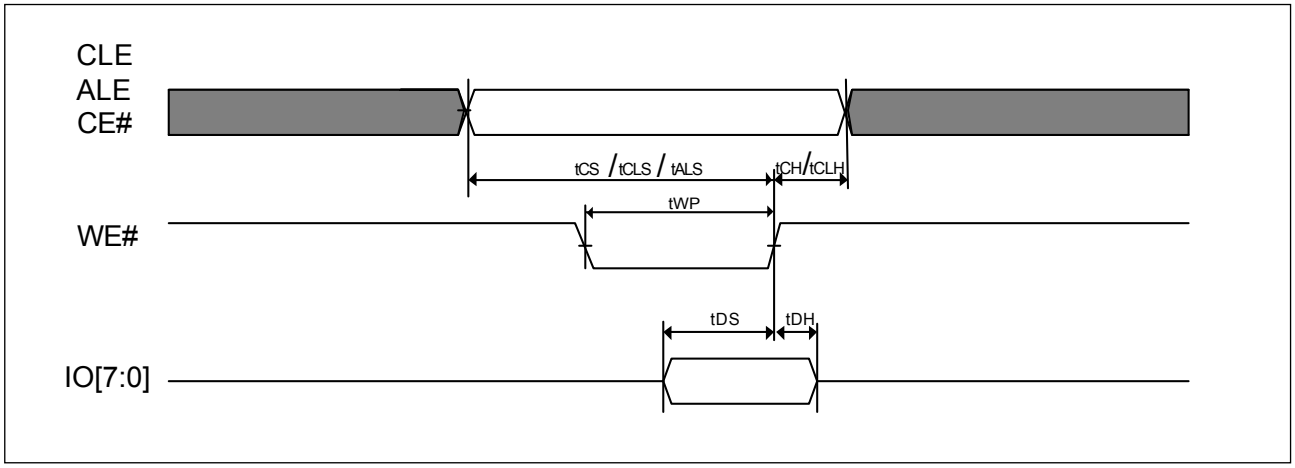


Figure 3. AC Waveforms for Address Input Cycle

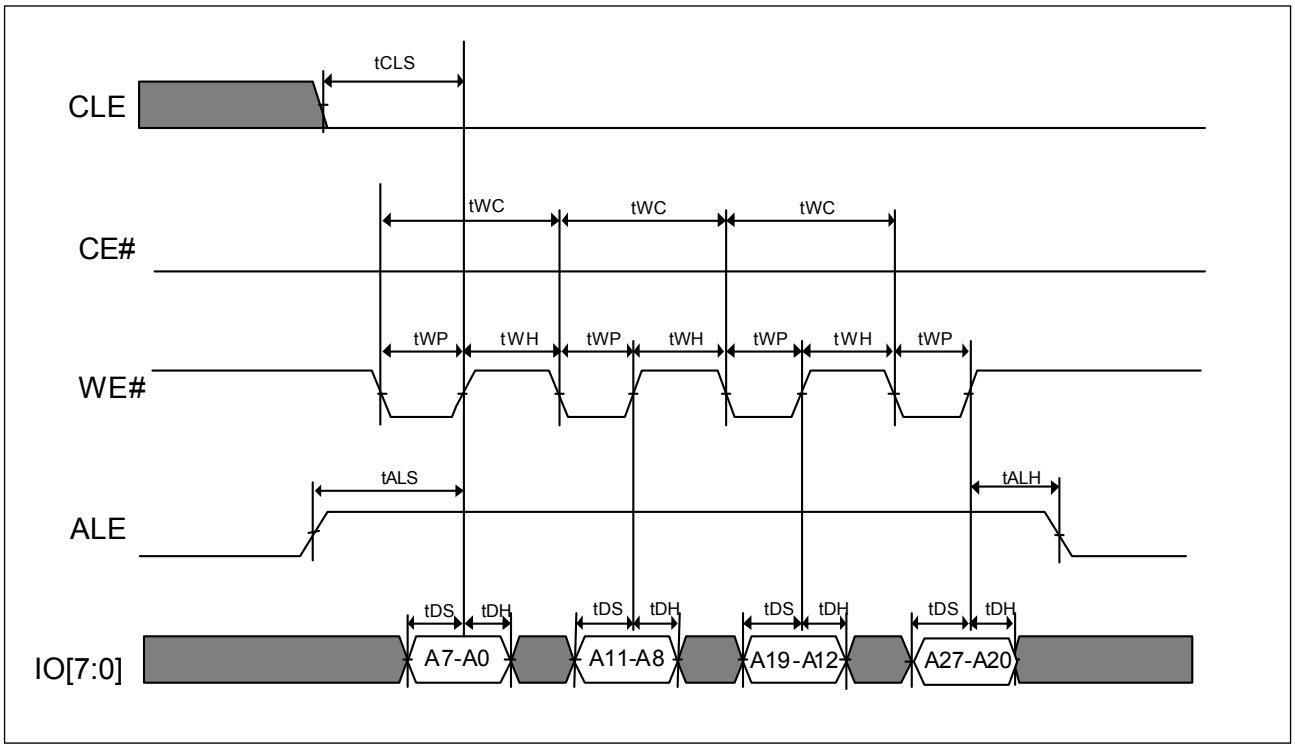


Figure 4. AC Waveforms for Command Input Cycle

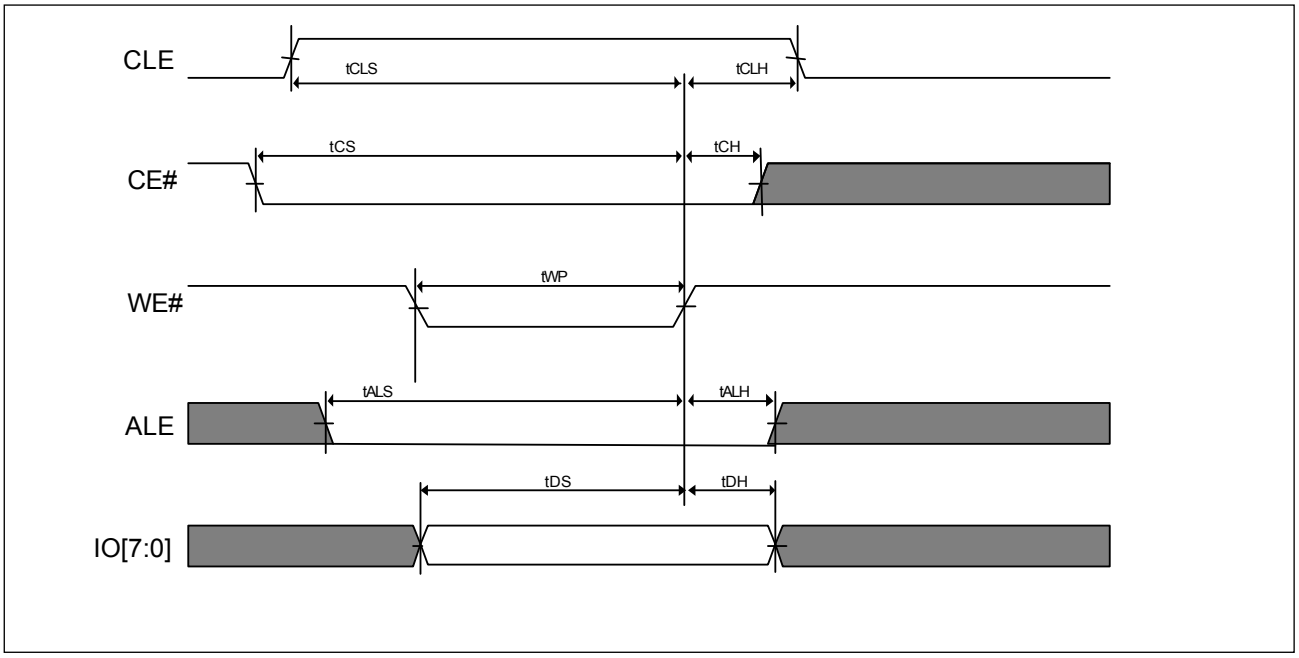
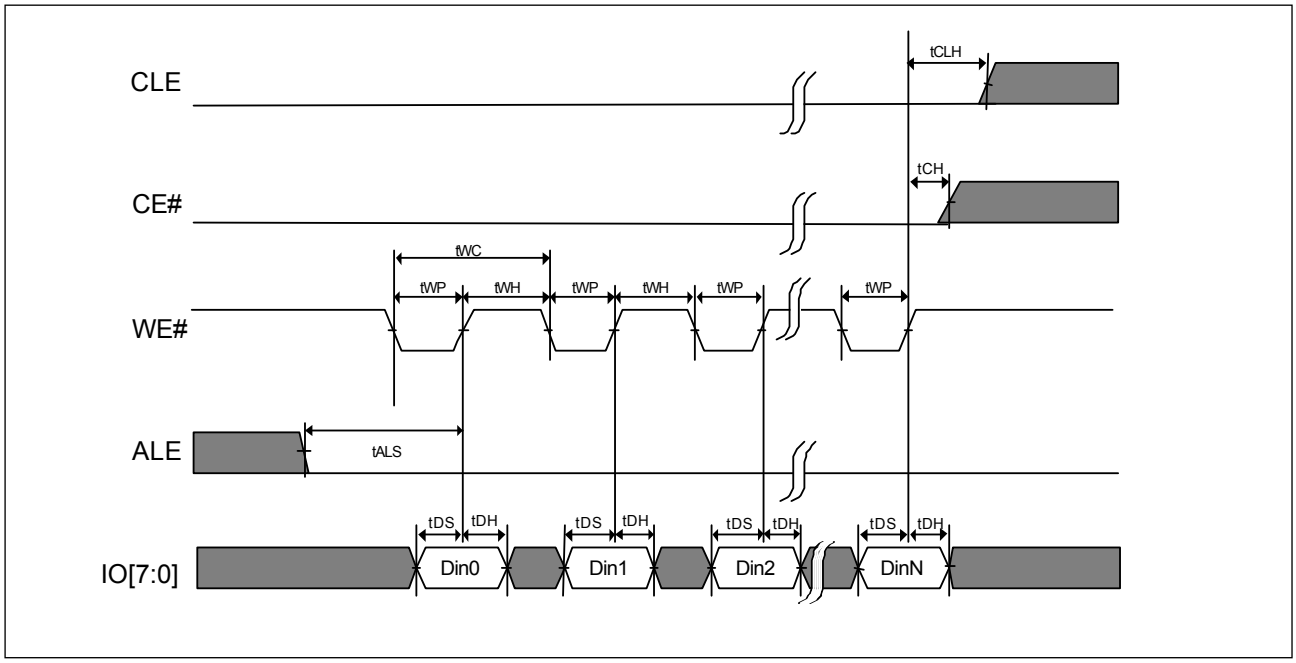


Figure 5. AC Waveforms for Data Input Cycle



PAGE READ

When power is on, the default stage of the NAND flash memory is at read mode, so the 00h command cycle is not needed for the read operation. The MX30LF1G08AA array is accessed in Page of 2,112 bytes. External reads begins after the R/B# pin goes to READY.

The Read operation may also be initiated by writing the 00h command and giving the address (column and row address) and being confirmed by the 30h command, the MX30LF1G08AA begins the internal read operation and the chip enters busy state. The data can be read out in sequence after the chip is ready. Refer to the waveform for Read Operation as below.

To access the data in the same page randomly, a command of 05h may be written and only column address following and then confirmed by E0h command. The random read mode is not supported during cache read operation.

Figure 6. AC Waveforms for Read Cycle

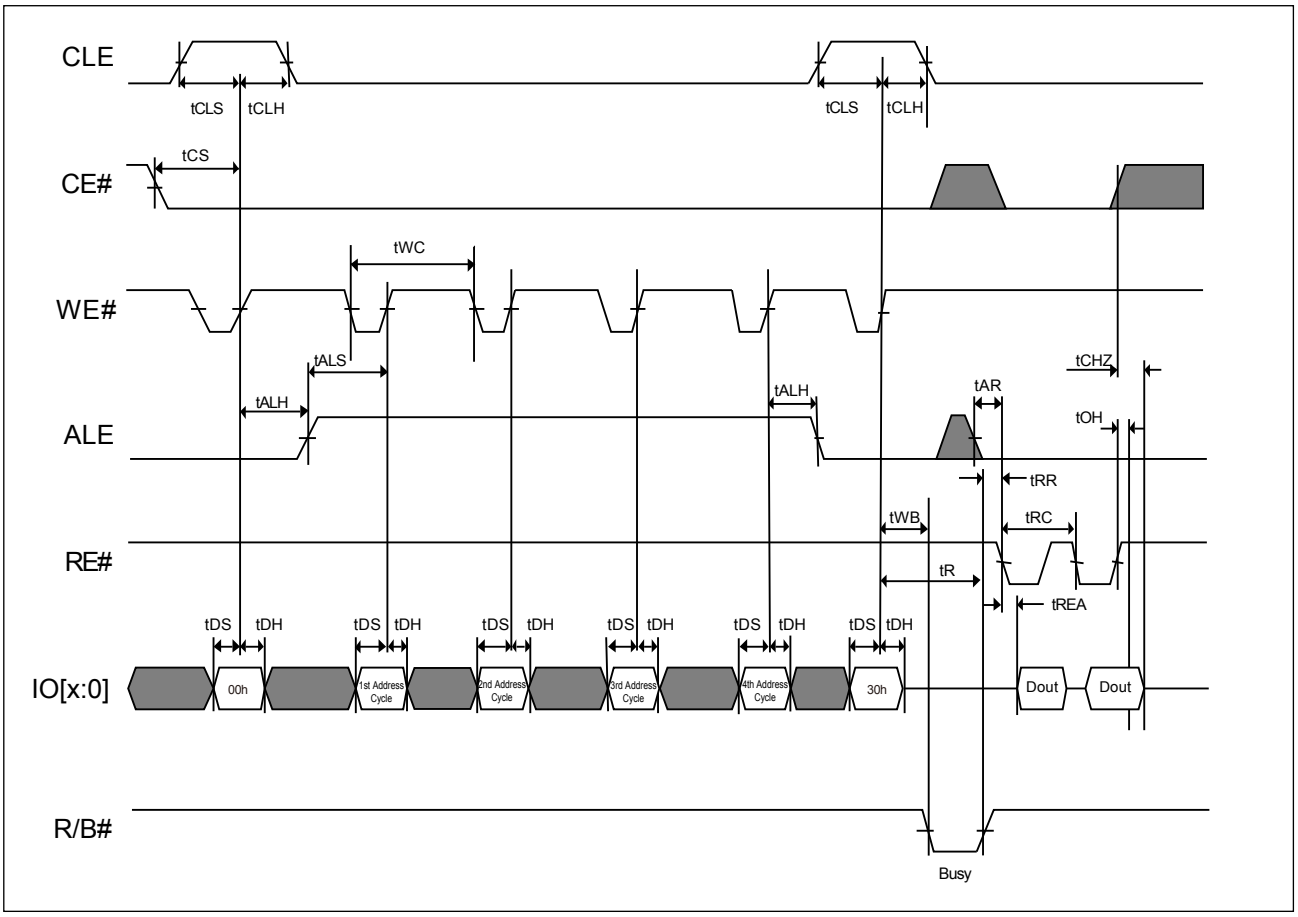


Figure 7. AC Waveforms for Read Operation (Intercepted by CE#)

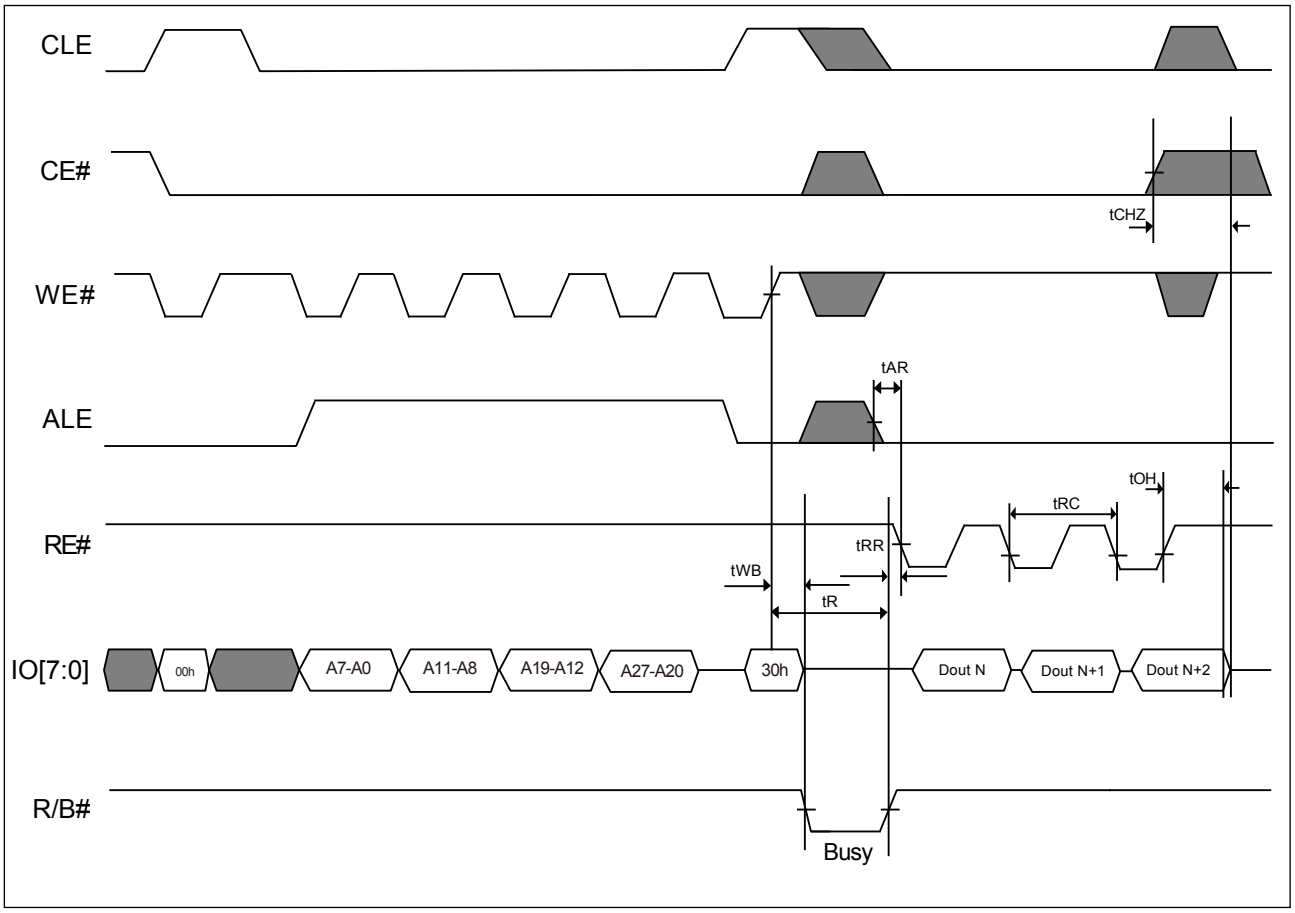
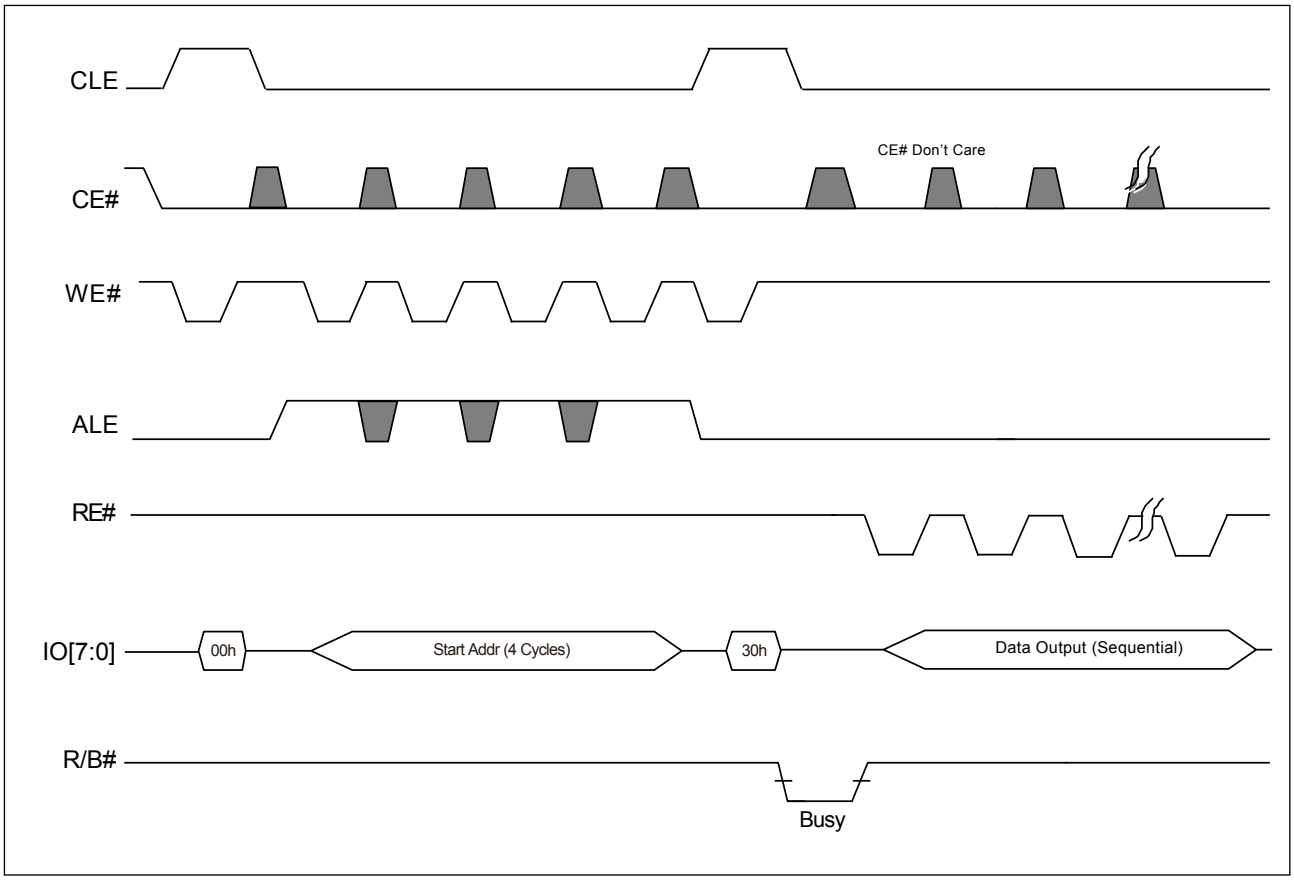


Figure 8. Read Operation with CE# Don't Care



Note: *The CE# "Don't Care" feature may simplify the system interface, which allows controller to directly download the code from flash device, and the CE# transitions will not stop the read operation during the latency time.*

Figure 9. AC Waveforms for Sequential Data Out Cycle (After Read)

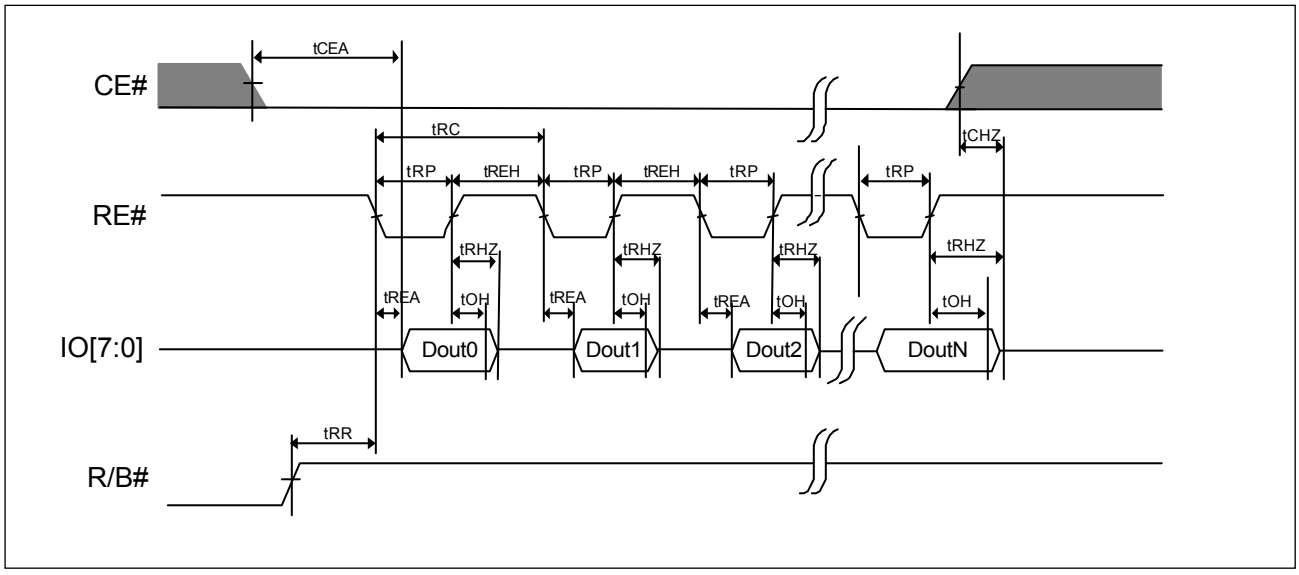
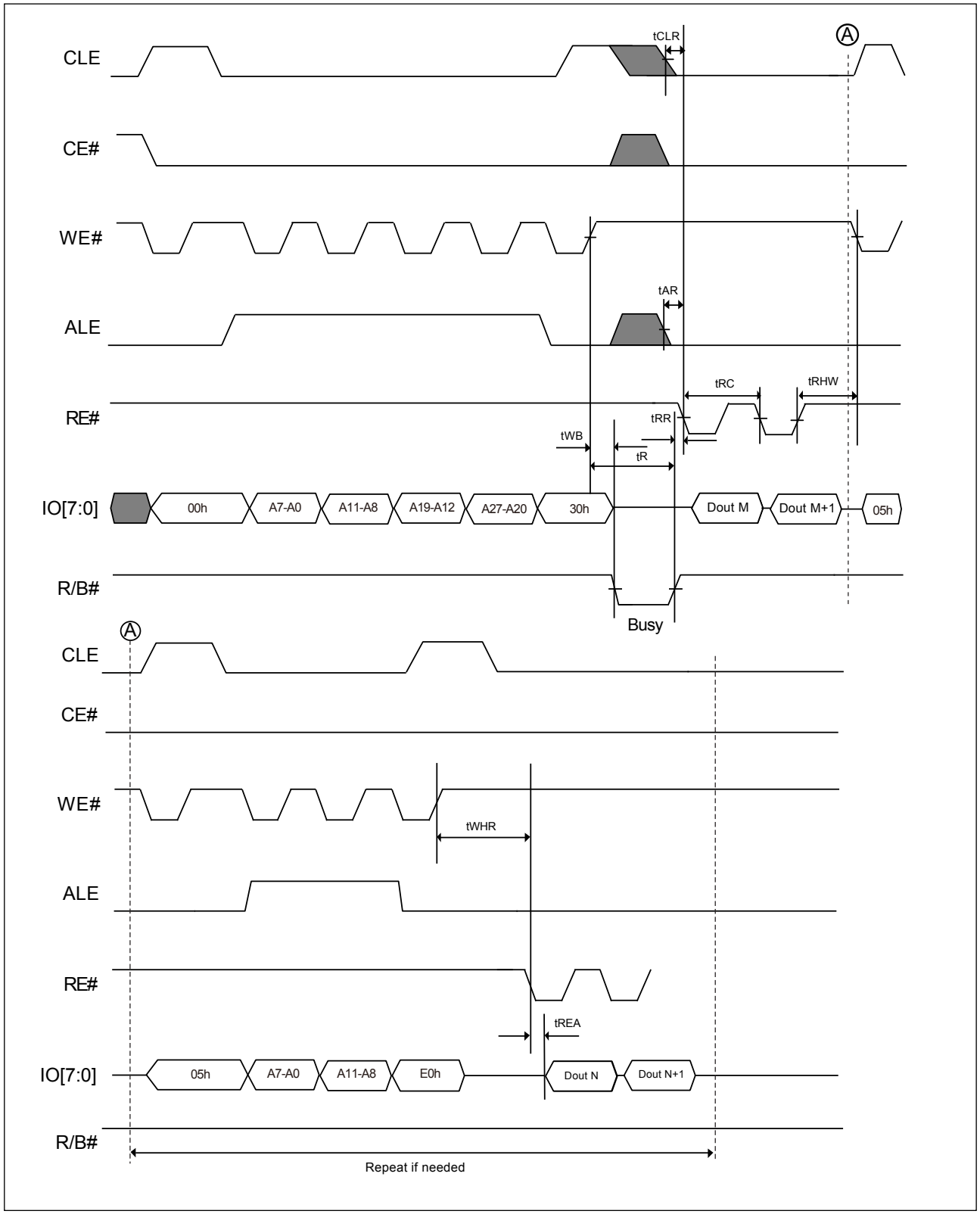


Figure 10. AC Waveforms for Random Data Output



CACHE READ

The cache read operation is for throughput enhancement by using the internal cache buffer. It allows automatic downloading of the consecutive pages and reading the entire flash memory, no additional dead time between pages or blocks. While the data is read out on one page, the data of next page can be read into the cache buffer.

After writing the 00h command, the column and row address should be given for the start page selection. The address A[11:0] for the start page should be 000h. Cache read begin command 31h should be issued to start the cache read operation.

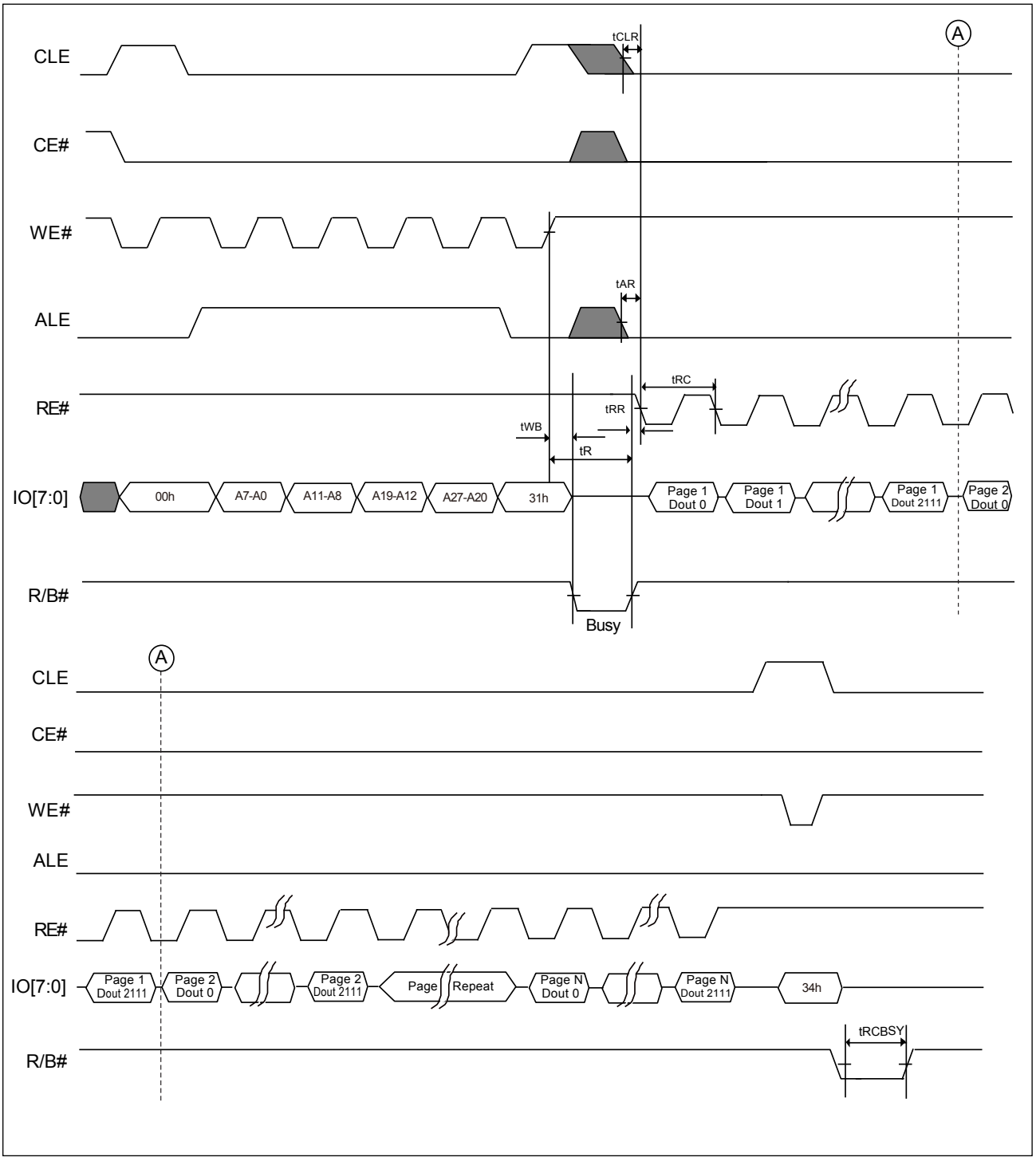
The random data out is not available for cache read operation. After the latency time tR, the data can be read out continuously.

The user can check the chip status by the following method:

- R/B# pin ("0" means the data is not ready, "1" means the user can read the data)

- Status Register (SR[6] behaves the same as R/B# pin, SR[5] indicates the internal chip operation, "0" means the chip is in internal operation and "1" means the chip is idle.) Status Register can be checked after the Read Status command (70h) is issued. Command 00h should be given to return to the cache read operation. To exit the cache read operation, the user needs to issue cache read end command (34h) or Reset command. After the command is issued, the device will become idle within 5 us.

Figure 11. AC Waveforms for Cache Read



PAGE PROGRAM

The memory is programmed by page, which is 2,112 bytes. After Program load command (80h) is issued and the row and column address is given, the data will be loaded into the chip sequentially. Random Data Input command (85h) allows multi-data load in non-sequential address. After data load is complete, program confirm command (10h) is issued to start the page program operation. Partial program in a page is allowed up to 4 times. However, the random data input mode for programming a page is allowed and number of times is not limited.

The status of the program completion can be detected by R/B# pin or Status register bit (IO6).

The program result is shown in the chip status bit (SR[0]). SR[0] = 1 indicates the Page Program is not successful and SR[0] = 0 means the program operation is successful.

During the Page Program progressing, only the read status register command and reset command are accepted, others are ignored.

Figure 12. AC Waveforms for Program Operation after Command 80H

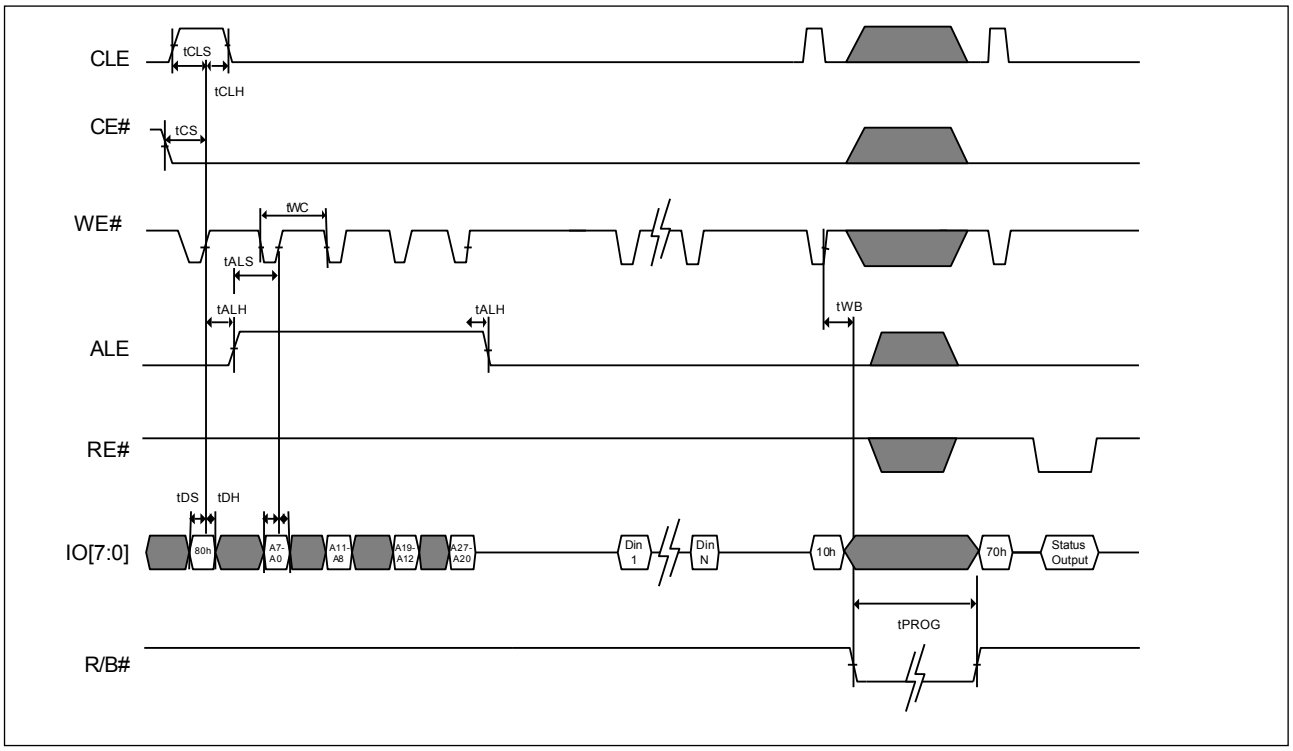
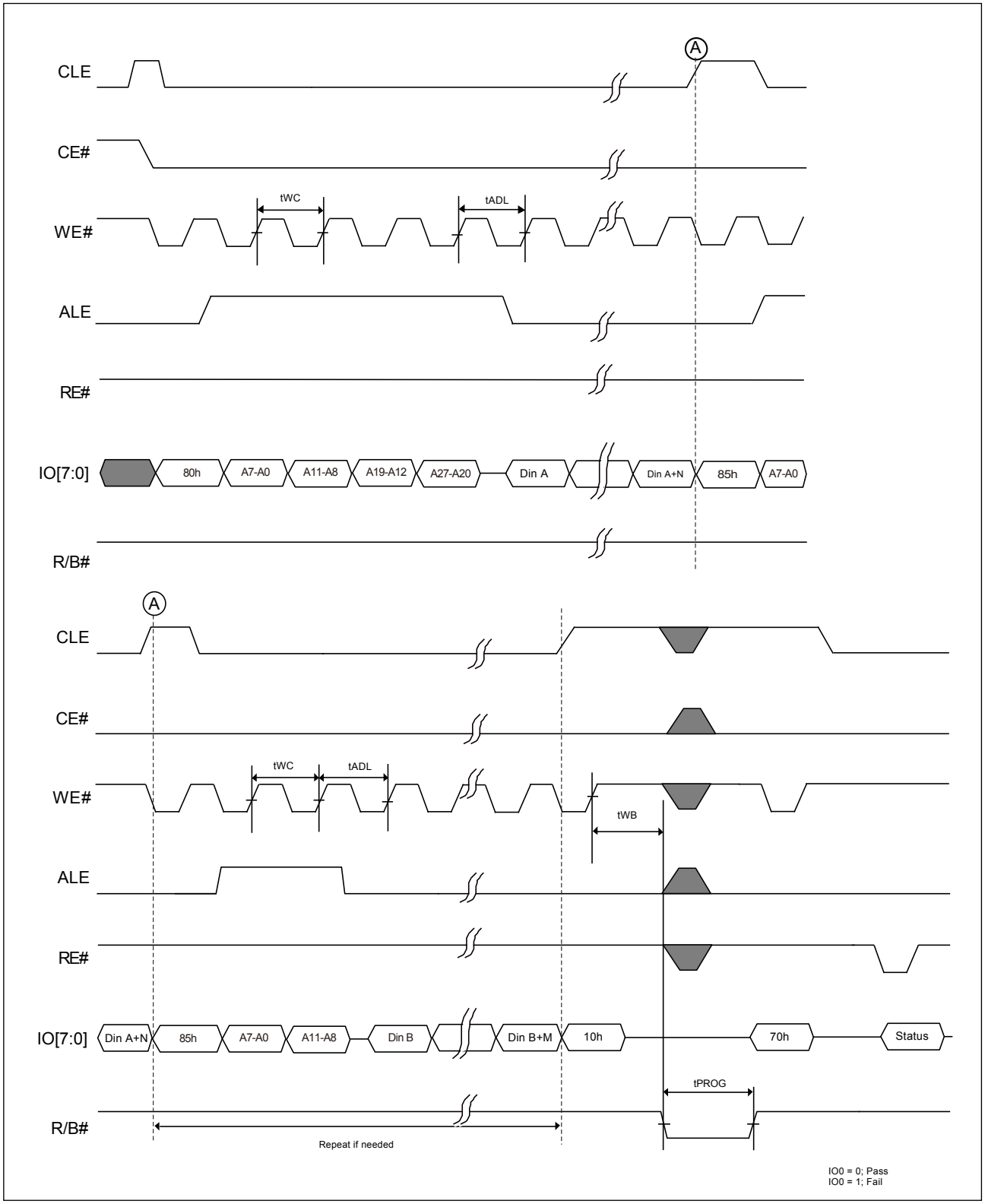
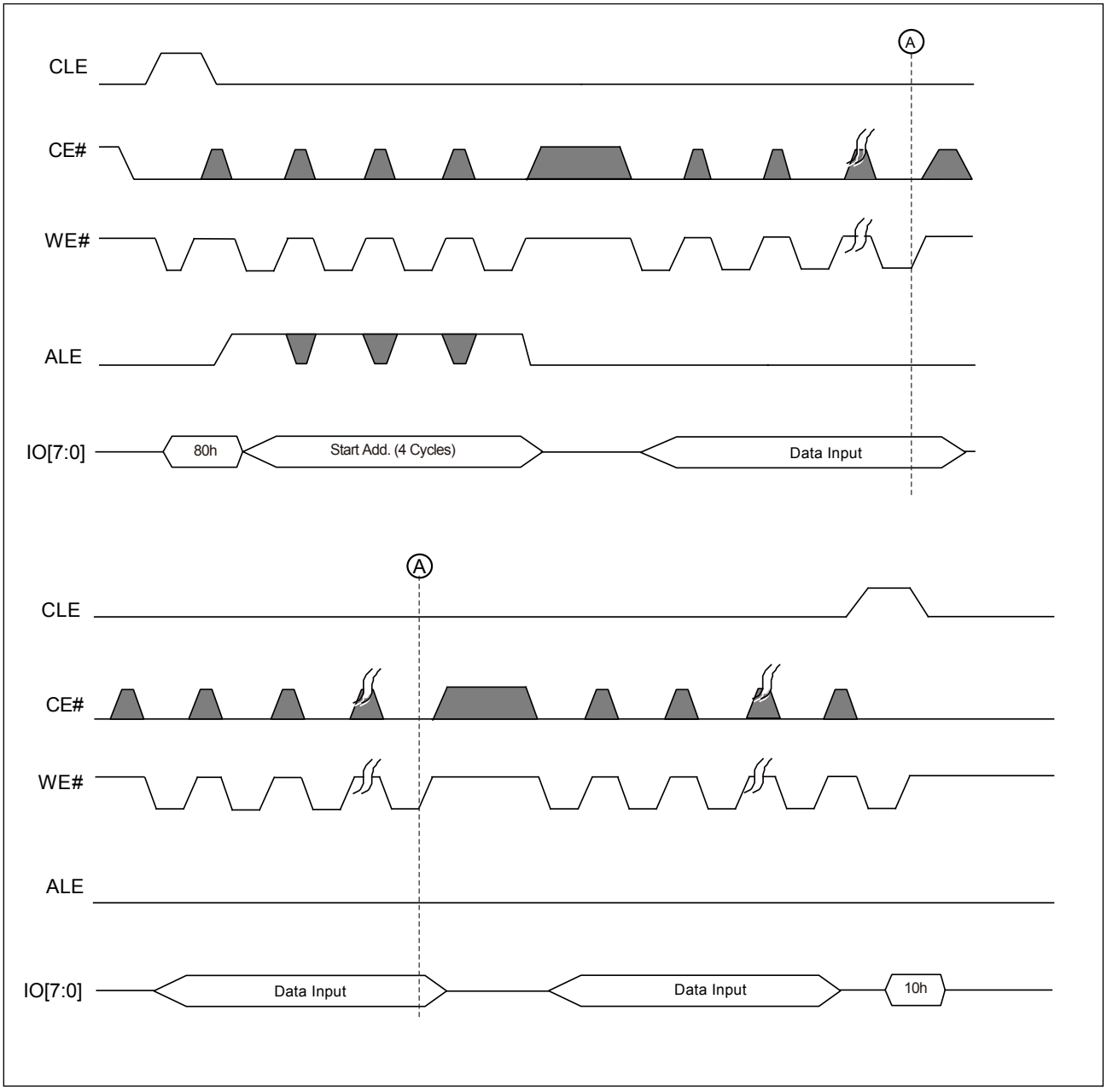


Figure 13. AC Waveforms for Random Data In (For Page Program)



Note: *Random Data In is also supported in cache program.*

Figure 14. Program Operation with CE# Don't Care



Note: *The CE# "Don't Care" feature may simplify the system interface, which allows the controller to directly write data into flash device, and the CE# transitions will not stop the program operation during the latency time.*

CACHE PROGRAM

The cache program feature enhances the program performance by using the cache buffer of 2,112-byte. The serial data can be input to the cache buffer while the previous data stored in the buffer are programming into the memory cell. Cache Program command sequence is almost the same as page program command sequence. Only the Program Confirm command (10h) is replaced by cache Program command (15h).

After the Cache Program command (15h) is issued. The user can check the status by the following methods.

- R/B# pin

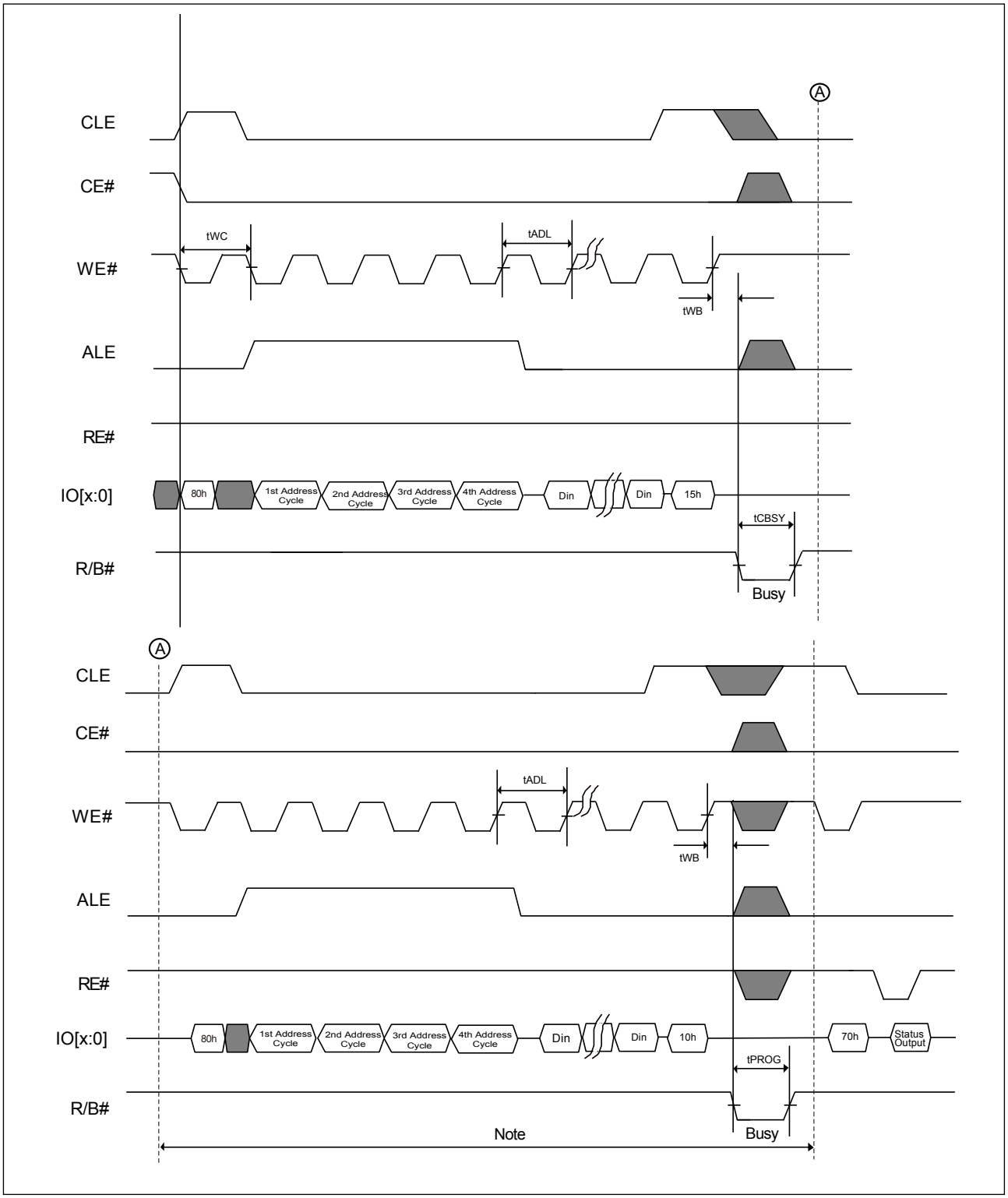
- Cache Status Bit (SR[6] = 0 indicates the cache is busy; SR[6] = 1 means the cache is ready).

The user can issue another Cache Program Command Sequence after the Cache is ready. The user can always monitor the chip state by Ready/Busy Status Bit (SR[5]). The user can issues either program confirm command (10h) or cache program command (15h) for the last page if the user monitor the chip status by issuing Read Status Command (70h).

However, if the user only monitors the R/B# pin, the user needs to issue the program confirm command (10h) for the last page.

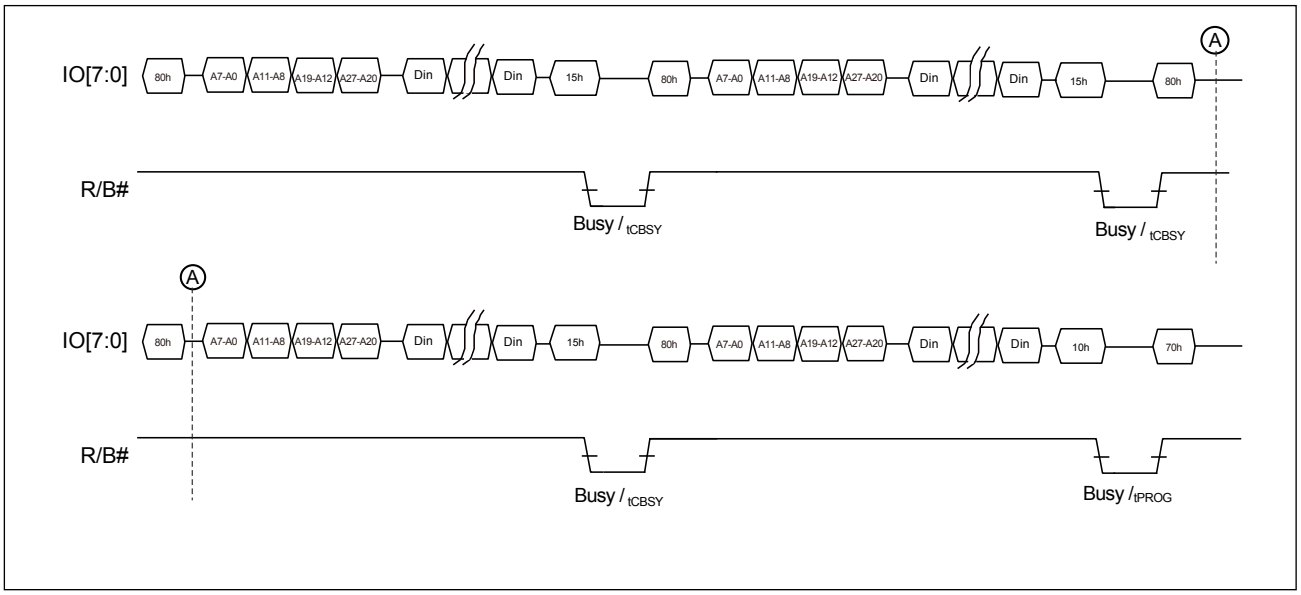
The user can check the Pass/Fail Status through P/F Status Bit (SR[0]) and Cache P/F Status Bit (SR[1]). SR[1] represents Pass/Fail Status of the previous page. SR[1] is updated when SR[6] change from 0 to 1 or Chip is ready. SR[0] shows the Pass/Fail status of the current page. It is updated when SR[5] change from "0" to "1" or the end of the internal programming. For more details, please refer to the related waveforms.

Figure 15-1. AC Waveforms for Cache Program



Note: *It indicates the last page Input & Program.*

Figure 15-2. Sequence of Cache Program



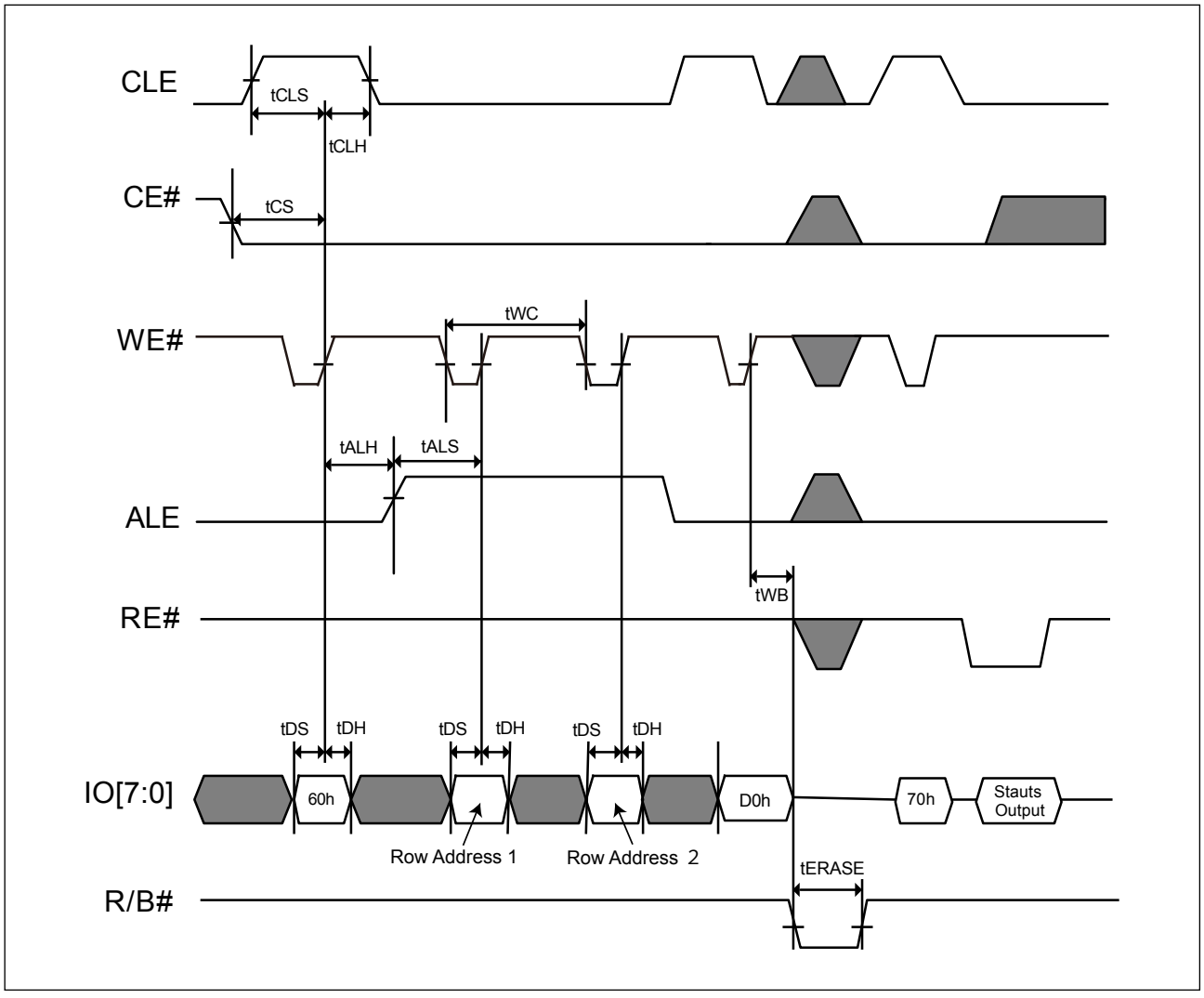
BLOCK ERASE

The MX30LF1G08AA supports a block erase command. This command will erase a block of 64 pages associated with the 10 most significant address bits (A27-A18).

The completion of the erase operation can be detected by R/B# pin or Status register bit (IO6). Recommend to check the status register bit IO0 after the erase operation completes.

During the erasing process, only the read status register command and reset command can be accepted, others are ignored.

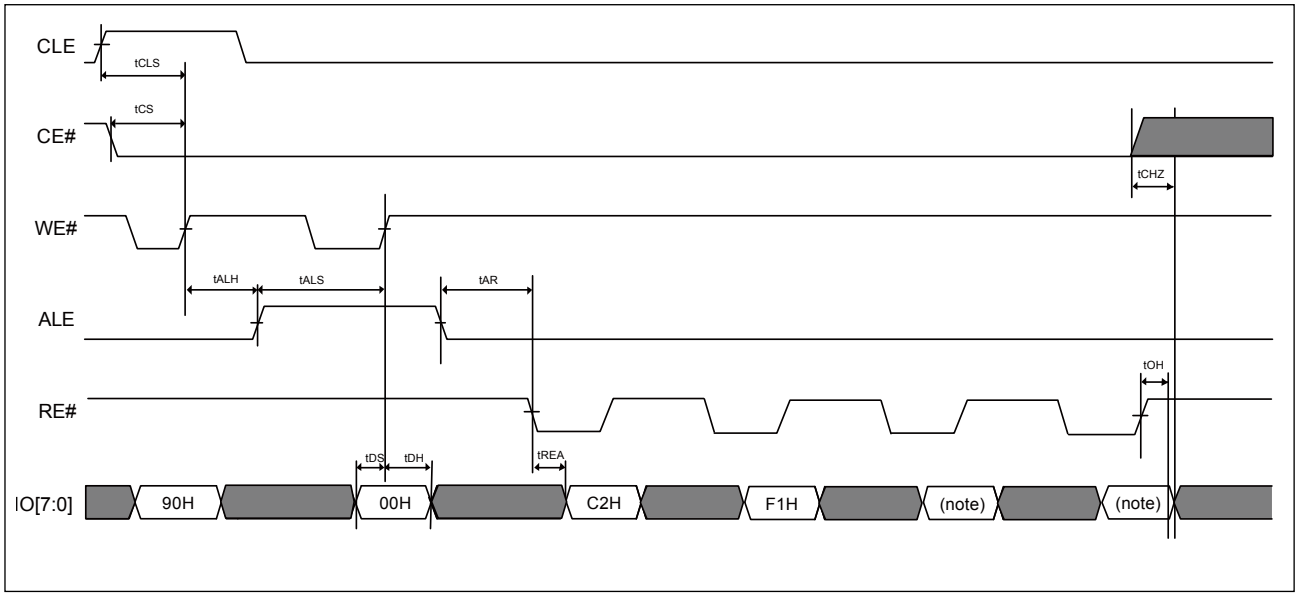
Figure 16. AC Waveforms for Erase Operation



ID READ

The device contains ID codes that identify the device type and the manufacturer. The ID READ command sequence includes one command Byte (90h), one address byte (00h). The Read ID command 90h may provide the manufacturer ID (C2h) of one-byte and device ID (F1h) of one-byte, also 3rd and 4th ID code are followed.

Figure 17. AC Waveforms for ID Read Operation



Note: *Also see* ***Table 12. ID Codes Read Out by ID Read Command 90H***.