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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

1G/2G/4G-bit NAND Flash Memory
(ECC-Free)
MX30LFxGE8AB

Contents

1. FEATURES

- 1G-bit/2G-bit/4G-bit SLC NAND Flash
  - Bus: x8
  - Page size: (2048+64)byte
  - Block size: (128K+4K)byte
  - Plane size:
    1024-block/plane x 1 for 1Gb
    1024-block/plane x 2 for 2Gb
    2048-block/plane x 2 for 4Gb
- **ONFI 1.0 compliant**
- **Multiplexed Command/Address/Data**
- **User Redundancy**
  - 64-byte attached to each page
- **Fast Read Access**
  - Latency of array to register: 45us (typ.)
  - Sequential read: 20ns
- **Page Program Operation**
  - Page program time: 320us (typ.)
- **Cache Program Support**
- **Block Erase Operation**
  - Block erase time: 1ms (typ.)
- **Single Voltage Operation:**
  - VCC: 2.7 ~ 3.6V
- **Low Power Dissipation**
  - Max. 30mA
    Active current (Read/Program/Erase)
- **Sleep Mode**
  - 50uA (Max.) standby current
- **Hardware Data Protection:** WP# pin
- **Device Status Indicators**
  - Ready/Busy (R/B#) pin
  - Status Register
- **Chip Enable Don't Care**
  - Simplify System Interface
- **Unique ID Read support (ONFI)**
- **Secure OTP support**
- **Electronic Signature**
- **High Reliability**
  - Internal ECC logic always enabling
  - Typical 100K P/E endurance cycle
  - Data Retention: 10 years
- **Wide Temperature Operating Range**
  -40°C to +85°C
- **Package:**
  - 48-TSOP(I) (12mm x 20mm)
  - 63-ball 9mmx11mm VFBGA (For 1Gb/2Gb)
  - 48-ball 6mm x 8mm VFBGA (For 1Gb)

  All packaged devices are RoHS Compliant and Halogen-free.

2. GENERAL DESCRIPTIONS

The MX30LFxGE8AB is a 1Gb to 4Gb SLC NAND Flash memory device. Its standard NAND Flash features and reliable quality make it most suitable for embedded system code and data storage.

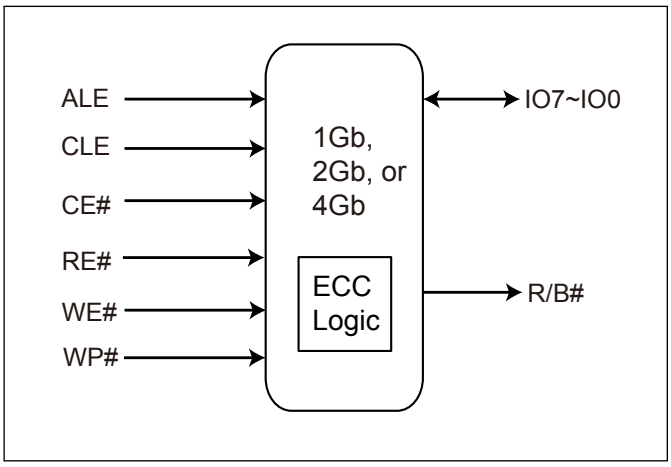
The product family does not require the host controller to support ECC since there is an internal ECC logic inside the Flash device for the error correction and detection.

The MX30LFxGE8AB is typically accessed in pages of 2,112 bytes both for read and for program operations.

The MX30LFxGE8AB array is organized as thousands of blocks, which is composed by 64 pages of (2,048+64) bytes in two NAND strings structure with 32 serial connected cells in each string. Each page has an additional 64 bytes for bad block marks and other purposes. The device has an on-chip buffer of 2,112 bytes for data load and access.

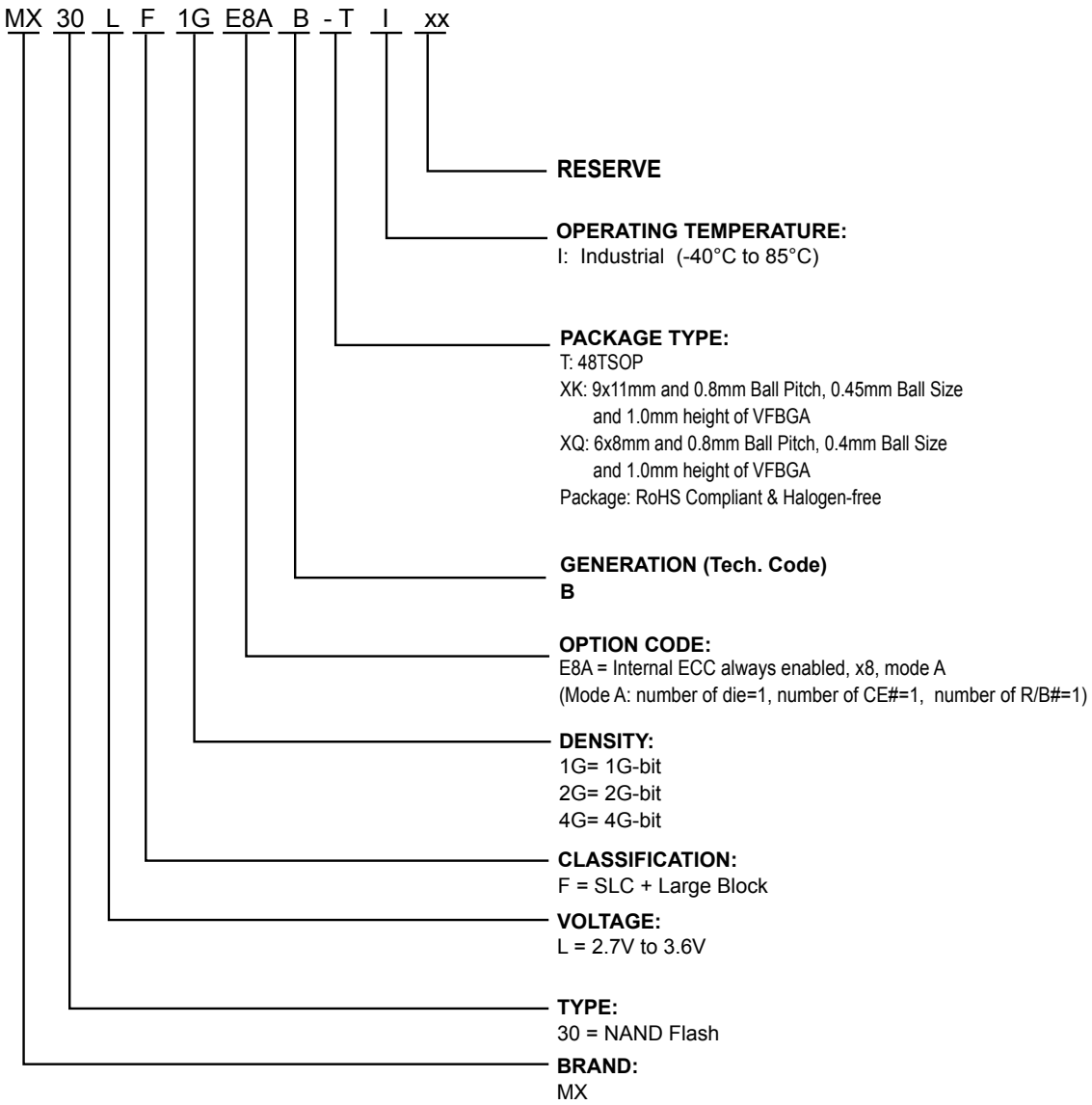
The MX30LFxGE8AB power consumption is 30mA during all modes of operations (Read/Program/Erase), and 50uA in standby mode.

Figure 1. Logic Diagram



2-1. ORDERING INFORMATION

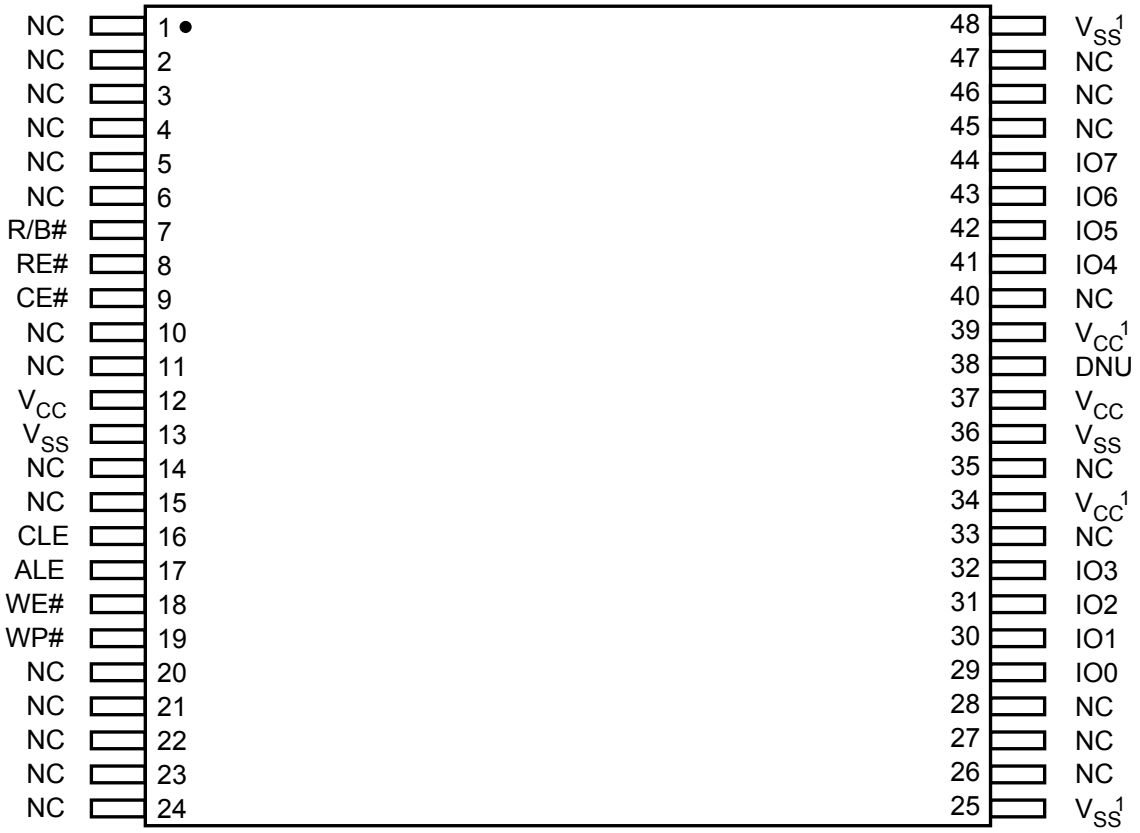
Part Name Description



Part Number	Density	Organization	VCC Range	Package	Temperature Grade
MX30LF1GE8AB-TI	1Gb	x8	3V	48-TSOP	Industrial
MX30LF1GE8AB-XKI	1Gb	x8	3V	63-VFBGA	Industrial
MX30LF1GE8AB-XQI	1Gb	x8	3V	48-VFBGA	Industrial
MX30LF2GE8AB-TI	2Gb	x8	3V	48-TSOP	Industrial
MX30LF2GE8AB-XKI	2Gb	x8	3V	63-VFBGA	Industrial
MX30LF4GE8AB-TI	4Gb	x8	3V	48-TSOP	Industrial

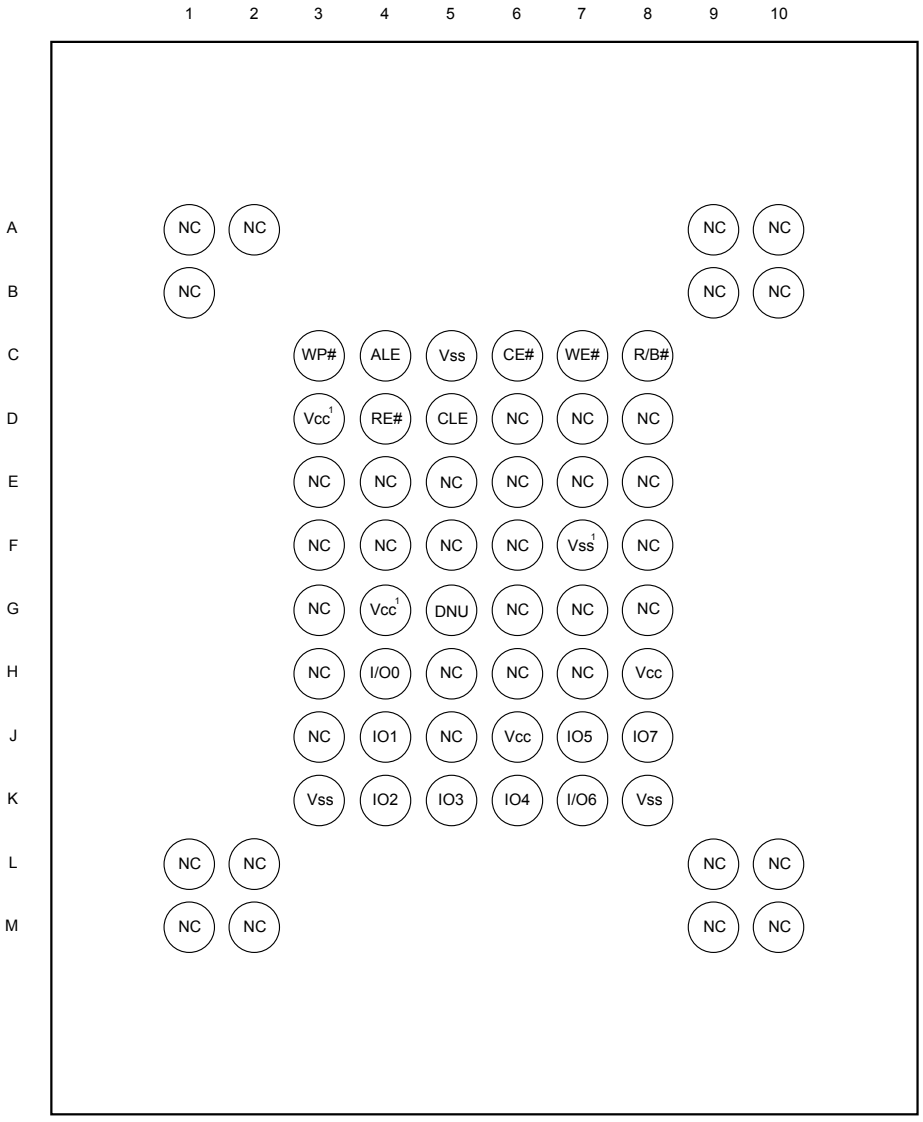
3. PIN CONFIGURATIONS

48-TSOP



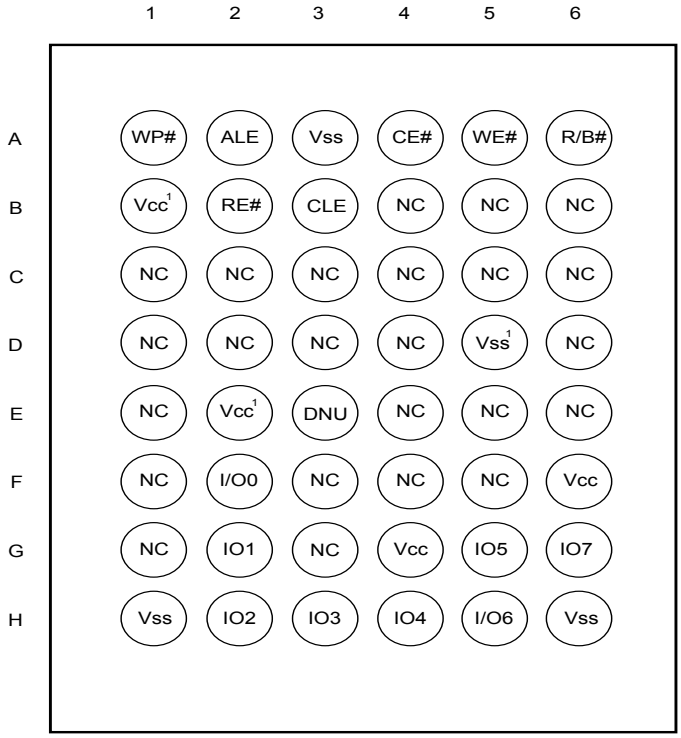
***Note** 1: These pins might not be connected internally. However, it is recommended to connect these pins to power (or ground) as designated for ONFI compatibility.*

63-ball 9mmx11mm VFBGA



Note 1. *These pins might not be connected internally; however, it is recommended to connect these pins to power (or ground) as designated for ONFI compatibility.*

48-ball 6x8mm VFBGA



Note 1. *These pins might not be connected internally; however, it is recommended to connect these pins to power (or ground) as designated for ONFI compatibility.*

3-1. PIN DESCRIPTIONS

SYMBOL	PIN NAME
IO7 - IO0	Data I/O port: IO7-IO0
CE#	Chip Enable (Active Low)
RE#	Read Enable (Active Low)
WE#	Write Enable (Active Low)
CLE	Command Latch Enable
ALE	Address Latch Enable
WP#	Write Protect (Active Low)
R/B#	Ready/Busy (Open Drain)
VSS	Ground
VCC	Power Supply for Device Operation
NC	Not Connected Internally
DNU	Do Not Use (Do Not Connect)

PIN FUNCTIONS

The MX30LFxGE8AB device is a sequential access memory that utilizes multiplexing input of Command/Address/Data.

Data I/O PORT: IO7- IO0

The IO7 to IO0 pins are for address/command input and data output to and from the device.

CHIP ENABLE: CE#

The device goes into low-power Standby Mode when CE# goes high during a read operation and not at busy stage.

The CE# goes low to enable the device to be ready for standard operation. When the CE# goes high, the device is deselected. However, when the device is at busy stage, the device will not go to standby mode when CE# pin goes high.

READ ENABLE: RE#

The RE# (Read Enable) allows the data to be output by a tREA time after the falling edge of RE#. The internal address counter is automatically increased by one at the falling edge of RE#.

WRITE ENABLE: WE#

When the WE# goes low, the address/data/command are latched at the rising edge of WE#.

COMMAND LATCH ENABLE: CLE

The CLE controls the command input. When the CLE goes high, the command data is latched at the rising edge of the WE#.

ADDRESS LATCH ENABLE: ALE

The ALE controls the address input. When the ALE goes high, the address is latched at the rising edge of WE#.

WRITE PROTECT: WP#

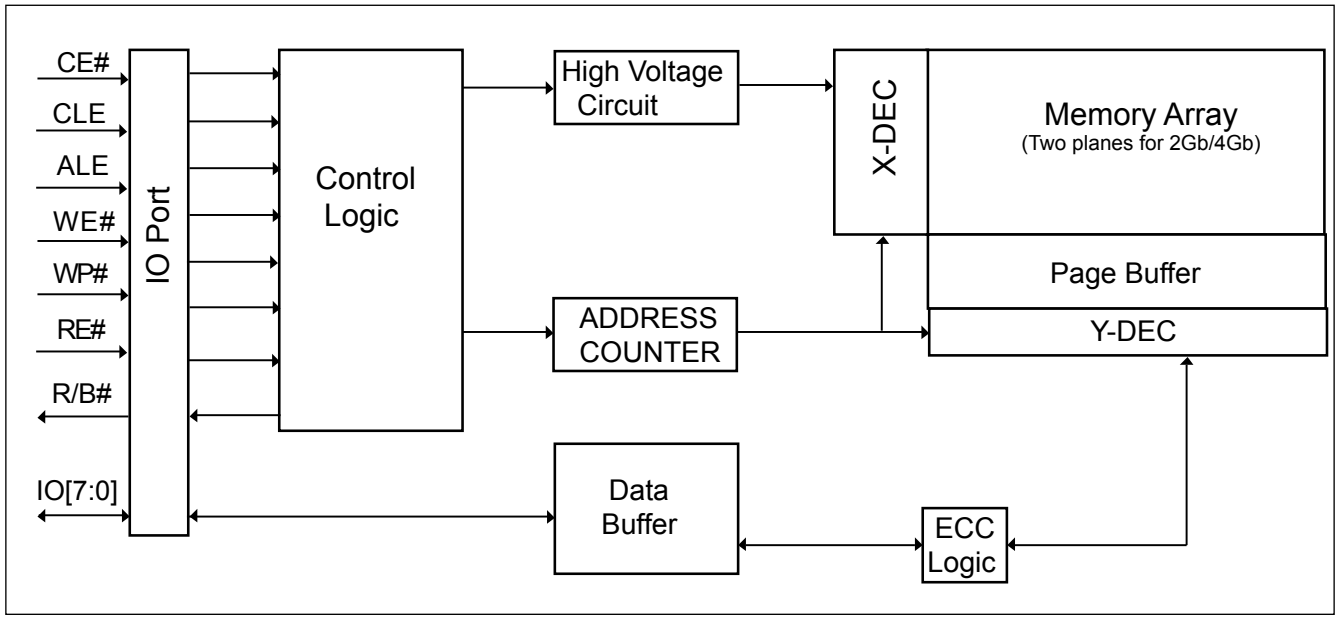
The WP# signal keeps low and then the memory will not accept the program/erase operation. It is recommended to keep WP# pin low during power on/off sequence. Please refer to the waveform of "Power On/Off Sequence".

READY/Busy: R/B#

The R/B# is an open-drain output pin. The R/B# outputs the ready/busy status of read/program/erase operation of the device. When the R/B# is at low, the device is busy for read or program or erase operation. When the R/B# is at high, the read/program/erase operation is finished.

Please refer to **"8-1. R/B#: Termination for The Ready/Busy# Pin (R/B#)"** for details.

4. BLOCK DIAGRAM



5. SCHEMATIC CELL LAYOUT AND ADDRESS ASSIGNMENT

MX30LFxGE8AB NAND device is divided into two planes for 2Gb and 4Gb (the 1Gb is single plane), which is composed by 64 pages of (2,048+64)-byte in two NAND strings structure with 32 serial connected cells in each string. Each page has an additional 64 bytes for bad block marks and other purposes. The device has an on-chip buffer of 2,112 bytes for data load and access. Each 2K-Byte page has the two area, one is the main area which is 2048-bytes and the other is spare area which is 64-byte.

There are four (for 1Gb) or five (for 2Gb/4Gb) address cycles for the address allocation, please refer to the table below.

Table 1. Address Allocation: MX30LFxGE8AB

Addresses	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Column address - 1st cycle	A7	A6	A5	A4	A3	A2	A1	A0
Column address - 2nd cycle	L	L	L	L	A11	A10	A9	A8
Row address - 3rd cycle	A19	A18[1]	A17	A16	A15	A14	A13	A12
Row address - 4th cycle	A27	A26	A25	A24	A23	A22	A21	A20
Row address - 5th cycle[4]	L	L	L	L	L	L	A29[3]	A28[2]

Notes:

1. *A18 is the plane selection for 2Gb/4Gb.*
2. *A28 is for 2Gb and 4Gb.*
3. *A29 is for 4Gb, "L" (Low) for 2Gb.*
4. *The 5th cycle is for 2Gb/4Gb.*

6. DEVICE OPERATIONS

6-1. Address Input/Command Input/Data Input

Address input bus operation is for address input to select the memory address. The command input bus operation is for giving command to the memory. The data input bus is for data input to the memory device.

Figure 2. AC Waveforms for Command / Address / Data Latch Timing

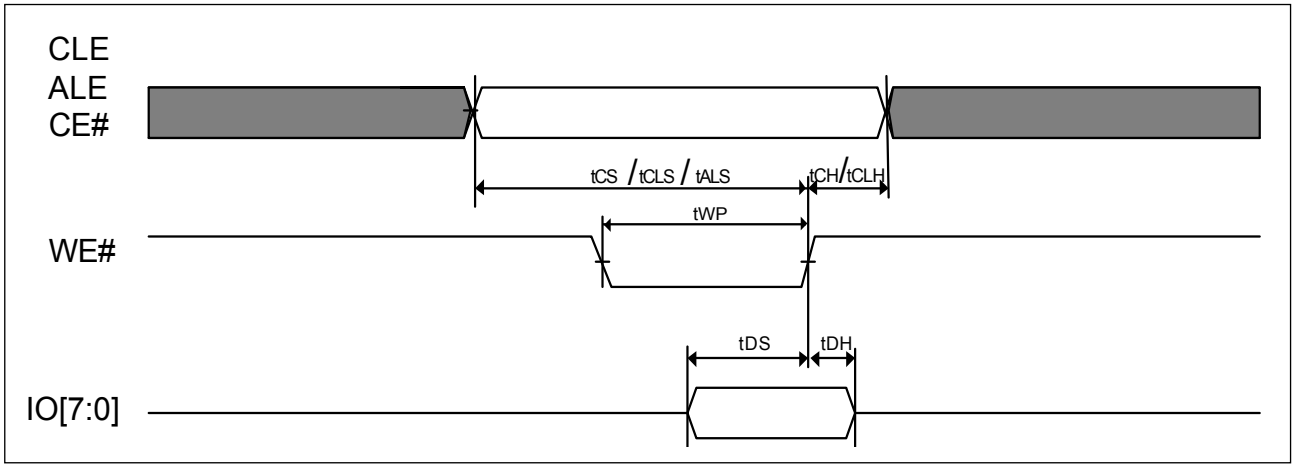


Figure 3. AC Waveforms for Address Input Cycle

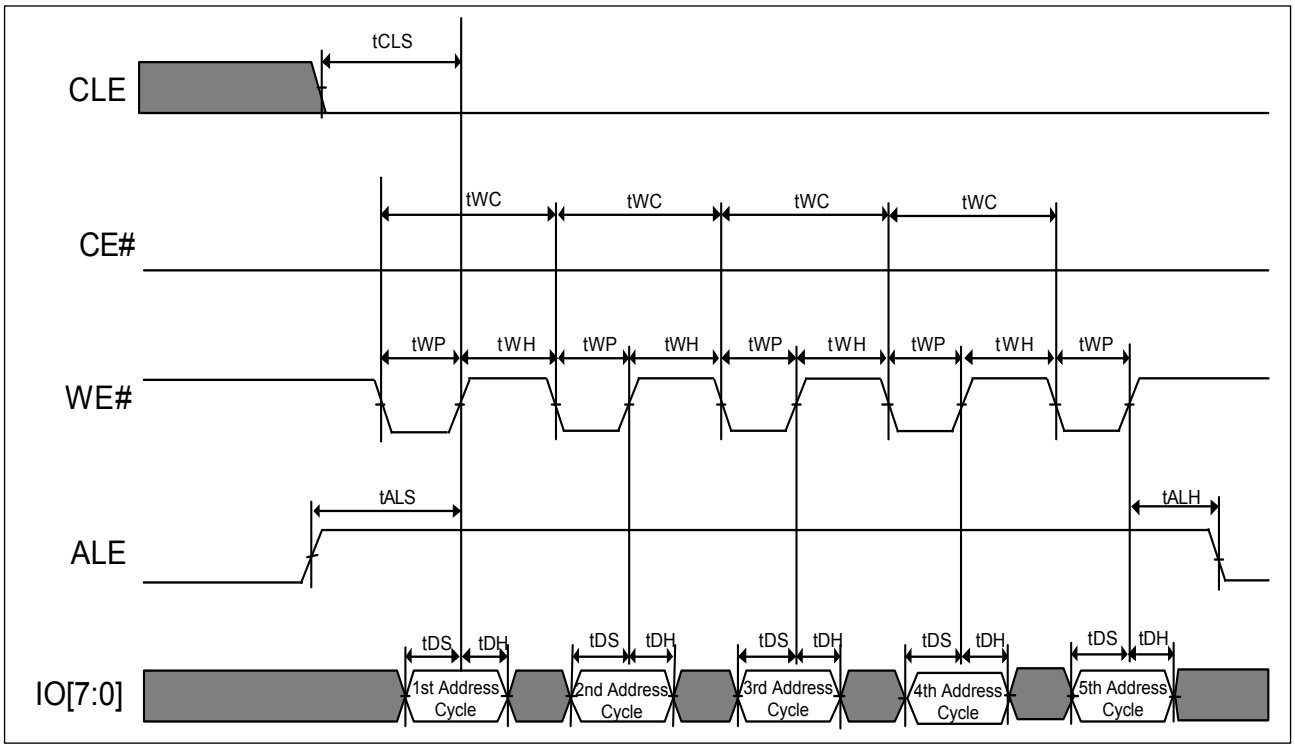


Figure 4. AC Waveforms for Command Input Cycle

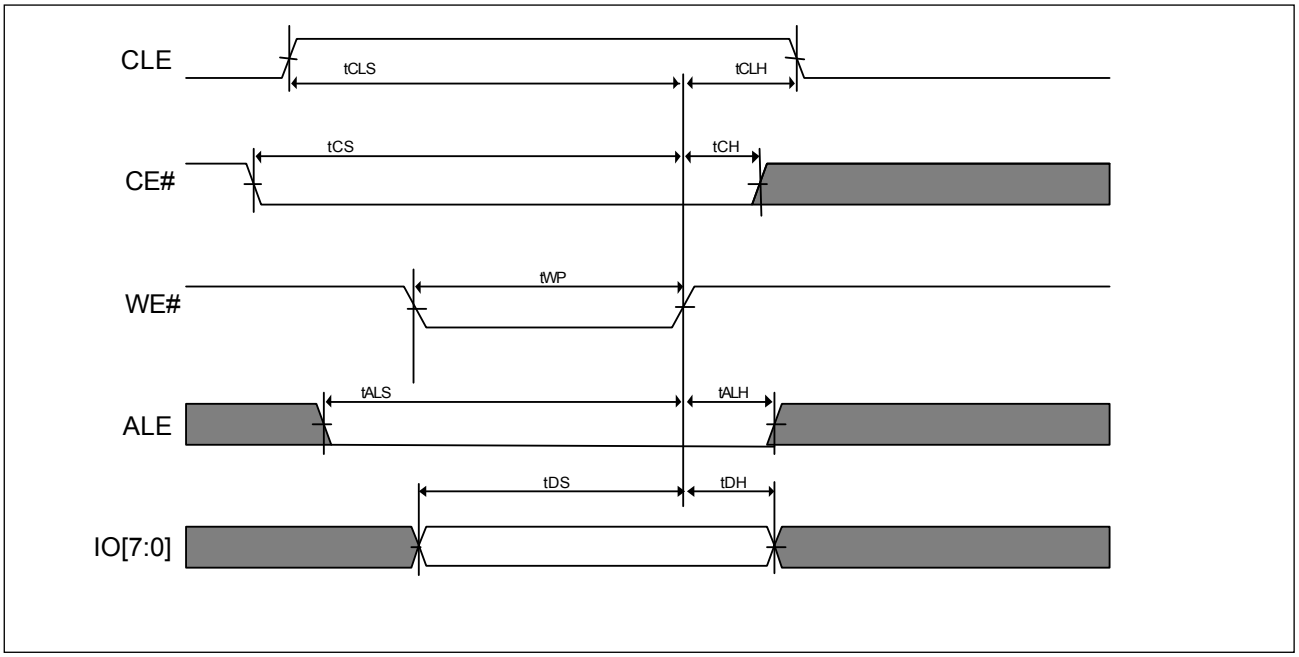
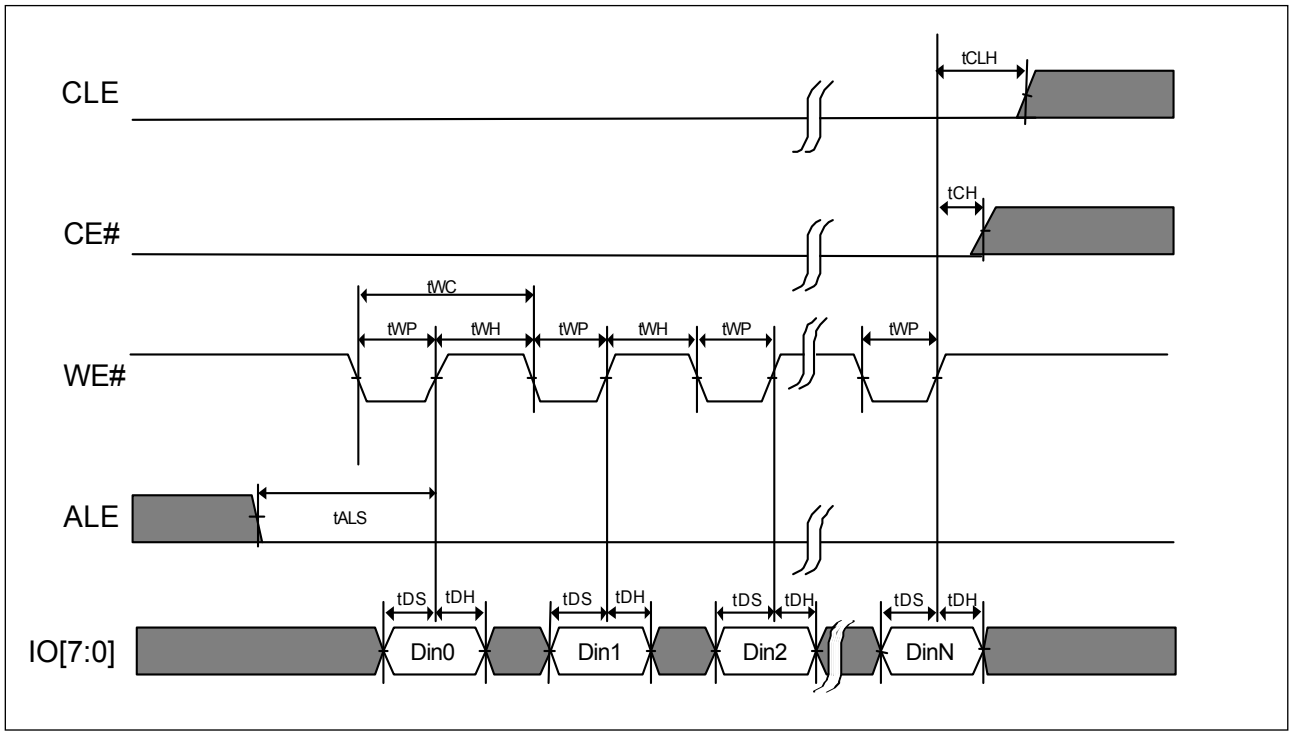


Figure 5. AC Waveforms for Data Input Cycle



6-2. Page Read

The MX30LFxGE8AB array is accessed in Page of 2,112 bytes. External reads begins after the R/B# pin goes to READY.

The Read operation may also be initiated by writing the 00h command and giving the address (column and row address) and being confirmed by the 30h command, the MX30LFxGE8AB begins the internal read operation and the chip enters busy state. The data can be read out in sequence after the chip is ready. Refer to the waveform for Read Operation as below.

If the host side uses a sequential access time (tRC) of less than 30ns, the data can be latched on the next falling edge of RE# as the waveform of EDO mode (**"Figure 9-2. AC Waveforms for Sequential Data Out Cycle (After Read) - EDO Mode"**).

To access the data in the same page randomly, a command of 05h may be written and only column address following and then confirmed by E0h command.

Figure 6. AC Waveforms for Read Cycle

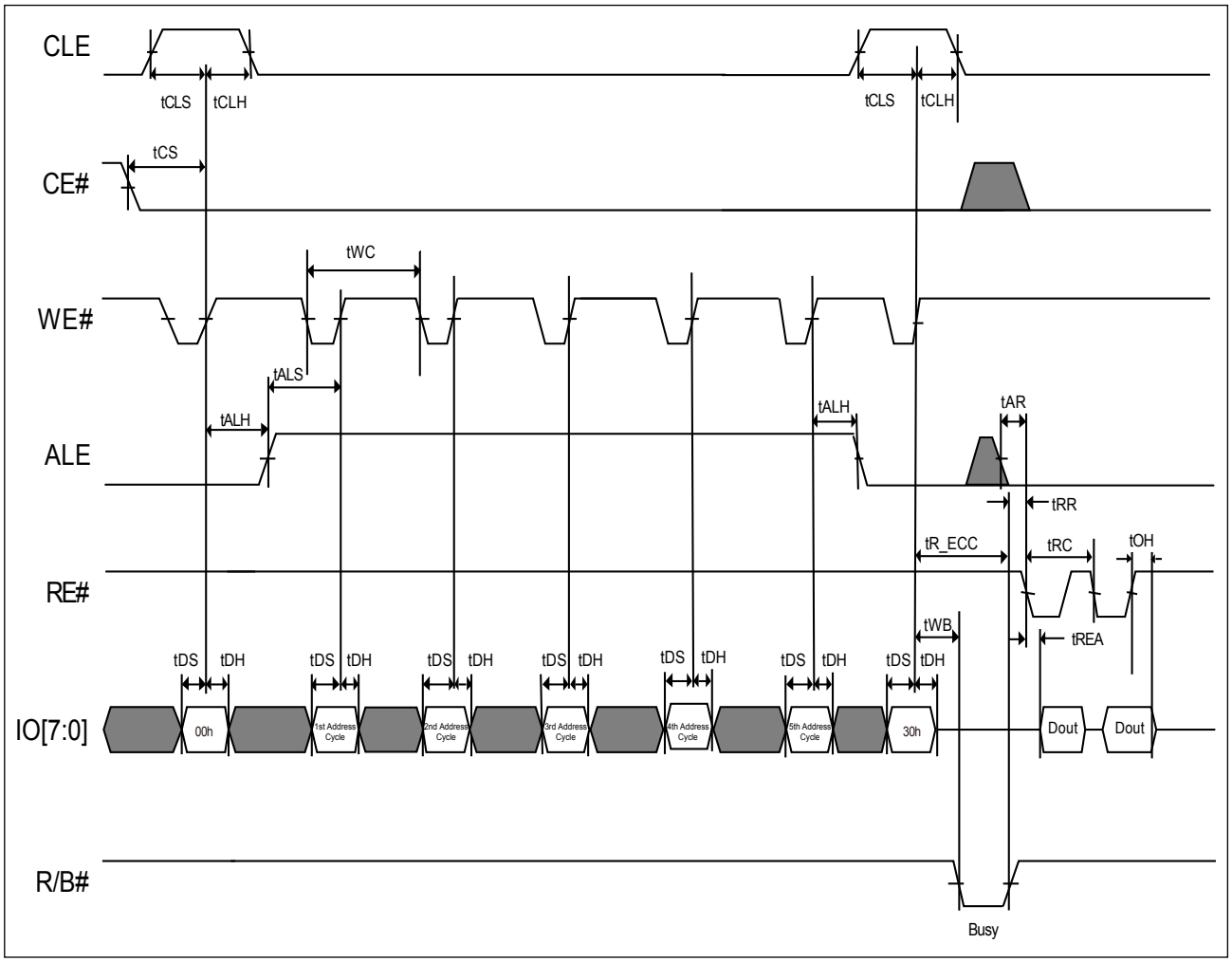


Figure 7. AC Waveforms for Read Operation (Intercepted by CE#)

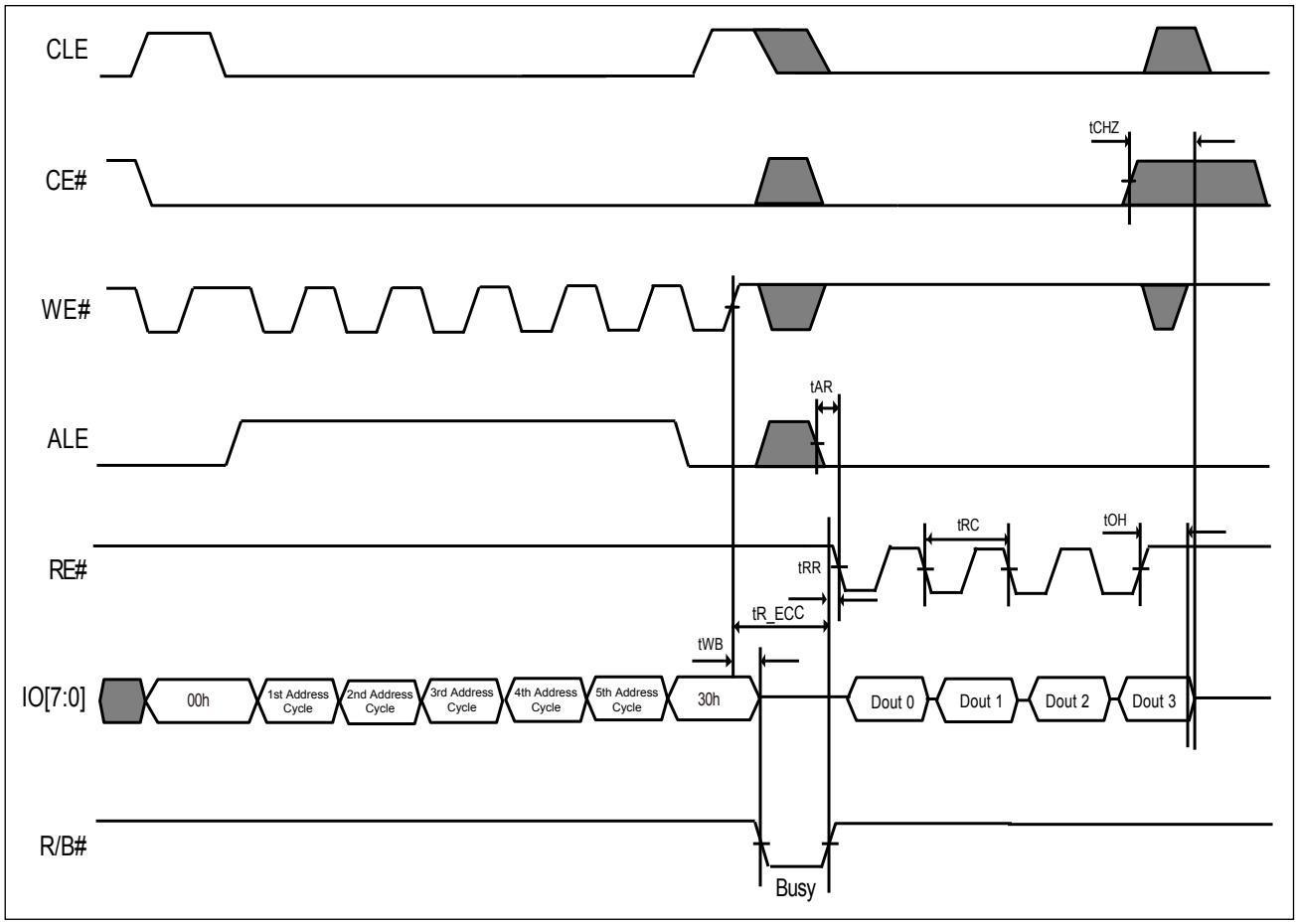
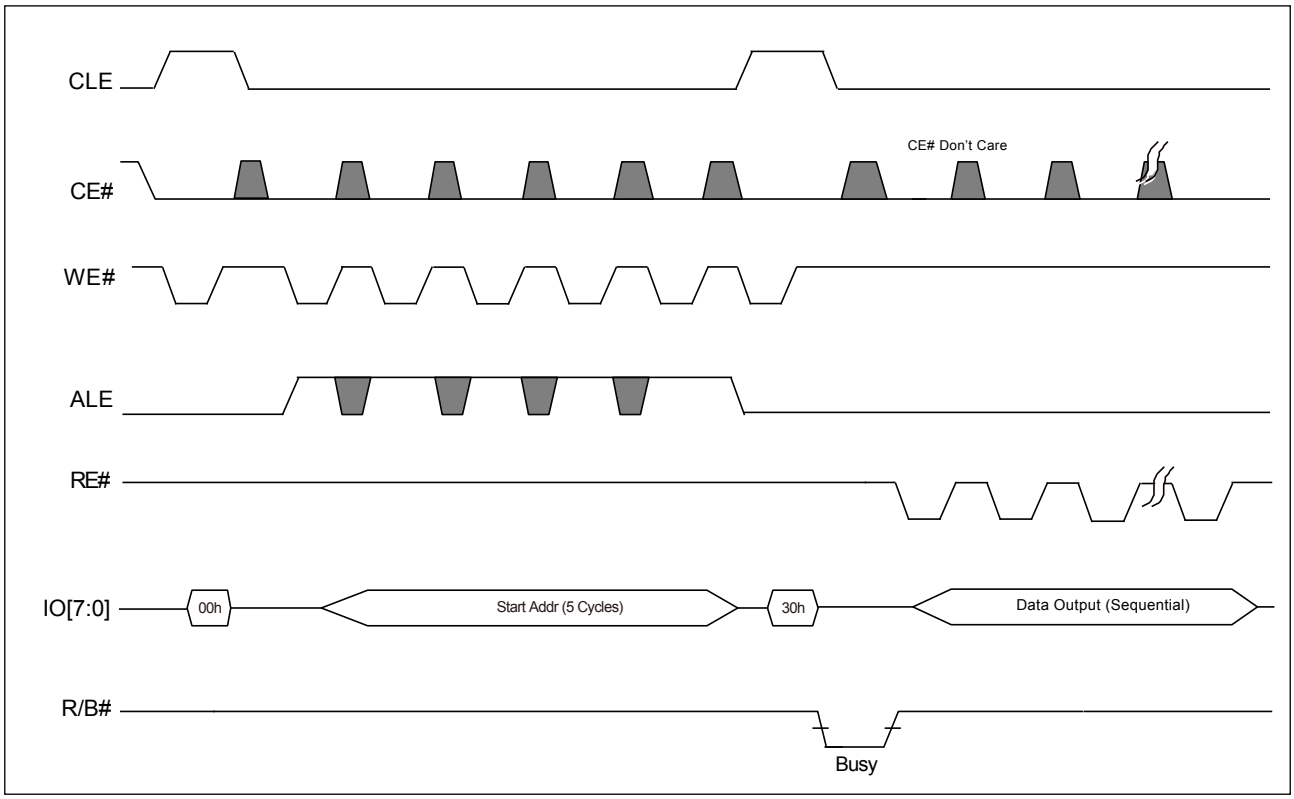


Figure 8. AC Waveforms for Read Operation (with CE# Don't Care)



Note: *The CE# "Don't Care" feature may simplify the system interface, which allows controller to directly download the code from flash device, and the CE# transitions will not stop the read operation during the latency time.*

Figure 9-1. AC Waveforms for Sequential Data Out Cycle (After Read)

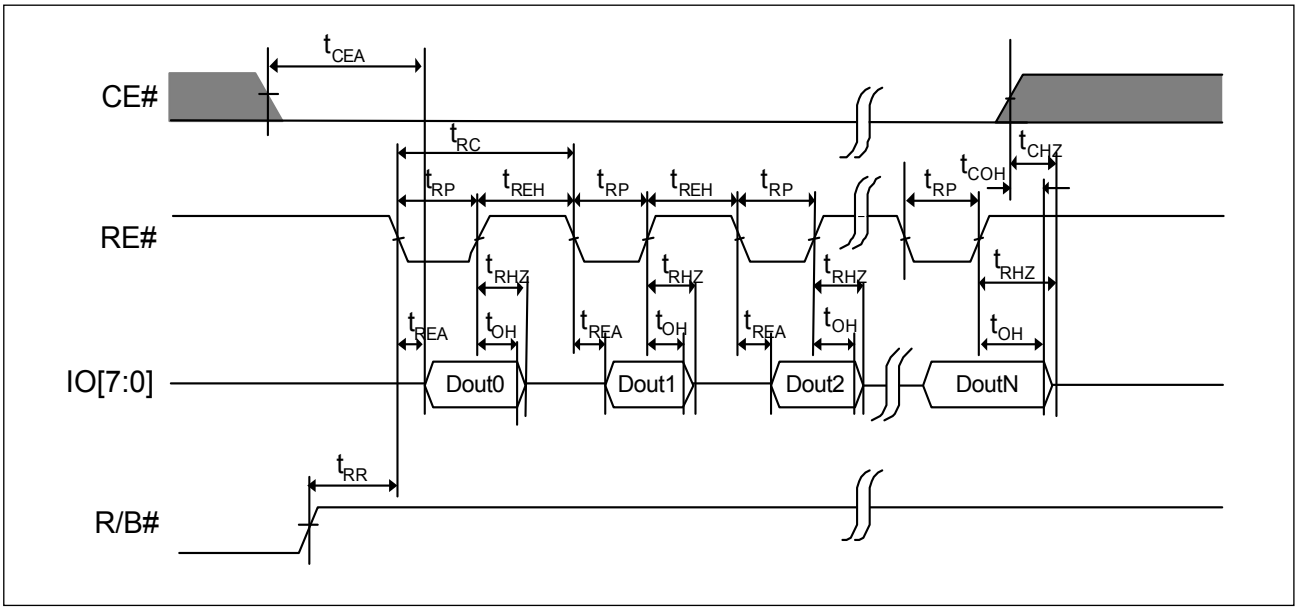


Figure 9-2. AC Waveforms for Sequential Data Out Cycle (After Read) - EDO Mode

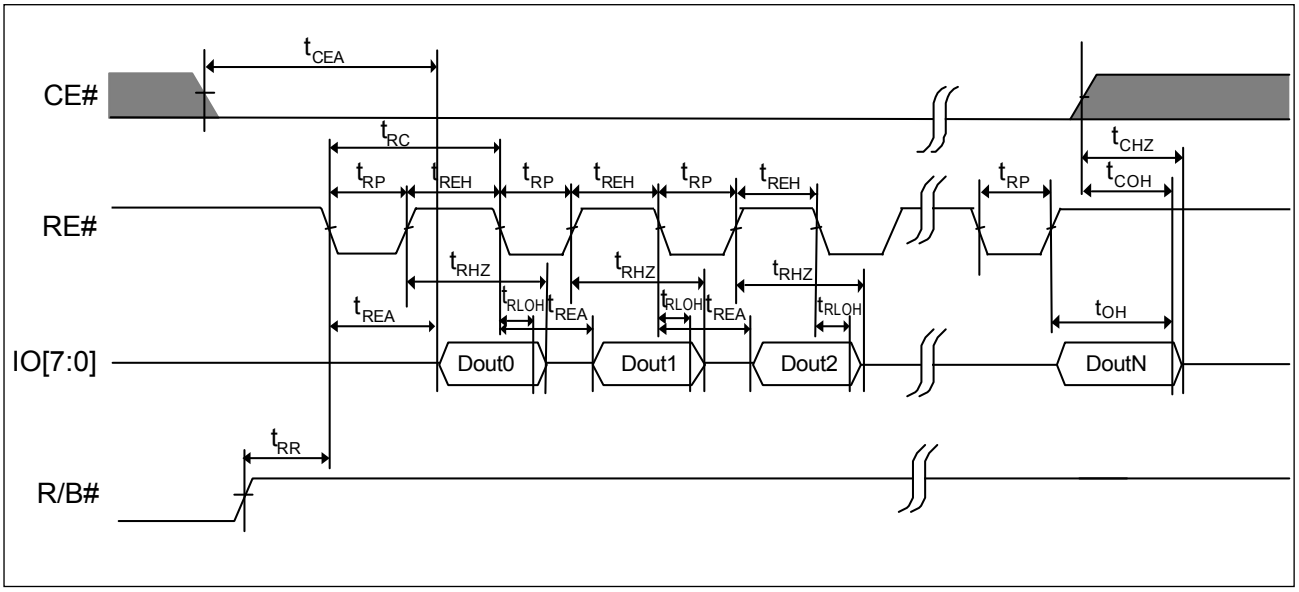
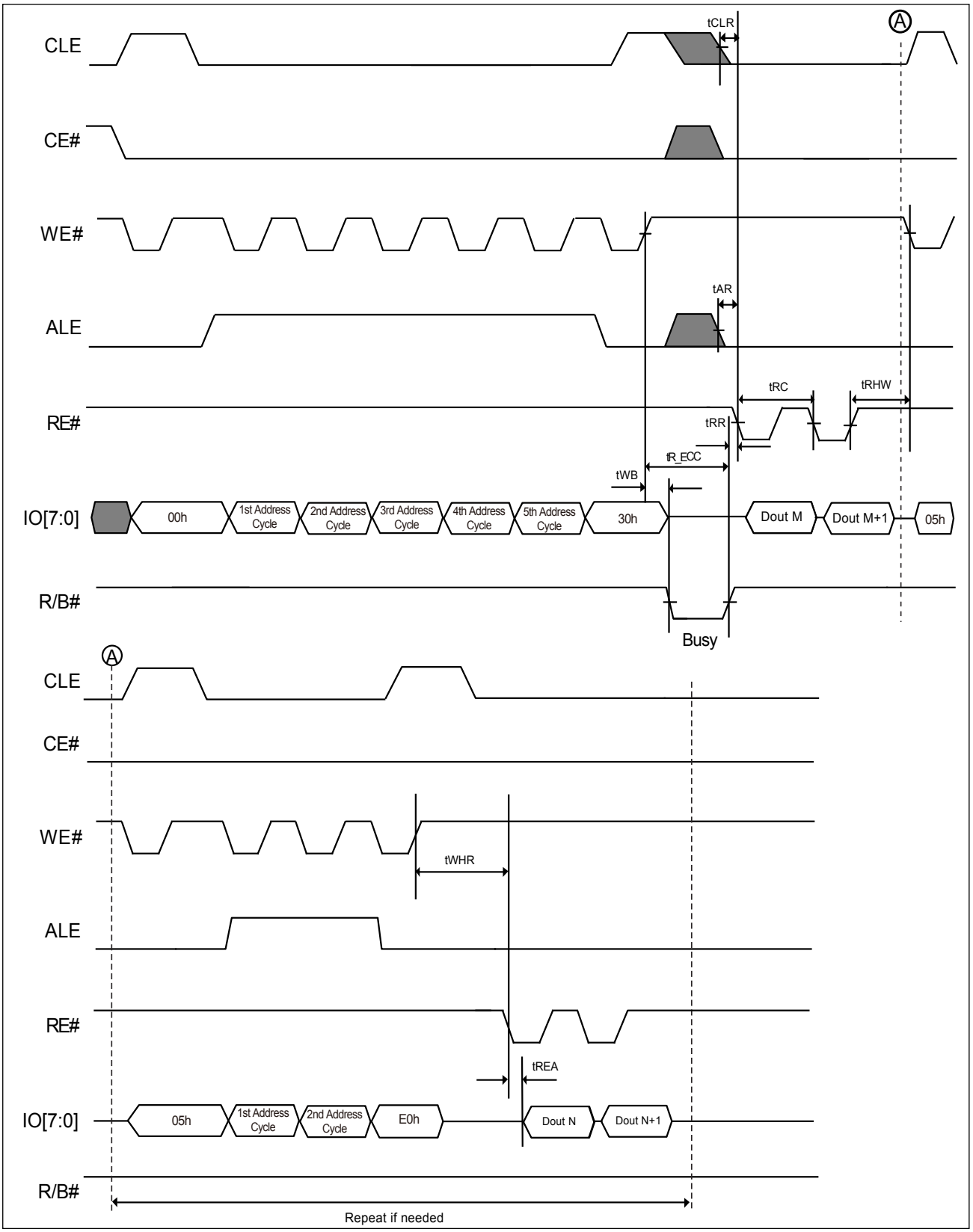


Figure 10. AC Waveforms for Random Data Output



6-3. Page Program

The memory is programmed by page, which is 2,112 bytes. After Program load command (80h) is issued and the row and column address is given, the data will be loaded into the chip sequentially. Random Data Input command (85h) allows multi-data load in non-sequential address. After data load is complete, program confirm command (10h) is issued to start the page program operation. The page program operation in a block should start from the low address to high address (A[17:12]). Partial program in a page is allowed up to 4 times. However, the random data input mode for programming a page is allowed and number of times is not limited.

The status of the program completion can be detected by R/B# pin or Status register bit SR[6].

The program result is shown in the chip status bit (SR[0]). SR[0] = 1 indicates the Page Program is not successful and SR[0] = 0 means the program operation is successful.

During the Page Program progressing, only the read status register command and reset command are accepted, others are ignored.

Figure 11. AC Waveforms for Program Operation after Command 80H

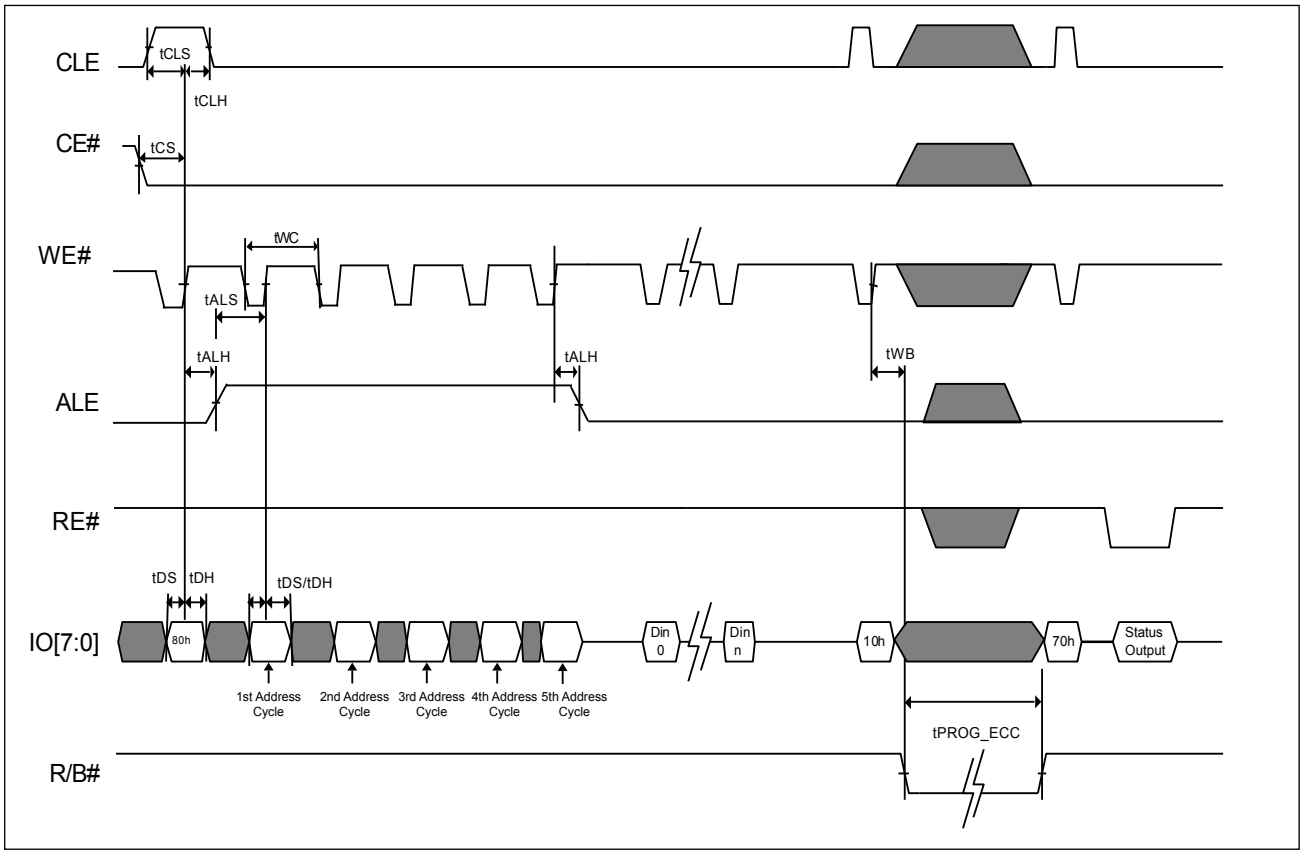
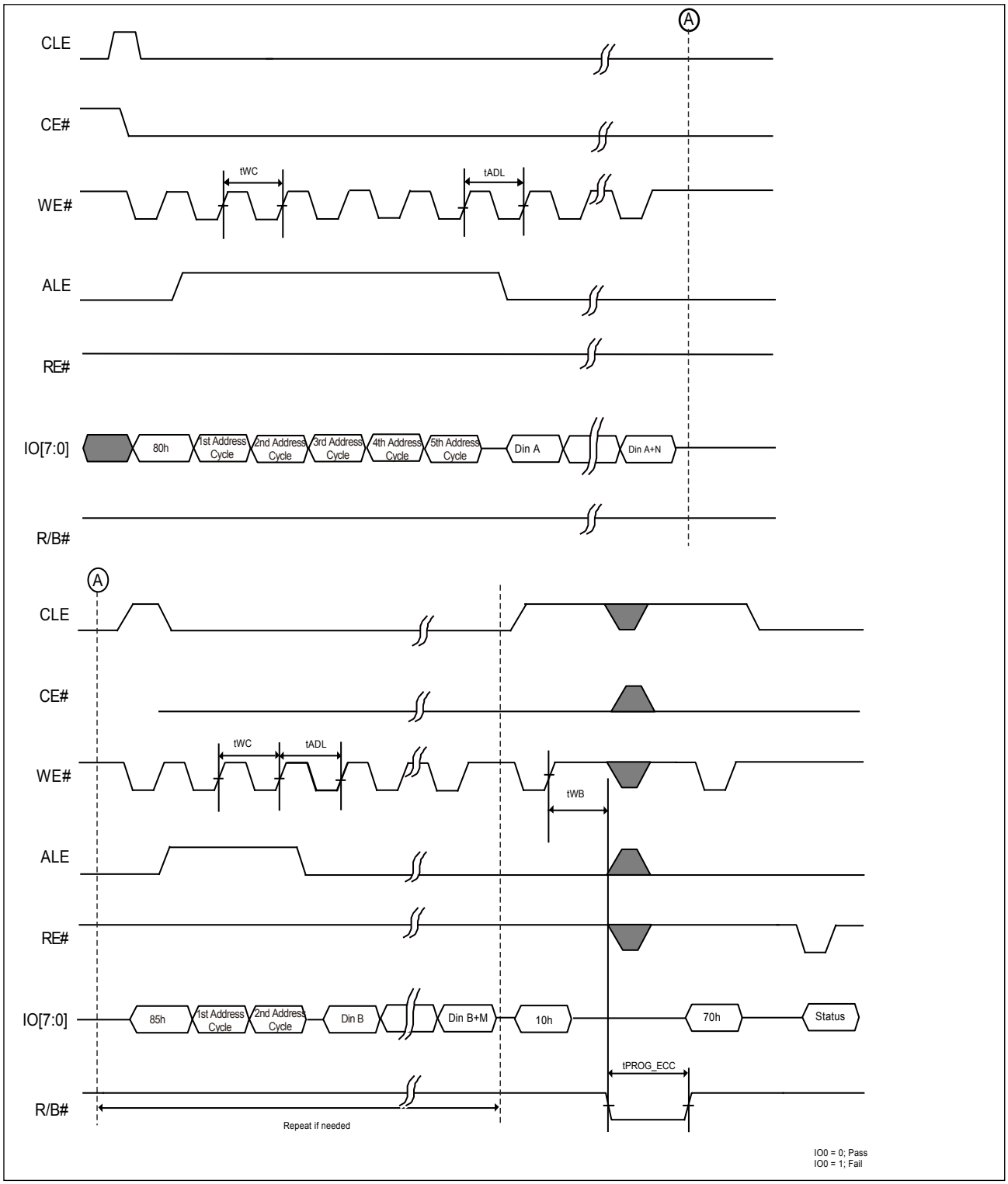
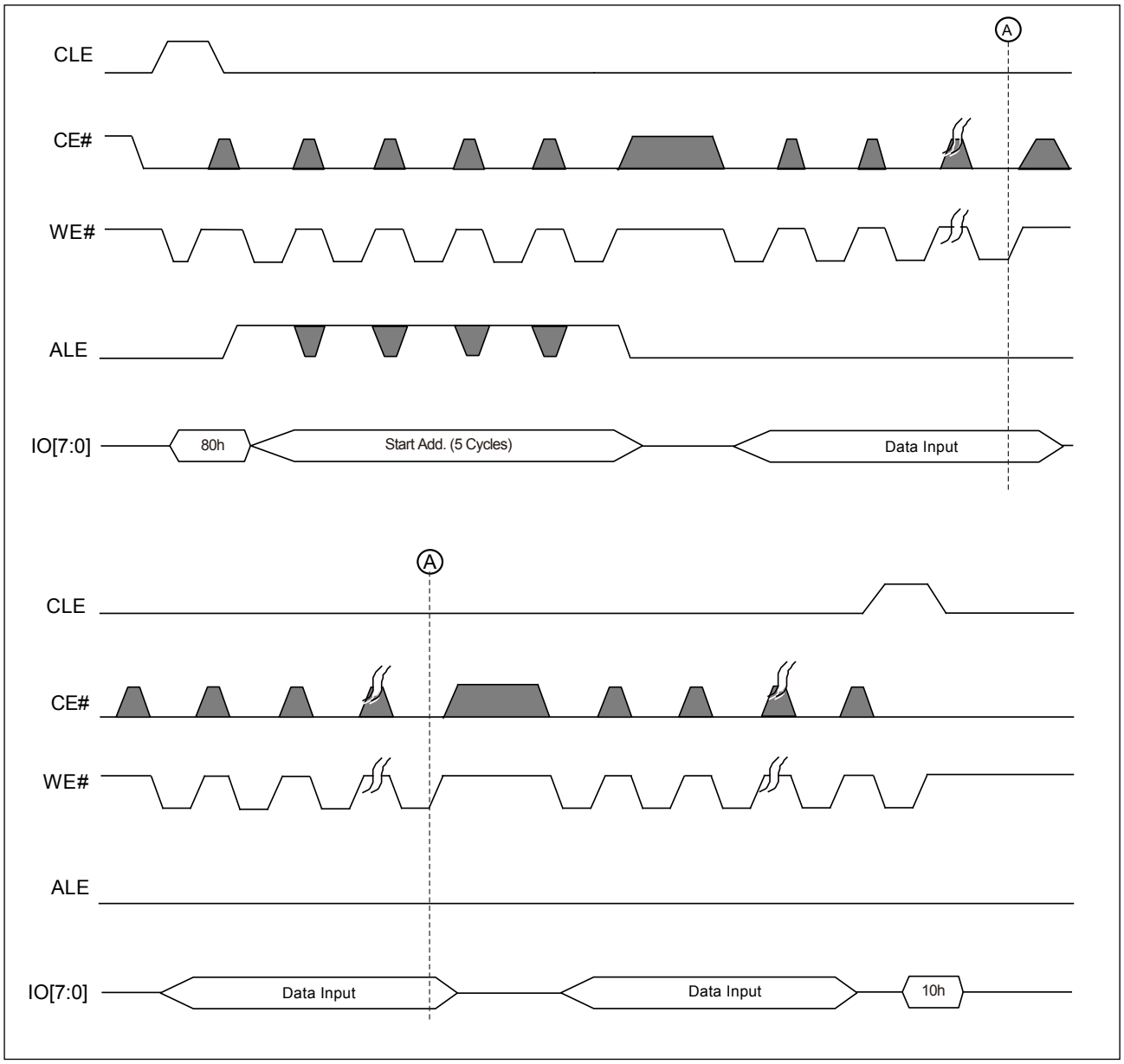


Figure 12. AC Waveforms for Random Data In (For Page Program)



Note: *Random Data In is also supported in cache program.*

Figure 13. AC Waveforms for Program Operation with CE# Don't Care



Note: *The CE# "Don't Care" feature may simplify the system interface, which allows the controller to directly write data into flash device, and the CE# transitions will not stop the program operation during the latency time.*

6-4. Cache Program

The cache program feature enhances the program performance by using the cache buffer of 2,112-byte. The serial data can be input to the cache buffer while the previous data stored in the buffer are programming into the memory cell. Cache Program command sequence is almost the same as page program command sequence. Only the Program Confirm command (10h) is replaced by cache Program command (15h).

After the Cache Program command (15h) is issued. The user can check the status by the following methods.

- R/B# pin

- Cache Status Bit (SR[6] = 0 indicates the cache is busy; SR[6] = 1 means the cache is ready).

The user can issue another Cache Program Command Sequence after the Cache is ready. The user can always monitor the chip state by Ready/Busy Status Bit (SR[5]). The user can issues either program confirm command (10h) or cache program command (15h) for the last page if the user monitor the chip status by issuing Read Status Command (70h).

However, if the user only monitors the R/B# pin, the user needs to issue the program confirm command (10h) for the last page.

The user can check the Pass/Fail Status through P/F Status Bit (SR[0]) and Cache P/F Status Bit (SR[1]). SR[1] represents Pass/Fail Status of the previous page. SR[1] is updated when SR[6] change from 0 to 1 or Chip is ready. SR[0] shows the Pass/Fail status of the current page. It is updated when SR[5] change from "0" to "1" or the end of the internal programming. For more details, please refer to the related waveforms.