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1.8V, 2G/4G-bit NAND Flash Memory

MX30UFxG26(28)AB

Contents

1. FEATURES

- 2G-bit/4G-bit SLC NAND Flash
  - Bus: x8, x16
  - Page size: (2048+112) byte for x8 bus, (1024+56) word for x16 bus
  - Block size: (128K+7K) byte for x8 bus, (64K+3.5K) word for x16 bus
  - Plane size:
    1024-block/plane x 2 for 2Gb
    2048-block/plane x 2 for 4Gb
- **ONFI 1.0 compliant**
- **Multiplexed Command/Address/Data**
- **User Redundancy**
  - 112-byte attached to each page
- **Fast Read Access**
  - Latency of array to register: 25us
  - Sequential read: 25ns
- **Cache Read Support**
- **Page Program Operation**
  - Page program time: 320us (typ.)
- **Cache Program Support**
- **Block Erase Operation**
  - Block erase time: 1ms (typ.)
- **Single Voltage Operation:**
  - VCC: 1.7 ~ 1.95V
- **Low Power Dissipation**
  - Max. 30mA (1.8V)
    Active current (Read/Program/Erase)
- **Sleep Mode**
  - 50uA (Max) standby current
- **Hardware Data Protection:** WP# pin
- **Device Status Indicators**
  - Ready/Busy (R/B#) pin
  - Status Register
- **Chip Enable Don't Care**
  - Simplify System Interface
- **Unique ID Read support (ONFI)**
- **Secure OTP support**
- **Electronic Signature (5 Cycles)**
- **High Reliability**
  - Endurance: typical 100K cycles (with 8-bit ECC per (512+28) Byte)
  - Data Retention: 10 years
- **Wide Temperature Operating Range**
  -40°C to +85°C
- **Package:**
  1) 48-TSOP(I) (12mm x 20mm)
  2) 63-ball 9mmx11mm VFBGA
  All packaged devices are RoHS Compliant and Halogen-free.

2. GENERAL DESCRIPTIONS

The MX30UFxG26(28)AB are 2Gb to 4Gb SLC NAND Flash memory devices. Its standard NAND Flash features and reliable quality of typical P/E cycles 100K (with ECC), which make it most suitable for embedded system code and data storage.

The product family requires 8-bit ECC per 540B.

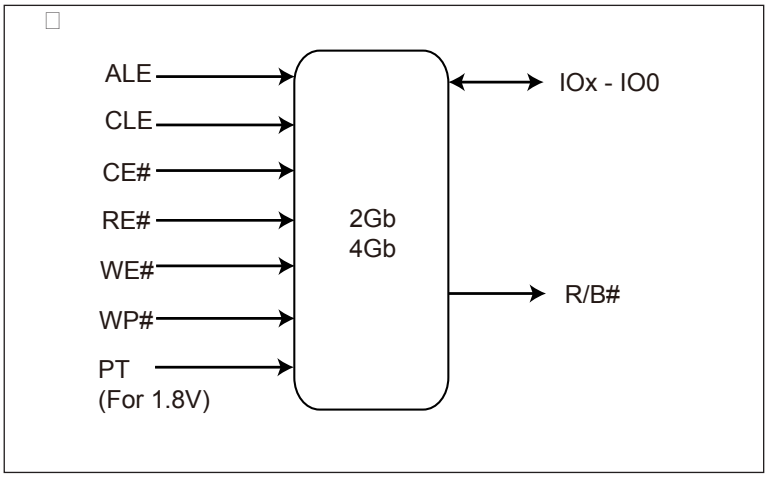
This device is typically accessed in pages of 2,160 bytes (x8) or 1080 words (x16), both for read and for program operations.

The device's array is organized as thousands of blocks, which is composed by 64 pages of (1024+32) words in two NAND strings structure with 32 serial connected cells in each string. Each page has an additional 56 words for ECC and other purposes. The device has an on-chip buffer of 2160 bytes or 1080 words (x16) for data load and access.

The Cache Read Operation of the MX30UFxG26(28)AB enables first-byte read-access latency of 25us and sequential read of 25ns and the latency time of next sequential page will be shorten from tR to tRCBSY.

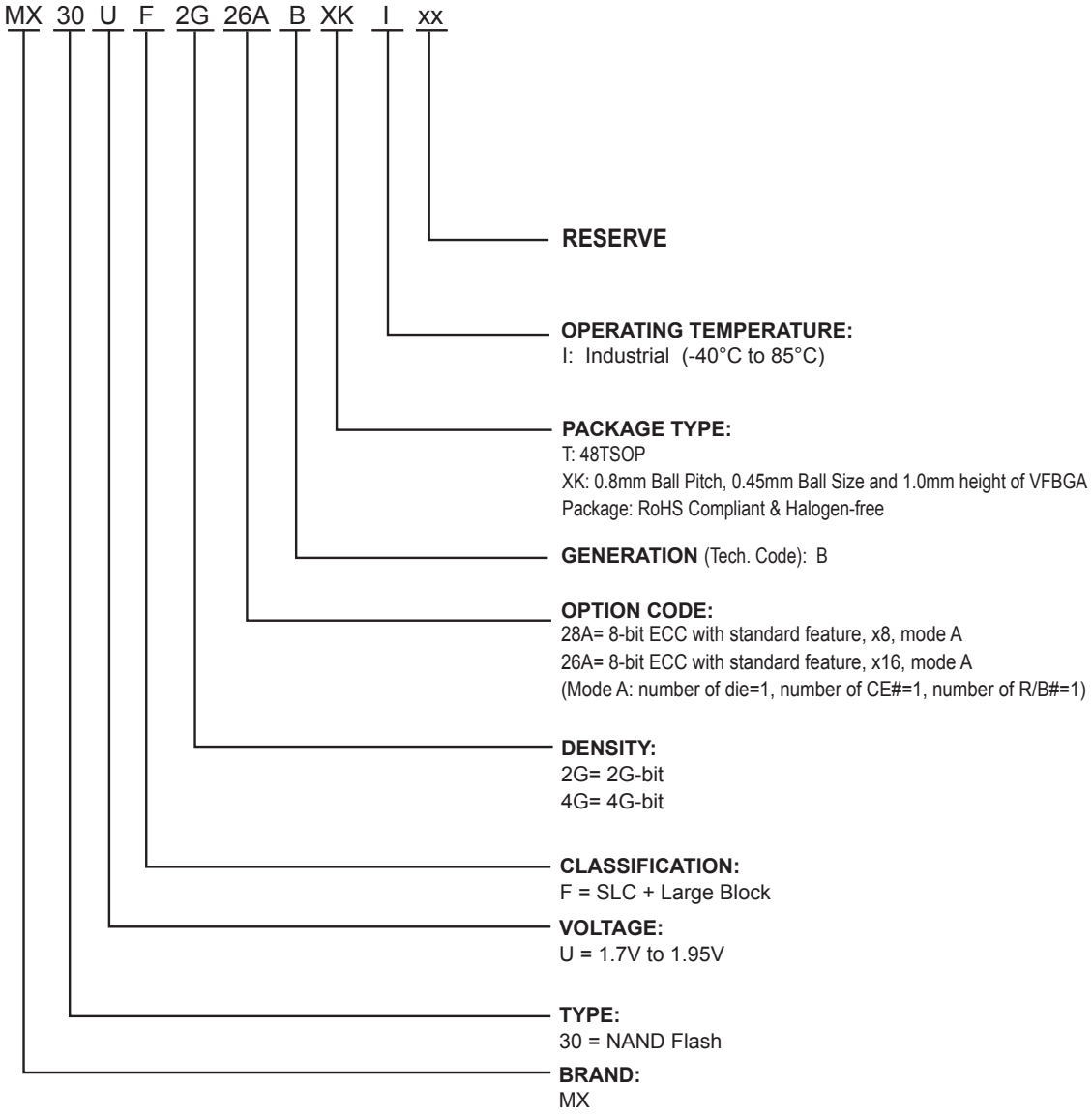
The MX30UFxG26(28)AB power consumption is 30mA during all modes of operations (Read/Program/Erase), and 50uA in standby mode.

Figure 1. Logic Diagram



2-1. ORDERING INFORMATION

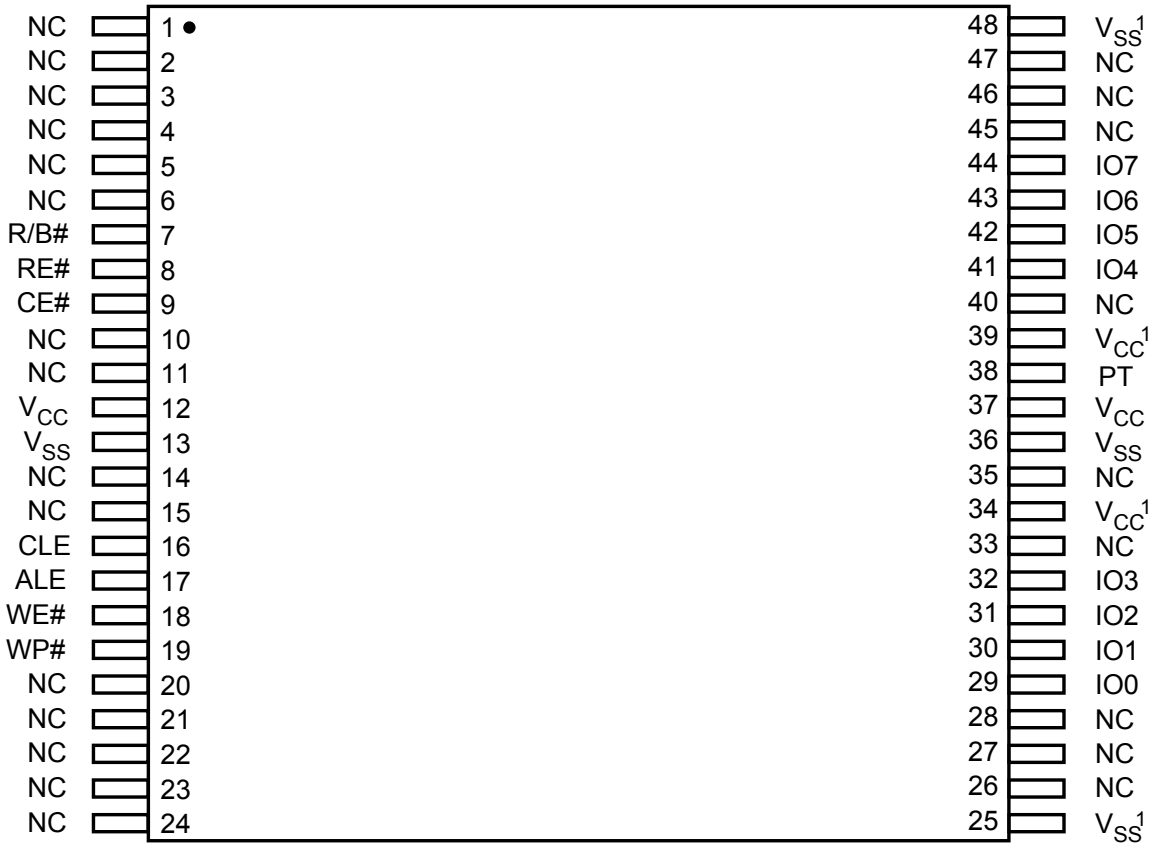
Part Name Description



Part Number	Density	Organization	VCC Range	Package	Temperature Grade
MX30UF2G28AB-XKI	2Gb	x8	1.8V	63-VFBGA	Industrial
MX30UF2G26AB-XKI	2Gb	x16	1.8V	63-VFBGA	Industrial
MX30UF2G28AB-TI	2Gb	x8	1.8V	48-TSOP	Industrial
MX30UF4G28AB-XKI	4Gb	x8	1.8V	63-VFBGA	Industrial
MX30UF4G26AB-XKI	4Gb	x16	1.8V	63-VFBGA	Industrial
MX30UF4G28AB-TI	4Gb	x8	1.8V	48-TSOP	Industrial

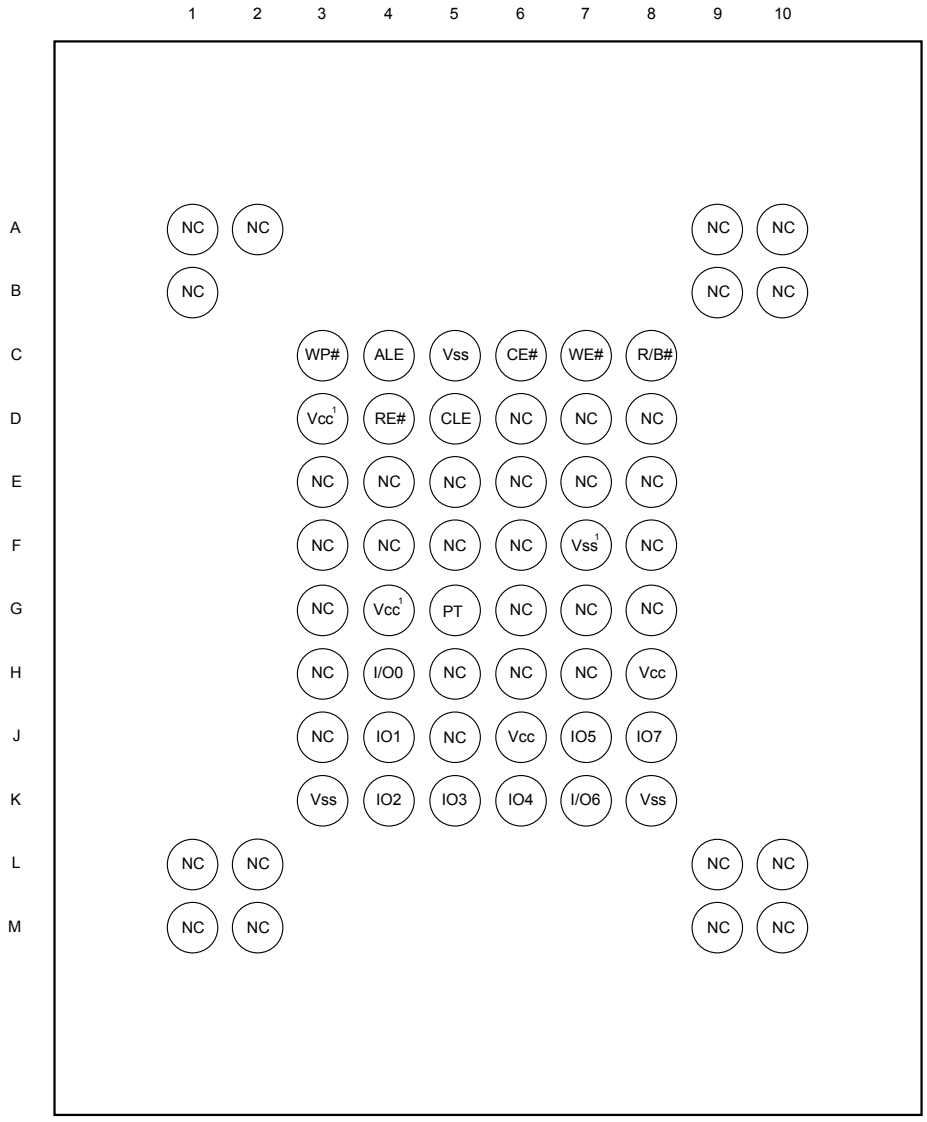
3. PIN CONFIGURATIONS

48-TSOP



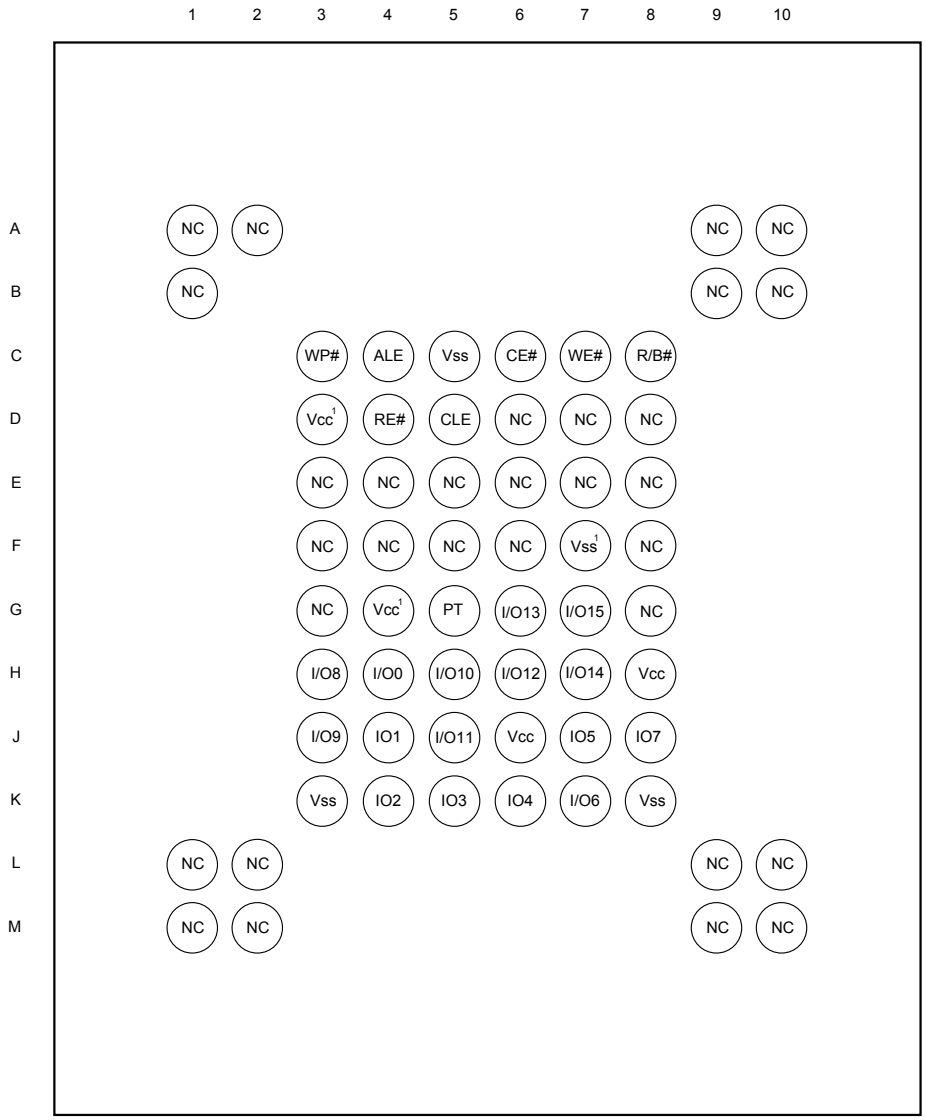
Note 1. *These pins might not be connected internally. However, it is recommended to connect these pins to power(or ground) as designated for ONFI compatibility.*

63-ball 9mmx11mm VFBGA (x8)



Note 1. *These pins might not be connected internally; however, it is recommended to connect these pins to power (or ground) as designated for ONFI compatibility.*

63-ball 9mmx11mm VFBGA (x16)



Note 1. *These pins might not be connected internally; however, it is recommended to connect these pins to power (or ground) as designated for ONFI compatibility.*

3-1. PIN DESCRIPTIONS

SYMBOL	PIN NAME
IOx - IO0	Data I/O port: IO7-IO0 for x8 device, IO15-IO0 for x16 device
CE#	Chip Enable (Active Low)
RE#	Read Enable (Active Low)
WE#	Write Enable (Active Low)
CLE	Command Latch Enable
ALE	Address Latch Enable
WP#	Write Protect (Active Low)
R/B#	Ready/Busy (Open Drain)
PT	Protection (Active High) for entire chip protection. A weak pull-down internally
VSS	Ground
VCC	Power Supply for Device Operation
NC	Not Connected Internally

PIN FUNCTIONS

The MX30UFxG26(28)AB device is a sequential access memory that utilizes multiplexing input of Command/Address/Data.

I/O PORT: IOx - IO0

The IOx to IO0 pins are for address/command input and data output to/from the device. IO7-IO0 pins are for x8 device, IO15-IO0 pins are for x16 device.

CHIP ENABLE: CE#

The device goes into low-power Standby Mode when CE# goes high during a read operation and not at busy stage.

The CE# goes low to enable the device to be ready for standard operation. When the CE# goes high, the device is deselected. However, when the device is at busy stage, the device will not go to standby mode when CE# pin goes high.

READ ENABLE: RE#

The RE# (Read Enable) allows the data to be output by a tREA time after the falling edge of RE#. The internal address counter is automatically increased by one at the falling edge of RE#.

WRITE ENABLE: WE#

When the WE# goes low, the address/data/command are latched at the rising edge of WE#.

COMMAND LATCH ENABLE: CLE

The CLE controls the command input. When the CLE goes high, the command data is latched at the rising edge of the WE#.

ADDRESS LATCH ENABLE: ALE

The ALE controls the address input. When the ALE goes high, the address is latched at the rising edge of WE#.

WRITE PROTECT: WP#

The WP# signal keeps low and then the memory will not accept the program/erase operation. It is recommended to keep WP# pin low during power on/off sequence. Please refer to the waveform of "Power On/Off Sequence".

READY/Busy: R/B#

The R/B# is an open-drain output pin. The R/B# outputs the ready/busy status of read/program/erase operation of the device. When the R/B# is at low, the device is busy for read or program or erase operation. When the R/B# is at high, the read/program/erase operation is finished.

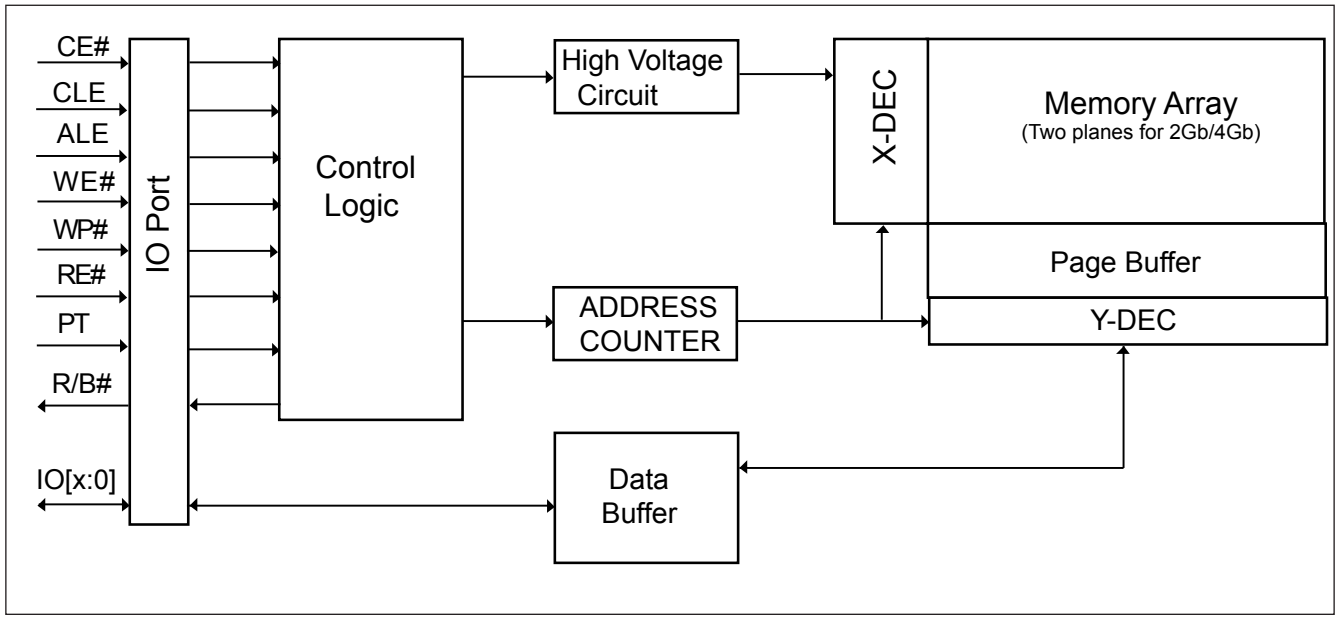
Please refer to **Section 9-1** for details.

PROTECTION: PT

The PT pin is the hardware method to protect the whole chip from program/erase operation. When the PT pin is at high at power-on, the whole chip is protected even the WP# is at high; the un-protect command and procedure is necessary before any program/erase operation. When the PT pin is connected to low or floating, the Protection function is disabled.

Please refer to **Section - Block Protection** for details.

4. BLOCK DIAGRAM



5. SCHEMATIC CELL LAYOUT AND ADDRESS ASSIGNMENT

The device is divided into two planes for 2Gb and 4Gb, which is composed by 64 pages of (2,048+112)-byte in two NAND strings structure with 32 serial connected cells in each string. Each page has an additional 112 bytes for ECC and other purposes. The device has an on-chip buffer of 2,160 bytes for data load and access. Each 2K-Byte page has the two area, one is the main area which is 2048-bytes and the other is spare area which is 112-byte.

There are five (for 2Gb/4Gb) address cycles for the address allocation, please refer to the lable below.

Table 1-1. Address Allocation (for x8): MX30UFxG28AB

Addresses	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Column address - 1st cycle	A7	A6	A5	A4	A3	A2	A1	A0
Column address - 2nd cycle	L	L	L	L	A11	A10	A9	A8
Row address - 3rd cycle	A19	A18[1]	A17	A16	A15	A14	A13	A12
Row address - 4th cycle	A27	A26	A25	A24	A23	A22	A21	A20
Row address - 5th cycle	L	L	L	L	L	L	A29[2]	A28

Notes:

1. *A18 is the plane selection for 2Gb/4Gb.*
2. *A28 is for 2Gb and 4Gb.*
3. *A29 is for 4Gb, "L" (Low) for 2Gb.*
4. *The 5th cycle is for the 2Gb/4Gb.*

Table 1-2. Address Allocation (for x16): MX30UFxG26AB

Addresses	IO15-IO8	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Column address - 1st cycle	L	A7	A6	A5	A4	A3	A2	A1	A0
Column address - 2nd cycle	L	L	L	L	L	L	A10	A9	A8
Row address - 3rd cycle	L	A18	A17[1]	A16	A15	A14	A13	A12	A11
Row address - 4th cycle	L	A26	A25	A24	A23	A22	A21	A20	A19
Row address - 5th cycle[4]	L	L	L	L	L	L	L	A28[3]	A27[2]

Notes:

1. *A17 is the plane selection for 2Gb/4Gb.*
2. *A27 is for 2Gb and 4Gb.*
3. *A28 is for 4Gb, "L" (Low) for 2Gb.*
4. *The 5th cycle is for the 2Gb/ 4Gb.*

6. DEVICE OPERATIONS

6-1. Address Input/Command Input/Data Input

Address input bus operation is for address input to select the memory address. The command input bus operation is for giving command to the memory. The data input bus is for data input to the memory device.

Figure 2. AC Waveforms for Command / Address / Data Latch Timing

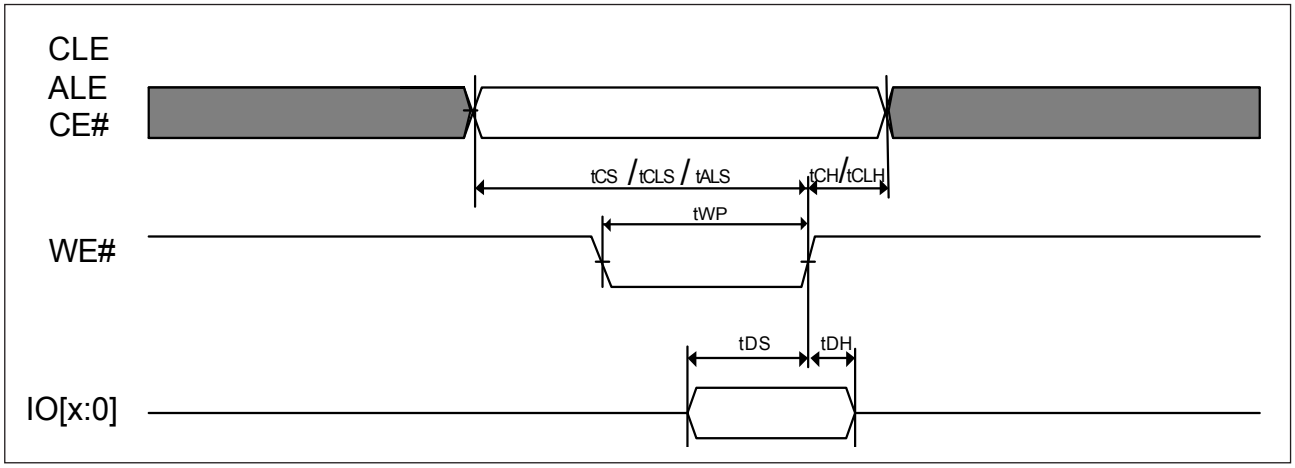


Figure 3. AC Waveforms for Address Input Cycle

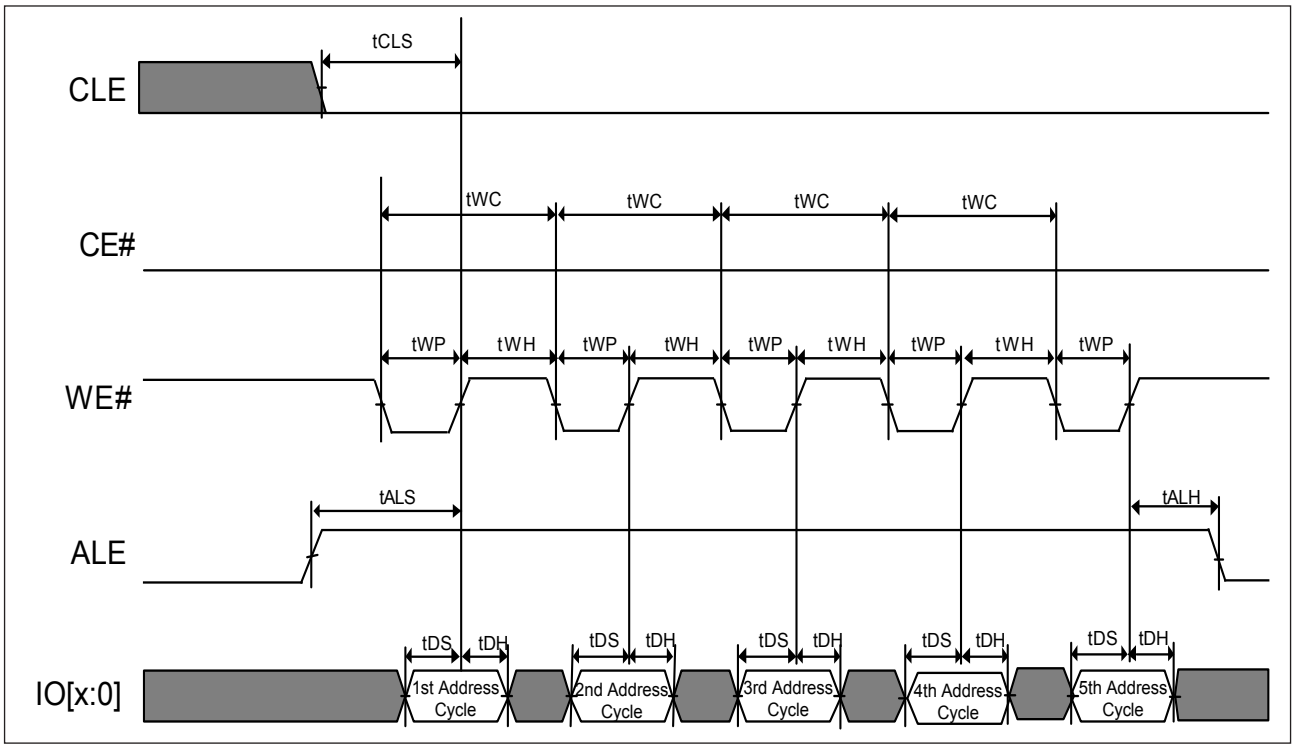


Figure 4. AC Waveforms for Command Input Cycle

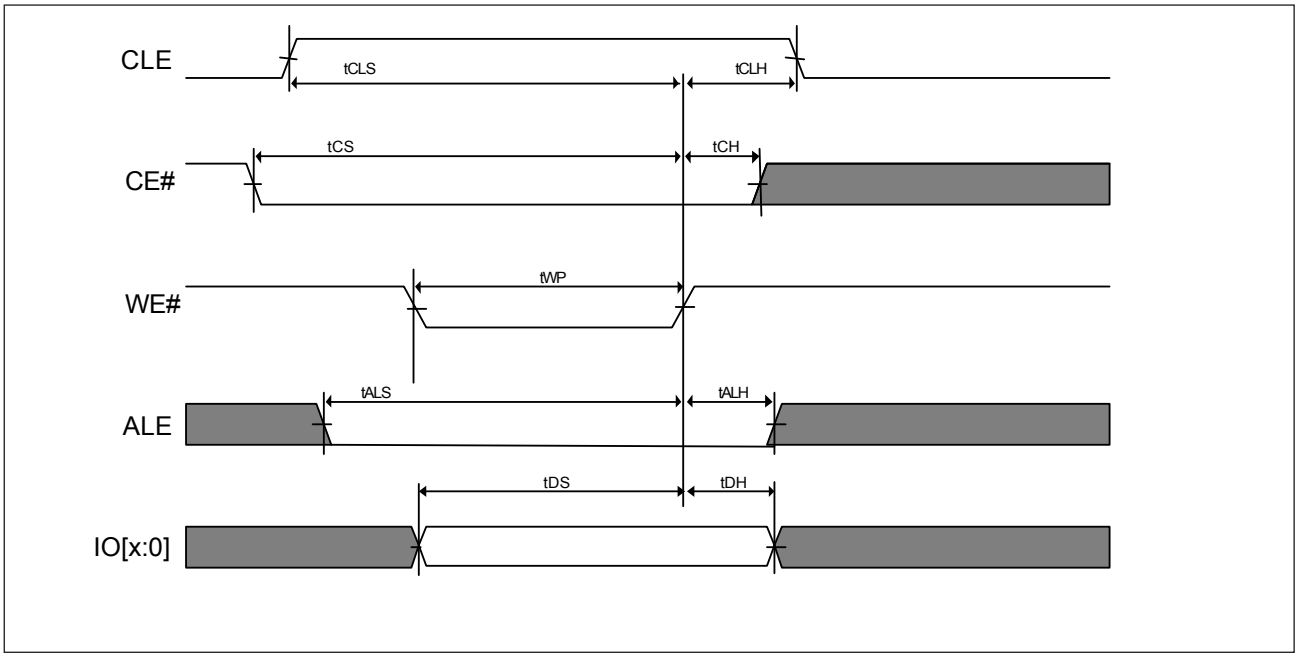
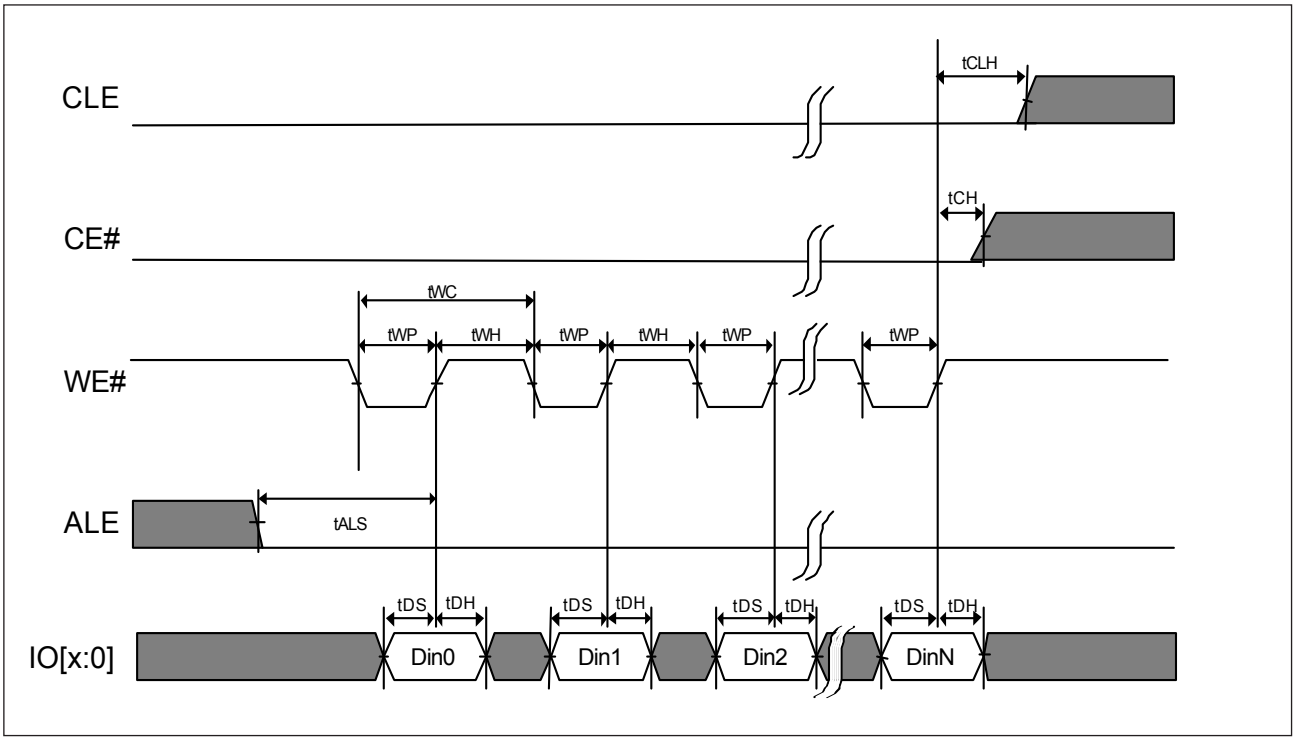


Figure 5. AC Waveforms for Data Input Cycle



6-2. Page Read

The MX30UFxG26(28)AB array is accessed in Page of 2160 bytes or 1,080 words. External reads begins after the R/B# pin goes to READY.

The Read operation may also be initiated by writing the 00h command and giving the address (column and row address) and being confirmed by the 30h command, the device begins the internal read operation and the chip enters busy state. The data can be read out in sequence after the chip is ready. Refer to the waveform for Read Operation as below.

If the host side uses a sequential access time (tRC) of less than 30ns, the data can be latched on the next falling edge of RE# as the waveform of EDO mode (**Figure 9-2**).

To access the data in the same page randomly, a command of 05h may be written and only column address following and then confirmed by E0h command.

Figure 6. AC Waveforms for Read Cycle

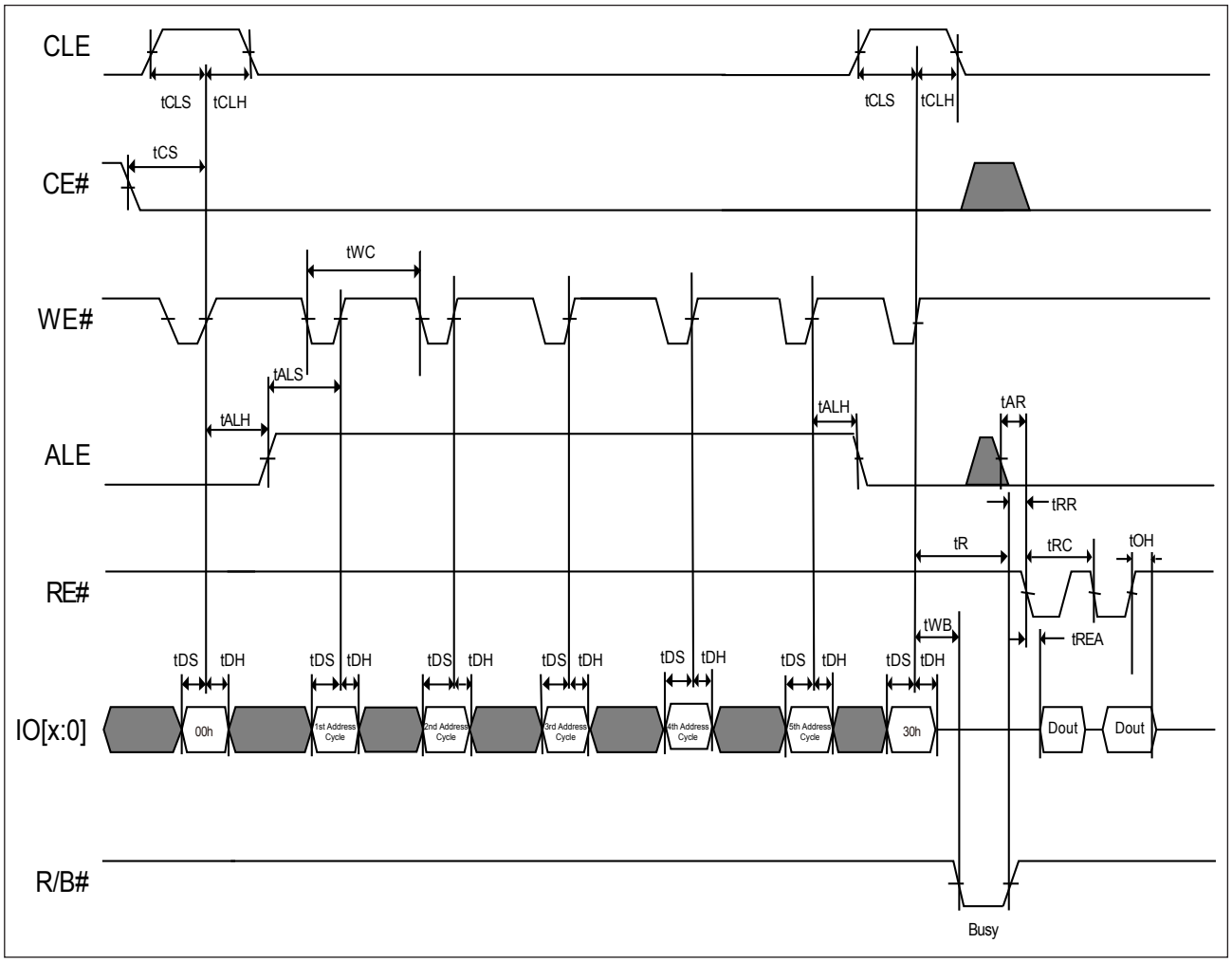


Figure 7. AC Waveforms for Read Operation (Intercepted by CE#)

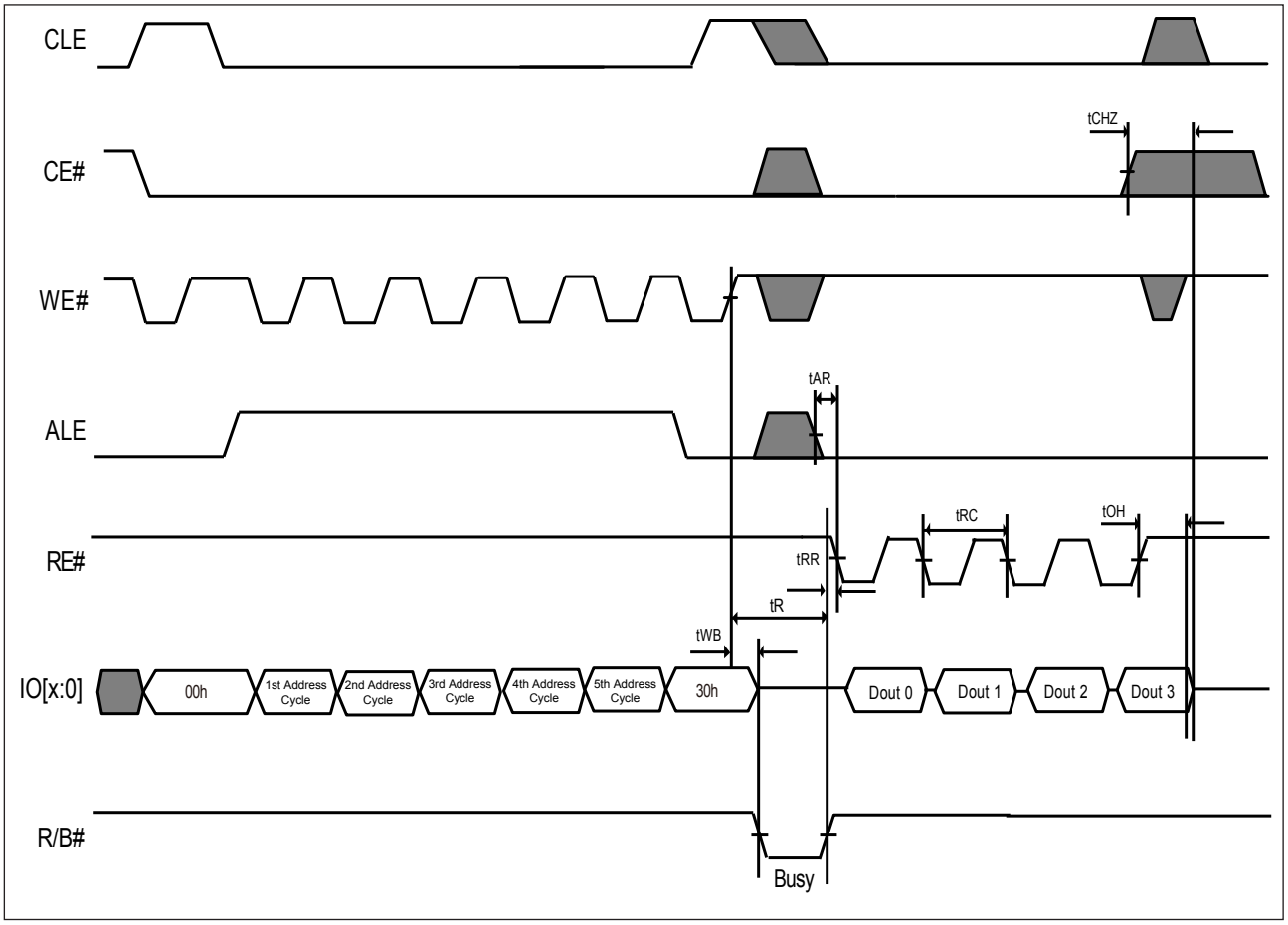
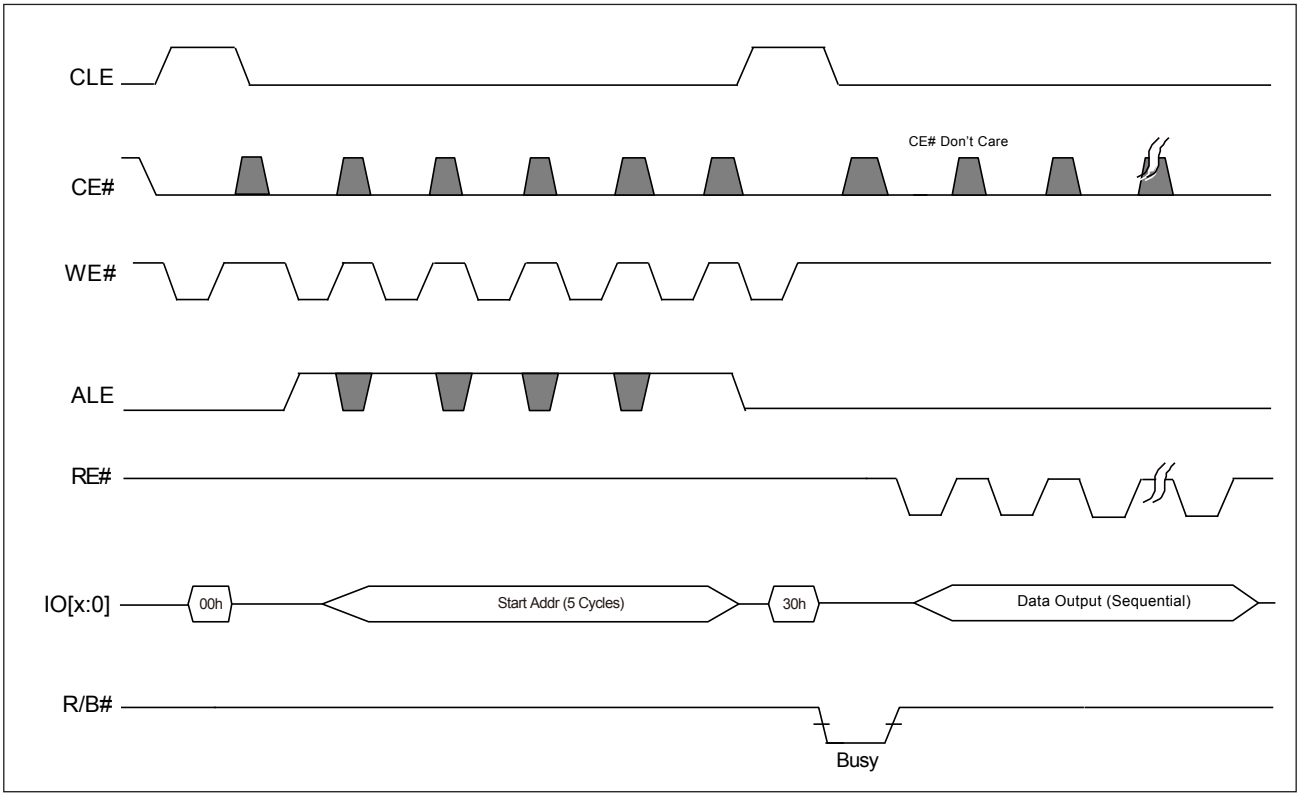


Figure 8. AC Waveforms for Read Operation (with CE# Don't Care)



Note: *The CE# "Don't Care" feature may simplify the system interface, which allows controller to directly download the code from flash device, and the CE# transitions will not stop the read operation during the latency time.*

Figure 9-1. AC Waveforms for Sequential Data Out Cycle (After Read)

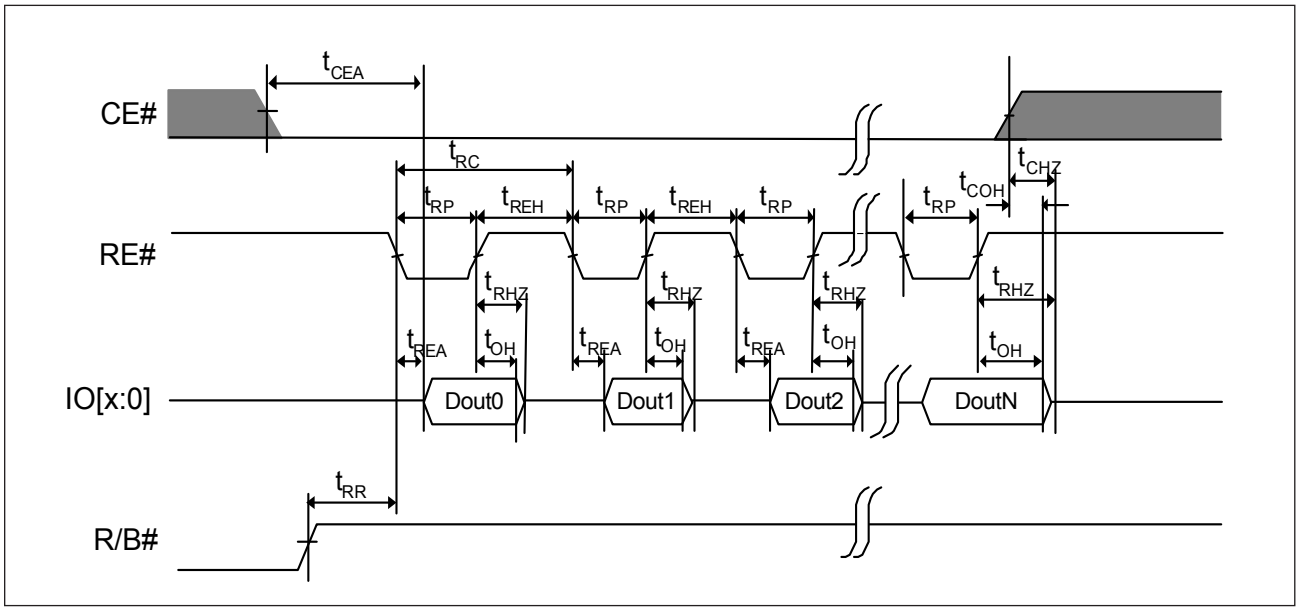


Figure 9-2. AC Waveforms for Sequential Data Out Cycle (After Read) - EDO Mode

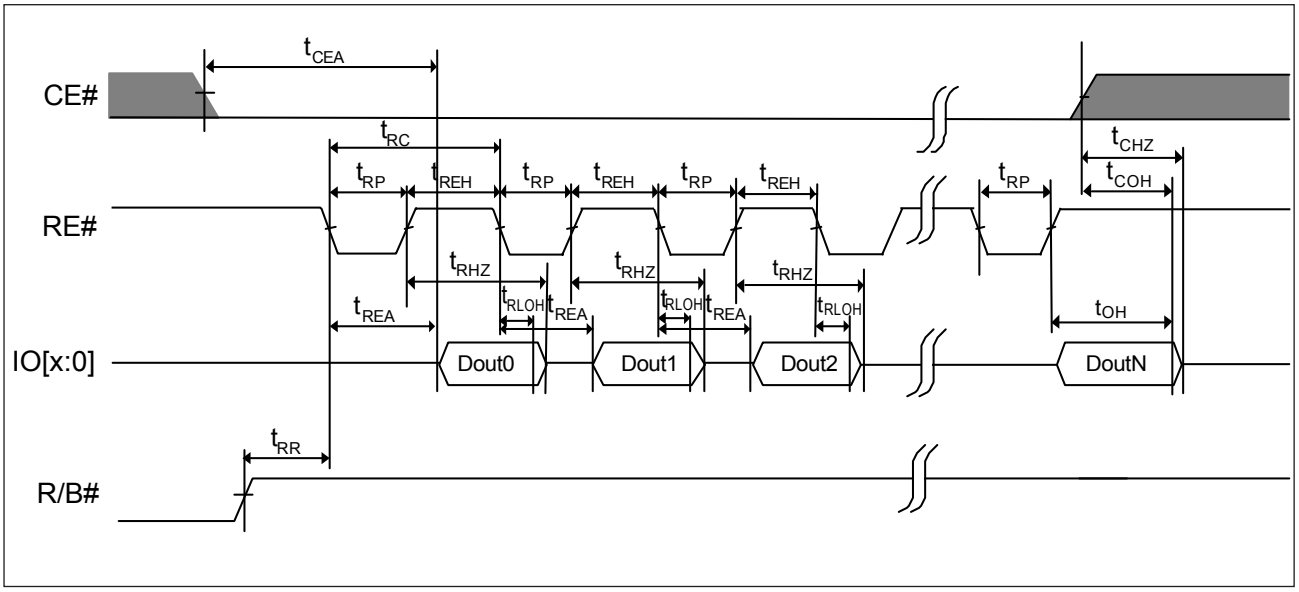
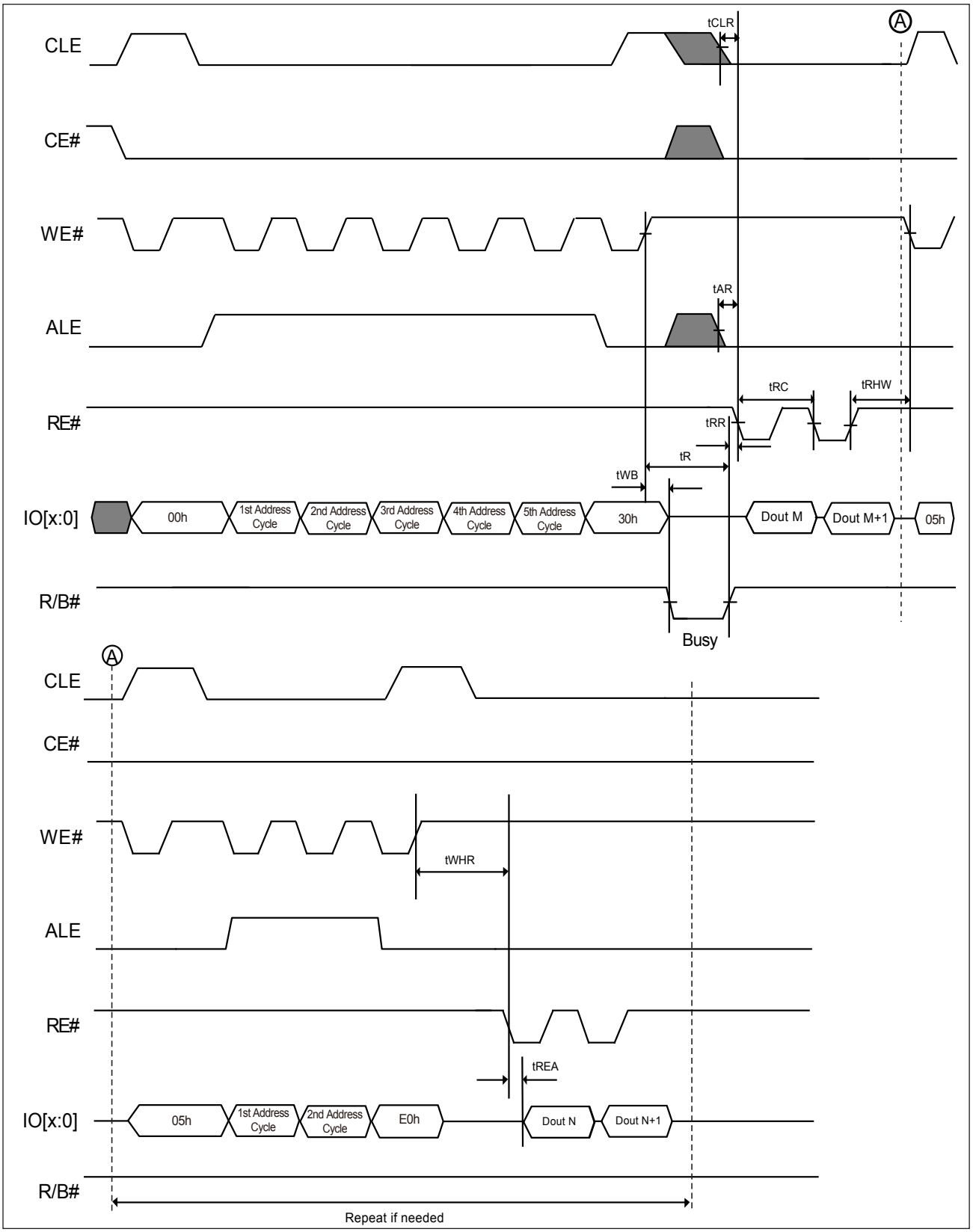


Figure 10. AC Waveforms for Random Data Output



6-3. Cache Read Sequential

The cache read sequential operation is for throughput enhancement by using the internal cache buffer. It allows the consecutive pages to be read-out without giving next page address, which reduces the latency time from tR to tRCBSY between pages or blocks. While the data is read out on one page, the data of next page can be read into the cache buffer.

After writing the 00h command, the column and row address should be given for the start page selection, and followed by the 30h command for address confirmation. After that, the CACHE READ operation starts after a latency time tR and following a 31h command with the latency time of tRCBSY, the data can be read-out sequentially from 1st column address (A[11:0]=00h) without giving next page address input. The 31h command is necessary to confirm the next cache read sequential operation and followed by a tRCBSY latency time before next page data is necessary. The CACHE READ SEQUENTIAL command is also valid for the consecutive page cross block.

The random data out (05h-E0h) command set is available to change the column address of the current page data in the cache register.

The user can check the chip status by the following method:

- R/B# pin ("0" means the data is not ready, "1" means the user can read the data)

- Status Register (SR[6] functions the same as R/B# pin, SR[5] indicates the internal chip operation, "0" means the chip is in internal operation and "1" means the chip is idle.) Status Register can be checked after the Read Status command (70h) is issued. Command 00h should be given to return to the cache read sequential operation.

To confirm the last page to be read-out during the cache read sequential operation, a 3Fh command is needed to replace the 31h command prior to the last data-out.

Figure 11-1. AC Waveforms for Cache Read Sequential