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MX66U1G45G

1.8V, 1G-BIT [x 1/x 2/x 4]
CMOS MXSMIO® (SERIAL MULTI I/O)
FLASH MEMORY

Key Features

- *Multi I/O Support - Single I/O, Dual I/O and Quad I/O*
- *Support DTR (Double Transfer Rate) Mode*
- *8/16/32/64 byte Wrap-Around Read Mode*

Contents

**1.8V 1G-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O)
FLASH MEMORY**

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- Single Power Supply Operation
  - 1.65 to 2.0 volt for read, erase, and program operations
- Protocol Support
  - Single I/O, Dual I/O and Quad I/O
- Latch-up protected to 100mA from -1V to Vcc +1V
- Fast read for SPI mode
  - Support fast clock frequency up to 166MHz
  - Support Fast Read, 2READ, DREAD, 4READ, QREAD instructions
  - Support DTR (Double Transfer Rate) Mode
  - Configurable dummy cycle number for fast read operation
- Quad Peripheral Interface (QPI) available
- Equal Sectors with 4K byte each, or Equal Blocks with 32K byte each or Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Programming :
  - 256byte page buffer
  - Quad Input/Output page program(4PP) to enhance program performance
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection

  The BP0-BP3 and T/B status bits define the size of the area to be protected against program and erase instructions
  - Advanced sector protection function
- Additional 8K bit security OTP
  - Features unique identifier
  - Factory locked identifiable, and customer lockable
- Command Reset
- Program/Erase Suspend and Resume operation
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
  - Hardware write protection or serial data Input/Output for 4 x I/O read mode
- NC/SIO3
  - No Connection or Serial input & Output for 4 x I/O read mode
- RESET#
  - Hardware Reset pin
- PACKAGE
  - 24-Ball BGA (5x5 ball array)
  - 16-pin SOP (300mil)
  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

MX66U1G45G is 1Gb bits Serial NOR Flash memory, which is configured as 134,217,728 x 8 internally. When it is in two or four I/O mode, the structure becomes 536,870,912 bits x 2 or 268,435,456 bits x 4. MX66U1G45G features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# and RESET# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX66U1G45G MXSMIO® (Serial Multi I/O) provides sequential read operation on whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis for erase command is executed on sector (4K-byte), block (32K-byte), or block (64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode.

The MX66U1G45G utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

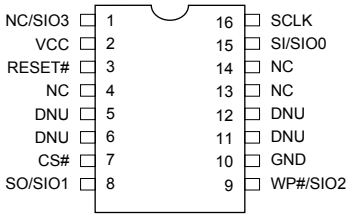
Table 1. Read performance Comparison

Numbers of Dummy Cycles	Fast Read (MHz)	Dual Output Fast Read (MHz)	Quad Output Fast Read (MHz)	Dual IO Fast Read (MHz)	Quad IO Fast Read (MHz)	Quad I/O DT Read (MHz)
4	-	-	-	84*	70	42
6	133	133	104	104	84*	52*
8	133*	133*	133*	133	104	66
10	166	166	166	166	133	100

Note: * mean default status

3. PIN CONFIGURATIONS

16-PIN SOP (300mil)



24-Ball BGA (5x5 ball array)

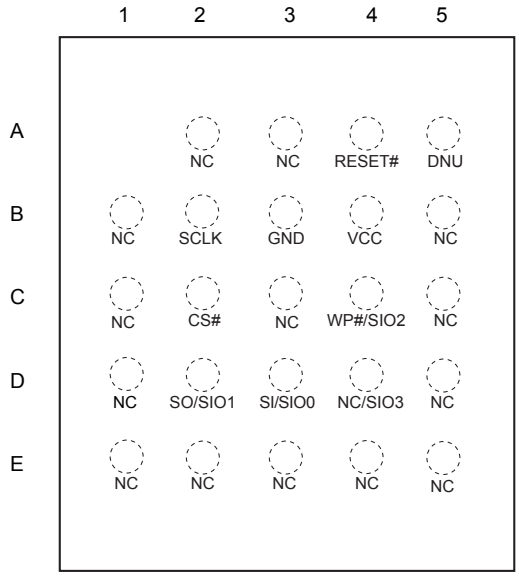
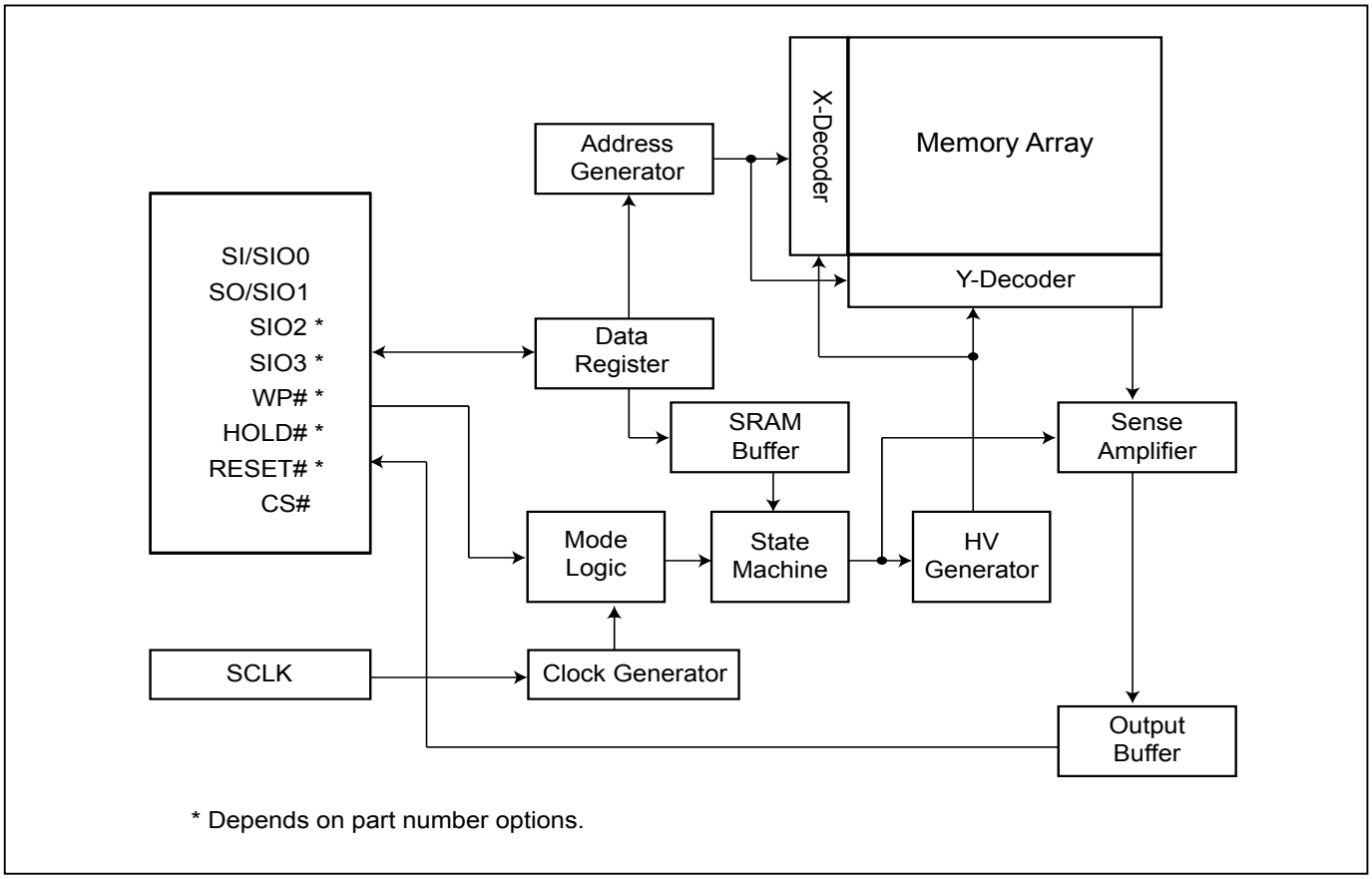


Table 2. PIN DESCRIPTION

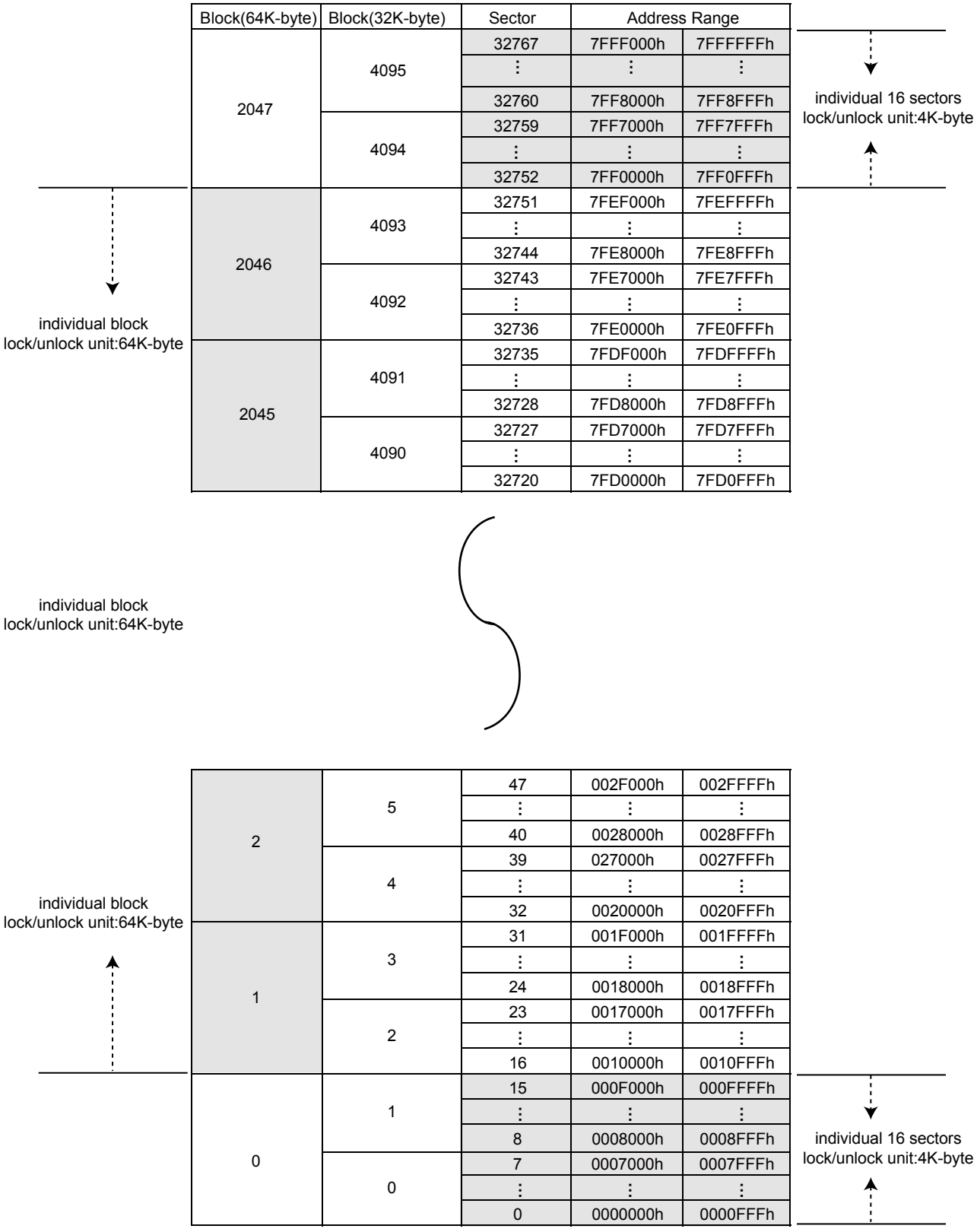
SYMBOL	DESCRIPTION
CS#	Chip Select
SCLK	Clock Input
RESET#	Hardware Reset Pin Active low (Note1)
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
WP#/SIO2	Write Protection Active Low or Serial Data Input & Output (for 4xI/O read mode)
NC/SIO3	No Connection or Serial Data Input & Output (for 4xI/O read mode)
VCC	Power Supply
GND	Ground
NC	No Connection
DNU	Do Not Use (It may connect to internal signal inside)

Note:
1. The pin of RESET# or WP#/SIO2 will remain internal pull up function while this pin is not physically connected in system configuration.
   However, the internal pull up function will be disabled if the system has physical connection to RESET# or WP#/SIO2 pin.

4. BLOCK DIAGRAM



5. MEMORY ORGANIZATION



Block(64K-byte)	Block(32K-byte)	Sector	Address Range	
2047	4095	32767	7FFF000h	7FFFFFFh
		⋮	⋮	⋮
		32760	7FF8000h	7FF8FFFh
	4094	32759	7FF7000h	7FF7FFFh
		⋮	⋮	⋮
		32752	7FF0000h	7FF0FFFh
2046	4093	32751	7FEF000h	7FEFFFFh
		⋮	⋮	⋮
		32744	7FE8000h	7FE8FFFh
	4092	32743	7FE7000h	7FE7FFFh
		⋮	⋮	⋮
		32736	7FE0000h	7FE0FFFh
2045	4091	32735	7FDF000h	7FDFFFFh
		⋮	⋮	⋮
		32728	7FD8000h	7FD8FFFh
	4090	32727	7FD7000h	7FD7FFFh
		⋮	⋮	⋮
		32720	7FD0000h	7FD0FFFh
2	5	47	002F000h	002FFFFh
		⋮	⋮	⋮
		40	0028000h	0028FFFh
	4	39	027000h	0027FFFh
		⋮	⋮	⋮
		32	0020000h	0020FFFh
1	3	31	001F000h	001FFFFh
		⋮	⋮	⋮
		24	0018000h	0018FFFh
	2	23	0017000h	0017FFFh
		⋮	⋮	⋮
		16	0010000h	0010FFFh
0	1	15	000F000h	000FFFFh
		⋮	⋮	⋮
		8	0008000h	0008FFFh
	0	7	0007000h	0007FFFh
		⋮	⋮	⋮
		0	0000000h	0000FFFh

6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES), Erase/Program suspend command, Erase/Program resume command and softreset command.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

6-1. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0 and T/B) bits to allow part of memory to be protected as read only. The protected area definition is shown as *"Table 3. Protected Area Sizes"*, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.
- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect bit.
- In four I/O and QPI mode, the feature of HPM will be disabled.

Table 3. Protected Area Sizes

Protected Area Sizes (T/B bit = 0)

Status bit				Protect Level
BP3	BP2	BP1	BP0	1Gb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 2047th)
0	0	1	0	2 (2 blocks, protected block 2046th~2047th)
0	0	1	1	3 (4 blocks, protected block 2044th~2047th)
0	1	0	0	4 (8 blocks, protected block 2040th~2047th)
0	1	0	1	5 (16 blocks, protected block 2032nd~2047th)
0	1	1	0	6 (32 blocks, protected block 2016th~2047th)
0	1	1	1	7 (64 blocks, protected block 1984th~2047th)
1	0	0	0	8 (128 blocks, protected block 1920th~2047th)
1	0	0	1	9 (256 blocks, protected block 1792nd~2047th)
1	0	1	0	10 (512 blocks, protected block 1536th~2047th)
1	0	1	1	11 (1024 blocks, protected block 1024th~2047th)
1	1	0	0	12 (2048 blocks, protected all)
1	1	0	1	13 (2048 blocks, protected all)
1	1	1	0	14 (2048 blocks, protected all)
1	1	1	1	15 (2048 blocks, protected all)

Protected Area Sizes (T/B bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	1Gb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 0th)
0	0	1	0	2 (2 blocks, protected block 0th~1st)
0	0	1	1	3 (4 blocks, protected block 0th~3rd)
0	1	0	0	4 (8 blocks, protected block 0th~7th)
0	1	0	1	5 (16 blocks, protected block 0th~15th)
0	1	1	0	6 (32 blocks, protected block 0th~31st)
0	1	1	1	7 (64 blocks, protected block 0th~63rd)
1	0	0	0	8 (128 blocks, protected block 0th~127th)
1	0	0	1	9 (256 blocks, protected block 0th~255th)
1	0	1	0	10 (512 blocks, protected block 0th~511th)
1	0	1	1	11 (1024 blocks, protected block 0th~1023rd)
1	1	0	0	12 (2048 blocks, protected all)
1	1	0	1	13 (2048 blocks, protected all)
1	1	1	0	14 (2048 blocks, protected all)
1	1	1	1	15 (2048 blocks, protected all)

6-2. Additional 8K-bit secured OTP

The secured OTP for unique identifier: to provide 8K-bit one-time program area for setting device unique serial number. Which may be set by factory or system customer.

- Security register bit 0 indicates whether the chip is locked by factory or not.

- To program the 8K-bit secured OTP by entering secured OTP mode (with Enter Security OTP command), and going through normal program procedure, and then exiting secured OTP mode by writing Exit Security OTP command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 10. Security Register Definition"* for security register bit definition and *"Table 4. 8K-bit Secured OTP Definition"* for address range definition.

- Note: Once lock-down by factory or customer, the corresponding range cannot be changed any more. While in secured OTP mode, array access is not allowed.

Table 4. 8K-bit Secured OTP Definition

Address range	Size	Lock-down
xxx000~xxx1FF	4096-bit	Determined by Customer
xxx200~xxx3FF	4096-bit	Determined by Factory

7. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this device, this device becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this device should be High-Z.

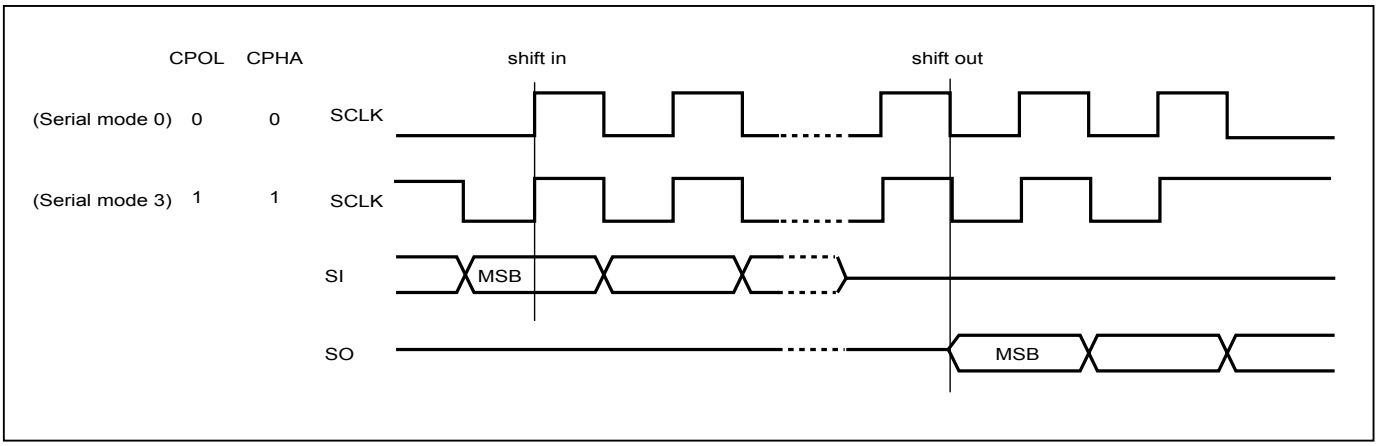
3. When correct command is inputted to this device, this device becomes active mode and keeps the active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as "Serial Modes Supported".

5. For the following instructions: RDID, RDSR, RDSCUR, READ/READ4B, FAST_READ/FAST_READ4B, 2READ/2READ4B, DREAD/DREAD4B, 4READ/4READ4B, QREAD/QREAD4B, RDSFDP, RES, REMS, QPIID, RDDPB, RDSPB, RDLR, RDEAR, RDFBR, RDCR the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE/SE4B, BE32K/BE32K4B, BE/BE4B, CE, PP/PP4B, 4PP/4PP4B, DP, ENSO, EXSO, WRSCUR, EN4B, EX4B, WPSEL, GBLK, GBULK, SUSPEND, RESUME, NOP, RSTEN, RST, EQIO, RSTQIO the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

Figure 2. Serial Input Timing

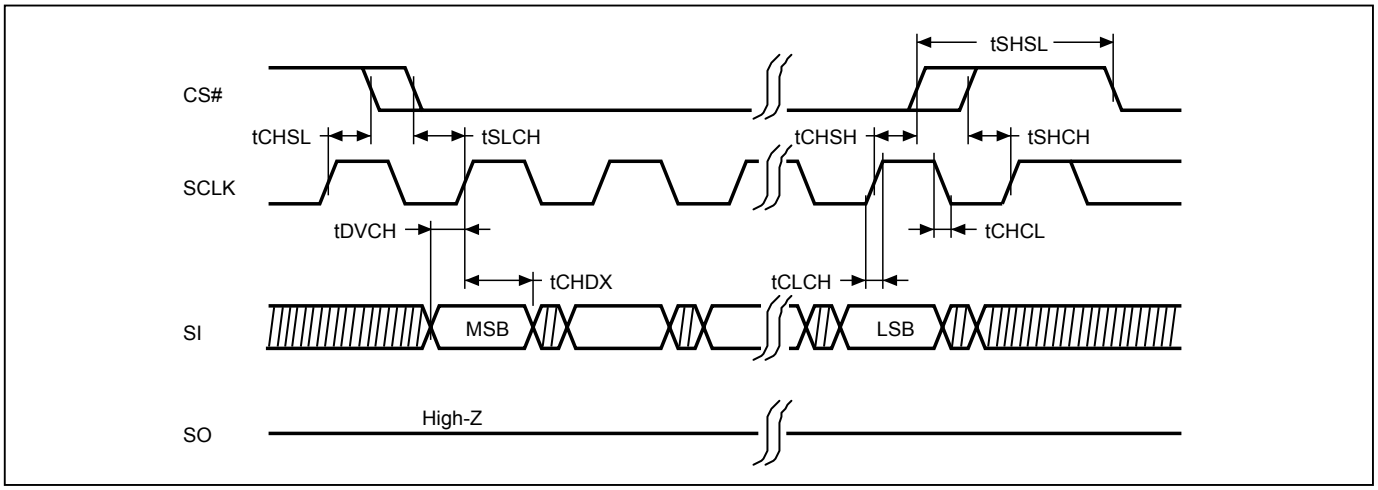


Figure 3. Output Timing (STR mode)

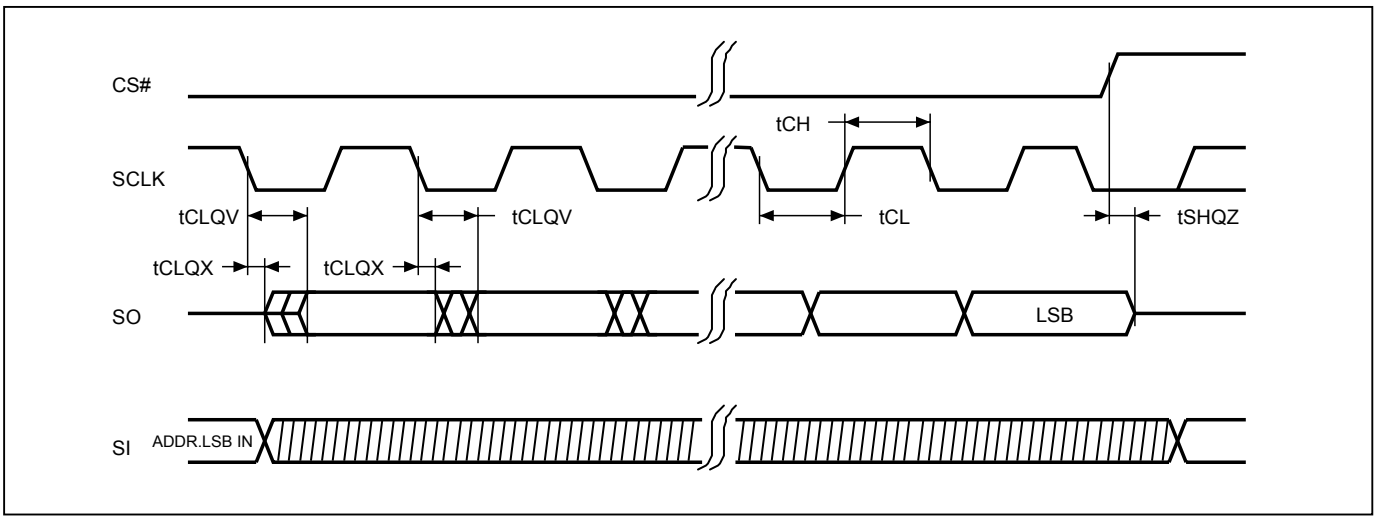
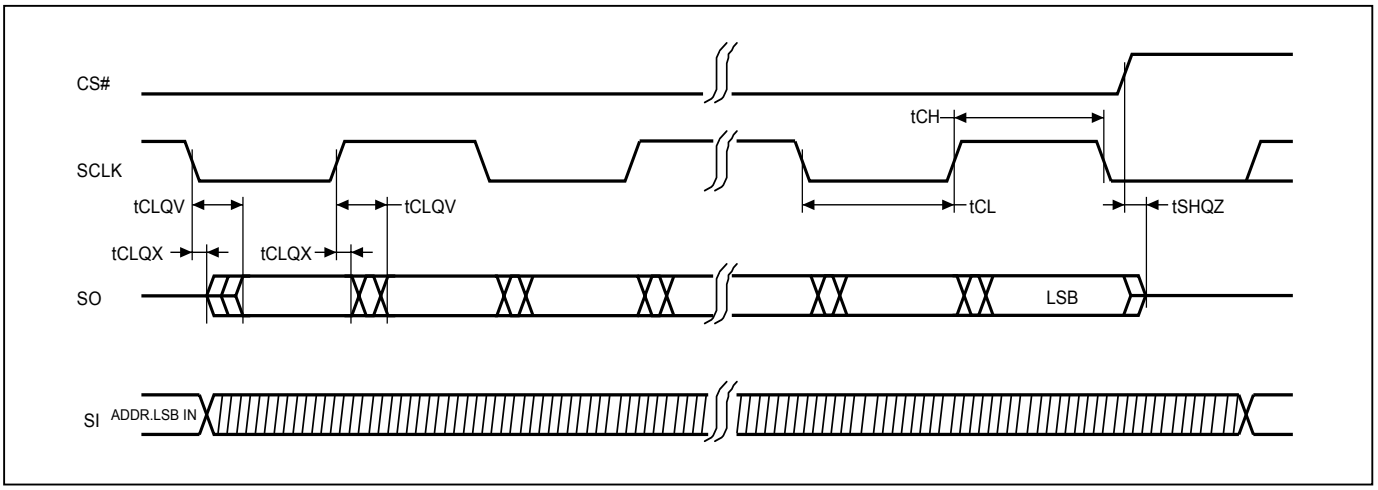


Figure 4. Output Timing (DTR mode)



7-1. 256Mb Address Protocol

The original 24 bit address protocol of Serial NOR Flash can only access density size below 128Mb. For the memory device of 256Mb and above, the 32bit address is requested for access higher memory size. The MX66U1G45G provides three different methods to access the whole density:

(1) Command entry 4-byte address mode:
Issue Enter 4-Byte mode command to set up the 4BYTE bit in Configuration Register bit. After 4BYTE bit has been set, the number of address cycle become 32-bit.

(2) Extended Address Register (EAR):
configure the memory device into eight 128Mb segments to select which one is active through the EAR<0-2>.

(3) 4-byte Address Command Set:
When issuing 4-byte address command set, 4-byte address (A31-A0) is requested after the instruction code. Please note that it is not necessary to issue EN4B command before issuing any of 4-byte command set.

Enter 4-Byte Address Mode

In 4-byte Address mode, all instructions are 32-bits address clock cycles. By using EN4B and EX4B to enable and disable the 4-byte address mode.

When 4-byte address mode is enabled, the EAR<0-2> becomes "don't care" for all instructions requiring 4-byte address. The EAR function will be disabled when 4-byte mode is enabled.

Extended Address Register

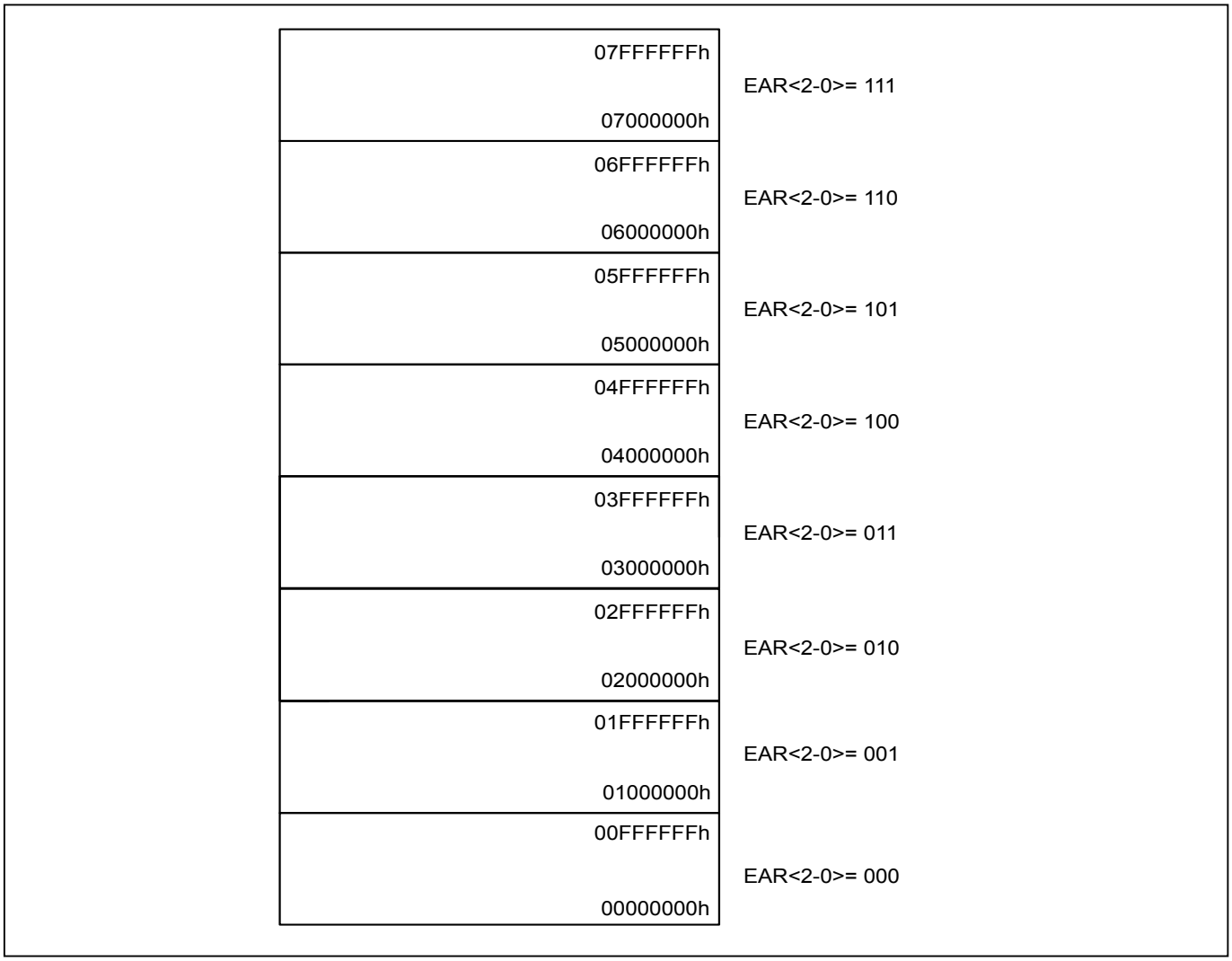
The device provides an 8-bit volatile register for extended Address Register: it identifies the extended address (A31~A24) above 128Mb density by using original 3-byte address.

Extended Address Register (EAR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A31	A30	A29	A28	A27	A26	A25	A24

For the MX66U1G45G the A31 to A27 are Don't Care. During EAR, reading these bits will read as 0. The bit 0 is default as "0".

Figure 5. EAR Operation Segments



When under EAR mode, Read, Program, Erase operates in the selected segment by using 3-byte address mode.

For the read operation, the whole array data can be continually read out with one command. Data output starts from the selected 128Mb block, but it can cross the boundary. When the last byte of the segment is reached, the next byte (in a continuous reading) is the first byte of the next segment. However, the EAR (Extended Address Register) value does not change. The random access reading can only be operated in the selected segment.

The Chip erase command will erase the whole chip and is not limited by EAR selected segment. However, the sector erase ,block erase , program operation are limited in selected segment and will not cross the boundary.

Figure 6. Write EAR Register (WREAR) Sequence (SPI Mode)

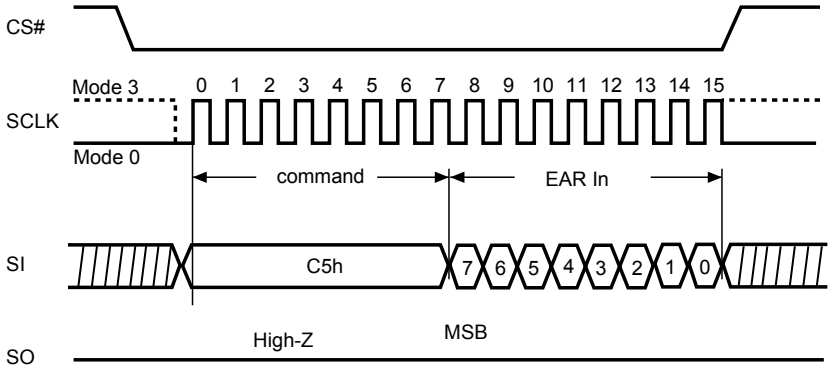


Figure 7. Write EAR Register (WREAR) Sequence (QPI Mode)

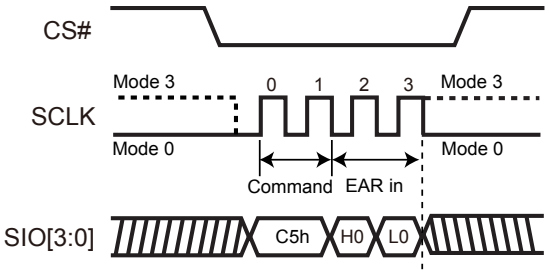


Figure 8. Read EAR (RDEAR) Sequence (SPI Mode)

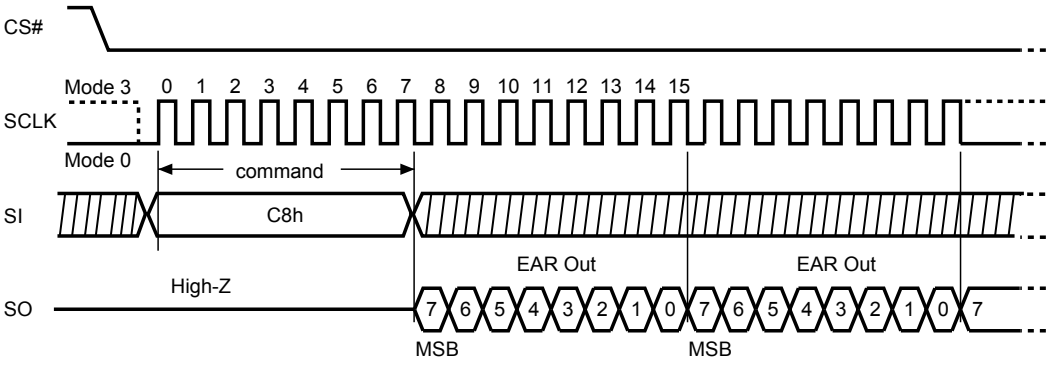
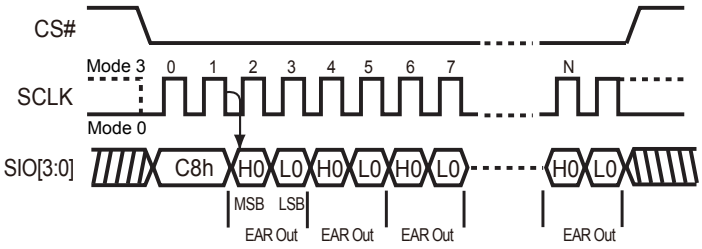


Figure 9. Read EAR (RDEAR) Sequence (QPI Mode)



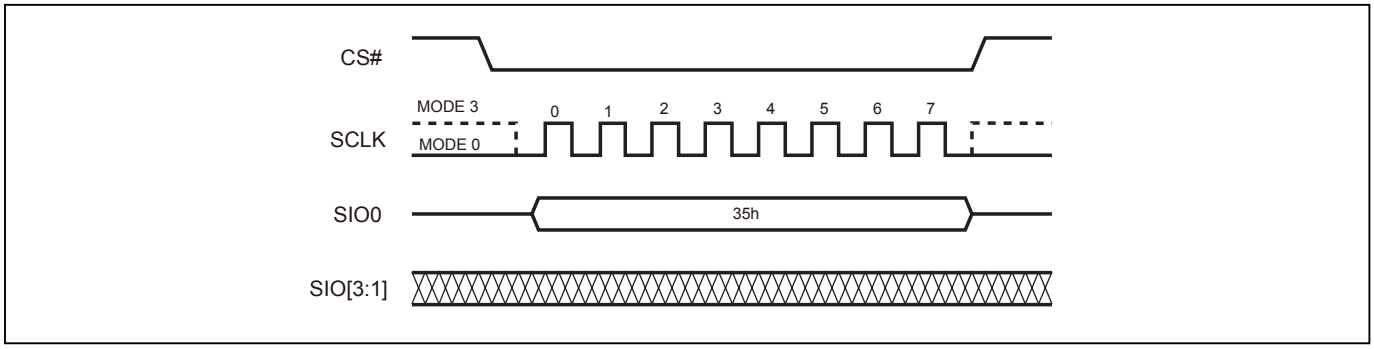
7-2. Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

Enable QPI mode

By issuing 35H command, the QPI mode is enable.

Figure 10. Enable QPI Sequence

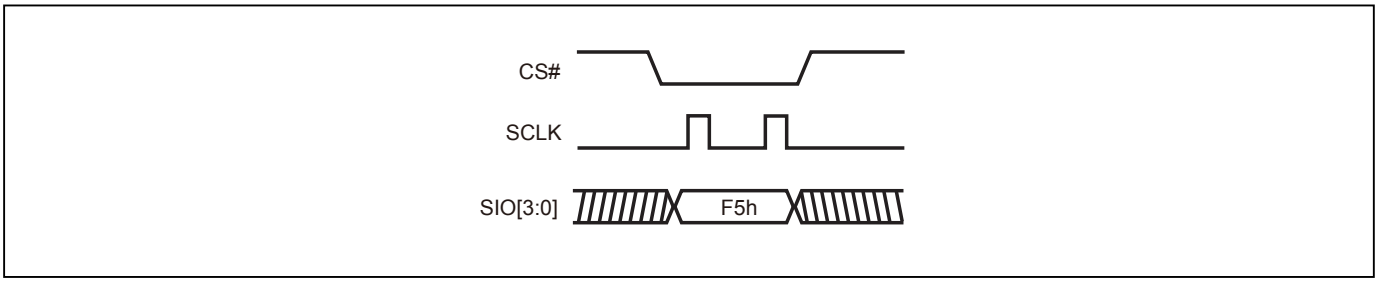


Reset QPI (RSTQIO)

To reset the QPI mode, the RSTQIO (F5H) command is required. After the RSTQIO command is issued, the device returns from QPI mode (4 I/O interface in command cycles) to SPI mode (1 I/O interface in command cycles).

Note:
For EQIO and RSTQIO commands, CS# high width has to follow "write spec" tSHSL for next instruction.

Figure 11. Reset QPI Mode



8. COMMAND SET

Table 5. Read/Write Array Commands

Command (byte)	READ (normal read)	FAST READ (fast read data)	2READ (2 x I/O read)	DREAD (1I 2O read)	4READ (4 I/O read)	QREAD (1I 4O read)	4DTRD (Quad I/O DT Read)
Mode	SPI	SPI	SPI	SPI	SPI/QPI	SPI	SPI/QPI
Address Bytes	3/4	3/4	3/4	3/4	3/4	3/4	3/4
1st byte	03 (hex)	0B (hex)	BB (hex)	3B (hex)	EB (hex)	6B (hex)	ED (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte		Dummy*	Dummy*	Dummy*	Dummy*	Dummy*	Dummy*
Data Cycles							
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by Dual output until CS# goes high	n bytes read out by 4 x I/O until CS# goes high	n bytes read out by Quad output until CS# goes high	n bytes read out (Double Transfer Rate) by 4xI/O until CS# goes high

Command (byte)	PP (page program)	4PP (quad page program)	SE (sector erase)	BE 32K (block erase 32KB)	BE (block erase 64KB)	CE (chip erase)
Mode	SPI/QPI	SPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	3/4	3/4	3/4	3/4	3/4	0
1st byte	02 (hex)	38 (hex)	20 (hex)	52 (hex)	D8 (hex)	60 or C7 (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	
5th byte						
Data Cycles	1-256	1-256				
Action	to program the selected page	quad input to program the selected page	to erase the selected sector	to erase the selected 32K block	to erase the selected block	to erase whole chip

* Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

Notes 2: Please note the address cycles above are based on 3-byte address mode. After enter 4-byte address mode by EN4B command, the address cycles will be increased to 4byte.

Table 6. Read/Write Array Commands (4 Byte Address Command Set)

Command (byte)	READ4B	FAST READ4B	2READ4B	DREAD4B	4READ4B	QREAD4B	4DTRD4B (Quad I/O DT Read)
Mode	SPI	SPI	SPI	SPI	SPI/QPI	SPI	SPI/QPI
Address Bytes	4	4	4	4	4	4	4
1st byte	13 (hex)	0C (hex)	BC (hex)	3C (hex)	EC (hex)	6C (hex)	EE (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte	ADD4	ADD4	ADD4	ADD4	ADD4	ADD4	ADD4
6th byte		Dummy*	Dummy*	Dummy*	Dummy*	Dummy*	Dummy*
Data Cycles							
Action	read data byte by 4 byte address	read data byte by 4 byte address	read data byte by 2 x I/O with 4 byte address	Read data byte by Dual Output with 4 byte address	read data byte by 4 x I/O with 4 byte address	Read data byte by Quad Output with 4 byte address	n bytes read out (Double Transfer Rate) by 4xI/O until CS# goes high

Command (byte)	PP4B	4PP4B	BE4B (block erase 64KB)	BE32K4B (block erase 32KB)	SE4B (Sector erase 4KB)
Mode	SPI/QPI	SPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	4	4	4	4	4
1st byte	12 (hex)	3E (hex)	DC (hex)	5C (hex)	21 (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte	ADD4	ADD4	ADD4	ADD4	ADD4
6th byte					
Data Cycles	1-256	1-256			
Action	to program the selected page with 4byte address	Quad input to program the selected page with 4byte address	to erase the selected (64KB) block with 4byte address	to erase the selected (32KB) block with 4byte address	to erase the selected (4KB) sector with 4byte address

Table 7. Register/Setting Commands

Command (byte)	WREN (write enable)	WRDI (write disable)	RDSR (read status register)	RDCR (read configuration register)	WRSR (write status/ configuration register)	RDEAR (read extended address register)	WREAR (write extended address register)
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	06 (hex)	04 (hex)	05 (hex)	15 (hex)	01 (hex)	C8 (hex)	C5 (hex)
2nd byte					Values		
3rd byte					Values		
4th byte							
5th byte							
Data Cycles					1-2		1
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to read out the values of the configuration register	to write new values of the status/ configuration register	read extended address register	write extended address register

Command (byte)	WPSEL (Write Protect Selection)	EQIO (Enable QPI)	RSTQIO (Reset QPI)	EN4B (enter 4-byte mode)	EX4B (exit 4-byte mode)	PGM/ERS Suspend (Suspends Program/ Erase)	PGM/ERS Resume (Resumes Program/ Erase)
Mode	SPI	SPI	QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	68 (hex)	35 (hex)	F5 (hex)	B7 (hex)	E9 (hex)	B0 (hex)	30 (hex)
2nd byte							
3rd byte							
4th byte							
5th byte							
Data Cycles							
Action	to enter and enable individal block protect mode	Entering the QPI mode	Exiting the QPI mode	to enter 4-byte mode and set 4BYTE bit as "1"	to exit 4-byte mode and clear 4BYTE bit to be "0"		

Command (byte)	DP (Deep power down)	RDP (Release from deep power down)	SBL (Set Burst Length)	RDFBR (read fast boot register)	WRFBR (write fast boot register)	ESFBR (erase fast boot register)
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI	SPI	SPI
1st byte	B9 (hex)	AB (hex)	C0 (hex)	16(hex)	17(hex)	18(hex)
2nd byte						
3rd byte						
4th byte						
5th byte						
Data Cycles				1-4	4	
Action	enters deep power down mode	release from deep power down mode	to set Burst length			

Table 8. ID/Security Commands

Command (byte)	RDID (read identific-ation)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	QPIID (QPI ID Read)	RDSFDP	ENSO (enter secured OTP)	EXSO (exit secured OTP)
Mode	SPI	SPI/QPI	SPI	QPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	0	0	0	0	3	0	0
1st byte	9F (hex)	AB (hex)	90 (hex)	AF (hex)	5A (hex)	B1 (hex)	C1 (hex)
2nd byte		x	x		ADD1		
3rd byte		x	x		ADD2		
4th byte			ADD1		ADD3		
5th byte					Dummy(8)(Note 4)		
Action	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	ID in QPI interface	Read SFDP mode	to enter the secured OTP mode	to exit the secured OTP mode

Command (byte)	RDSCUR (read security register)	WRSCUR (write security register)	GBLK (gang block lock)	GBULK (gang block unlock)	WRLR (write Lock register)	RDLR (read Lock register)	WRSPB (SPB bit program)
Mode	SPI/QPI	SPI/QPI	SPI	SPI	SPI	SPI	SPI
Address Bytes	0	0	0	0	0	0	4
1st byte	2B (hex)	2F (hex)	7E (hex)	98 (hex)	2C (hex)	2D (hex)	E3 (hex)
2nd byte							ADD1
3rd byte							ADD2
4th byte							ADD3
5th byte							ADD4
Data Cycles					2	2	
Action	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)	whole chip write protect	whole chip unprotect			

Command (byte)	ESSPB (all SPB bit erase)	RDSPB (read SPB status)	WRDPB (write DPB register)	RDDPB (read DPB register)	RDPASS (read password register)	WRPASS (write password register)	PASSULK (password unlock)
Mode	SPI	SPI	SPI	SPI	SPI	SPI	SPI
Address Bytes	0	4	4	4	4	4	4
1st byte	E4 (hex)	E2 (hex)	E1 (hex)	E0 (hex)	27 (hex)	28 (hex)	29 (hex)
2nd byte		ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte		ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte		ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte		ADD4	ADD4	ADD4	ADD4	ADD4	ADD4
6th byte					Dummy(8)(Note 4)		
Data Cycles		1	1	1	8	8	8
Action							

Table 9. Reset Commands

Command (byte)	NOP (No Operation)	RSTEN (Reset Enable)	RST (Reset Memory)
Mode	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	00 (hex)	66 (hex)	99 (hex)
2nd byte			
3rd byte			
4th byte			
5th byte			
Action			

Note 1: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.
Note 2: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.
Note 3: The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.
Note 4: The number in parentheses after “ADD” or “Data” or “Dummy” stands for how many clock cycles it has. For example, "Data(8)" represents there are 8 clock cycles for the data in. Please note the number after "ADD" are based on 3-byte address mode, for 4-byte address mode, which will be increased.