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19-0158; Rev 0; 7/93

Complete, Dual, 12-Bit Multiplying DACs

General Description

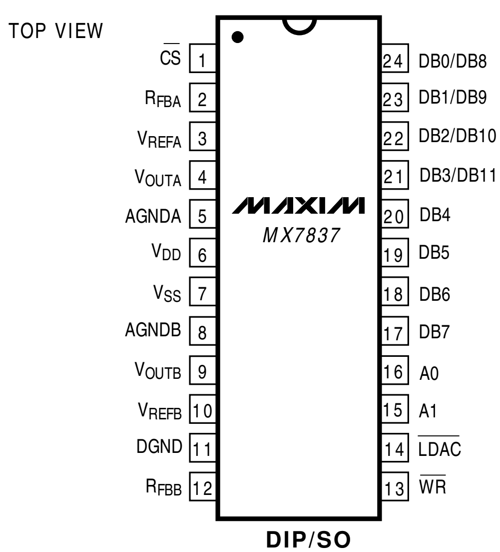
The MX7837/MX7847 are dual, 12-bit, multiplying, voltage-output digital-to-analog converters (DACs). Each DAC has an output amplifier and a feedback resistor. The output amplifier is capable of developing ±10V across a 2kΩ load. The amplifier feedback resistor is internally connected to V_{OUT} on the MX7847. No external trims are required to achieve full 12-bit performance over the entire operating temperature range.

The MX7847 has a 12-bit parallel data input, whereas the MX7837 operates with a double-buffered 8-bit-bus interface that loads data in two write operations. All logic signals are level triggered and are TTL and CMOS compatible. Fast timing specifications make these DACs compatible with most microprocessors.

Applications

Small Component-Count Analog Systems
Digital Offset/Gain Adjustments
Industrial Process Control
Function Generators
Automatic Test Equipment
Automatic Calibration
Machine and Motion Control Systems
Waveform Reconstruction
Synchro Applications

Pin Configurations



MX7847 on last page.

Features

- ♦ **Two 12-Bit Multiplying DACs with Buffered Voltage Output**
- ♦ **Specified with ±12V or ±15V Supplies**
- ♦ **No External Adjustments Required**
- ♦ **Fast Timing Specifications**
- ♦ **24-Pin DIP and SO Packages**
- ♦ **12-Bit Parallel Interface (MX7847)**
  8-Bit + 4-Bit Interface (MX7837)

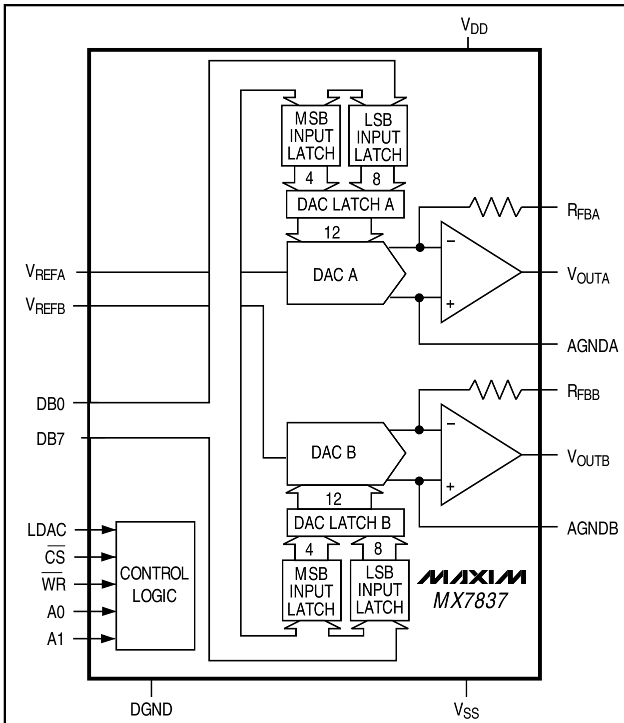
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MX7837JN	0°C to +70°C	24 Narrow Plastic DIP	±1
MX7837KN	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MX7837JR	0°C to +70°C	24 Wide SO	±1
MX7837KR	0°C to +70°C	24 Wide SO	±1/2
MX7837C/D	0°C to +70°C	Dice*	±1

Ordering Information continued on last page.

* *Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuits



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Complete, Dual, 12-Bit Multiplying DACs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND, AGNDA, AGNDB ....-0.3V to +17V
V_{SS} to DGND, AGNDA, AGNDB (Note 1) ....+0.3V to -17V
V_{REFA}, V_{REFB} to AGNDA, AGNDB .. (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
AGNDA, AGNDB to DGND.........................-0.3V to (V_{DD} + 0.3V)
V_{OUTA}, V_{OUTB} to AGNDA, AGNDB .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
R_{FBA}, R_{FBB} to AGNDA, AGNDB ....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Digital Inputs to DGND ....-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 13.33mW/°C above +70°C)....1067mW
SO (derate 11.76mW/°C above +70°C).........................941mW
Narrow CERDIP (derate 12.50mW/°C above +70°C) ..1000mW

Operating Temperature Ranges:
MX78_7J_/K_ ....0°C to +70°C
MX78_7A_/B_ .... -40°C to +85°C
MX78_7SQ/TQ .... -55°C to +125°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10sec) ....+300°C

Note 1: If V_{SS} is open-circuited with V_{DD} and either AGND applied, the V_{SS} pin will float positive exceeding the *Absolute Maximum Ratings*. If this possibility exists, a Schottky diode connected between V_{SS} and GND ensures the maximum ratings will be observed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V, V_{REFA} = V_{REFB} = +10V, R_L = 2kΩ, C_L = 100pF, V_{OUT} connected to R_{FB} (MX7837), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (Note 3)								
Resolution	N				12			Bits
Relative Accuracy	INL	MX78_7J/A/S					±1	LSB
		MX78_7K/B/T					±1/2	
Differential Nonlinearity	DNL	Guaranteed monotonic					±1	LSB
Zero-Code Offset Error		Loaded with all 0s, tempco = ±5µV/°C typ	T_A = +25°C				±2	mV
			T_A = T_{MIN} to T_{MAX}	MX78_7J/A			±4	
				MX78_7K/B			±3	
				MX78_7S/T			±5	
Gain Error		Loaded with all 1s, tempco = ±2ppm of FSR/°C typ	T_A = +25°C	MX78_7J/A/S			±5	LSB
				MX78_7K/B/T			±2	
			T_A = T_{MIN} to T_{MAX}	MX78_7J/A/S			±7	
				MX78_7K/B/T			±4	
REFERENCE INPUTS								
V_{REF} Input Resistance					8	10	13	kΩ
V_{REFA}, V_{REFB} Resistance Matching						±0.5	±3	%
DIGITAL INPUTS								
Input High Voltage	V_{INH}				2.4			V
Input Low Voltage	V_{INL}						0.8	
Input Current		Digital inputs at 0V and V_{DD}					±1	µA
Input Capacitance (Note 4)							8	pF
ANALOG OUTPUTS								
DC Output Impedance						0.2		Ω
Short-Circuit Current		V_{OUT} connected to AGND				15		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V, V_{REFA} = V_{REFB} = +10V, R_L = 2kΩ, C_L = 100pF, V_{OUT} connected to R_{FB} (MX7837), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
V_{DD} Range	V_{DD}		11.4		16.5	V
V_{SS} Range	V_{SS}		-11.4		-16.5	V
Positive Supply Current	I_{DD}	Output unloaded		5	10	mA
Negative Supply Current	I_{SS}	Output unloaded		4	6	mA
Power-Supply Rejection	ΔGain/ΔV_{DD}	V_{DD} = 15V ±5%, V_{REF} = -10V			±0.01	% per %
	ΔGain/ΔV_{SS}	V_{SS} = -15V ±5%, V_{REF} = 10V			±0.01	
	ΔGain/ΔV_{DD}	V_{DD} = 12V ±5%, V_{REF} = -8.9V			±0.01	
	ΔGain/ΔV_{SS}	V_{SS} = -12V ±5%, V_{REF} = 8.9V			±0.01	
AC CHARACTERISTICS						
Voltage-Output Settling Time	t_S	Settling time to within ±1/2LSB of final DAC value; DAC latch alternately loaded will all 0s and all 1s		4		µs
Slew Rate				7		V/µs
Digital-to Analog Glitch Impulse	Q	DAC latch alternately loaded with 01…11 and 10…00		60		nV-s
Channel-to-Channel Isolation (V_{REFA} to V_{OUTB}, V_{REFB} to V_{OUTA})		V_{REF} = 20p-p, 10kHz sine wave, Alternate DAC Latch Loaded with all 0s		-95		dB
Multiplying Feedthrough Error		$V_{REF\_}$ = 20V_{p-p}, 10kHz sine wave, latches loaded with all 0s		-90		dB
Unity-Gain Small-Signal Bandwidth		V_{REF} = 100mV_{p-p} sine wave, DAC latch loaded with all 1s		1		MHz
Full-Power Bandwidth		V_{REF} = 20V_{p-p} sine wave, DAC latch loaded with all 1s		125		kHz
Total Harmonic Distortion	THD	V_{REF} = 6V_{RMS}, 1kHz, DAC latch loaded with all 1s		-88		dB
Digital Crosstalk		Code transition from all 0s to all 1s; see *Typical Operating Characteristics* graphs		10		nV-s
Output Noise Voltage at +25°C (0.1Hz to 10Hz)		Amplifier noise and Johnson noise of R_{FB}		2		µV_{RMS}

Note 2: The analog outputs can swing to within 2.5V of the supply rails. Hence, for good linearity towards full-scale, $|V_{REFA}|$ and $|V_{REFB}|$ must be at least 2.5V lower than V_{DD} and $|V_{SS}|$. Tests done with supply voltages below ±12.5V are done with V_{REFA} = V_{REFB} = ±8.9V.
Note 3: Static performance tested at V_{DD} = +15V, V_{SS} = -15V. Performance over supplies guaranteed by PSRR test.
Note 4: Guaranteed by design.

Complete, Dual, 12-Bit Multiplying DACs

TIMING CHARACTERISTICS

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 5)

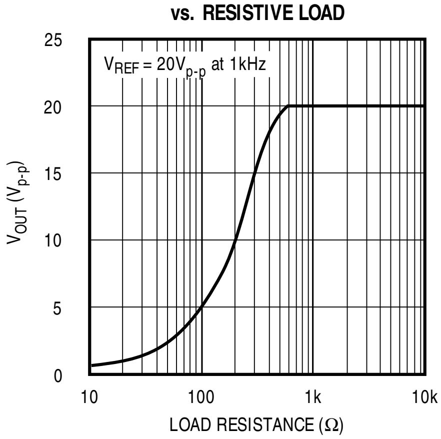
PARAMETER	SYMBOL	CONDITIONS	MX78_7J/K/A/B MIN	MX78_7J/K/A/B MAX	MX78_7S/T MIN	MX78_7S/T MAX	UNITS
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_1		0		0		ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_2		0		0		ns
$\overline{WR}$ Pulse Width	t_3		80		80		ns
Data to $\overline{WR}$ Setup Time	t_4		80		80		ns
Data to $\overline{WR}$ Hold Time	t_5		10		10		ns
Address to $\overline{WR}$ SetupTime	t_6	MX7837 only	15		15		ns
Address to $\overline{WR}$ Hold Time	t_7	MX7837 only	15		15		ns
$\overline{LDAC}$ Pulse Width	t_8	MX7837 only	80		80		ns

Note 5: All input signals are specified with $t_R = t_F \leq$ 5ns. Logic swing is 0V to 5V.

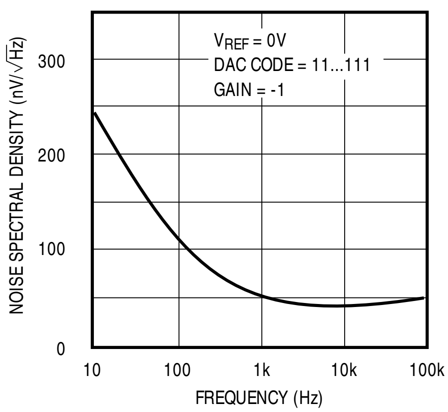
Typical Operating Characteristics

(T_A = +25°C, V_{DD} = 15V, V_{SS} = -15V, R_L = 2kΩ, C_L = 100pF, unless otherwise noted)

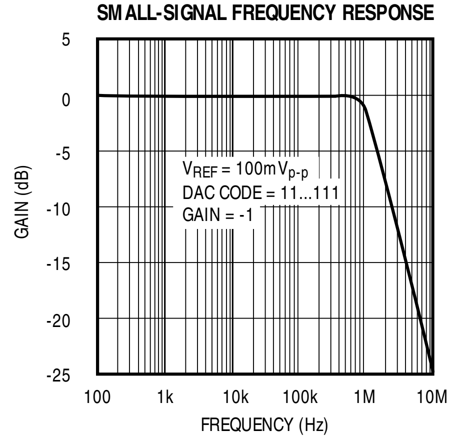
OUTPUT VOLTAGE SWING vs. RESISTIVE LOAD



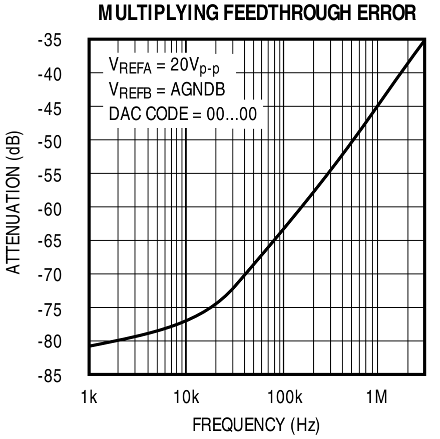
NOISE SPECTRAL DENSITY



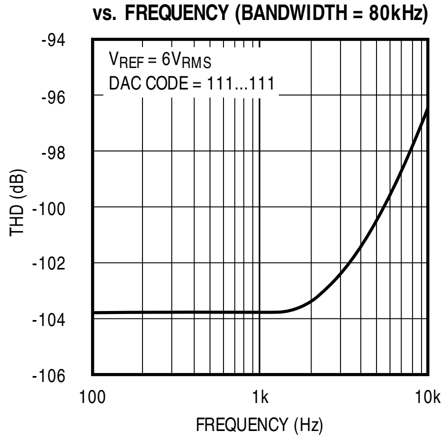
SMALL-SIGNAL FREQUENCY RESPONSE



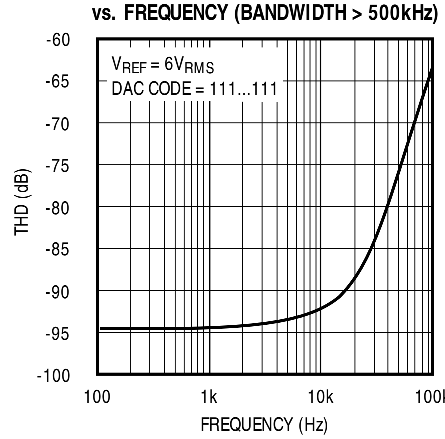
MULTIPLYING FEEDTHROUGH ERROR



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (BANDWIDTH = 80kHz)



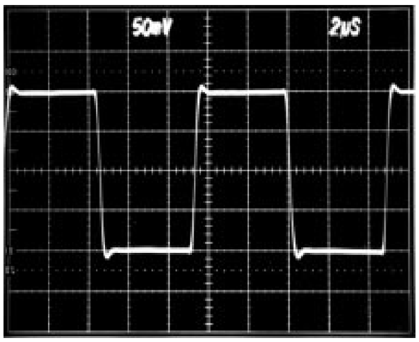
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (BANDWIDTH > 500kHz)



Typical Operating Characteristics (continued)

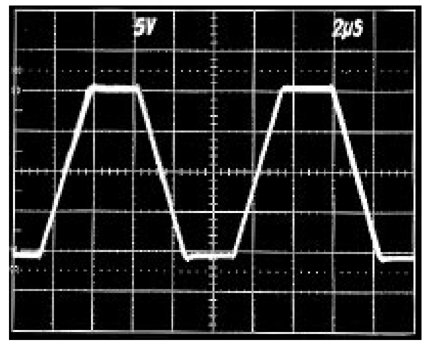
(T_A = +25°C, V_{DD} = 15V, V_{SS} = -15V, R_L = 2kΩ, C_L = 100pF, unless otherwise noted.)

SMALL-SIGNAL PULSE RESPONSE



A = V_{OUTA}, 50mV/div
TIMEBASE = 2μs/div
V_{REFA} = ±100mV SQUARE WAVE

LARGE-SIGNAL PULSE RESPONSE



A = V_{OUTA}, 5V/div
TIMEBASE = 2μs/div
V_{REFA} = ±10V SQUARE WAVE

Pin Description

PIN		NAME	FUNCTION
MX7837	MX7847		
1	–	$\overline{CS}$	Chip Select – active-low logic input
–	1	$\overline{CSA}$	Chip-Select Input for DAC A – active-low logic input
2	–	R_{FBA}	Amplifier Feedback Resistor for DAC A
–	2	$\overline{CSB}$	Chip-Select Input for DAC B – active-low logic input
3	3	V_{REFA}	Reference Input Voltage for DAC A
4	4	V_{OUTA}	Analog Output Voltage from DAC A
5	5	AGNDA	Analog Ground for DAC A
6	6	V_{DD}	Positive Power Supply
7	7	V_{SS}	Negative Power Supply
8	8	AGNDB	Analog Ground for DAC B
9	9	V_{OUTB}	Analog Output Voltage from DAC B
10	10	V_{REFB}	Reference Input Voltage for DAC B
11	11	DGND	Digital Ground
12	–	R_{FBB}	Amplifier Feedback Resistor for DAC B
–	12	DB11	Data Bit 11 (MSB)
13	13	$\overline{WR}$	Write Input – active-low logic input (MX7837); positive-edge-triggered input used with $\overline{CSA}$ and $\overline{CSB}$ (MX7847)
14	–	$\overline{LDAC}$	Asynchronous Load – DAC input, active-low
–	14-24	DB10-DB0	Data Bit 10 to Data Bit 0 (LSB)
15	–	A1	Address Input – most significant address input for input latches
16	–	A0	Address Input – least significant address input for input latches
17-20	–	DB7-DB4	Data Bit 7 to Data Bit 4
21-24	–	DB3/DB11-DB0/DB8	Data Bit 3 to Data Bit 0 (LSB), or Data Bit 11 (MSB) to Data Bit 8

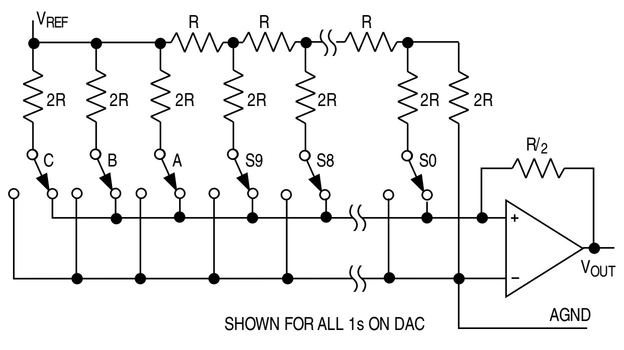


Figure 1. D/A Simplified Circuit Diagram

Detailed Description

D/A Section

Figure 1 shows a simplified circuit diagram for one of the DACs and the output amplifier. Using a segmented scheme, the two MSBs of the 12-bit data word are decoded to drive the three switches (A to C). The remaining 10 bits drive the switches (S0 to S9) in a standard R-2R ladder.

Each switch (A to C) directs 1/4 of the total reference current, and the remaining current passes through the R-2R section.

The output amplifier and feedback resistor convert current to voltage as follows: $V_{OUT\_} = (-D)(V_{REF\_})$, where D is the fractional representation of the digital word. (D can be set from 0 to 4095/4096.)

The output amplifier is capable of developing ±10V across a 2kΩ load. It is internally compensated and settles to 0.01% FSR (1/2LSB) in less than 4µs. V_{OUT} on the MX7837 is not internally connected to R_{FB}.

Interface Logic Information (MX7847)

Figure 2 shows the MX7847 input control logic. The device contains two independent DACs, each with its own $\overline{CS}$ input and a common $\overline{WR}$ input. $\overline{CSA}$ and $\overline{WR}$ control data loading to the DAC A latch, and $\overline{CSB}$ and $\overline{WR}$ control data loading to the DAC B latch. The latches are edge triggered so that input data is latched to the respective latch on $\overline{WR}$'s rising edge. The same data will be latched to both DACs if $\overline{CSA}$ and $\overline{CSB}$ are low and $\overline{WR}$ is taken high. Table 1 shows the device control-logic truth table, and Figure 3 shows the write-cycle timing diagram.

Table 1. MX7847 Truth Table

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	Function
X	X	1	No Data Transfer
1	1	X	No Data Transfer
0	1	⨍	Data Latched to DAC A
1	0	⨍	Data Latched to DAC B
0	0	⨍	Data Latched to Both DACs
⨍	1	0	Data Latched to DAC A
1	⨍	0	Data Latched to DAC B
⨍	⨍	0	Data Latched to Both DACs

X = Don't Care ⨍ = Rising Edge Triggered

Interface Logic Information (MX7837)

The MX7837 input loading structure is configured for interfacing with 8-bit-wide data-bus microprocessors. Each DAC has two 12-bit latches: an input latch, and a DAC latch. Each input latch is subdivided into a least-significant 8-bit latch and a most-significant 4-bit latch. The data held in the DAC latches determines the outputs. Figure 4 shows the MX7837 input control logic, and Figure 5 shows the write-cycle timing diagram.

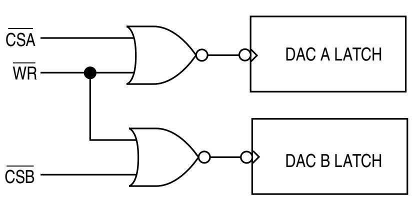


Figure 2. MX7847 Input Control Logic

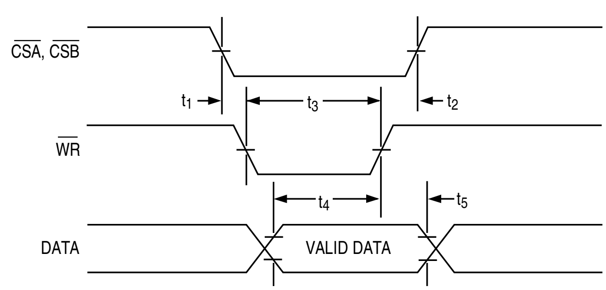


Figure 3. MX7847 Write-Cycle Timing Diagram

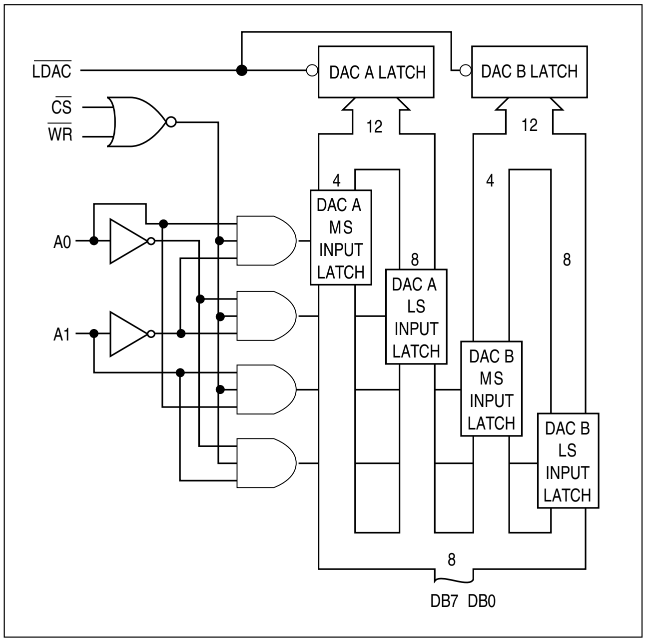


Figure 4. MX7837 Input Control Logic

$\overline{CS}$, $\overline{WR}$, A0, and A1 control data loading to the input latches. The eight data inputs accept right-justified data, which can be loaded to the input latches in any sequence. If $\overline{LDAC}$ is held high, loading data to the input latches will not change the analog output. A0 and A1 determine which input latch will receive the data when $\overline{CS}$ and $\overline{WR}$ are low. Table 2 shows the control logic truth table.

Table 2. MX7837 Truth Table

$\overline{CS}$	$\overline{WR}$	A1	A0	$\overline{LDAC}$	Function
1	X	X	X	1	No Data Transfer
X	1	X	X	1	No Data Transfer
0	0	0	0	1	DAC A LS Input Latch Transparent
0	0	0	1	1	DAC A MS Input Latch Transparent
0	0	1	0	1	DAC B LS Input Latch Transparent
0	0	1	1	1	DAC B MS Input Latch Transparent
1	1	X	X	0	Updated Simultaneously from the Respective Input Latches

X = Don't Care

The $\overline{LDAC}$ input controls 12-bit data transfer from the input latches to the DAC latches. When $\overline{LDAC}$ is taken low, both DAC latches (thus, both analog outputs) are updated simultaneously. When $\overline{LDAC}$ is low, the DAC latches are transparent; DAC data is latched on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ input is asynchronous

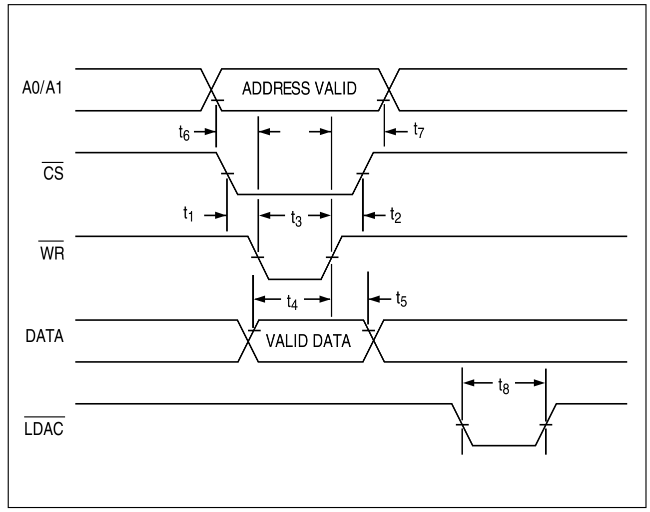


Figure 5. MX7837 Write-Cycle Timing Diagram

and independent of $\overline{WR}$. This is useful in many applications, especially in updating multiple MX7837s simultaneously. However, be careful when exercising $\overline{LDAC}$ during a write cycle; if an $\overline{LDAC}$ operation overlaps a $\overline{CS}$ and $\overline{WR}$ operation, invalid data may be latched to the output. To avoid this, $\overline{LDAC}$ must remain low after $\overline{CS}$ or $\overline{WR}$ have returned high for a period equal to or greater than t_8, the minimum $\overline{LDAC}$ pulse width.

Unipolar Binary Operation

Figure 6 shows DAC A (MX7837/MX7847) connected for unipolar binary operation. Similar connections apply for DAC B. When V_{IN} is an AC signal, the circuit performs 2-quadrant multiplication. Table 3 shows the code table for this circuit. On the MX7847, the R_{FB} feedback resistor is internally connected to V_{OUT}.

Table 3. Unipolar Code Table

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$-V_{IN} \times \left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN} \times \left(\frac{2048}{4096}\right) = -\frac{1}{2}V_{IN}$
0000 0000 0001	$-V_{IN} \times \left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Note: $1LSB = \left(\frac{V_{IN}}{4096}\right)$

Bipolar Operation (4-Quadrant Multiplication)

Figure 7 shows the MX7837/MX7847 connected for binary operation. The offset-binary coding is shown in Table 4. When V_{IN} is an AC signal, the circuit performs 4-quadrant multiplication. R1, R2, and R3 resistors should be 0.01% ratio matched to maintain gain-error specifications. On the MX7847, the R_{FB} feedback resistor is internally connected to V_{OUT}.

Table 4. Bipolar Code Table

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+V_{IN} \times \left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN} \times \left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{IN} \times \left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN} \times \left(\frac{2048}{2048}\right) = -V_{IN}$

Note : $1LSB = \left(\frac{V_{IN}}{2048}\right)$

Applications Information

Ground Management

The use of an uninterrupted ground plane is strongly recommended. AC or transient voltages between analog and digital grounds (between AGNDA/AGNDB and DGND) can inject noise into the analog circuitry. Connect the MX7837/MX7847 AGNDs and DGND directly to the ground plane or to a star ground to ensure that they are at the same potential. In complex systems with separate analog and digital ground planes, connect two diodes (1N914 or equivalent) in inverse parallel between the AGND and DGND pins.

Power-Supply Decoupling

To minimize noise, decouple the V_{DD} and V_{SS} lines to DGND using a 10µF capacitor in parallel with a 0.1µF ceramic capacitor. Minimize capacitor lead lengths for best noise rejection.

Operation with Reduced Power-Supply Voltages

The MX7837/MX7847 are specified for operation with V_{DD}/V_{SS} = ±11.4V to ±16.5V. However, the output amplifier requires 2.5V of headroom, so the reference input should not come within 2.5V of V_{DD}/V_{SS} in order to maintain accuracy at full scale.

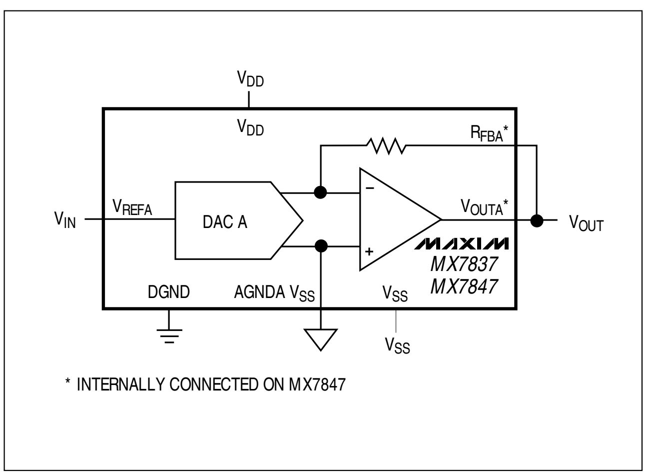


Figure 6. Unipolar Binary Operation

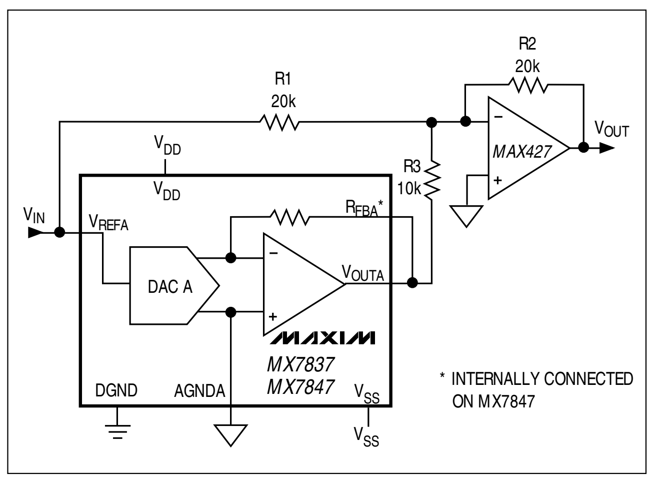
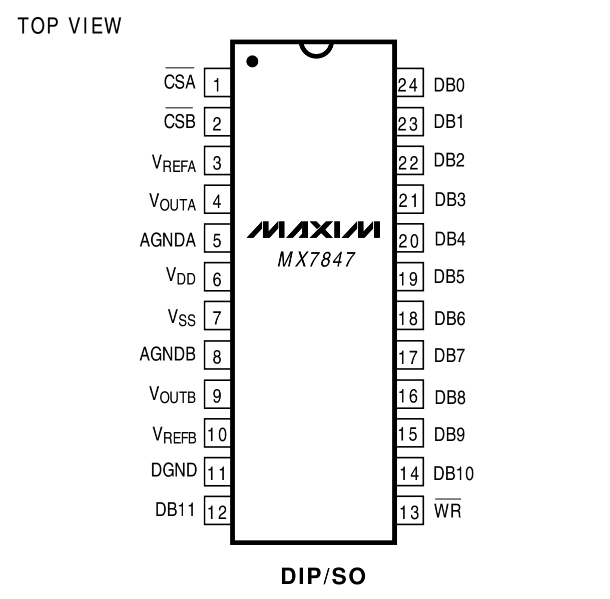
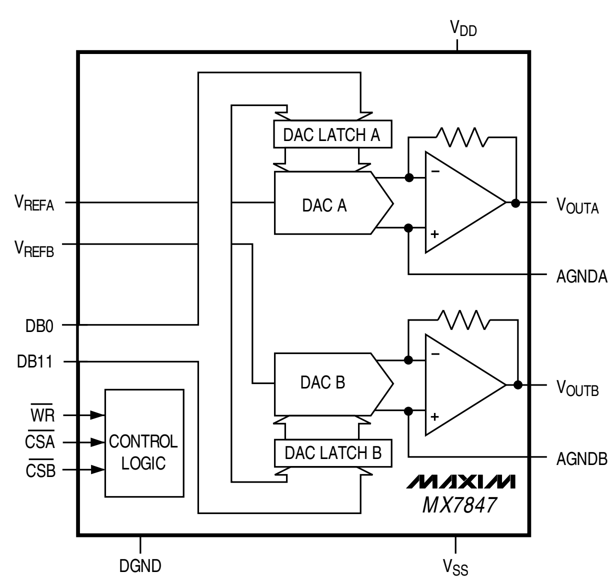


Figure 7. Bipolar Offset Binary Operation

Pin Configurations (continued)



Typical Operating Circuits (continued)



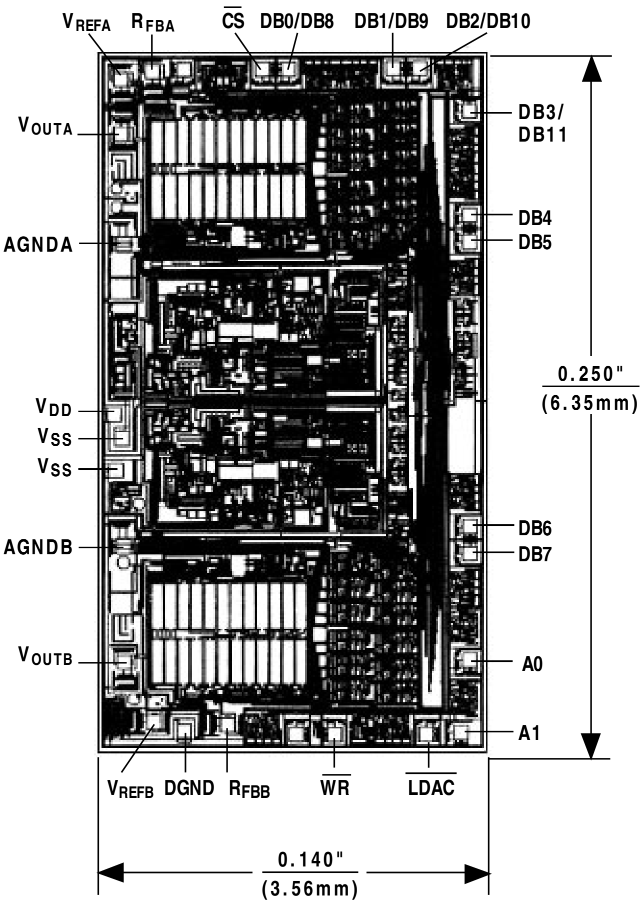
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MX7837AN	-40°C to +85°C	24 Narrow Plastic DIP	±1
MX7837BN	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MX7837AR	-40°C to +85°C	24 Wide SO	±1
MX7837BR	-40°C to +85°C	24 Wide SO	±1/2
MX7837AQ	-40°C to +85°C	24 Narrow CERDIP	±1
MX7837BQ	-40°C to +85°C	24 Narrow CERDIP	±1/2
MX7837SQ	-55°C to +125°C	24 Narrow CERDIP	±1
MX7837TQ	-55°C to +125°C	24 Narrow CERDIP	±1/2
MX7847JN	0°C to +70°C	24 Narrow Plastic DIP	±1
MX7847KN	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MX7847JR	0°C to +70°C	24 Wide SO	±1
MX7847KR	0°C to +70°C	24 Wide SO	±1/2
MX7847C/D	0°C to +70°C	Dice*	±1
MX7847AN	-40°C to +85°C	24 Narrow Plastic DIP	±1
MX7847BN	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MX7847AR	-40°C to +85°C	24 Wide SO	±1
MX7847BR	-40°C to +85°C	24 Wide SO	±1/2
MX7847AQ	-40°C to +85°C	24 Narrow CERDIP	±1
MX7847BQ	-40°C to +85°C	24 Narrow CERDIP	±1/2
MX7847SQ	-55°C to +125°C	24 Narrow CERDIP	±1
MX7847TQ	-55°C to +125°C	24 Narrow CERDIP	±1/2

Complete, Dual, 12-Bit Multiplying DACs

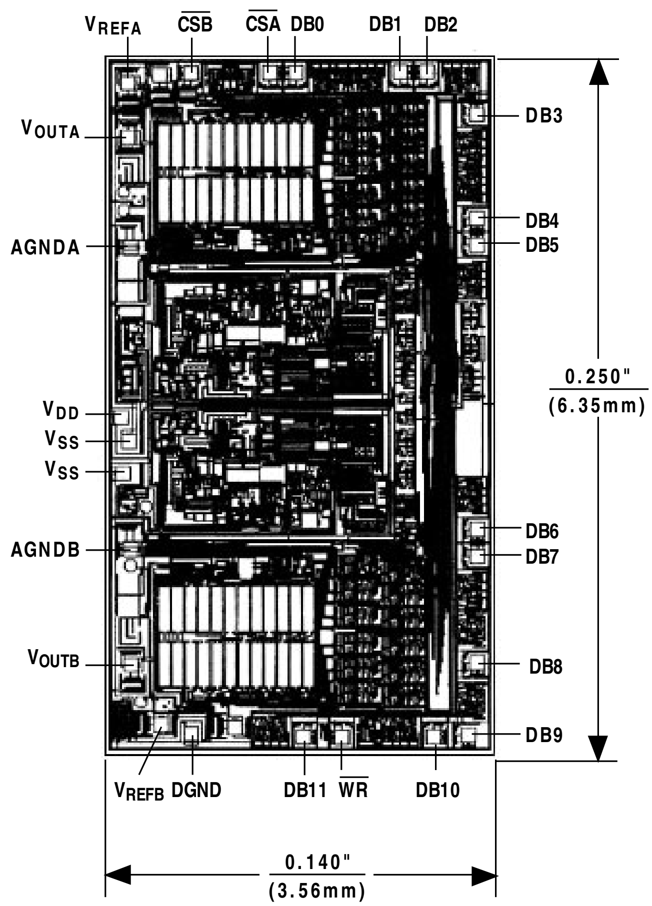
Chip Topographies

MX7837



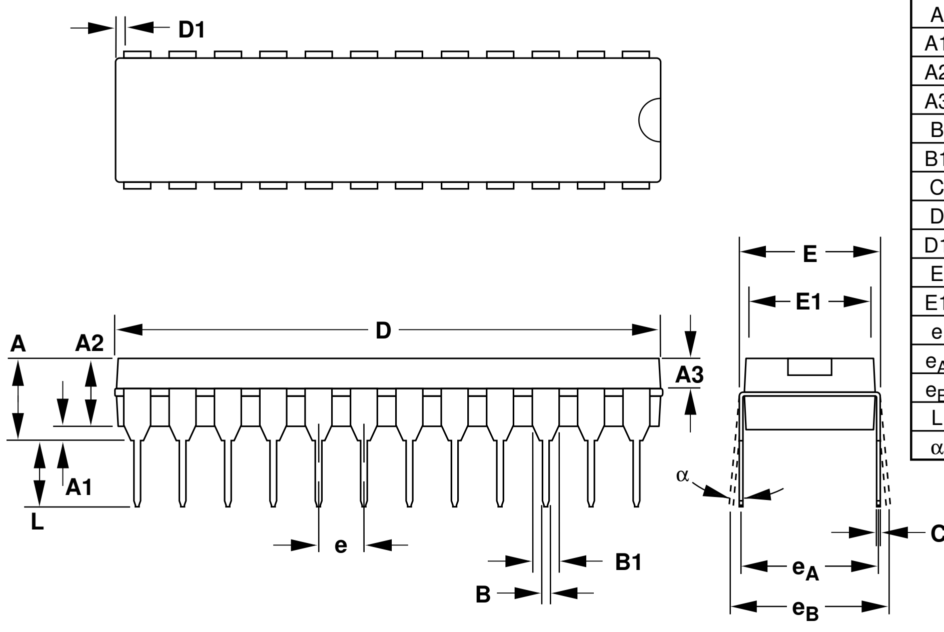
TRANSISTOR COUNT: 1240;
SUBSTRATE CONNECTED TO V_{DD}.

MX7847



TRANSISTOR COUNT: 1240;
SUBSTRATE CONNECTED TO V_{DD}.

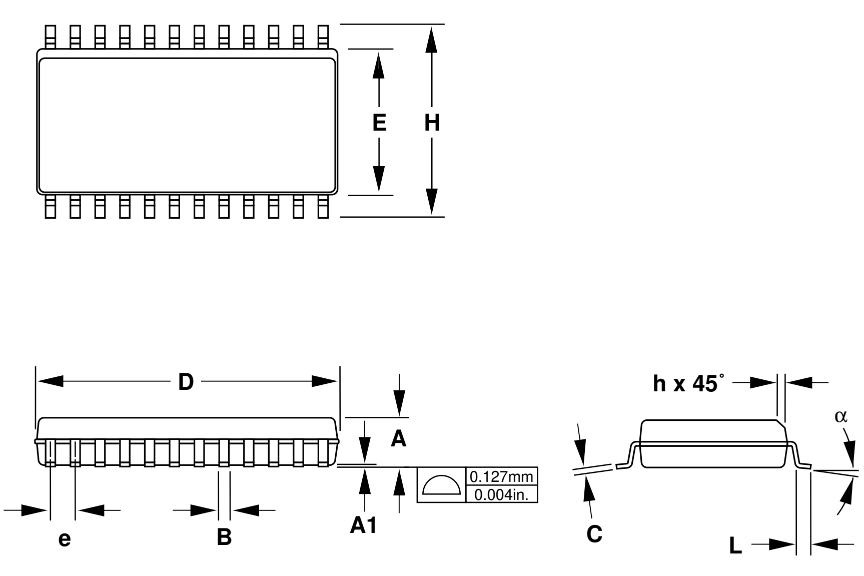
Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	1.235	1.265	31.37	32.13
D1	0.050	0.080	1.27	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0˚	15˚	0˚	15˚

21-337A

24-PIN PLASTIC DUAL-IN-LINE (NARROW) PACKAGE

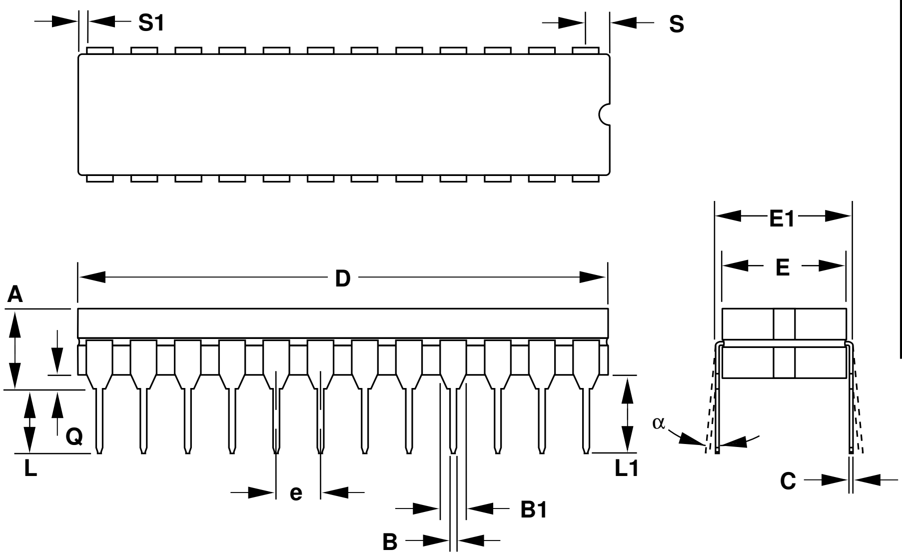


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.20	15.60
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27
α	0˚	8˚	0˚	8˚

21-338A

24-PIN PLASTIC SMALL-OUTLINE PACKAGE

Package Information (continued)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
D	–	1.280	–	32.51
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.060	0.38	1.52
S	–	0.098	–	2.49
S1	0.005	–	0.13	–
α	0˚	15˚	0˚	15˚

21-340B

24-PIN CERAMIC DUAL-IN-LINE (NARROW) PACKAGE