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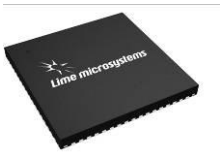
MYRIAD RF



MyriadRF

Development Kit

Rev: 1.0r4
Last modified: 03/05/2013

Contents

1 Introduction 8
2 Development System Contents 9
3 Development System Connections 11
3.1 Basic Connections 11
3.2 Myriad-RF Board Connections 11
3.2.1. X2 – +5V Supply Connector 13
3.2.2. X3 – Digital I/O Connector 13
3.2.3. X4 and X5 – Analog IQ Connectors 15
3.2.4. X6 and X7 – RF Input and Output 15
3.2.5. X8 – External CLK Connector 15
3.2.6. X9 – External SPI Connector 15
3.3 Digial Interface Board Connections 16
3.3.1. J1 and J3 - + 5 V power Connectors 17
3.3.2. J2 – Digital I/O Connector 17
3.3.3. J4 – Mini USB Connector 18
3.3.4. J5 – EEPREOM Boot memory connector 18
3.3.5. J6 – CLK Output Connector 18
3.3.6. J7 – Frequency Synthesizer Enable Connector 19
3.3.7. J8 and J9 – Main Power Supply Connector 19
3.3.8. JA1 – FPGA Module Connectors Array 20
3.4 Hardware options: Clocking, SPI, GPIO truth table & Standalone. 21
3.5 Reference Frequency and Data Clocks Distribution 21
3.6 SPI Options 22
3.7 GPIO control truth table 22
3.8 Standalone Mode 23
4 Installing and Running the PC Software Application 24
4.1 Windows USB driver installations 24
4.2 Firmware installation for USB microcontroller 27
4.2.1. Downloading firmware to the FX2LP's RAM 28
4.2.2. Downloading firmware to the empty EEPROM 29
4.2.3. Downloading firmware to the not empty EEPROM 29
4.3 FPGA Programming over Embedded USB – Blaster 29
4.3.1. FPGA software Installation procedure 29
4.3.2. Software Functionality 31
4.4 Turn On and SPI Check 32
4.5 Ctr6002dr2 – Software Description 34
4.5.1. System Interface 34
4.5.2. Top level 36

4.5.3. TX PLL + DSM 38
4.5.4. Rx PLL + DSM 42
4.5.5. Tx LPF 47
4.5.6. Tx RF 48
4.5.7. Rx LPF 49
4.5.8. RX VGA2 50
4.5.9. RX FE 52
4.5.10. ADC/DAC 55
4.5.11. Board 58

5 Trasnmitter and Receiver Basic Setup 59

5.1 Transmitter Setup and Basic Testing 59
5.1.1. Top Level Setting 59
5.1.2. TX LPF & Gain Setting 60
5.1.3. TX PLL Setup 61
5.2 Testing TX Output 62
5.2.1. TX Basic Operation Checks 63
5.3 Receiver Setup and Basic Testing 64
5.3.1. Top Level Settings 64
5.3.2. RX LPF & Gain Setting 65
5.3.3. RX PLL Setup 66
5.4 Testing RX Analogue Output 68
5.4.1. RX Basic Operation Checks 68

6 LMS6002D Calibration Procedures 69

6.1 TX LO Leakage Calibration 69
6.2 Transmit I/Q Balance Calibration 72
6.3 Receiver DC Calibration 75
6.4 Calibration Process Summary 79

7 Appendix A – Saving and Retreiving SPI Test Setups 80

7.1 Saving a Setup 80
7.2 Loading *.prj Files 81

8 Appendix B – PC and USB Controller Communication 84

8.1 COM Port Settings 84
8.2 Communication testing 85
8.3 Controlling Reset line of LMS6002 85
8.4 Read data from LMS6002 85
8.5 Write data to LMS6002 86

9 Appendix C – Test System Connections 87

9.1 Basic Setup 87
9.2 Transmitter Test System Connections 88

9.3 Receive Test System Connections 88
10 Appendix D – Signal Generator Setup 89
10.1 Agilent MXG Setup 89
10.2 Downloading *.wfm Files to the Signal Generator 92

Table of Figures

Figure 1 Development System 9
Figure 2 Development System Content 10
Figure 3 Myriad-RF board connection descriptions. 12
Figure 4 DEO – Interface board connection descriptions. 16
Figure 5 Digital I/O connector 17
Figure 6 Mini USB conector. 18
Figure 7 CLK output connector. 18
Figure 8 Frequency synthesizer enable connector 19
Figure 9 Main power supply connector 19
Figure 10 FPGA Module connectors array. 20
Figure 11 Hardware wizard. 25
Figure 12 Hardware wizard. Install driver manually 25
Figure 13 Hardware wizard. Choose the required from the folder 26
Figure 14 Hardware installation warning window 26
Figure 15 Default FX2LP firmware, supplied by internal logic 27
Figure 16 FX2LP after custom firmware is downloaded 28
Figure 17 View of the Quartus II Programmer 30
Figure 18 GUI communication settings. 32
Figure 19 GUI register test. 33
Figure 20 GUI register test log. 33
Figure 21 GUI System window. 34
Figure 22 GUI Top Level window 36
Figure 23 GUI TxPLL + DSM window 38
Figure 24 PLL mode. 39
Figure 25 Output Frequency – GHz 39
Figure 26 Calculated Values for Fractional Mode 40
Figure 27 VCO Capacitance 40
Figure 28 Current VCO and MUX/DIV selections 40
Figure 29 VCO Capacitance 41
Figure 30 CP Current and Offset 41
Figure 31 Frequency versus capacitance calibration table data 42
Figure 32 RX PLL + DSM page 43
Figure 33 PLL Mode 44
Figure 34 Setting receiver frequency - GHz 44
Figure 35 Calculated values for fractional mode 44
Figure 36 VCO Capacitance 45
Figure 37 Current VCO and MUX/DIV selections 45
Figure 38 VCO Capacitance 45
Figure 39 CP Current and Offset 46
Figure 40 Frequency vs capacitance calibration table data 46

Figure 41 Tx LPF page 47
Figure 42 Tx RF page 48
Figure 43 Rx LPF page 49
Figure 44 Rx VGA2 page 50
Figure 45 Rx FE (Front End) 52
Figure 46 LNA Control setting 53
Figure 47 MIX Control settings 54
Figure 48 ADC/DAC page 55
Figure 49 DAC enable control timing for TX 56
Figure 50 ADC enable control timing for RX 56
Figure 51 ADC/DAC Reference control – default settings 57
Figure 52 ADC Control settings 57
Figure 53 Board section 58
Figure 54 Top Level Settings 60
Figure 55 Setting Tx LPF bandwidth 60
Figure 56 Tx gain setting and PA selection 61
Figure 57 Tx PLL setting 62
Figure 58 Basic TX testing using DC offset resulting in LO leakage 62
Figure 59 Top Level Settings 64
Figure 60 Setting Rx LPF to 7 MHz 65
Figure 61 Setting Rx VGA2 gain 65
Figure 62 Rx LNA and VGA1 settings 66
Figure 63 Rx PLL settings 67
Figure 64 Oscilloscope capture of 1 MHz I & Q Sine wave outputs 68
Figure 65 Transmit Output 70
Figure 66 System Window. Use Automated Calibration 70
Figure 67 Transmit Output After Calibration 71
Figure 68 Tx RF window 71
Figure 69 Transmit output after calibration 72
Figure 70 Initial -1 MHz Image Spectrum 73
Figure 71 Phase angle calibration 73
Figure 72 Amplitude balance calibration 74
Figure 73 Transmit EVM performance after calibration 74
Figure 74 Rx FE page 75
Figure 75 Rx LPF tab 76
Figure 76 Rx VGA2 Tab 76
Figure 77 Receiver LO leakage 77
Figure 78 Rx VGA1 DC Offset Adjust in RX FE Tab 77
Figure 79 Rx automatic DC calibration result 78
Figure 80 Save Project feature 81
Figure 81 Open project 81
Figure 82 Auto Download feature 82
Figure 83 Download Button for Previously Saved Setup 82
Figure 84 Test system connections for receive and transmit Testing 87

Figure 85 Transmitter test setup 88
Figure 86 Receiver test setup 88
Figure 87 Agilent N5181A/82A MXG Front Panel 89

1

Introduction

The Myriad – RF Development Kit is a low cost universal radio development platform, based on flexible, multi standard LMS6002DFN transceiver and Altera FPGA module. It enables developers to implement their products for a wide variety of wireless communication applications efficiently. The main ideas are to:

- Make use of a ready-made design and implementation to accelerate the development time.
- Experiment and evaluate new modulation schemes and wireless systems, operating over a wide frequency range.
- Easily modify and manufacture the platform for new designs using the Open Source database for the complete Kit.

This document provides the following information:

- Detailed description of the hardware platform including setup.
- Software installation, setup and programing of the LMS6002DFN.
- Example files on running of the complete platform including the Altera FPGA module.

2

Development System Contents

Fully operational development system contains Myriad-RF board, Digital interface board (interface board) and *DEO – Nano* development kit. See Figure 1 Development System below:

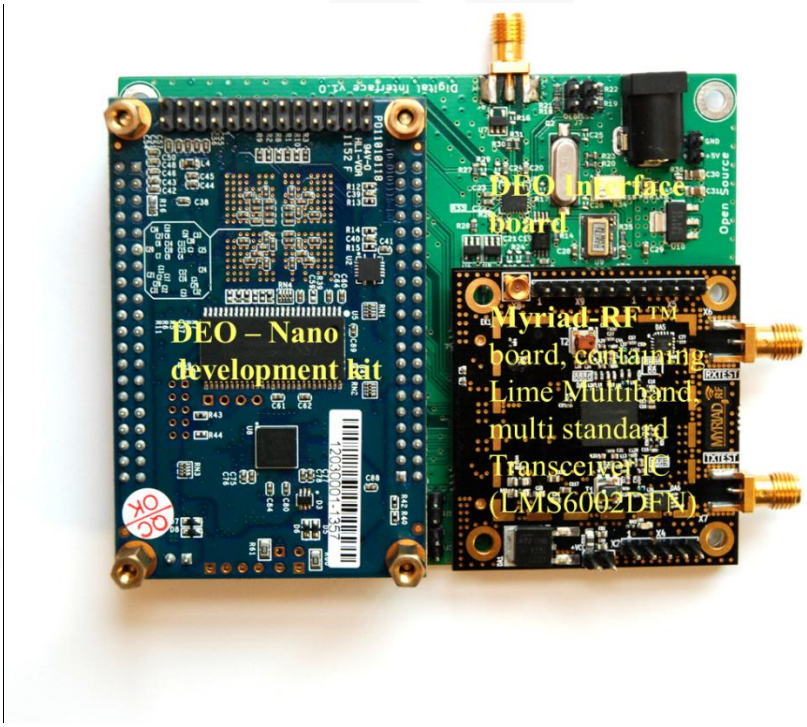
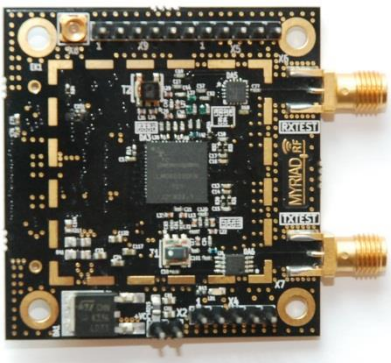
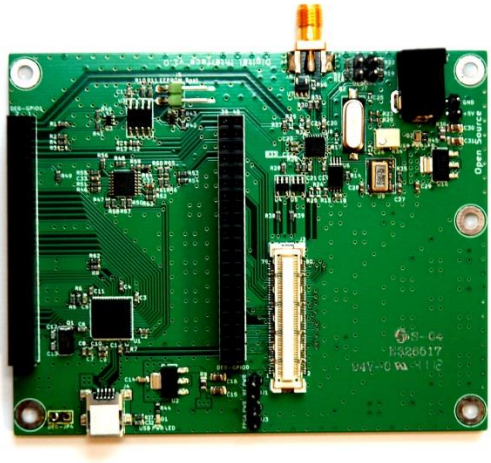


Figure 1 Development System

DEO – Nano
Development Kit



Myriad-RF Board



Digital Interface Board

AC – DC adaptor +5 V

Software

Figure 2 Development System Content

3

Development Kit Connections

3.1 Basic Connections

The Myriad-RF Board can be used as a standalone board or in conjunction with the interface board for a direct connection to the TerAsic DEO – Nano development kit. The Myriad-RF board is connected to the interface board via the standard connector FX10A-80P, connecting digital interface to *DEO – Nano* development kit. The following sections describe the connections on both boards as well as the overall functionality with the DEO board.

3.2 Myriad-RF Board Connections

The analog differential IQ interface is also available on Myriad-RF board and provided via X3 and X4 connectors, see figure 3. X6 and X7 are the RF connection for receive input and transmitter output on the RF board, see figure 3. The RF board is tuned to support band 1 (Tx 2140 MHz and Rx 1950 MHz) and broadband operation. The front end switches are configurable for selected receiver input and transmitter output via GPIO's. The GPIO's are controlled by FPGA module. The truth table for each selection mode (RX and/or TX) is shown in truth table, section 3.7.

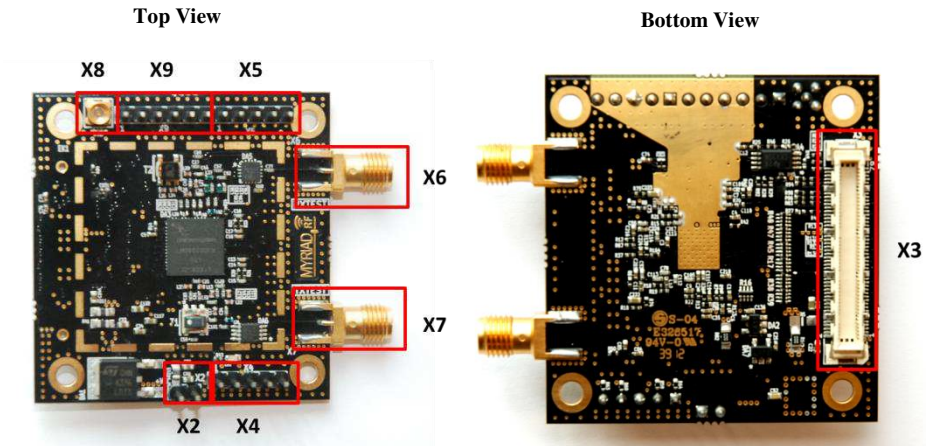


Figure 3 Myriad-RF board connection descriptions.

The following table describes the pin assignment for each connector on the Myriad-RF board.

Connector	Name	Description
X2	+5 V supply	External +5 V supply.
X3	Digital I/O	The FX10A-80P is a standard connector used to interface the RF board directly to interface board or any other baseband board.
X4	TX Analog I/Q	Connector used to supply Transmit analog I/Q signals.
X5	RX Analog I/Q	Connector used to measure Receive analog I/Q signals.
X6	RXTEST	SMA connector provides connection to low band or high band RX input. Requires preselected RF switch configuration.
X7	TXTEST	SMA connector that provides connection to low band or high band TX output. Requires preselected RF switch configuration.
X8	Ext – CLK	Connector used to supply PLL clock externally Please refer to section 3.7 for more information.
X9	Ext – SPI	Connector used to control LMS6002DFN SPI registers externally. SPI register are controlled via X3 connector. Please refer to section 3.6 for more information.

Table 1 Myriad-RF Board Connector Assignments

3.2.1. X2 – +5V Supply Connector

The pin header type connecter used to supply +5 V for Myriad-RF board in standalone mode.

3.2.2. X3 – Digital I/O Connector

The Myriad-RF board X3 connector (type FX10A-80P0) is pin compatible with J1 connector on interface board, see figure 4. It provides the digital and SPI interface for LMS6002DFN together with the supply voltage and GPIO control for RF switches for Myriad-RF board. The pin descriptions on this connector are given in the table below:

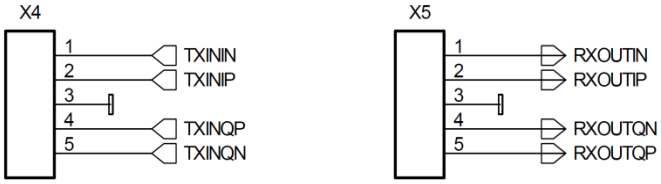
Pin No	Pin Name	Type	Description
1	+5 V	in DC	+5 V power supply
2	+5 V	in DC	+5 V power supply
3	+5 V	in DC	+5 V power supply
4	+5 V	in DC	+5 V power supply
5	GND		Ground pin
6	GND		Ground pin
7	+3.3V	in DC	+3.3 V power supply optional
8	+3.3 V	in DC	+3.3 V power supply optional
9	+3.3V	in DC	+3.3 V power supply optional
10	+3.3V	in DC	+3.3 V power supply optional
11	GND		Ground pin
12	GND		Ground pin
13	-		Not used
14	-		Not used
15	-		Not used
16	-		Not used
17	GND		Ground pin
18	GND		Ground pin
19	TXIQSEL	in cmos	TX digital interface IQ flag
20	-		Not used
21	-		Not used
22	-		Not used
23	TXD0	in cmos	DACs digital input, bit 0 (LSB)
24	TXD1	in cmos	DACs digital input, bit 1
25	TXD2	in cmos	DACs digital input, bit 2
26	TXD3	in cmos	DACs digital input, bit 3
27	GND		Ground pin
28	GND		Ground pin
29	TXD4	in cmos	DACs digital input, bit 4
30	TXD5	in cmos	DACs digital input, bit 5

31	TXD6	in cmos	DACs digital input, bit 6
32	TXD7	in cmos	DACs digital input, bit 7
33	TXD8	in cmos	DACs digital input, bit 8
34	TXD9	in cmos	DACs digital input, bit 9
35	TXD10	in cmos	DACs digital input, bit 10
36	TXD11	in cmos	DACs digital input, bit 11 (MSB)
37	GND		Ground pin
38	GND		Ground pin
39	RXIQSEL	out cmos	RX digital interface IQ flag
40	-		Not used
41	-		Not used
42	-		Not used
43	RXD0	out cmos	ADCs digital output, bit 0 (LSB)
44	RXD1	out cmos	ADCs digital output, bit 1
45	RXD2	out cmos	ADCs digital output, bit 2
46	RXD3	out cmos	ADCs digital output, bit 3
47	GND		Ground pin
48	GND		Ground pin
49	RXD4	out cmos	ADCs digital output, bit 4
50	RXD5	out cmos	ADCs digital output, bit 5
51	RXD6	out cmos	ADCs digital output, bit 6
52	RXD7	out cmos	ADCs digital output, bit 7
53	RXD8	out cmos	ADCs digital output, bit 8
54	RXD9	out cmos	ADCs digital output, bit 9
55	RXD10	out cmos	ADCs digital output, bit 10
56	RXD11	out cmos	ADCs digital output, bit 11 (MSB)
57	GND		Ground pin
58	GND		Ground pin
59	RXCLK	in cmos	RX digital interface clock
60	TXCLK	in cmos	TX digital interface clock
61	-		Not used
62	-		Not used
63	GND		Ground pin
64	GND		Ground pin
65	GPIO0		
66	RESET	in cmos	Hardware reset, active low
67	GPIO1		
68	SPI_MOSI	out cmos	Serial port data out
69	GPIO2		
70	SPI_MISO	in/out cmos	Serial port data in/out
71	-		Not used
72	SPI_CLK	in cmos	Serial port clock, positive edge sensitive

73	GND		Ground pin
74	SPI_NCSO	in cmos	Serial port enable, active low
75	CLK_IN	in cmos	PLL reference clock input
76	-		Not used
77	GND		Ground pin
78	-		Not used
79	TXEN	in cmos	Transmitter enable, active high
80	RXEN	in cmos	Receiver enable, active high
81	GND		Ground pin
82	GND		Ground pin
83	GND		Ground pin
84	GND		Ground pin
85	GND		Ground pin
86	GND		Ground pin
87	GND		Ground pin
88	GND		Ground pin

Table 2 X3 connector pin description

3.2.3. X4 and X5 – Analog IQ Connectors



Pin header type connectors on the Myriad-RF board, provide analog IQ signals I/O.

3.2.4. X6 and X7 – RF Input and Output

The X6 and X7 are SMA type connectors which provide Receive input and Transmit output to the LMS6002DFN, respectively. These are generally used to connect to antenna or test equipment.

3.2.5. X8 – External CLK Connector

The X8 is micro miniature coaxial connector (MMCX8400). It is optional and used to supply external clock in standalone mode.

3.2.6. X9 – External SPI Connector

This is a pin header type connector used for SPI interface to LMS602DFN. This is optional, if the board is used in standalone mode.

3.3 Digial Interface Board Connections

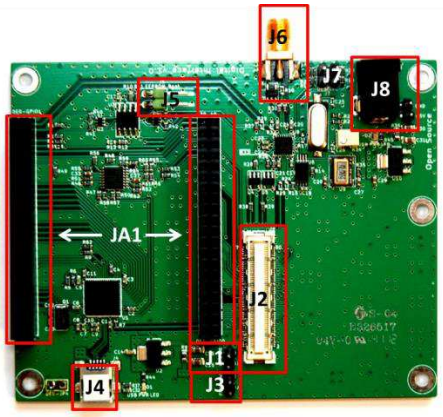


Figure 4 DEO – Interface board connection descriptions.

The following table describes the pin assignment for each connector on the digital interface board.

Connector	Name	Description
J1	RF PWR	Optional +5 V power supply for Myriad-RF board.
J2	Digital I/O	The FX10A-80P is a standard connector used to interface the Myriad-RF board directly to a base band board.
J3	FPGA PWR	Optional +5 V power supply for FPGA Module.
J4	Mini USB	Port used to connect to USB microcontroller.
J5	EEPROM Boot	Enables memory access for USB microcontroller.
J6	CLK output	Used to synchronize measurement equipment. Clock output generated with onboard frequency synthesizer.
J7	Frequency synthesizer Enable	Programmable synthesizer operation control. Enables synthesizer outputs.
J8	Main power supply	+ 5V power supply feed for digital interface board as well and Myriad-RF board. Connector type SPC4077.
J9	Main power supply	+ 5V power supply feed for digital nterface board as well and Myriad-RF board. Connector type 2 way pin header.
JA1	FPGA Module connectors array	The connector array designed to plug *DEO - Nano* development board on to the DEO Interface Board.

Table 3 Interface board connectors

3.3.1. J1 and J3 - + 5 V power Connectors

The pin header type connectors used as jumpers to supply +5 V for Myriad-RF board and FPGA module. The options are used as shown below:

- Use jumper on J1 if Myriad-RF power from interface board.
- Use jumper on J3 if *DEO – Nano* Development Kit is supplied from interface board.

3.3.2. J2 – Digital I/O Connector

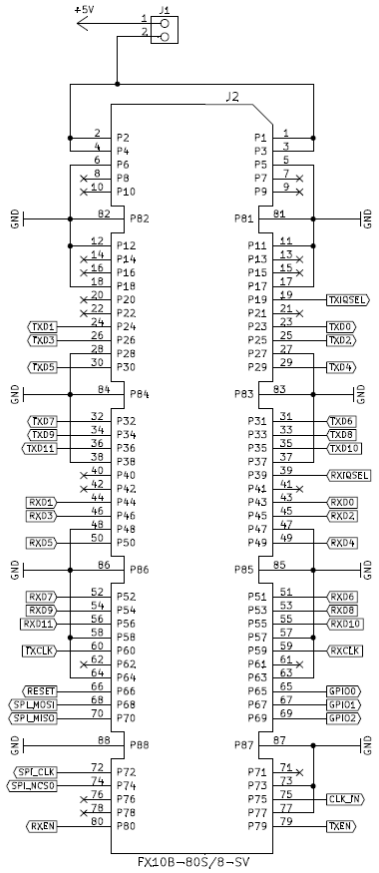


Figure 5 Digital I/O connector

The Myriad-RF board is directly plugged into the J1 connector. The digital I/Q connector is a digital transmit (TX) and receive (RX) interface to the ADC/DAC of the LMS6002D. The SPI interface for LMS6002DFN can also be established via J1 connector.

3.3.3. J4 – Mini USB Connector

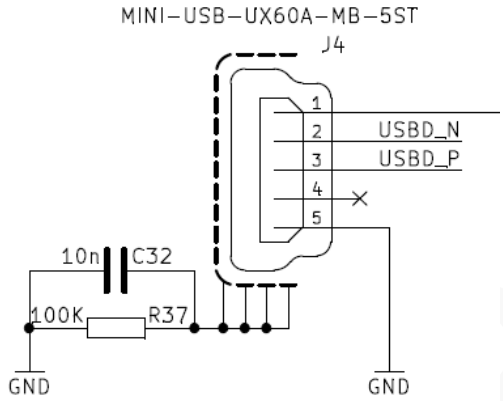


Figure 6 Mini USB conector.

The interface with USB microcontroller and PC is established via mini USB connector. This connector also powers up the microcontroller.

3.3.4. J5 – EEPREOM Boot memory connector

This connector enables USB microcontroller to load the firmware at startup.

3.3.5. J6 – CLK Output Connector

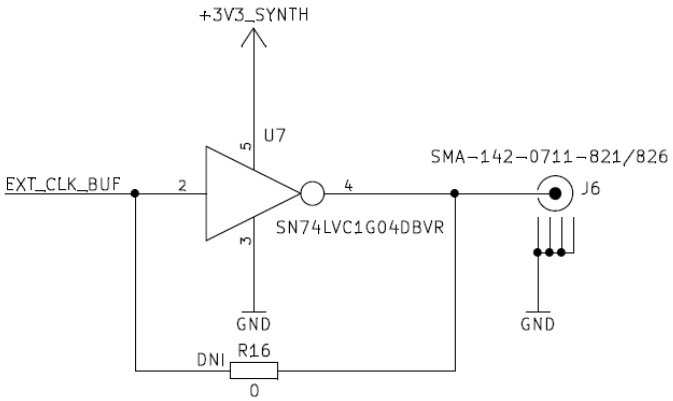


Figure 7 CLK output connector.

J6 is SMA type connector, used to synchronize measurement equipment with development kit.

3.3.6. J7 – Frequency Synthesizer Enable Connector

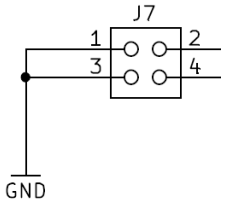


Figure 8 Frequency synthesizer enable connector

This is a pin header type connector. Pin 3 and pin 4 have to be shorted in normal operation, thus enabling frequency synthesizer outputs.

3.3.7. J8 and J9 – Main Power Supply Connector

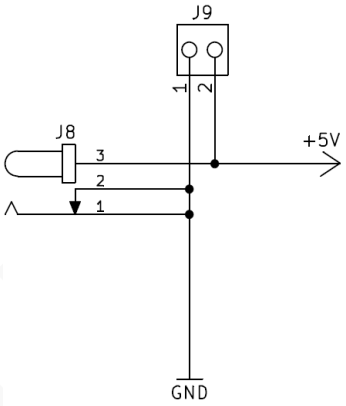


Figure 9 Main power supply connector

The main power supply connector is on interface the board, providing power to both the interface as well as the Myriad-RF board.

3.3.8. JA1 – FPGA Module Connectors Array

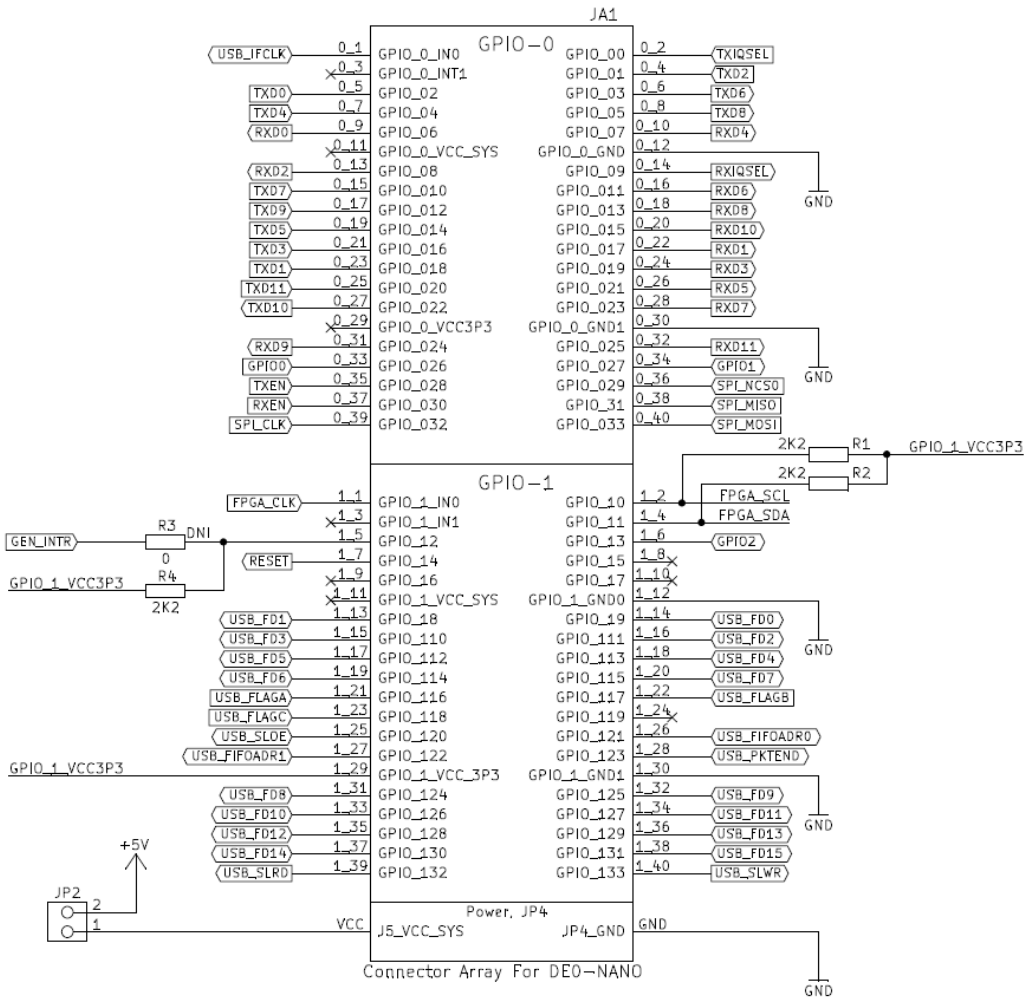


Figure 10 FPGA Module connectors array.

JA1 is a connection array for the *DEO – Nano* development kit. Physically, there are two separate connectors on the board. This connector establishes the interface between Myriad-RF board digital interface and FPGA module with the PC.

3.4 Hardware options: Clocking, SPI, GPIO truth table & Standalone.

This section describes the configurations and set up procedures for:

- Reference frequency and data clocks distribution (Section 3.6).
- GPIO control truth table (Section 3.7).
- Standalone mode (Section 3.8).

The board is shipped in a default mode for basic operation. Various options are available depending on the system configuration required for testing or development work. The options are summarized below and the following sections describe the board modifications required to achieve these configurations.

3.5 Reference Frequency and Data Clocks Distribution

The LMS6002D device provides a flexible clocking scheme which enables the PLL clock, RX clock and TX clock to be independently set.

The development kit is shipped with a default mode using the on board 30.72MHz clock for PLL clock only. The board can be reconfigured to allow users to provide clock frequency for digital interface and PLL clock using programmable clock generator from Silicon Labs (Si5356) which is capable of synthesizing four independent frequencies. The device has four outputs connected to LMS6002DFN PLL clock, RX data interface clock, TX data interface clock and to the J6 connector.

In order to reprogram the frequency from the default setting of 30.72 MHz, please use component change as given in the table below. Please note that NF denotes that component is not fitted:

Reference clock options		
Description / **Component**	**Default mode. PLL clock set to 30.72 MHz**	**Programmable mode. PLL clock can be reprogramed.**
R15	0 Ohm	NF
R24	NF	0 Ohm

Table 4 Reference clock configurations

More information how to progra Frequency synthesizer in 4.5.11 cahpter.

3.6 SPI Options

Interface board offer two option for the SPI communication with Myriad RF board:

1. SPI communication established via FPGA (and via interface board USB microcontroller).
2. SPI communication established via USB microcontroller.

In order to make sure stable SPI communication for desired option, the component change on interface board is given in a table below. Please note that NF denotes that component is not fitted:

SPI Options		
Components	**SPI via FPGA**	**SPI via USB controller**
R48	NF	0 Ohm
R58	NF	0 Ohm
R51	NF	0 Ohm
R46	NF	0 Ohm
R52	NF	0 Ohm

Table 5 SPI options

Note: When SPI communication is selected via USB microcontroller the FPGA lines SPI_NCSO, SPI_MISO, SPI_MOSI, SPI_CLK have to be set to tri-state.

Note: When SPI via FPGA option is selected the Cypress microcontroller has to be programed using firmware version 6 (*firmware_v1r06)*. When SPI via USB microcontroller ption is selected the Cypress microcontroller has to be programed using firmware version 7 (*firmware_v1r08)*. More information how to program Cypress chip in chapter "*4.2 Firmware installation for USB microcontroller"*

3.7 GPIO control truth table

The RF switches on the RF board are controlled via the GPIO 0-2 logic signals, provided by the FPGA module on the interface board. This enables the user to choose RF input/output depending on the operation frequency. The truth table of the GPIO 0-2 settings is shown below.

LMS6002D RF Input/output	**GPIO 0**	**GPIO 1**	**GPIO 2**	**Description**
TX out 1	X	X	0	High band output (1500 – 3800 MHz)
TX out 2	X	X	1	Broadband output
Rx in 1	1	1	X	Low band input (300 – 2200 MHz)
Rx in 2	0	1	X	High band input (1500-3800MHz)

Rx in 3	0	0	X	Broadband input

Table 6 GPIO truth table

Note: LMS6002D RF input/output have to be selected/programed with SPI registers. This is done using GUI software.

3.8 Standalone Mode

The Myriad-RF board can operate in standalone mode. Setup for standalone mode is as follows:

- Connect +5 V power supply to X2 connector on the Myriad-RF board.
- Connect SPI control to X9 connector.
- Connect wanted reference clock to X8 connector. Fit R49 resistor.

In this mode you are able to fully control LMS6002DFN chip register and perform some basic RF measurements using IQ Analog inputs/outputs.

4

Installing and Running the PC Software Application

4.1 Windows USB driver installations

Before plugging USB cable to mini USB port on the interface board:

1. Download the software package from Myriad website [download].
2. Log in as Administrator to your Windows machine for the free USB port.

Plug the USB cable to mini USB port on the interface board. Driver installation window will pop-up. After installation procedure begins, exit/cancel Windows search! Select to install drivers manually.

Figure 11 Hardware wizard.

Next, chose to install driver from specific location.

Figure 12 Hardware wizard. Install driver manually

Select to install drivers manually and point to the driver which can be found in the **cyusb_driver** folder. Please choose the driver suitable for your operating system:

- Windows 2000(w2K)
- Windows XP (wxp)
- Windows Vista (wlh)
- Windows 7 (wlh)

CPU type:

- x86(32bit-i386)
- x64(64bit-amd64)