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Micron Serial NOR Flash Memory

3V, Multiple I/O, 4KB Sector Erase

N25Q128A

Features

- SPI-compatible serial bus interface
- 108 MHz (MAX) clock frequency
- 2.7–3.6V single supply voltage
- Dual/quad I/O instruction provides increased throughput up to 432 MHz
- Supported protocols
  – Extended SPI, dual I/O, and quad I/O
- Execute-in-place (XIP) mode for all three protocols
  – Configurable via volatile or nonvolatile registers
  – Enables memory to work in XIP mode directly after power-on
- PROGRAM/ERASE SUSPEND operations
- Continuous read of entire memory via a single command
  – Fast read
  – Quad or dual output fast read
  – Quad or dual I/O fast read
- Flexible to fit application
  – Configurable number of dummy cycles
  – Output buffer configurable
- Software reset
- 64-byte, user-lockable, one-time programmable (OTP) dedicated area
- Erase capability
  – Subsector erase 4KB uniform granularity blocks
  – Sector erase 64KB uniform granularity blocks
  – Full-chip erase

- Write protection
  – Software write protection applicable to every 64KB sector via volatile lock bit
  – Hardware write protection: protected area size defined by five nonvolatile bits (BP0, BP1, BP2, BP3, and TB)
  – Additional smart protections, available upon request
- Electronic signature
  – JEDEC-standard 2-byte signature (BA18h)
  – Unique ID code (UID): 17 read-only bytes, including:
    - Two additional extended device ID (EDID) bytes to identify device factory options
    - Customized factory data (14 bytes)
- Minimum 100,000 ERASE cycles per sector
- More than 20 years data retention
- Packages JEDEC standard, all RoHS compliant
  – F7 = V-PDFN-8 6mm x 5mm Sawn (MLP8 6mm x 5mm)
  – F8 = V-PDFN-8 8mm x 6mm (MLP8 8mm x 6mm)
  – 12 = T-PBGA-24b05 6mm x 8mm
  – SF = SOP2-16 300 mils body width (SO16W)
  – SE = SOP2-8 208 mils body width (SO8W)

Products and specifications discussed herein are subject to change by Micron without notice.

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Device Description

The N25Q is the first high-performance multiple input/output serial Flash memory device manufactured on 65nm NOR technology. It features execute-in-place (XIP) functionality, advanced write protection mechanisms, and a high-speed SPI-compatible bus interface. The innovative, high-performance, dual and quad input/output instructions enable double or quadruple the transfer bandwidth for READ and PROGRAM operations.

Features

The memory is organized as 256 (64KB) main sectors that are further divided into 16 subsectors each (4096 subsectors in total). The memory can be erased one 4KB subsector at a time, 64KB sectors at a time, or as a whole.

The memory can be write protected by software through volatile and nonvolatile protection features, depending on the application needs. The protection granularity is of 64KB (sector granularity) for volatile protections

The device has 64 one-time programmable (OTP) bytes that can be read and programmed with the READ OTP and PROGRAM OTP commands. These 64 bytes can also be permanently locked with a PROGRAM OTP command.

The device also has the ability to pause and resume PROGRAM and ERASE cycles by using dedicated PROGRAM/ERASE SUSPEND and RESUME instructions.

Operating Protocols

The memory can be operated with three different protocols:

• Extended SPI (standard SPI protocol upgraded with dual and quad operations)
• Dual I/O SPI
• Quad I/O SPI

The standard SPI protocol is extended and enhanced by dual and quad operations. In addition, the dual SPI and quad SPI protocols improve the data access time and throughput of a single I/O device by transmitting commands, addresses, and data across two or four data lines.

XIP Mode

XIP mode requires only an address (no instruction) to output data, improving random access time and eliminating the need to shadow code onto RAM for fast execution.

All protocols support XIP operation. For flexibility, multiple XIP entry and exit methods are available. For applications that must enter XIP mode immediately after powering up, XIP mode can be set as the default mode through the nonvolatile configuration register bits.

Device Configurability

The N25Q family offers additional features that are configured through the nonvolatile configuration register for default and/or nonvolatile settings. Volatile settings can be configured through the volatile and volatile-enhanced configuration registers. These configurable features include the following:

- Number of dummy cycles for the fast READ commands
- Output buffer impedance
- SPI protocol types (extended SPI, DIO-SPI, or QIO-SPI)
- Required XIP mode
- Enabling/disabling HOLD (RESET function)
- Enabling/disabling wrap mode

Figure 1: Logic Diagram
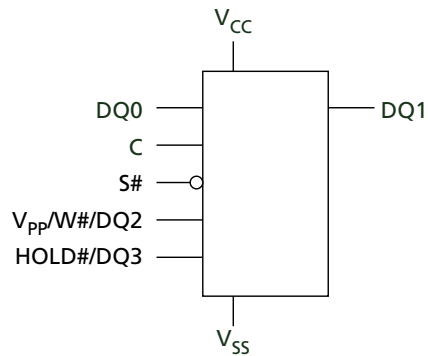
Note: 1. Reset functionality is available in devices with a dedicated part number. See Part Number Ordering Information for more details.

Signal Assignments

Figure 2: 8-Pin, VDFPN8 – MLP8 and SOP2 – SO8W (Top View)

```
        S# ⊏ 1        8 ⊐ V_CC
       DQ1 ⊏ 2        7 ⊐ HOLD#/DQ3
W#/V_PP/DQ2 ⊏ 3        6 ⊐ C
       V_SS ⊏ 4        5 ⊐ DQ0
```
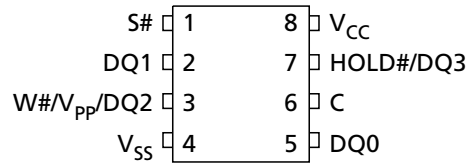
Notes: 1. On the underside of the MLP8 package, there is an exposed central pad that is pulled internally to V_{SS} and must not be connected to any other voltage or signal line on the PCB.
2. Reset functionality is available in devices with a dedicated part number. See Part Number Ordering Information for complete package names and details.

Figure 3: 16-Pin, Plastic Small Outline – SO16 (Top View)
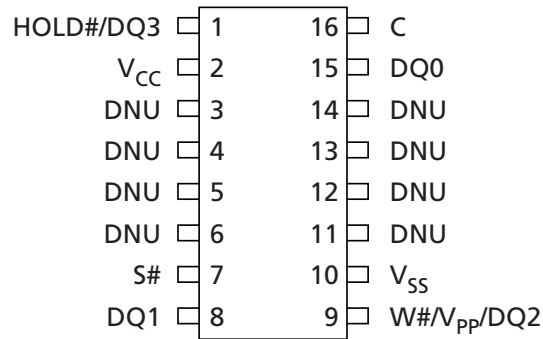
```
 HOLD#/DQ3 ⊏ 1       16 ⊐ C
      V_CC ⊏ 2       15 ⊐ DQ0
       DNU ⊏ 3       14 ⊐ DNU
       DNU ⊏ 4       13 ⊐ DNU
       DNU ⊏ 5       12 ⊐ DNU
       DNU ⊏ 6       11 ⊐ DNU
        S# ⊏ 7       10 ⊐ V_SS
       DQ1 ⊏ 8        9 ⊐ W#/V_PP/DQ2
```

Note: 1. Reset functionality is available in devices with a dedicated part number. See Part Number Ordering Information for complete package names and details.

Figure 4: 24-Ball TBGA (Balls Down)

	1	2	3	4	5
A		NC	NC	NC	NC
B	NC	C	V_{SS}	V_{CC}	NC
C	NC	S#	NC	W#/V_{PP}/DQ2	NC
D	NC	DQ1	DQ0	HOLD#/DQ3	NC
E	NC	NC	NC	NC	NC
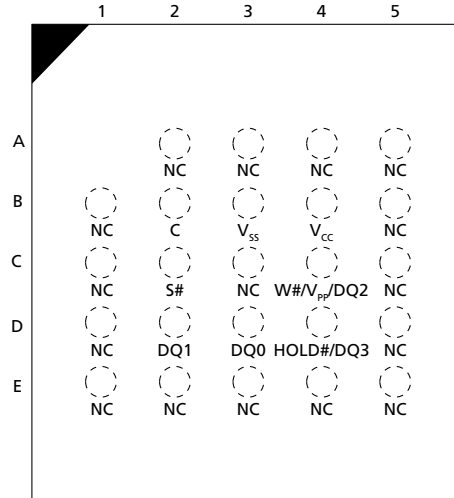
Note: 1. See Part Number Ordering Information for complete package names and details.

Signal Descriptions

The signal description table below is a comprehensive list of signals for the N25 family devices. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 1: Signal Descriptions

Symbol	Type	Description
C	Input	**Clock:** Provides the timing of the serial interface. Commands, addresses, or data present at serial data inputs are latched on the rising edge of the clock. Data is shifted out on the falling edge of the clock.
S#	Input	**Chip select:** When S# is HIGH, the device is deselected and DQ1 is at High-Z. When in extended SPI mode, with the device deselected, DQ1 is tri-stated. Unless an internal PROGRAM, ERASE, or WRITE STATUS REGISTER cycle is in progress, the device enters standby power mode (not deep power-down mode). Driving S# LOW enables the device, placing it in the active power mode. After power-up, a falling edge on S# is required prior to the start of any command.
DQ0	Input and I/O	**Serial data:** Transfers data serially into the device. It receives command codes, addresses, and the data to be programmed. Values are latched on the rising edge of the clock. DQ0 is used for input/output during the following operations: DUAL OUTPUT FAST READ, QUAD OUTPUT FAST READ, DUAL INPUT/OUTPUT FAST READ, and QUAD INPUT/OUTPUT FAST READ. When used for output, data is shifted out on the falling edge of the clock. In DIO-SPI, DQ0 always acts as an input/output. In QIO-SPI, DQ0 always acts as an input/output, with the exception of the PROGRAM or ERASE cycle performed with V_{PP}. The device temporarily enters the extended SPI protocol and then returns to QIO-SPI as soon as V_{PP} goes LOW.
DQ1	Output and I/O	**Serial data:** Transfers data serially out of the device. Data is shifted out on the falling edge of the clock. DQ1 is used for input/output during the following operations: DUAL INPUT FAST PROGRAM, QUAD INPUT FAST PROGRAM, DUAL INPUT EXTENDED FAST PROGRAM, and QUAD INPUT EXTENDED FAST PROGRAM. When used for input, data is latched on the rising edge of the clock. In DIO-SPI, DQ1 always acts as an input/output. In QIO-SPI, DQ1 always acts as an input/output, with the exception of the PROGRAM or ERASE cycle performed with the enhanced program supply voltage (V_{PP}). In this case the device temporarily enters the extended SPI protocol and then returns to QIO-SPI as soon as V_{PP} goes LOW.
DQ2	Input and I/O	**DQ2:** When in QIO-SPI mode or in extended SPI mode using QUAD FAST READ commands, the signal functions as DQ2, providing input/output. All data input drivers are always enabled except when used as an output. Micron recommends customers drive the data signals normally (to avoid unnecessary switching current) and float the signals before the memory device drives data on them.
DQ3	Input and I/O	**DQ3:** When in quad SPI mode or in extended SPI mode using quad FAST READ commands, the signal functions as DQ3, providing input/output. HOLD# is disabled and RESET# is disabled if the device is selected.
RESET#	Control Input	**RESET:** This is a hardware RESET# signal. When RESET# is driven HIGH, the memory is in the normal operating mode. When RESET# is driven LOW, the memory enters reset mode and output is High-Z. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost.

Table 1: Signal Descriptions (Continued)

Symbol	Type	Description
HOLD#	Control Input	**HOLD:** Pauses any serial communications with the device without deselecting the device. DQ1 (output) is High-Z. DQ0 (input) and the clock are "Don't Care." To enable HOLD, the device must be selected with S# driven LOW. HOLD# is used for input/output during the following operations: QUAD OUTPUT FAST READ, QUAD INPUT/OUTPUT FAST READ, QUAD INPUT FAST PROGRAM, and QUAD INPUT EXTENDED FAST PROGRAM. In QIO-SPI, HOLD# acts as an I/O (DQ3 functionality), and the HOLD# functionality is disabled when the device is selected. When the device is deselected (S# is HIGH) in parts with RESET# functionality, it is possible to reset the device unless this functionality is not disabled by means of dedicated registers bits. The HOLD# functionality can be disabled using bit 4 of the NVCR or bit 4 of the VECR. On devices that include DTR mode capability, the HOLD# functionality is disabled as soon as a DTR operation is recognized.
W#	Control Input	**Write protect:** W# can be used as a protection control input or in QIO-SPI operations. When in extended SPI with single or dual commands, the WRITE PROTECT function is selectable by the voltage range applied to the signal. If voltage range is low (0V to V_{CC}), the signal acts as a write protection control input. The memory size protected against PROGRAM or ERASE operations is locked as specified in the status register block protect bits 3:0. W# is used as an input/output (DQ2 functionality) during QUAD INPUT FAST READ and QUAD INPUT/OUTPUT FAST READ operations and in QIO-SPI.
V_{PP}	Power	**Supply voltage:** If V_{PP} is in the voltage range of V_{PPH}, the signal acts as an additional power supply, as defined in the AC Measurement Conditions table. During QIFP, QIEFP, and QIO-SPI PROGRAM/ERASE operations, it is possible to use the additional V_{PP} power supply to speed up internal operations. However, to enable this functionality, it is necessary to set bit 3 of the VECR to 0. In this case, V_{PP} is used as an I/O until the end of the operation. After the last input data is shifted in, the application should apply V_{PP} voltage to V_{PP} within 200ms to speed up the internal operations. If the V_{PP} voltage is not applied within 200ms, the PROGRAM/ERASE operations start at standard speed. The default value of VECR bit 3 is 1, and the V_{PP} functionality for quad I/O modify operations is disabled.
V_{CC}	Power	**Device core power supply:** Source voltage.
V_{SS}	Ground	**Ground:** Reference for the V_{CC} supply voltage.
DNU	–	Do not use.
NC	–	No connect.

Memory Organization

Memory Configuration and Block Diagram

Each page of memory can be individually programmed. Bits are programmed from one through zero. The device is subsector, sector, or bulk-erasable, but not page-erasable. Bits are erased from zero through one. The memory is configured as 16,777,216 bytes (8 bits each); 256 sectors (64KB each); 4096 subsectors (4KB each); and 65,536 pages (256 bytes each); and 64 OTP bytes are located outside the main memory array.

Figure 5: Block Diagram
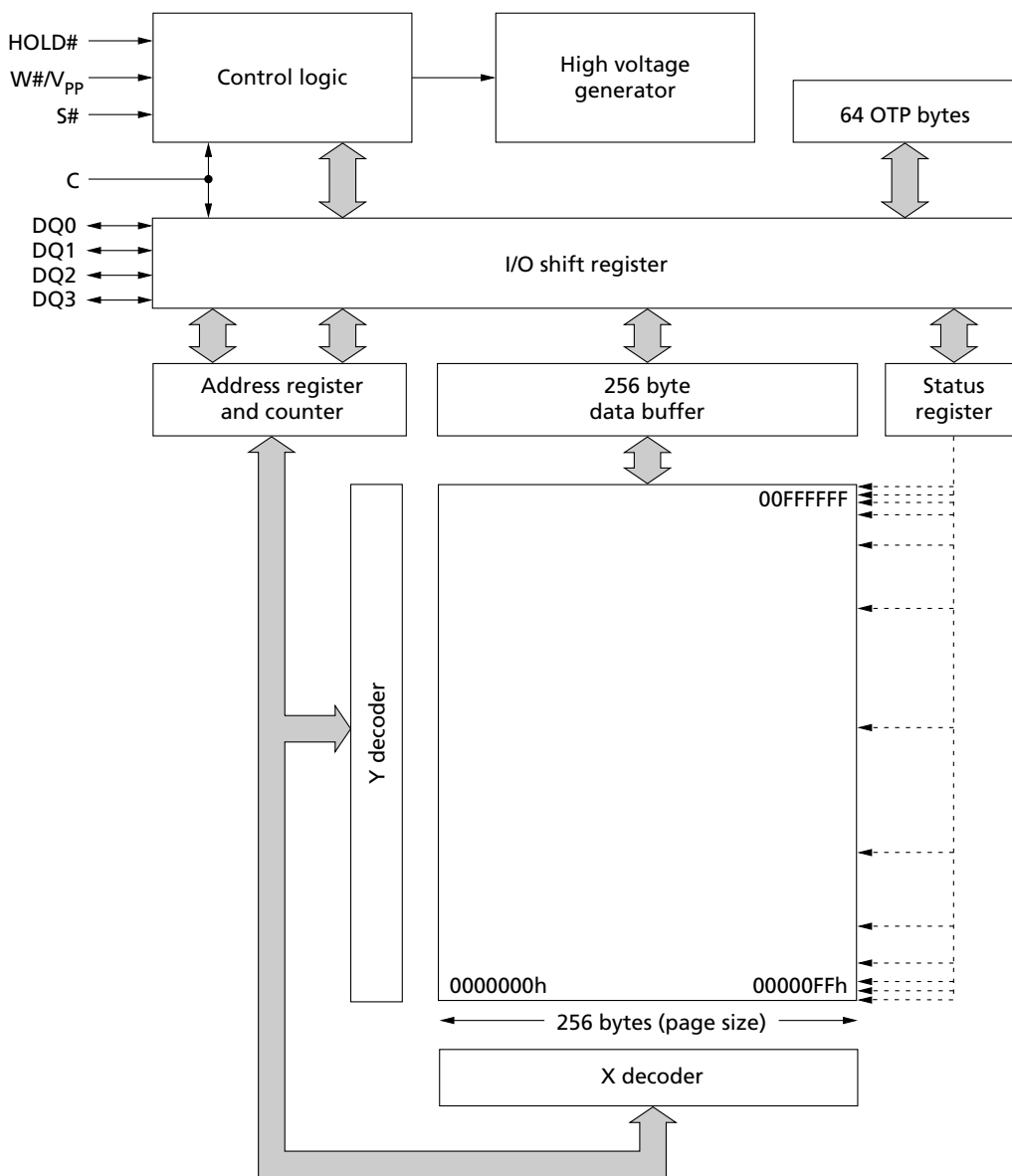
Memory Map – 128Mb Density

Table 2: Sectors[255:0]

Sector	Subsector	Address Range	
		Start	**End**
255	4095	00FF F000h	00FF FFFFh
	⋮	⋮	⋮
	4080	00FF 0000h	00FF 0FFFh
⋮	⋮	⋮	⋮
127	2047	007F F000h	007F FFFFh
	⋮	⋮	⋮
	2032	007F 0000h	007F 0FFFh
⋮	⋮	⋮	⋮
63	1023	003F F000h	003F FFFFh
	⋮	⋮	⋮
	1008	003F 0000h	003F 0FFFh
⋮	⋮	⋮	⋮
0	15	0000 F000h	0000 FFFFh
	⋮	⋮	⋮
	0	0000 0000h	0000 0FFFh

Device Protection

Table 3: Data Protection using Device Protocols

Note 1 applies to the entire table

Protection by:	Description
Power-on reset and internal timer	Protects the device against inadvertent data changes while the power supply is outside the operating specification.
Command execution check	Ensures that the number of clock pulses is a multiple of one byte before executing a PROGRAM or ERASE command, or any command that writes to the device registers.
WRITE ENABLE operation	Ensures that commands modifying device data must be preceded by a WRITE ENABLE command, which sets the write enable latch bit in the status register.

Note: 1. Extended, dual, and quad SPI protocol functionality ensures that device data is protected from excessive noise.

Table 4: Memory Sector Protection Truth Table

Note 1 applies to the entire table

Sector Lock Register		Memory Sector Protection Status
Sector Lock Down Bit	Sector Write Lock Bit	
0	0	Sector unprotected from PROGRAM and ERASE operations. Protection status reversible.
0	1	Sector protected from PROGRAM and ERASE operations. Protection status reversible.
1	0	Sector unprotected from PROGRAM and ERASE operations. Protection status not reversible except by power cycle or reset.
1	1	Sector protected from PROGRAM and ERASE operations. Protection status not reversible except by power cycle or reset.

Note: 1. Sector lock register bits are written to when the WRITE LOCK REGISTER command is executed. The command will not execute unless the sector lock down bit is cleared (see the WRITE LOCK REGISTER command).

Table 5: Protected Area Sizes – Upper Area

Note 1 applies to the entire table

Status Register Content					Memory Content	
Top/ Bottom Bit	BP3	BP2	BP1	BP0	Protected Area	Unprotected Area
0	0	0	0	0	None	All sectors
0	0	0	0	1	Upper 256th	Sectors (0 to 254)
0	0	0	1	0	Upper 128th	Sectors (0 to 253)
0	0	0	1	1	Upper 64th	Sectors (0 to 251)
0	0	1	0	0	Upper 32th	Sectors (0 to 247)
0	0	1	0	1	Upper 16nd	Sectors (0 to 239)

Table 5: Protected Area Sizes – Upper Area (Continued)

Note 1 applies to the entire table

Status Register Content					Memory Content	
Top/ Bottom Bit	BP3	BP2	BP1	BP0	Protected Area	Unprotected Area
0	0	1	1	0	Upper 8th	Sectors (0 to 223)
0	0	1	1	1	Upper quarter	Sectors (0 to 191)
0	1	0	0	0	Upper half	Sectors (0 to 127)
0	1	0	0	1	All sectors	None
0	1	0	1	0	All sectors	None
0	1	0	1	1	All sectors	None
0	1	1	0	0	All sectors	None
0	1	1	0	1	All sectors	None
0	1	1	1	0	All sectors	None
0	1	1	1	1	All sectors	None

Note: 1. See the Status Register for details on the top/bottom bit and the BP 3:0 bits.

Table 6: Protected Area Sizes – Lower Area

Note 1 applies to the entire table

Status Register Content					Memory Content	
Top/ Bottom Bit	BP3	BP2	BP1	BP0	Protected Area	Unprotected Area
1	0	0	0	0	None	All sectors
1	0	0	0	1	Lower 256th	Sectors (1 to 255)
1	0	0	1	0	Lower 128th	Sectors (2 to 255)
1	0	0	1	1	Lower 64th	Sectors (4 to 255)
1	0	1	0	0	Lower 32th	Sectors (8 to 255)
1	0	1	0	1	Lower 16nd	Sectors (16 to 255)
1	0	1	1	0	Lower 8th	Sectors (32 to 255)
1	0	1	1	1	Lower quarter	Sectors (64 to 255)
1	1	0	0	0	Lower half	Sectors (128 to 255)
1	1	0	0	1	All sectors	None
1	1	0	1	0	All sectors	None
1	1	0	1	1	All sectors	None
1	1	1	0	0	All sectors	None
1	1	1	0	1	All sectors	None
1	1	1	1	0	All sectors	None
1	1	1	1	1	All sectors	None

Note: 1. See the Status Register for details on the top/bottom bit and the BP 3:0 bits.

Serial Peripheral Interface Modes

The device can be driven by a microcontroller while its serial peripheral interface is in either of the two modes shown here. The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring data. Input data is latched in on the rising edge of the clock, and output data is available from the falling edge of the clock.

Table 7: SPI Modes

Note 1 applies to the entire table

SPI Modes	Clock Polarity
CPOL = 0, CPHA = 0	C remains at 0 for (CPOL = 0, CPHA = 0)
CPOL = 1, CPHA = 1	C remains at 1 for (CPOL = 1, CPHA = 1)

Note: 1. The listed SPI modes are supported in extended, dual, and quad SPI protocols.

Shown below is an example of three memory devices in extended SPI protocol in a simple connection to an MCU on an SPI bus. Because only one device is selected at a time, that one device drives DQ1, while the other devices are High-Z.

Resistors ensure the device is not selected if the bus master leaves S# High-Z. The bus master might enter a state in which all input/output is High-Z simultaneously, such as when the bus master is reset. Therefore, the serial clock must be connected to an external pull-down resistor so that S# is pulled HIGH while the serial clock is pulled LOW. This ensures that S# and the serial clock are not HIGH simultaneously and that ^{t}SHCH is met. The typical resistor value of 100kΩ, assuming that the time constant R × Cp (Cp = parasitic capacitance of the bus line), is shorter than the time the bus master leaves the SPI bus in High-Z.

Example: Cp = 50pF, that is R × Cp = 5µs. The application must ensure that the bus master never leaves the SPI bus High-Z for a time period shorter than 5µs. W# and HOLD# should be driven either HIGH or LOW, as appropriate.
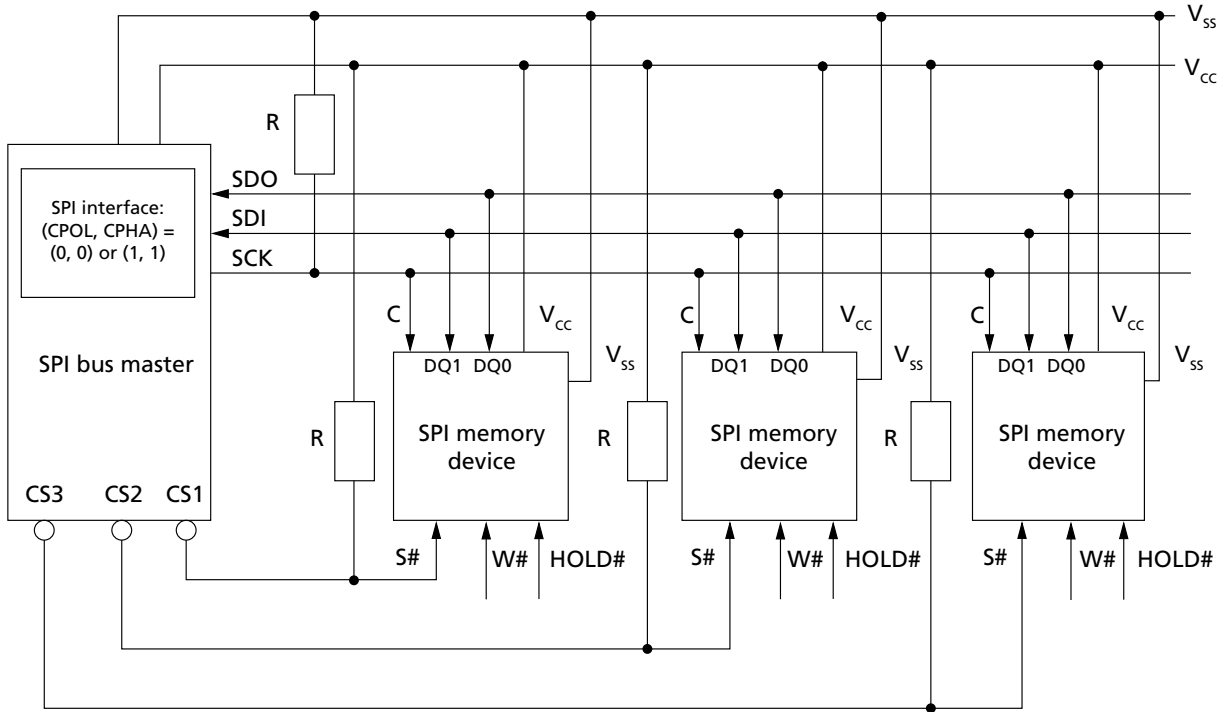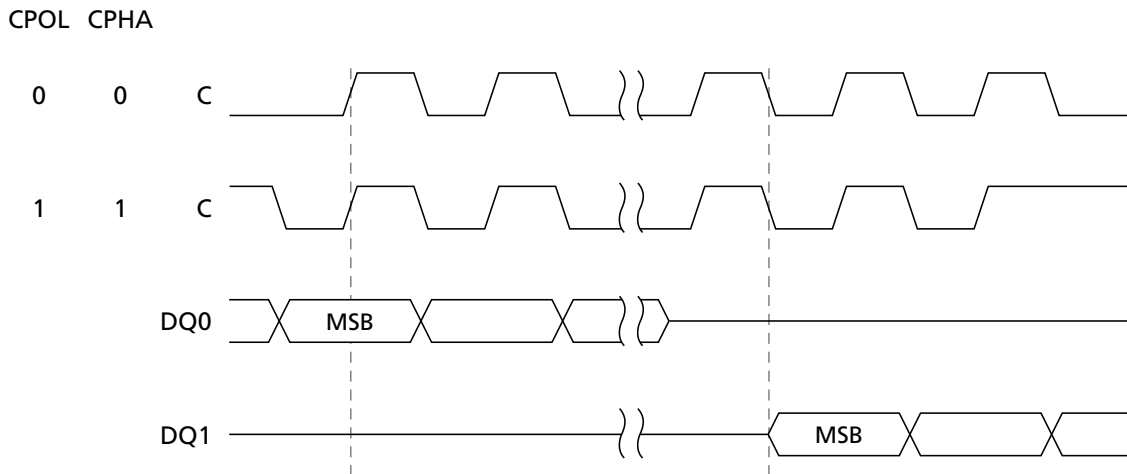
Figure 6: Bus Master and Memory Devices on the SPI Bus

Figure 7: SPI Modes

SPI Protocols

Table 8: Extended, Dual, and Quad SPI Protocols

Protocol Name	Command Input	Address Input	Data Input/Output	Description
Extended	DQ0	Multiple DQ*n* lines, depending on the command	Multiple DQ*n* lines, depending on the command	Device default protocol from the factory. Additional commands extend the standard SPI protocol and enable address or data transmission on multiple DQ*n* lines.
Dual	DQ[1:0]	DQ[1:0]	DQ[1:0]	**Volatile selectable:** When the enhanced volatile configuration register bit 6 is set to 0 and bit 7 is set to 1, the device enters the dual SPI protocol immediately after the WRITE ENHANCED VOLATILE CONFIGURATION REGISTER command. The device returns to the default protocol after the next power-on. In addition, the device can return to default protocol using the rescue sequence or through new WRITE ENHANCED VOLATILE CONFIGURATION REGISTER command, without power-off or power-on. **Nonvolatile selectable:** When nonvolatile configuration register bit 2 is set, the device enters the dual SPI protocol after the next power-on. Once this register bit is set, the device defaults to the dual SPI protocol after all subsequent power-on sequences until the nonvolatile configuration register bit is reset to 1.
Quad[1]	DQ[3:0]	DQ[3:0]	DQ[3:0]	**Volatile selectable:** When the enhanced volatile configuration register bit 7 is set to 0, the device enters the quad SPI protocol immediately after the WRITE ENHANCED VOLATILE CONFIGURATION REGISTER command. The device returns to the default protocol after the next power-on. In addition, the device can return to default protocol using the rescue sequence or through new WRITE ENHANCED VOLATILE CONFIGURATION REGISTER command, without power-off or power-on. **Nonvolatile selectable:** When nonvolatile configuration register bit 3 is set to 0, the device enters the quad SPI protocol after the next power-on. Once this register bit is set, the device defaults to the quad SPI protocol after all subsequent power-on sequences until the nonvolatile configuration register bit is reset to 1.

Note: 1. In quad SPI protocol, all command/address input and data I/O are transmitted on four lines except during a PROGRAM and ERASE cycle performed with V_{PP}. In this case, the device enters the extended SPI protocol to temporarily allow the application to perform a PROGRAM/ERASE SUSPEND operation or to check the write-in-progress bit in the status register or the program/erase controller bit in the flag status register. Then, when V_{PP} goes LOW, the device returns to the quad SPI protocol.

Nonvolatile and Volatile Registers

The device features the following volatile and nonvolatile registers that users can access to store device parameters and operating configurations:

- Status register
- Nonvolatile and volatile configuration registers
- Enhanced volatile configuration register
- Flag status register
- Lock register

Note: The lock register is defined in READ LOCK REGISTER Command.

In addition to these user-accessible registers, the working condition of memory is set by an internal configuration register that is not directly accessible to users. As shown below, parameters in the internal configuration register are loaded from the nonvolatile configuration register during each device boot phase or power-on reset. In this sense, then, the nonvolatile configuration register contains the default settings of memory.

Also, during the life of an application, each time a WRITE VOLATILE or ENHANCED VOLATILE CONFIGURATION REGISTER command executes to set configuration parameters in these respective registers, these new settings are copied to the internal configuration register. Therefore, memory settings can be changed in real time. However, at the next power-on reset, the memory boots according to the memory settings defined in the nonvolatile configuration register parameters.

Figure 8: Internal Configuration Register
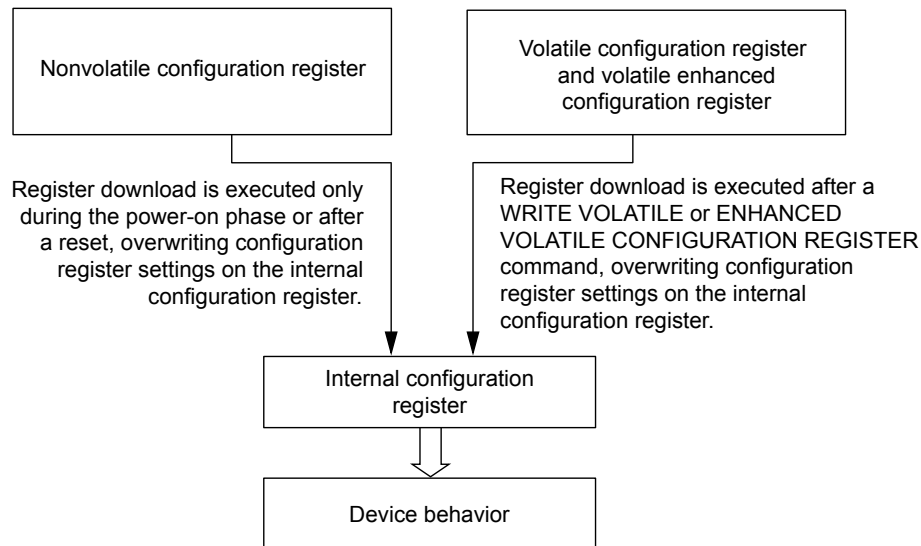
Status Register

Table 9: Status Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
7	Status register write enable/disable	0 = Enabled 1 = Disabled	**Nonvolatile bit:** Used with the W#/V_{PP} signal to enable or disable writing to the status register.	2
5	Top/bottom	0 = Top 1 = Bottom	**Nonvolatile bit:** Determines whether the protected memory area defined by the block protect bits starts from the top or bottom of the memory array.	3
6, 4:2	Block protect 3–0	See Protected Area Sizes – Upper Area and Lower Area tables in Device Protection	**Nonvolatile bit:** Defines memory to be software protected against PROGRAM or ERASE operations. When one or more block protect bits is set to 1, a designated memory area is protected from PROGRAM and ERASE operations.	3
1	Write enable latch	0 = Cleared (Default) 1 = Set	**Volatile bit:** The device always powers up with this bit cleared to prevent inadvertent WRITE STATUS REGISTER, PROGRAM, or ERASE operations. To enable these operations, the WRITE ENABLE operation must be executed first to set this bit.	4
0	Write in progress	0 = Ready 1 = Busy	**Volatile bit:** Indicates if one of the following command cycles is in progress: WRITE STATUS REGISTER WRITE NONVOLATILE CONFIGURATION REGISTER PROGRAM ERASE	4

Notes: 1. Bits can be read from or written to using READ STATUS REGISTER or WRITE STATUS REGISTER commands, respectively.
2. The status register write enable/disable bit, combined with the W#/V_{PP} signal as described in the Signal Descriptions, provides hardware data protection for the device as follows: When the enable/disable bit is set to 1, and the W#/V_{PP} signal is driven LOW, the status register nonvolatile bits become read-only and the WRITE STATUS REGISTER operation will not execute. The only way to exit this hardware-protected mode is to drive W#/V_{PP} HIGH.
3. See Protected Area Sizes tables in Device Protection. The BULK ERASE command is executed only if all bits are 0.
4. Volatile bits are cleared to 0 by a power cycle or reset.

Nonvolatile and Volatile Configuration Registers

Table 10: Nonvolatile Configuration Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
15:12	Number of dummy clock cycles	0000 (identical to 1111) 0001 0010 . . 1101 1110 1111	Sets the number of dummy clock cycles subsequent to all FAST READ commands. The default setting targets the maximum allowed frequency and guarantees backward compatibility.	2, 3
11:9	XIP mode at power-on reset	000 = XIP: Fast Read 001 = XIP: Dual Output Fast Read 010 = XIP: Dual I/O Fast Read 011 = XIP: Quad Output Fast Read 100 = XIP: Quad I/O Fast Read 101 = Reserved 110 = Reserved 111 = Disabled (Default)	Enables the device to operate in the selected XIP mode immediately after power-on reset.	
8:6	Output driver strength	000 = Reserved 001 = 90 Ohms 010 = 60 Ohms 011 = 45 Ohms 100 = Reserved 101 = 20 Ohms 110 = 15 Ohms 111 = 30 (Default)	Optimizes impedance at $V_{CC}/2$ output voltage.	
5	Reserved	X	"Don't Care."	
4	Reset/hold	0 = Disabled 1 = Enabled (Default)	Enables or disables hold or reset. (Available on dedicated part numbers.)	
3	Quad I/O protocol	0 = Enabled 1 = Disabled (Default, Extended SPI protcocol)	Enables or disables quad I/O protocol.	4
2	Dual I/O protocol	0 = Enabled 1 = Disabled (Default, Extended SPI protocol)	Enables or disables dual I/O protocol.	4
1:0	Reserved	X	"Don't Care."	
1:0	Reserved	X	"Don't Care."	
0	Lock nonvolatile configuration register	0 = Disabled 1 = Enabled (Default)	When this bit is set to 0, the nonvolatile configuration register becomes permanently write protected and any WRITE NONVOLATILE CONFIGURATION REGISTER command is ignored.	

Notes: 1. Settings determine device memory configuration after power-on. The device ships from the factory with all bits erased to 1 (FFFFh). The register is read from or written to by READ NONVOLATILE CONFIGURATION REGISTER or WRITE NONVOLATILE CONFIGURATION REGISTER commands, respectively.

2. The 0000 and 1111 settings are identical in that they both define the default state, which is the maximum frequency of ^fc = 108 MHz. This ensures backward compatibility.

3. If the number of dummy clock cycles is insufficient for the operating frequency, the memory reads wrong data. The number of cycles must be set according to and sufficient for the clock frequency, which varies by the type of FAST READ command, as shown in the Supported Clock Frequencies table.

4. If bits 2 and 3 are both set to 0, the device operates in quad I/O. When bits 2 or 3 are reset to 0, the device operates in dual I/O or quad I/O respectively, after the next power-on.

Table 11: Volatile Configuration Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
7:4	Number of dummy clock cycles	0000 (identical to 1111) 0001 0010 . . 1101 1110 1111	Sets the number of dummy clock cycles subsequent to all FAST READ commands. The default setting targets maximum allowed frequency and guarantees backward compatibility.	2, 3
3	XIP	0 1	Enables or disables XIP. For device part numbers with feature digit equal to 2 or 4, this bit is always "Don't Care," so the device operates in XIP mode without setting this bit.	
2	Reserved	X = Default	0b = Fixed value.	
1:0	Wrap	00 = 16-byte boundary aligned	16-byte wrap: Output data wraps within an aligned 16-byte boundary starting from the 3-byte address issued after the command code.	4
		01 = 32-byte boundary aligned	32-byte wrap: Output data wraps within an aligned 32-byte boundary starting from the 3-byte address issued after the command code.	
		10 = 64-byte boundary aligned	64-byte wrap: Output data wraps within an aligned 64-byte boundary starting from the 3-byte address issued after the command code.	
		11 = sequential (default)	Continuous reading (default): All bytes are read sequentially.	

Notes:
1. Settings determine the device memory configuration upon a change of those settings by the WRITE VOLATILE CONFIGURATION REGISTER command. The register is read from or written to by READ VOLATILE CONFIGURATION REGISTER or WRITE VOLATILE CONFIGURATION REGISTER commands respectively.

2. The 0000 and 1111 settings are identical in that they both define the default state, which is the maximum frequency of ^fc = 108 MHz. This ensures backward compatibility.

3. If the number of dummy clock cycles is insufficient for the operating frequency, the memory reads wrong data. The number of cycles must be set according to and be sufficient for the clock frequency, which varies by the type of FAST READ command, as shown in the Supported Clock Frequencies table.

4. See the Sequence of Bytes During Wrap table.

Table 12: Sequence of Bytes During Wrap

Starting Address	16-Byte Wrap	32-Byte Wrap	64-Byte Wrap
0	0-1-2- . . . -15-0-1- . .	0-1-2- . . . -31-0-1- . .	0-1-2- . . . -63-0-1- . .
1	1-2- . . . -15-0-1-2- . .	1-2- . . . -31-0-1-2- . .	1-2- . . . -63-0-1-2- . .
15	15-0-1-2-3- . . . -15-0-1- . .	15-16-17- . . . -31-0-1- . .	15-16-17- . . . -63-0-1- . .
31	31-16-17- . . . -31-16-17- . .	31-0-1-2-3- . . . -31-0-1- . .	31-32-33- . . . -63-0-1- . .
63	63-48-49- . . . -63-48-49- . .	63-32-33- . . . -63-32-33- . .	63-0-1- . . . -63-0-1- . .

Table 13: Supported Clock Frequencies

Note 1 applies to entire table

Number of Dummy Clock Cycles	FAST READ	DUAL OUTPUT FAST READ	DUAL I/O FAST READ	QUAD OUTPUT FAST READ	QUAD I/O FAST READ	Unit
1	90	80	50	43	30	
2	100	90	70	60	40	
3	108	100	80	75	50	
4	108	105	90	90	60	
5	108	108	100	100	70	MHz
6	108	108	105	105	80	
7	108	108	108	108	86	
8	108	108	108	108	95	
9	108	108	108	108	105	
10	108	108	108	108	108	

Note: 1. Values are guaranteed by characterization and not 100% tested in production.

Enhanced Volatile Configuration Register

Table 14: Enhanced Volatile Configuration Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
7	Quad I/O protocol	0 = Enabled 1 = Disabled (Default, extended SPI protocol)	Enables or disables quad I/O protocol.	2
6	Dual I/O protocol	0 = Enabled 1 = Disabled (Default, extended SPI protocol)	Enables or disables dual I/O protocol.	2
5	Reserved	X = Default	0b = Fixed value.	
4	Reset/hold	0 = Disabled 1 = Enabled (Default)	Enables or disables hold or reset. (Available on dedicated part numbers.)	

Table 14: Enhanced Volatile Configuration Register Bit Definitions (Continued)

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
3	V$_{PP}$ accelerator	0 = Enabled 1 = Disabled (Default)	Enables or disables V$_{PP}$ acceleration for QUAD INPUT FAST PROGRAM and QUAD INPUT EXTENDED FAST PROGRAM OPERATIONS.	
2:0	Output driver strength	000 = Reserved 001 = 90 Ohms 010 = 60 Ohms 011 = 45 Ohms 100 = Reserved 101 = 20 Ohms 110 = 15 Ohms 111 = 30 (Default)	Optimizes impedance at V$_{CC}$/2 output voltage.	

Notes: 1. Settings determine the device memory configuration upon a change of those settings by the WRITE ENHANCED VOLATILE CONFIGURATION REGISTER command. The register is read from or written to in all protocols by READ ENHANCED VOLATILE CONFIGURATION REGISTER or WRITE ENHANCED VOLATILE CONFIGURATION REGISTER commands, respectively.

2. If bits 6 and 7 are both set to 0, the device operates in quad I/O. When either bit 6 or 7 is reset to 0, the device operates in dual I/O or quad I/O, respectively, following the next WRITE ENHANCED VOLATILE CONFIGURATION command.

Flag Status Register

Table 15: Flag Status Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
7	Program or erase controller	0 = Busy 1 = Ready	**Status bit:** Indicates whether a PROGRAM, ERASE, WRITE STATUS REGISTER, or WRITE NONVOLATILE CONFIGURATION command cycle is in progress.	2, 3
6	Erase suspend	0 = Not in effect 1 = In effect	**Status bit:** Indicates whether an ERASE operation has been or is going to be suspended.	3
5	Erase	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether an ERASE operation has succeeded or failed.	4, 5
4	Program	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether a PROGRAM operation has succeeded or failed. Also indicates an attempt to program a 0 to a 1 when V$_{PP}$ = V$_{PPH}$ and the data pattern is a multiple of 64 bits.	4, 5
3	V$_{PP}$	0 = Enabled 1 = Disabled (Default)	**Error bit:** Indicates an invalid voltage on V$_{PP}$ during a PROGRAM or ERASE operation.	4, 5
2	Program suspend	0 = Not in effect 1 = In effect	**Status bit:** Indicates whether a PROGRAM operation has been or is going to be suspended.	3

Table 15: Flag Status Register Bit Definitions (Continued)

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
1	Protection	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether an ERASE or a PROGRAM operation has attempted to modify the protected array sector, or whether a PROGRAM operation has attempted to access the locked OTP space.	4, 5
0	Reserved	Reserved	Reserved	

Notes: 1. Register bits are read by READ FLAG STATUS REGISTER command. All bits are volatile.
2. These program/erase controller settings apply only to PROGRAM or ERASE command cycles in progress, or to the specific WRITE command cycles in progress as shown here.
3. Status bits are reset automatically.
4. Error bits must be reset by CLEAR FLAG STATUS REGISTER command.
5. Typical errors include operation failures and protection errors caused by issuing a command before the error bit has been reset to 0.