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numonyx

N25Q128

128-Mbit 3 V, multiple I/O, 4-Kbyte subsector erase on boot sectors, XiP enabled, serial flash memory with 108 MHz SPI bus interface

Features

- SPI-compatible serial bus interface
- 108 MHz (maximum) clock frequency
- 2.7 V to 3.6 V single supply voltage
- Supports legacy SPI protocol and new Quad I/O or Dual I/O SPI protocol
- Quad/Dual I/O instructions resulting in an equivalent clock frequency up to 432 MHz:
- XIP mode for all three protocols
  - Configurable via volatile or non-volatile registers: enables XiP mode directly after power on
- Program/Erase suspend instructions
- Continuous read (entire memory) via single instruction:
  - Fast Read
  - Quad or Dual Output Fast Read
  - Quad or Dual I/O Fast Read
- Flexible to fit application:
  - Configurable number of dummy cycles
  - Output buffer configurable
  - Fast POR instruction: decrease power-on time
  - Reset function (upon customer request)
- 64-byte user-lockable, one-time programmable (OTP) area
- Erase capability
  - Subsector (4-Kbyte) granularity in the 8 boot sectors (bottom or top parts)
  - Sector (64-Kbyte) granularity
- Write protections
  - Software write protection applicable to every 64-Kbyte sector (volatile lock bit)
  - Hardware write protection: protected area size defined by non-volatile bits (BP0, BP1, BP2, BP3 and TB bit)
  - Additional smart protections available upon customer request
- Electronic signature
  - JEDEC standard two-byte signature (BA18h)
  - Additional 2 Extended Device ID (EDID) bytes to identify device factory options
  - Unique ID code (UID) with 14 bytes read-only, available upon customer request
- More than 100,000 program/erase cycles per sector
- More than 20 years data retention
- Packages (all packages RoHS compliant)
  - F8 = VDFPN8 8 x 6 mm (MLP8)
  - 12 = TBGA24 6 x 8 mm
  - F6 = VDFPN8 6 x 5 mm (MLP)
  - SF = SO16 (300 mils body width)
  - SE = SO8W (SO8 208 mils body width)

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1 Description

The N25Q128 is a 128 Mbit (16Mb x 8) serial Flash memory, with advanced write protection mechanisms. It is accessed by a high speed SPI-compatible bus and features the possibility to work in XIP (“eXecution in Place”) mode.

The N25Q128 supports innovative, high-performance quad/dual I/O instructions, these new instructions allow to double or quadruple the transfer bandwidth for read and program operations.

Furthermore the memory can be operated with 3 different protocols:

- Standard SPI (Extended SPI protocol)
- Dual I/O SPI
- Quad I/O SPI

The Standard SPI protocol is enriched by the new quad and dual instructions (Extended SPI protocol). For Dual I/O SPI (DIO-SPI) all the instructions codes, the addresses and the data are always transmitted across two data lines. For Quad I/O SPI (QIO-SPI) the instructions codes, the addresses and the data are always transmitted across four data lines thus enabling a tremendous improvement in both random access time and data throughput.

The memory can work in “XIP mode”, that means the device only requires the addresses and not the instructions to output the data. This mode dramatically reduces random access time thus enabling many applications requiring fast code execution without shadowing the memory content on a RAM.

The XIP mode can be used with QIO-SPI, DIO-SPI, or Extended SPI protocol, and can be entered and exited using different dedicated instructions to allow maximum flexibility: for applications required to enter in XIP mode right after power up of the device, this can be set as default mode by using dedicated Non Volatile Register (NVR) bits.

It is also possible to reduce the power on sequence time with the Fast POR (Power on Reset) feature, enabling a reduction of the latency time before the first read instruction can be performed. Another feature is the ability to pause and resume program and erase cycles by using dedicated Program/Erase Suspend and Resume instructions.

The N25Q128 memory offers the following additional Features to be configured by using the Non Volatile Configuration Register (NVCR) for default /Non-Volatile settings or by using the Volatile and Volatile Enhanced Configuration Registers for Volatile settings:

- the number of dummy cycles for fast read instructions (single, dual and, quad I/O) according to the operating frequency
- the output buffer impedance
- the type of SPI protocol (extended SPI, DIO-SPI or QIO-SPI)
- the required XIP mode
- Fast or standard POR sequence
- the Hold (Reset) functionality enabling/disabling

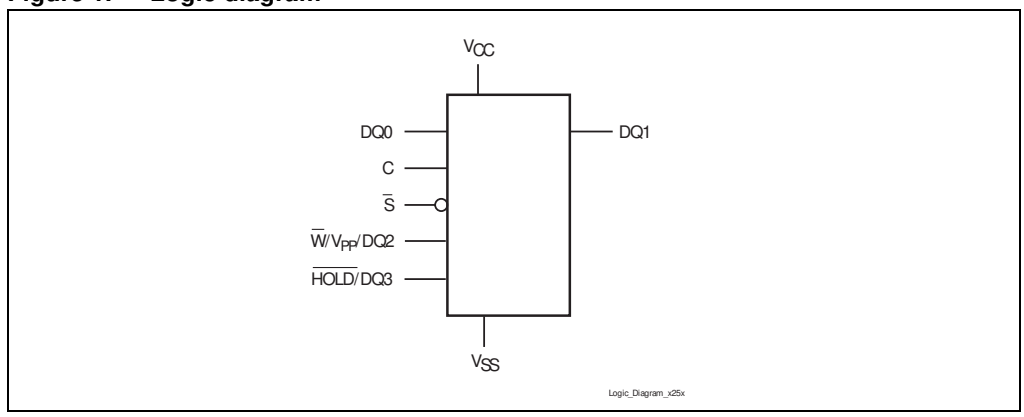
The memory is organized as 248 (64-Kbyte) main sectors, in products with Bottom or Top architecture there are 8 64-Kbyte boot sectors, and each boot sector is further divided into 16 4-Kbyte subsectors (128 subsectors in total). The boot sectors can be erased a 4-Kbyte subsector at a time or as a 64-Kbyte sector at a time. The entire memory can be also erased at a time or by sector.

The memory can be write protected by software using a mix of volatile and non-volatile protection features, depending on the application needs. The protection granularity is of 64-Kbyte (sector granularity) for volatile protections.

The N25Q128 has 64 one-time-programmable bytes (OTP bytes) that can be read and programmed using two dedicated instructions, Read OTP (ROTP) and Program OTP (POTP), respectively. These 64 bytes can be permanently locked by a particular Program OTP (POTP) sequence. Once they have been locked, they become read-only and this state cannot be reversed.

Many different N25Q128 configurations are available, please refer to the ordering scheme page for the possibilities. Additional features are available as security options (The Security features are described in a dedicated Application Note). Please contact your nearest Numonyx Sales office for more information.

Figure 1. Logic diagram



Note: Reset functionality is available in devices with a dedicated part number. See Section 16: Ordering information.

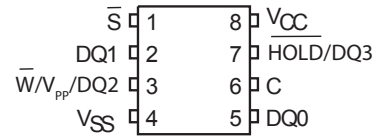
Table 1. Signal names

Signal	Description	I/O
C	Serial Clock	Input
DQ0	Serial Data input	I/O(1)
DQ1	Serial Data output	I/O(2)
S	Chip Select	Input
W/VPP/DQ2	Write Protect/Enhanced Program supply voltage/additional data I/O	I/O(3)
HOLD/DQ3(4)	Hold (Reset function available upon customer request)/additional data I/O	I/O(3)
V_{CC}	Supply voltage	–
V_{SS}	Ground	–

1. Provides dual and quad I/O for Extended SPI protocol instructions, dual I/O for Dual I/O SPI protocol instructions, and quad I/O for Quad I/O SPI protocol instructions.
2. Provides dual and quad instruction input for Extended SPI protocol, dual instruction input for Dual I/O SPI protocol, and quad instruction input for Quad I/O SPI protocol.
3. Provides quad I/O for Extended SPI protocol instructions, and quad I/O for Quad I/O SPI protocol instructions.
4. Reset functionality available with a dedicated part number. See *Section 16: Ordering information*.

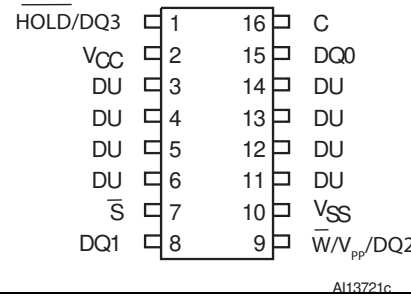
Note: There is an exposed central pad on the underside of the VDFPN8 package. This is pulled, internally, to VSS, and must not be connected to any other voltage or signal line on the PCB.

Figure 2. VDFPN8 connections



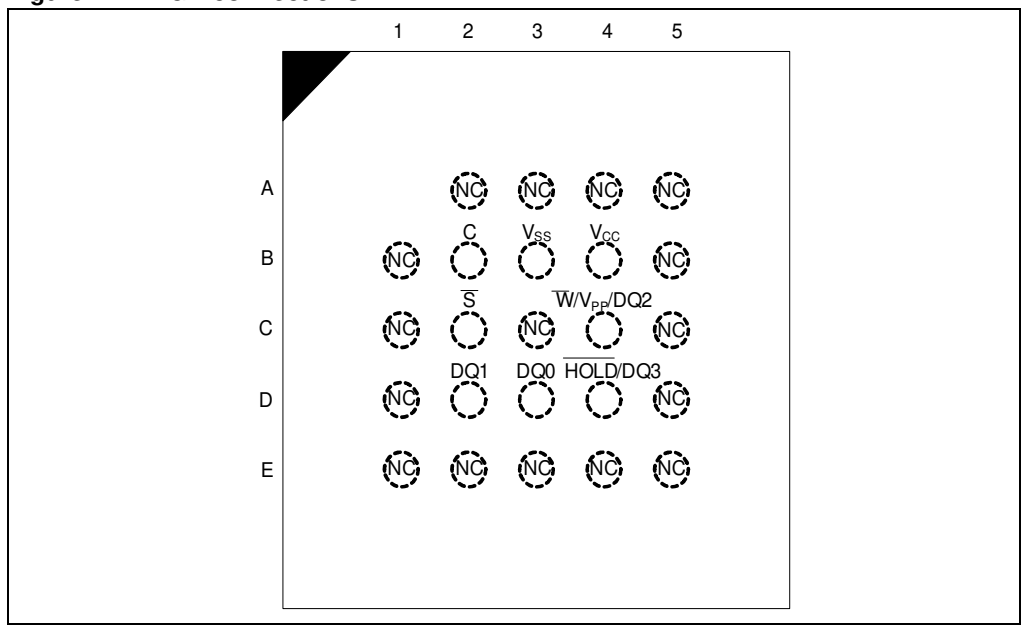
1. Reset functionality available in devices with a dedicated part number. See *Section 16: Ordering information*.

Figure 3. SO16 connections



1. DU = don't use.
2. See *Package mechanical* section for package dimensions, and how to identify pin-1.
3. Reset functionality available in devices with a dedicated part number. See *Section 16: Ordering information*.

Figure 4. BGA connections



1. NC = No Connect.
2. See *Figure 112.: TBGA - 6 x 8 mm, 24-ball, mechanical package outline*.

2 Signal descriptions

2.1 Serial data output (DQ1)

This output signal is used to transfer data serially out of the device. Data are shifted out on the falling edge of Serial Clock (C). When used as an Input, It is latched on the rising edge of the Serial Clock (C).

In the Extended SPI protocol, during the Quad and Dual Input Fast Program (QIFP, DIFP) instructions and during the Quad and Dual Input Extended Fast Program (QIEFP, DIEFP) instructions, pin DQ1 is used also as an input.

In the Dual I/O SPI protocol (DIO-SPI) the DQ1 pin always acts as an input/output.

In the Quad I/O SPI protocol (QIO-SPI) the DQ1 pin always acts as an input/output, with the exception of the Program or Erase cycle performed with the Enhanced Program Supply Voltage (VPP). In this case the device temporarily goes in Extended SPI protocol. The protocol then becomes QIO-SPI as soon as the VPP pin voltage goes low.

2.2 Serial data input (DQ0)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C). Data are shifted out on the falling edge of the Serial Clock (C).

In the Extended SPI protocol, during the Quad and Dual Output Fast Read (QOFR, DOFR) and the Quad and Dual Input/Output Fast Read (QIOFR, DIOFR) instructions, pin DQ0 is also used as an input/output.

In the DIO-SPI protocol the DQ0 pin always acts as an input/output.

In the QIO-SPI protocol, the DQ0 pin always acts as an input/output, with the exception of the Program or Erase cycle performed with the VPP. In this case the device temporarily goes in Extended SPI protocol. Then, the protocol returns to QIO-SPI as soon as the VPP pin voltage goes low.

2.3 Serial Clock (C)

This input signal provides the timing for the serial interface. Instructions, addresses, or data present at serial data input (DQ0) are latched on the rising edge of Serial Clock (C). Data are shifted out on the falling edge of the Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is high, the device is deselected and serial data output (DQ1) is at high impedance. Unless an internal program, erase or write status register cycle is in progress, the device will be in the standby power mode (this is not the deep power-down mode). Driving Chip Select ($\overline{S}$) low enables the device, placing it in the active power mode.

After power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Hold ($\overline{\text{HOLD}}$) or Reset ($\overline{\text{Reset}}$)

The Hold ($\overline{\text{HOLD}}$) signal is used to pause any serial communications with the device without deselecting the device.

Reset functionality is present instead of Hold in devices with a dedicated part number. See *Section 16: Ordering information*.

During Hold condition, the Serial Data output (DQ1) is in high impedance, and Serial Data input (DQ0) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{\text{S}}$) driven Low.

For devices featuring Reset instead of Hold functionality, the Reset ($\overline{\text{Reset}}$) input provides a hardware reset for the memory.

When Reset ($\overline{\text{Reset}}$) is driven High, the memory is in the normal operating mode. When Reset ($\overline{\text{Reset}}$) is driven Low, the memory will enter the Reset mode. In this mode, the output is high impedance.

Driving Reset ($\overline{\text{Reset}}$) Low while an internal operation is in progress will affect this operation (write, program or erase cycle) and data may be lost.

In the Extended SPI protocol, during the QOFR, QIOFR, QIFP and the Quad Extended Fast Program (QIEFP) instructions, the Hold ($\overline{\text{Reset}}$) / DQ3 is used as an input/output (DQ3 functionality).

In QIO-SPI, the $\overline{\text{Hold}}$ ($\overline{\text{Reset}}$) / DQ3 pin acts as an I/O (DQ3 functionality), and the $\overline{\text{HOLD}}$ ($\overline{\text{Reset}}$) functionality disabled when the device is selected. When the device is deselected ($\overline{\text{S}}$ signal is high), in parts with Reset functionality, it is possible to reset the device unless this functionality is not disabled by mean of dedicated registers bits.

The HOLD (Reset) functionality can be disabled using bit 3 of the NVCR or bit 4 of the VECR.

2.6 Write protect/enhanced program supply voltage ($\overline{W}$/VPP), DQ2

$\overline{W}$/VPP/DQ2 can be used as:

- A protection control input.
- A power supply pin.
- I/O in Extended SPI protocol quad instructions and in QIO-SPI protocol instructions.

When the device is operated in Extended SPI protocol with single or dual instructions, the two functions $\overline{W}$ or VPP are selected by the voltage range applied to the pin. If the $\overline{W}$/VPP input is kept in a low voltage range (0 V to VCC) the pin is seen as a control input. This input signal is used to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in the BP[0:3] bits of the Status Register. (See *Table 2.: Status register format*).

If VPP is in the range of VPPH, it acts as an additional power supply during the Program or Erase cycles (See *Table 28.: Operating conditions*). In this case VPP must be stable until the Program or Erase algorithm is completed.

During the Extended SPI protocol, the QOFR and QIOFR instructions, and the QIO-SPI protocol instructions, the pin $\overline{W}$/VPP/DQ2 is used as an input/output (DQ2 functionality).

Using the Extended SPI protocol the QIFP, QIEFP and the QIO-SPI Program/Erase instructions, it is still possible to use the VPP additional power supply to speed up internal operations. However, to enable this possibility it is necessary to set bit 3 of the Volatile Enhanced Configuration Register to 0.

In this case the $\overline{W}$/VPP/DQ2 pin is used as an I/O pin until the end of the instruction sequence. After the last input data is shifted in, the application should apply VPP voltage to $\overline{W}$/VPP/DQ2 within 200 ms to speed up the internal operations. If the VPP voltage is not applied within 200 ms the Program/Erase operations start with standard speed.

The default value of the VECR bit 3 is 1, and the VPP functionality for Quad I/O modify instruction is disabled.

2.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

2.8 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

3 SPI Modes

These devices can be driven by a micro controller with its SPI peripheral running in either of the two following modes:

CPOL=0, CPHA=0

CPOL=1, CPHA=1

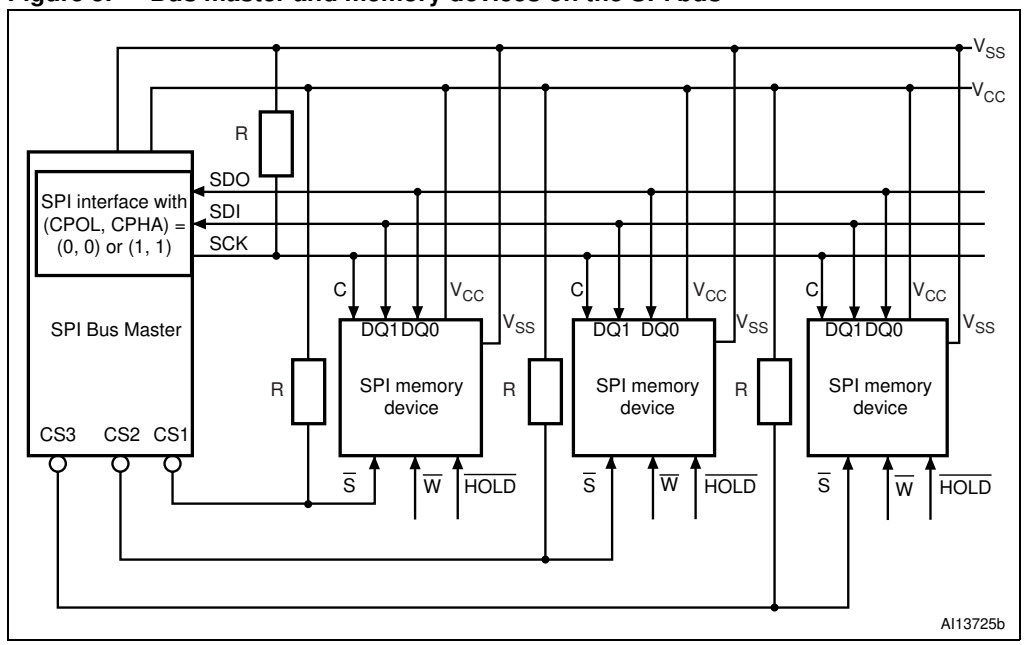
For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 5*, is the clock polarity when the bus master is in standby mode and not transferring data:

C remains at 0 for (CPOL=0, CPHA=0)

C remains at 1 for (CPOL=1, CPHA=1)

Figure 5. Bus master and memory devices on the SPI bus

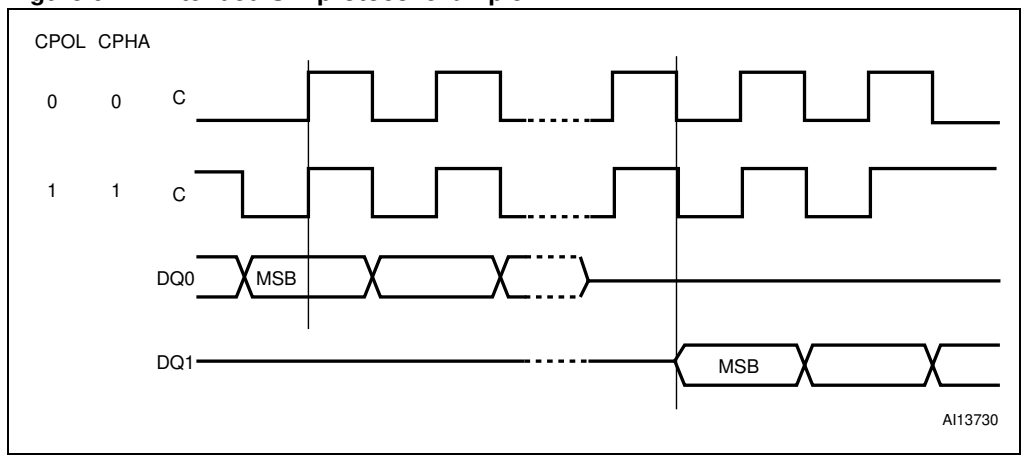


Shown here is an example of three devices working in Extended SPI protocol for simplicity connected to an MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the serial data output (DQ1) line at a time; the other devices are high impedance. Resistors R ensures that the N25Q128 is not selected if the bus master leaves the $\overline{S}$ line in the high impedance state. As the bus master may enter a state where all inputs/outputs are in high impedance at the same time (for example, when the bus master is reset), the clock line (C) must be connected to an external pull-down resistor so that, when all inputs/outputs become high impedance, the $\overline{S}$ line is pulled High while the C line is pulled Low. This ensures that $\overline{S}$ and C do not become High at the same time, and so that the t_{SHCH} requirement is met. The typical value of R is 100 kΩ, assuming that the time constant $R*C_p$

(C_p = parasitic capacitance of the bus line) is shorter than the time during which the bus master leaves the SPI bus in high impedance.

Example: C_p = 50 pF, that is $R*C_p$ = 5 µs <=> the application must ensure that the bus master never leaves the SPI bus in the high impedance state for a time period shorter than 5 µs. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, High or Low as appropriate.

Figure 6. Extended SPI protocol example



4 SPI Protocols

The N25Q128 memory can work with 3 different Serial protocols:

- Extended SPI protocol.
- Dual I/O SPI (DIO-SPI) protocol.
- Quad I/O SPI (QIO-SPI) protocol.

It is possible to choose among the three protocols by means of user volatile or non-volatile configuration bits.It's not possible to mix Extended SPI, DIO-SPI, and QIO-SPI protocols. The device can operate in XIP mode in all 3 protocols.

4.1 Extended SPI protocol

This is an extension of the standard (legacy) SPI protocol. Instructions are transmitted on a single data line (DQ0), while addresses and data are transmitted by one, two or four data lines (DQ0, DQ1, W/VPP(DQ2) and HOLD / (DQ3) according to the instruction.

When used in the Extended SPI protocol, these devices can be driven by a micro controller in either of the two following modes:

- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

Please refer to the SPI modes for a detailed description of these two modes

4.2 Dual I/O SPI (DIO-SPI) protocol

Dual I/O SPI (DIO-SPI) protocol: instructions, addresses and I/O data are always transmitted on two data lines (DQ0 and DQ1).

Also when in DIO-SPI mode, the device can be driven by a micro controller in either of the two following modes:

- CPOL= 0, CPHA= 0
- CPOL= 1, CPHA= 1

Please refer to the SPI modes for a detailed description of these two modes.

Note: *Extended SPI protocol Dual I/O instructions allow only address and data to be transmitted over two data lines. However,* DIO-SPI *allows instructions, addresses, and data to be transmitted on two data lines.*

This mode can be set using two ways

- **Volatile:** by setting bit 6 of the VECR to 0. The device enters DIO-SPI protocol immediately after the Write Enhanced Volatile Configuration Register sequence completes. The device returns to the default working mode (defined by NVCR) on power on.
- **Default/ Non-Volatile:** This is default mode on power-up. By setting bit 2 of the NVCR to 0. The device enters DIO-SPI protocol on the subsequent power-on. After all subsequent power-on sequences, the device still starts in DIO-SPI protocol unless bit 2 of NVCR is set to 1 (default value, corresponding to Extended SPI protocol) or bit 3 of NVCR is set to 0 (corresponding to QIO-SPI protocol).

4.3 Quad SPI (QIO-SPI) protocol

Quad SPI (QIO-SPI) protocol: instructions, addresses, and I/O data are always transmitted on four data lines DQ0, DQ1, W/VPP(DQ2), and HOLD / (DQ3).

The exception is the Program/Erase cycle performed with the VPP, in which case the device temporarily goes to Extended SPI protocol. Going temporarily into Extended SPI protocol allows the application either to:

- check the polling bits: WIP bit in the Status Register or Program/Erase Controller bit in the Flag Status Register
- perform Program/Erase suspend functions.

Note: As soon as the VPP pin voltage goes low, the protocol returns to the QIO-SPI protocol.

In QIO-SPI protocol the W and HOLD/ (RESET) functionality is disabled when the device is selected (S signal low).

When used in the QIO-SPI mode, these devices can be driven by a micro controller in either of the two following modes:

- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

Please refer to the SPI modes for a detailed description of the 2 modes.

Note: In the Extended SPI protocol only Address and data are allowed to be transmitted on 4 data lines, However in QIO-SPI protocol, the address, data and instructions are transmitted across 4 data lines.

This working mode is set in either bit 7 of the Volatile Enhanced Configuration Register (VECR) or in bit 3 of the Non Volatile Configuration Register (NVCR).

This mode can be set using two ways

- **Volatile:** by setting bit 7 of the VECR to 0, the device enters QIO-SPI protocol immediately after the Write Enhanced Volatile Configuration Register sequence completes. The device returns to the default working protocol (defined by the NVCR) on the next power on.
- **Default/ Non- Volatile:** This is default protocol on power up. By setting bit 3 of the NVCR to 0, the device enters QIO-SPI protocol on the subsequent power-on. After all subsequent power-on sequences, the device still starts in QIO-SPI protocol unless bit 3 of the NVCR is set to 1 (default value, corresponding to Extended SPI mode).

5 Operating features

5.1 Extended SPI Protocol Operating features

5.1.1 Read Operations

To read the memory content in Extended SPI protocol different instructions are available: READ, Fast Read, Dual Output Fast Read, Dual Input Output Fast Read, Quad Output Fast Read and Quad Input Output Fast read, allowing the application to choose an instruction to send addresses and receive data by one, two or four data lines.

Note: In the Extended SPI protocol the instruction code is always sent on one data line (DQ0): to use two or four data lines the user must use either the DIO-SPI or the QIO-SPI protocol respectively.

For fast read instructions the number of dummy clock cycles is configurable by using VCR bits [7:4] or NVCR bits [15:12].

After a successful reading instruction a reduced tSHSL equal to 20 ns is allowed to further improve random access time (in all the other cases tSHSL should be at least 50 ns). See *Table 32.: AC Characteristics*.

5.1.2 Page programming

To program one data byte, two instructions are required: write enable (WREN), which is one byte, and a page program (PP) sequence, which consists of four bytes plus data. This is followed by the internal program cycle (of duration t_{PP}).

To spread this overhead, the page program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from ‘1’ to ‘0’), provided that they lie in consecutive addresses on the same page of memory.

For optimized timings, it is recommended to use the page program (PP) instruction to program all consecutive targeted bytes in a single sequence versus using several page program (PP) sequences with each containing only a few bytes (see *Section 5.2.3: Page programming* and *Table 32: AC Characteristics*).

5.1.3 Dual input fast program

The dual input fast program (DIFP) instruction makes it possible to program up to 256 bytes using two input pins at the same time (by changing bits from ‘1’ to ‘0’).

For optimized timings, it is recommended to use the DIFP instruction to program all consecutive targeted bytes in a single sequence rather using several DIFP sequences each containing only a few bytes (see *Section 9.1.12: Dual Input Fast Program (DIFP)*).

5.1.4 Dual Input Extended Fast Program

The Dual Input Extended Fast Program (DIEFP) instruction is an enhanced version of the Dual Input Fast Program instruction, allowing to transmit address across two data lines.

For optimized timings, it is recommended to use the DIEFP instruction to program all consecutive targeted bytes in a single sequence rather than using several DIEFP sequences, each containing only a few bytes.

5.1.5 Quad Input Fast Program

The Quad Input Fast Program (QIFP) instruction makes it possible to program up to 256 bytes using 4 input pins at the same time (by changing bits from 1 to 0).

For optimized timings, it is recommended to use the QIFP instruction to program all consecutive targeted bytes in a single sequence rather than using several QIFP sequences each containing only a few bytes.

5.1.6 Quad Input Extended Fast Program

The Quad Input Extended Fast Program (QIEFP) instruction is an enhanced version of the Quad Input Fast Program instruction, allowing parallel input on the 4 input pins, including the address being sent to the device.

For optimized timings, it is recommended to use the QIEFP instruction to program all consecutive targeted bytes in a single sequence rather than using several QIEFP sequences each containing only a few bytes.

5.1.7 Subsector erase, sector erase and bulk erase

The page program (PP) instruction allows bits to be reset from ‘1’ to’0’. In order to do this the bytes of memory need to be erased to all 1s (FFh).

This can be achieved as follows:

- a subsector at a time, using the subsector erase (SSE) instruction (only available on the 8 boot sectors at the bottom or top addressable area of a device with a dedicated part number); See *Section 16: Ordering information*;
- a sector at a time, using the sector erase (SE) instruction;
- throughout the entire memory, using the bulk erase (BE) instruction.

This starts an internal erase cycle (of duration t_{SSE}, t_{SE} or t_{BE}). The erase instruction must be preceded by a write enable (WREN) instruction.

5.1.8 Polling during a write, program or erase cycle

A further improvement in the time to Write Status Register (WRSR), POTP, PP, DIFP,DIEFP,QIFP, QIEFP or Erase (SSE, SE or BE) can be achieved by not waiting for the worst case delay (tW, tPP, tSSE, tSE, or tBE). The application program can monitor if the required internal operation is completed, by polling the dedicated register bits to establish when the previous Write, Program or Erase cycle is complete.

The information on the memory being in progress for a Program, Erase, or Write instruction can be checked either on the Write In Progress (WIP) bit of the Status Register or in the Program/Erase Controller bit of the Flag Status Register.

Note: The Program/Erase Controller bit is the opposite state of the WIP bit in the Status Register.

In the Flag Status Register additional information can be checked, as eventual Program/Erase failures by mean of the Program or erase Error bits.

5.1.9 Active power and standby power modes

When Chip Select ($\overline{S}$) is Low, the device is selected, and in the active power mode.

When Chip Select ($\overline{S}$) is High, the device is deselected, but could remain in the active power mode until all internal cycles have completed (program, erase, write status register). The device then goes in to the standby power mode. The device consumption drops to I_{CC1}.

5.1.10 Hold (or Reset) condition

The Hold ($\overline{HOLD}$) signal is used to pause serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any write status register, program or erase cycle that is currently in progress.

To enter the hold condition, the device must be selected, with Chip Select ($\overline{S}$) Low.

The hold condition starts on the falling edge of the Hold ($\overline{HOLD}$) signal, provided that the Serial Clock (C) is Low (as shown in *Figure 7*).

The hold condition ends on the rising edge of the Hold ($\overline{HOLD}$) signal, provided that the Serial Clock (C) is Low.

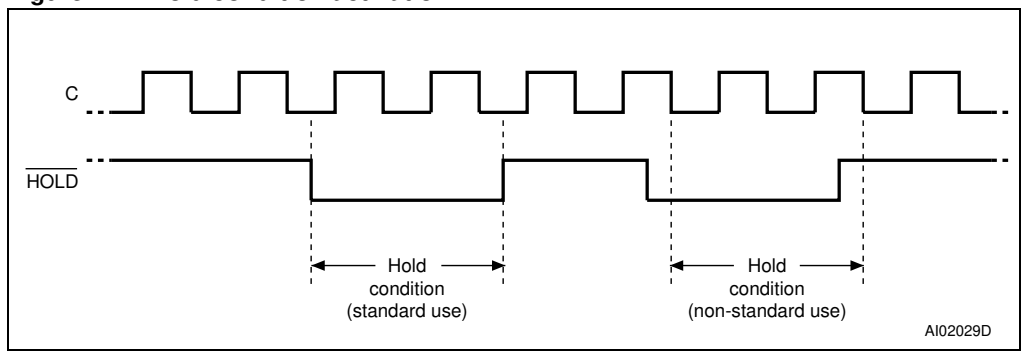
If the falling edge does not coincide with Serial Clock (C) being Low, the hold condition starts after Serial Clock (C) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (C) being Low, the hold condition ends after Serial Clock (C) next goes Low (this is shown in *Figure 7*).

During the hold condition, the serial data output (DQ1) is high impedance, and serial data input (DQ0) and Serial Clock (C) are don't care.

Normally, the device is kept selected, with Chip Select ($\overline{S}$) driven Low for the whole duration of the hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the hold condition.

If Chip Select ($\overline{S}$) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold ($\overline{HOLD}$) High, and then to drive Chip Select ($\overline{S}$) Low. This prevents the device from going back to the hold condition.

Figure 7. Hold condition activation



Reset functionality is available instead of Hold in parts with a dedicated part number. See *Section 16: Ordering information*.

Driving Reset ($\overline{Reset}$) Low while an internal operation is in progress will affect this operation (write, program or erase cycle) and data may be lost. On Reset going Low, the device enters