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1. DESCRIPTION

The N681386/87, implements a single channel FXS telephone line interface optimized for short loop applications. It integrates SLCC (Subscriber Line Control Circuit) functionality with a programmable CODEC and a DC/DC controller. The SLCC supports internal ringing up to 90 V_{PK} (5 REN at 4k ft) ideal for Customer Premise Equipment (CPE). The CODEC can be configured for μ-law, A-law or 16-bit linear PCM encoding. It also supports a comprehensive set of signaling capabilities required to supervise and control the telephone lines. These include tone generation, ring tones, DTMF detection/ generation as well as FSK generation. An on-chip Pulse Width Modulation (PWM) driver allows control of an inductor based DC/DC converter. Programmable impedance and trans-hybrid balancing allow for worldwide deployment.

2. FEATURES

- Complete BORSCHT functions
- Internal balanced and unbalanced ringing up to 90 V_{PK} (5 REN up to 4k ft)
- Integrated Power Management Options
  - Integrated DC/DC controller regulates battery voltage to minimize power dissipation in all operating modes
  - Programmable external battery switching
- Programmable linefeed characteristics
  - Ringing Frequency, Amplitude, and Cadence
  - Trapezoidal and Sinusoidal waveforms
  - Two wire AC impedance, and trans-hybrid balance
  - Constant Current feed (20 to 41) mA
  - Ring Trip and Loop Closure Thresholds
  - Ground Key Detection
- Programmable signal generation and detection
  - DTMF generation/ detection and Tone generation
  - Frequency Shift Keying (FSK) Enhanced Caller ID generation (Type I and Type II)
- Loop test and diagnostics support
  - Integrated loopback modes
  - Real-time linefeed monitoring
  - On-chip temperature sensor
  - Line Card Diagnostics Support
- Digital interfaces
  - PCM: G.711 μ-Law, A-Law and 16-bit linear
  - GCI and SPI bus
  - Programmable audio path gains
- Both PCM Master and Slave modes supported
- On-chip PLL for flexible clocking options including 1.0 MHz and 2.0 MHz BCLK operation
- Operating voltage: 3.3V
- Narrowband Codec (N681386)
- Wideband and Narrowband codec (N681387)
- Optional integrated (N681622) or discrete Subscriber Line Feed Circuit

APPLICATIONS

- Residential VoIP Gateways / Routers/ IP-PBX
- Fiber to the Premise/Home (FTTP/H)
- Wireless Local Loop
- Optical Network Terminals (ONT)
- Analog Telephone Adapter (ATA)
- Voice enabled DSL/Cable Modems
- Integrated Access Devices
- Set Top Boxes

Ordering Information

Part Number	Temp Range (°C)	Package	Package Material
N681386DG N681387DG	-40 to 85	48-LQFP	Pb-Free
N681386YG N681387YG	-40 to 85	48-QFN	Pb-Free
N681622YG	-40 to 85	20-QFN	Pb-Free

! WARNING !

HIGH VOLTAGE WARNING
USE EXTREME CAUTION

High voltage sources could cause serious injury or death if not used in accordance with design and/or user specifications, if they are used by untrained or unqualified personnel. Before testing Nuvoton's products read and understand all instructions, and safety procedures as in industry standard safe practices.

3. PIN CONFIGURATION

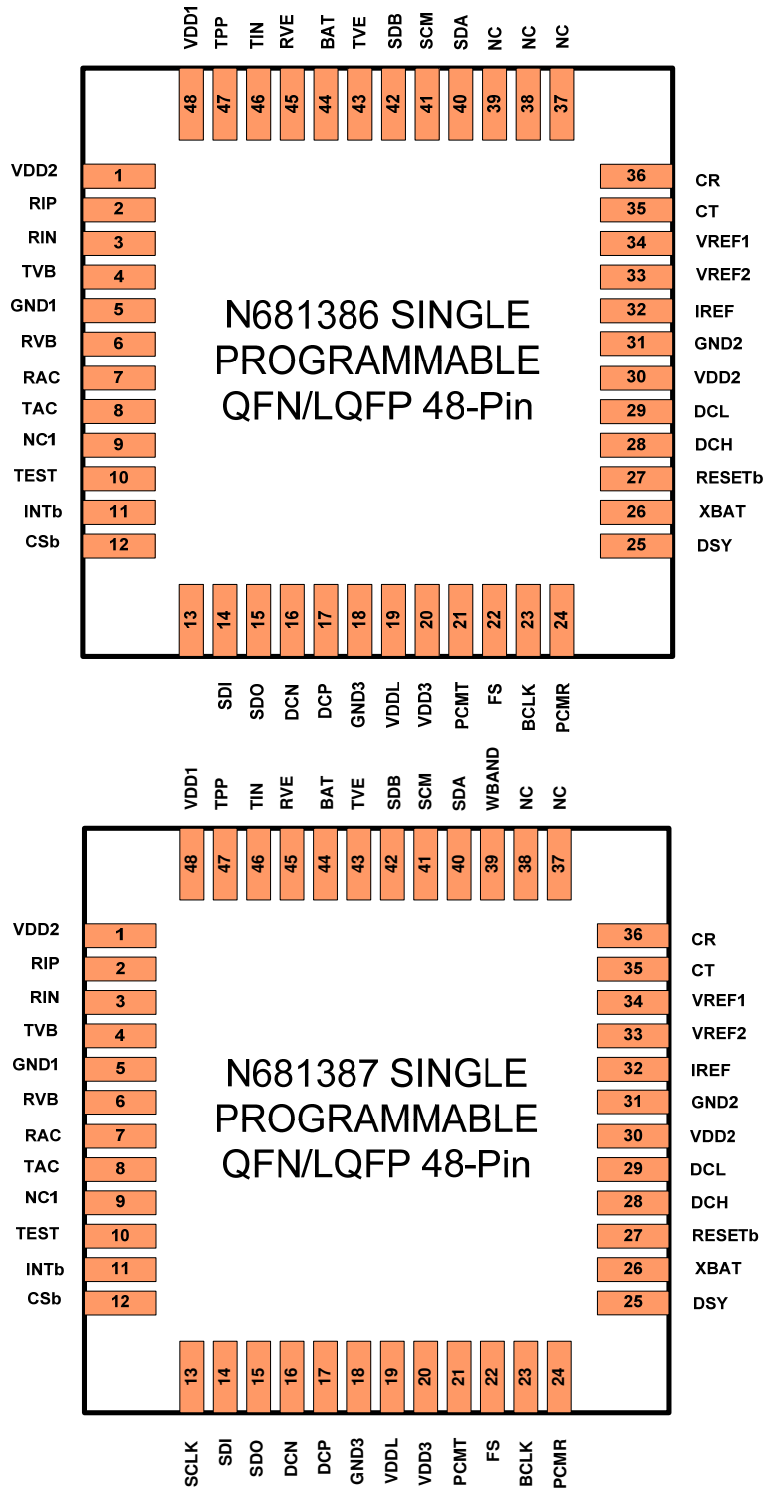

Figure 1: N681386/87 Pin Configuration

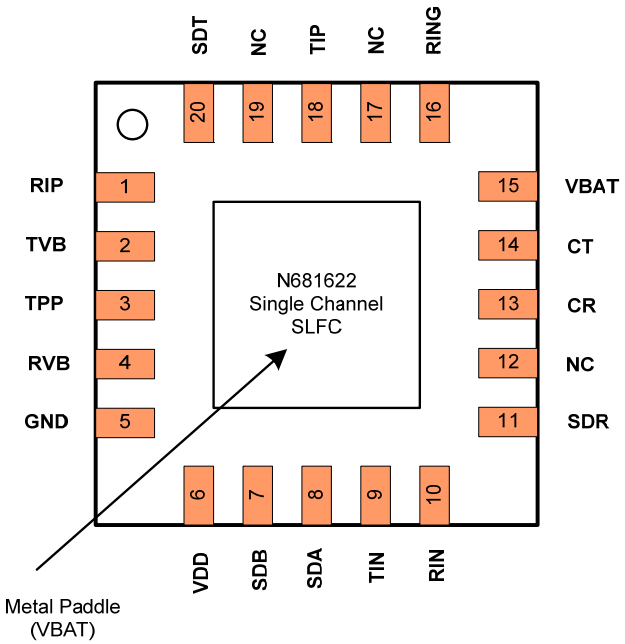

Figure 2: N681622 Subscriber Line Feed Circuit (SLFC) Pin Configuration

4. PIN DESCRIPTION

4.1. N681386/87 Pin Description

Pin Name	Pin No.	Functionality	A/D	Pin Type
VDD1	1	Line-driver 3.3 V supply	A	P
RIP	2	Positive RING Driver current source & Voltage sense	A	I/O
RIN	3	Negative RING Driver current source	A	O
TVB	4	Positive TIP Driver Base Voltage Control	A	O
GND	5	Line-driver ground supply	A	G
RVB	6	Positive RING Driver Base Voltage Control	A	O
RAC	7	RING Voice Band Input	A	I
TAC	8	TIP Voice Band Input	A	I
NC	9	No connect		
TEST	10	For internal testing only. Needs to be tied to ground during normal operation	D	I
INTb	11	Interrupt. Maskable interrupt. Open drain output for wired-or operation	D	O
CSb	12	Chip Select. When inactive, SCLK and SDI are ignored and SDO is high impedance. When active, serial port is operational	D	I
SCLK	13	Serial port bit clock. Controls serial data on SDO and latches data on SDI	D	I
SDI	14	Serial port data in. Serial port control data	D	I
SDO	15	Serial port data out. Serial port control data	D	O
DCN	16	DC/DC converter Control for external NPN BJT	D	O
DCP	17	DC/DC Converter Control for external PNP BJT	D	O
GND3	18	Logic I/O ground supply	D	G
VDDL	19	Logic supply voltage. This pin should not be connected up to an external supply. Use only as shown in application diagram.	D	I/O
VDD3	20	3.3 V Logic I/O supply	D	P
PCMT	21	Serial PCM Transmit data	D	O
FS	22	8 or 16 kHz Frame Sync	D	I/O
BCLK	23	PCM Bit Clock. Also used as internal PLL reference clock	D	I
PCMR	24	Serial PCM Receive data	D	I
DSY	25	SPI Daisy Chain Enable	D	I
XBAT	26	External Battery Supply Enable. Disables DC/DC Controller when set high	D	I
RESETb	27	Reset. Active Low. Hardware reset used to place all control registers in default state.	D	I

Pin Name	Pin No.	Functionality	A/D	Pin Type
DCH	28	DC/DC Converter Current Sense Higher input Voltage	A	I
DCL	29	DC/DC Converter Current Sense Lower input Voltage	A	I
VDD2	30	3.3 V Analog AC path and reference Supply Voltage	A	P
GND2	31	Analog AC path and reference Supply ground	A	P
IREF	32	Current Reference	A	I/O
VREF2	33	Precision Reference Voltage	A	I/O
VREF1	34	Mid Supply Reference Voltage	A	I/O
CT	35	External Capacitor TIP	A	I/O
CR	36	External Capacitor RING	A	I/O
NC	37	No Connect		
NC	38	No Connect		
WBAND	39	Wideband enable (only on N681387)	D	I
SDA	40	Subscriber Loop Differential sense signal A from linefeed circuit	A	I
SCM	41	Subscriber Common Mode sense signal from linefeed circuit	A	I
SDB	42	Subscriber Loop Differential sense signal B from linefeed circuit	A	I
TVE	43	TIP line-driver emitter voltage sense	A	I
BAT	44	Battery voltage monitoring	A	I
RVE	45	RING line-driver emitter voltage sense	A	I
TIN	46	Negative TIP Driver current source	A	O
TPP	47	Positive TIP Driver current source & Voltage sense	A	I/O
VDD1	48	Line-driver 3.3 V supply	A	P

Table 1: N681386/87 Pin Description

A	Analog
D	Digital
G	Ground

O	Output
I	Input
P	Power

4.2. N681622 Pin Description

Pin Name	Pin No.	Functionality	Type	Pin Type
RIP	1	Ring Driver Pull up Current from 34.8 Ohm resistor	LV	I/O
TVB	2	Tip Pull-Up Driver control voltage	LV	I
TPP	3	Tip Driver Pull up Current from 34.8 Ohm resistor	LV	I/O
RVB	4	Ring Pull-Up Driver control voltage	LV	I
GND	5	Supply ground (0V)	LV	G
VDD	6	3.3V Supply	LV	P
SDB	7	Subscriber differential signal B	LV	O
SDA	8	Subscriber differential signal A	LV	O
TIN	9	Tip DC Pull-Down current	LV	I
RIN	10	Ring DC Pull-Down current	LV	I
SDR	11	Subscriber differential Ring input	HV	I/O
NC	12	Not connected		
CR	13	Ring Pull-Down filter capacitor	HV	I/O
CT	14	Tip Pull-Down filter capacitor	HV	I/O
VBAT	15	Battery Supply Voltage	HV	P
RING	16	Ring terminal	HV	O
NC	17	Not connected		
TIP	18	Tip terminal	HV	O
NC	19	Not connected		
SDT	20	Subscriber differential Tip input	HV	I/O

Table 2: N681622 Pin Description

LV	Low Voltage
HV	High Voltage
G	Ground

O	Output
I	Input
P	Power

5. BLOCK DIAGRAM

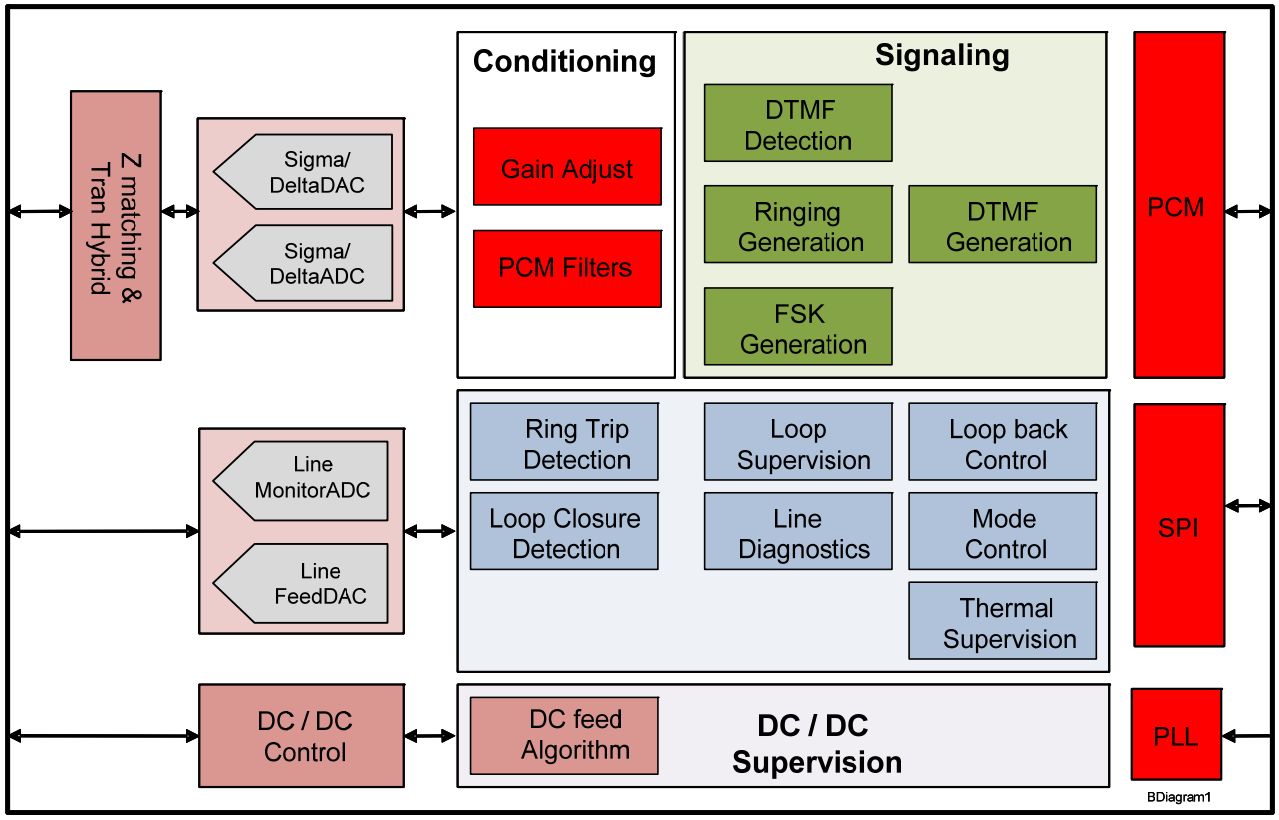

Figure 3: N681386/87 Block Diagram

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9. ABSOLUTE MAXIMUM RATINGS

9.1. Single Programmable Extended Codec/SLCC (N681386/87)

Condition	Value
Junction temperature	150^0C
Storage temperature range	-65^0C to $+150^0$C
LQFP-48 Thermal Resistance, typical	76 ^{o}C/W
QFN-48 Thermal Resistance, typical	27.1 ^{o}C/W
Voltage applied to any pin	(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Input current applied to any digital input pin	+/- 10 mA
ESD (Human Body Model)	2000 V
V_{DD} - V_{SS}	-0.5V to +3.63V
Power Dissipation	0.7W

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

9.2. Subscriber Line Feed Circuit (N681622)

Parameter	Symbol	Value	Unit
VDD Supply Voltage	VDD	-0.5 - 5	V
VBAT Supply Voltage	VBAT	-104	V
Input Voltage HV IO	VINHV	(VBAT-0.3) to (VDD+0.3)	V
Input Voltage LV IO	VINLV	-0.3 to (VDD+0.3)	V
ESD, HBM		JESD22 Class 1C	V
Operating Temperature **	TA	-40 - 100	C
Storage Temperature	TS	-40 - 150	C
Thermal Resistance QFN20	Rthja	45	C/W
Power Dissipation	Pmax	0.9	W

** When the dice temperature reaches over 130°C, the device reliability may be adversely affected.

10. OPERATING CONDITIONS

10.1. Single Programmable Extended Codec/SLCC (N681386/87)

Condition	Symbol	Min	Typ	Max	Unit
Industrial operating temperature	TA	-40		+85	C
Supply voltage (V_{DD})	VDD	3.13		3.47	V
Ground voltage (V_{SS})	VSS		0		V

***Note**: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.*

10.2. Subscriber Line Feed Circuit (N681622)

Parameter	Symbol	Min	Typ	Max	Unit
Industrial operating temperature	TA	-40		85	C
Supply voltage (V_{DD})	VDD	3.13	3.3	3.47	V
VBAT Supply Voltage	VBAT	-100	-	-9	V

11. ELECTRICAL CHARACTERISTICS

11.1. GENERAL PARAMETERS (N681386/87)

V_{DD}=3.13 V to 3.47 V; V_{SS}=0 V; T_A = -40^{0}C to +85^{0}C;

Symbol	Parameters	Conditions	Min (2)	Typ (1)	Max (2)	Units
V_{IL}	Logic Input LOW Voltage		-0.3	--	0.8	V
V_{IH}	Logic Input HIGH Voltage		2	--	3.6	V
V_T	Threshold point			1.41		V
V_{OL}	Logic Output LOW Voltage	INTB,FS,PCMT,SDO: I_{OL} = 4 mA DCP, DCN: I_{OL} = 16 mA	--	--	0.4	V
V_{OH}	Logic Output HIGH Voltage	FS,PCMT,SDO: I_{OH} = 4mA DCP, DCN: I_{OH} = 16 mA	2.4	--		V
I_{IL}	Input HIGH & LOW Leakage Current	$V_{SS}<V_{IN}<V_{DD}$ No pull-up or pull-down	--	--	+/-10	uA
I_{OZ}	Tri-state Leakage Current	$V_{SS}<V_O<V_{DD}$ High Z State	--	--	+/-10	uA
C_{IN}	Digital Input Capacitance		--	3	--	pF
C_{OUT}	Digital Output Capacitance	V_O High Z	--	3	--	pF

1. Typical values: TA = 25°C , VDD = 3.3 V
2. All min/max limits are guaranteed by Nuvoton via electrical testing or characterization. Not all specifications are 100 percent tested.

11.2. SUPPLY PARAMETERS DISCRETE SOLUTION (N681386/87 AND DISCRETE LINE DRIVER)

V_{DD}=3.13 V to 3.47 V; V_{SS}=0 V; T_A=-40^{0}C to +85^{0}C;

Symbol	Parameters	Conditions	Min	Typ (1)	Max (2)	Units
I_{PD}	Total Power Down Supply Current	RESETb = 0V, Vdd1..Vdd3 FS=BCLK=0V		12	100	uA
I_{SB}	Total Standby Supply Current	RESETb = VDD, VDD1 .. VDD3 FS=BCLK=0V, Line state Open		8.0	11.3	mA
I_{VDD}	Total Supply Current for all supplies @3.3V (linefeed states)	Open (ADC and DAC disabled)		21		mA
		Forward/Reverse Active I_{LIM}=20 mA		66		mA
		Forward/Reverse ON-HOOK Transmission		45		mA
		Forward/Reverse Idle (ADC and DAC disabled)		29		mA
		TIP/RING Open		28		mA
		Ringing, Sine wave, REN=1, V_{PK}=56 V		50		mA
I_{VBAT}	Total Battery Supply	Open, VBAT = 72V		0.72		mA

Symbol	Parameters	Conditions	Min	Typ (1)	Max (2)	Units
	Current	Forward/Reverse Active I_{LIM}=20 mA,		30		mA
		Forward/Reverse ON-HOOK Transmission, XBTA:XTBOT=0, VBAT = 54V		12		mA
		Forward/Reverse Idle, VBAT = 54V		1.3		mA
		TIP/RING Open, VBAT = 54V		1.0		mA
		Ringing, Sine wave, REN=1, VBAT = 71V		6.0		mA

1. *Typical values: TA = 25°C , VDD = 3.3 V*
2. *All min/max limits are guaranteed by Nuvoton via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *The supply current for the DC/DC converter can be calculated by : IDC/DC=IVBAT*VBAT/(efficiency*VDC/DC)*

11.3. SUPPLY PARAMETERS SLFC SOLUTION (N681386/87 AND N681622)

Parameter	Symbol	Condition	MIN	TYP	Max	Unit
VDD Supply Current	IDDO	Open State		24.0		mA
	IDDI	Low Power Idle State, VBAT=-50V		21.4		mA
	IDDA	Active State		63.3		mA
	IDDR	Ringing, 1REN, 40Vrms		TBD		mA
	IDDOT	On-Hook Transmit		47.9		mA
	IDDTO	Tip/Ring Open		TBD		mA
VBAT Supply Current	IBTO	Open State		0.4		mA
	IBTI	Low Power Idle State, VBAT=-50V	-	0.2	1.2	mA
	IBTA	Active State		29.0		mA
	IBTR	Ringing, 1REN, 40Vrms		TBD		mA
	IBTOT	On-Hook Transmit		14.1		mA
	IBTTO	Tip/Ring Open		TBD		mA

11.4. MONITORING A/D PARAMETERS

V_{DD}=3.13 V to 3.47 V; V_{SS}=0 V; T_A=-40^{0}C to +85^{0}C

Symbol	Parameters	Min	Typ	Max	Units
INL	Integral Nonlinearity (8-bit resolution)		+/-0.5		LSB
DNL	Differential Nonlinearity (8-bit resolution)		+/-0.5		LSB
	Gain Error (Current)			20	%
	Gain Error (Voltage)			10	%
	Sample Rate per channel	--	--	800	Hz
	Number of channels	--	16	--	

Typically at 12-bit the INL and DNL is 2 LSB.

11.5. ANALOG SIGNAL LEVEL AND GAIN PARAMETERS

V_{DD}=3.13 V to 3.47 V; V_{SS}=0 V; T_A=-40^{0}C to +85^{0}C; Loading 600 Ω

PARAMETER	SYM.	CONDITION	TYP.	TRANSMIT (A/D)		RECEIVE (D/A)		UNIT
				MIN.	MAX.	MIN.	MAX.	
Absolute Level	L_{ABS}	0 dBm0 = 0 dBm @ 600Ω	1.0954	---	---	---	---	V_{PK}
Max. Transmit Level	T_{XMAX}	3.17 dBm0 for u-Law 3.14 dBm0 for A-Law(1)	1.5779 1.5725	--- ---	--- ---	--- ---	--- ---	V_{PK} V_{PK}
Absolute Gain (0 dBm0 @ 1020 Hz; T_A=+25°C)	G_{ABS}	0 dBm0 @ 1020 Hz, V_{DD} =3.3V; T_A=+25°C; assuming ideal line impedance matching	0	-0.40	+0.40	-0.40	+0.40	dB
Absolute Gain variation with Temperature	G_{ABST}	T_A=0°C to T_A=+70°C T_A=-40°C to T_A=+85°C	0	-0.10 -0.20	+0.10 +0.20	-0.10 -0.20	+0.10 +0.20	dB
Absolute Gain variation with Supply Voltage	G_{ABSS}	V_{DD}=3.13 V – 3.47 V; 0dBm0 @ 1020 Hz; T_A=+25°C	0	-0.10	+0.10	-0.10	+0.10	dB
Frequency Response	G_{RTV}		See Figure					
Gain Variation vs. Level Tone (1020 Hz relative to –10 dBm0)	G_{LT}	+3 to –40 dBm0 -40 to –50 dBm0 -50 to –60 dBm0	--- --- ---	-0.3 -0.6 -1.6	+0.3 +0.6 +1.6	-0.3 -0.6 -1.6	+0.3 +0.6 +1.6	dB
Gain Step Variation	G_{ST}	-6 dB to 6 dB	0	-	+/- 0.025	-	+/-0.025	dB
Absolute Group Delay	T_{ABS}	1200 Hz	---	633	650	286	300	usec
Group Delay Distortion (relative to group delay @ 1200 Hz)	T_D		See Figure					

1. Default Gain Setting

11.6. 2-WIRE TO 4-WIRE CONVERSION PARAMETERS

V_{DD}=3.13 V to 3.47 V; V_{SS}=0 V; T_A=-40^{0}C to +85^{0}C; Loading 600 Ω

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
Return Loss	R_L	200 Hz to 3.4 kHz, 600 Ohm	26	40		dB
Trans hybrid Balance	H_B	200 Hz to 3.4 kHz, 600 Ohm	26	40		dB

11.7. 2-WIRE PARAMETERS

V_{DD}=3.13 V to 3.47 V; V_{SS}=0 V; T_A=-40^{0}C to +85^{0}C; Loading 600 Ω

PARAMETER	SYM.	CONDITION	MIN	TYP	MAX	UNIT
Longitudinal Conversion Loss	L_{CL}	300 Hz to 600 Hz	40		---	dB
		600 Hz to 3.4 kHz,	46			
Longitudinal to Metallic or PCM Balance	L_{ML}	300 Hz to 600 Hz	40	52	---	dB
	L_{MH}	600 Hz to 3.4 kHz,	46	55	---	dB
Longitudinal Impedance	L_Z	300 Hz to 3.4 kHz	---	18.5		Ohms
Longitudinal Current	L_I	Active OFF-HOOK; 300 Hz to 3.4 kHz	---	6.7		mA

11.8. LINEFEED CHARACTERISTICS

V_{DD}=3.13 V to 3.47 V; V_{SS}=0 V; T_A=-40^{0}C to +85^{0}C; Loading 600 Ω

Parameter	Sym.	Condition	MIN	TYP	MAX	Unit
RING amplitude	V_{TR}	5 REN load; sine wave; R_{LOOP} =160 Ohm; V_{BAT} = –75 V	44	45	---	V_{RMS}
Loop closure / Ground start threshold accuracy	I_{lt}	I_{lt} = 11.43 mA	---	---	+/-20	%
RING trip threshold accuracy	I_{rt}	I_{rt} = 40.64 mA	---	---	+/-20	%
Trapezoidal RING crest factor accuracy		Crest factor = 1.3	---	---	+/- 0.05	
Sinusoidal RING crest factor	R_{cf}		1.35	---	1.45	
Ringing frequency accuracy		F = 20 Hz	---	---	+/-1	%
Ringing cadence accuracy		Accuracy of on/off time	---	---	+/-50	ms
DC Loop Current Accuracy		ILIM = 20 mA, R_{LOAD} = 500 ohm		---	+/-20	%
DC Open Circuit Voltage Accuracy		Active Mode; V_{OH} = 48 V, $V_{TIP} – V_{RING}$		---	+/-4	V
Power alarm threshold accuracy		Power Threshold = 300 mW	---	---	+/-25	%

11.9. ANALOG DISTORTION AND NOISE PARAMETERS

V_{DD}=3.13 V – 3.47 V; V_{SS}=0 V; T_A=-40^{0}C to +85^{0}C; Loading 600 Ω

PARAMETER	SYM.	CONDITION	TRANSMIT (A/D)			RECEIVE (D/A)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Total Distortion vs. Level Tone u-Law	D_{LTu}	1020 Hz, C-Message Weighted	See Figure			See Figure			
Total Distortion vs. Level Tone, A-Law	D_{LTA}	1020 Hz, Psophometric Weighting							
Audio Tone Generator Signal-to-Distortion Ratio	D_{LTT}	0 dBm0, Active OFF-HOOK and OHT, ideal impedance matching	45	---	---	45	---	---	dB
Spurious Out-Of-Band (300 Hz to 3400 Hz @ 0dBm0)	D_{SPO}	4600 Hz to 7600 Hz 7600 Hz to 8400 Hz 8400 Hz to 100000 Hz	NA	NA	NA	---	-70 -70 -65	-30 -40 -30	dB
Spurious In-Band (700 Hz to 1100 Hz @ 0dBm0)	D_{SPI}	300 to 3200 Hz	---	---	-47	---	---	-47	dB
Intermodulation Distortion (300 Hz to 3400 Hz –4 to –21 dBm0)	D_{IM}	Two tones	---	---	-45	---	---	-45	dB
Idle Channel Noise	N_{IDL}	u-Law; C-message A-Law; Psophometric 16-bit Linear	--- --- ---	13 -74	18 -69	--- --- ---	1 -90	14 -76	dBrnc0 dBm0p
Power Supply Rejection	$PSRR_A$	V_{DDA}; DC to 3.4 kHz	40	---	---	40	---	---	dB
Power Supply Rejection	$PSRR_B$	V_{BAT}; DC to 3.4 kHz	40	---	---	40	---	---	dB

12. FUNCTIONAL DESCRIPTION

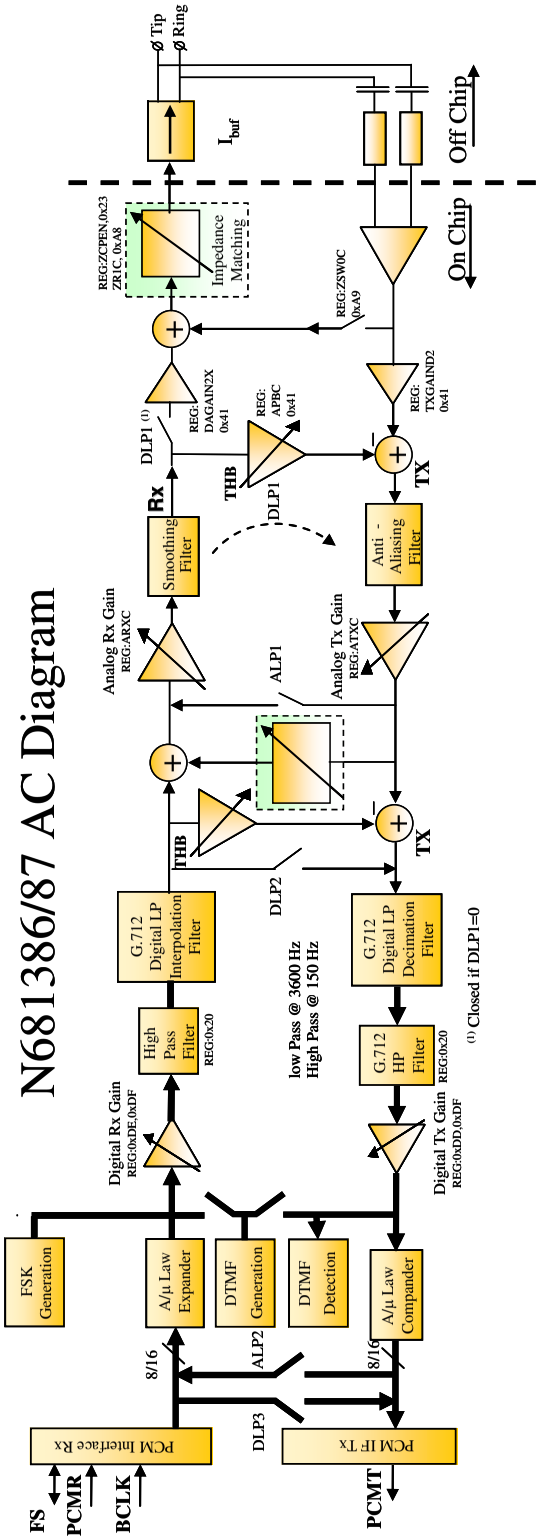

Figure 4: AC signal Path