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# DATA SHEET

## **74F193**

Up/down binary counter with separate  
up/down clocks

Product specification

1995 Jul 17

IC15 Data Handbook

# Up/down binary counter with separate up/down clocks

# 74F193

## FEATURES

- Synchronous reversible 4-bit counting
- Asynchronous parallel load capability
- Asynchronous reset (clear)
- Cascadable without external logic

## DESCRIPTION

The 74F193 is a 4-bit synchronous up/down counter in the binary mode. Separate up/down clocks, CP<sub>U</sub> and CP<sub>D</sub> respectively, simplify operation. The outputs change state synchronously with the Low-to-High transition of either clock input. If the CP<sub>U</sub> clock is pulsed while CP<sub>D</sub> is held High, the device will count up. If CP<sub>D</sub> clock is pulsed while CP<sub>U</sub> is held High, the device will count down. The device can be cleared at any time by the asynchronous reset pin. It may also be loaded in parallel by activating the asynchronous parallel load pin.

Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, asynchronous preset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a Low-to-High transition on the CP<sub>D</sub> input will decrease the count by one, while a similar transition on the CP<sub>U</sub> input will advance the count by one.

One clock should be held High while counting with the other, because the circuit will either count by twos or not at all, depending on the state of the first JK flip-flop, which cannot toggle as long as either clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts.

The Terminal Count Up ( $\overline{TC}_U$ ) and Terminal Count Down ( $\overline{TC}_D$ ) outputs are normally High. When the circuit has reached the maximum count state of 15, the next High-to-Low transition of CP<sub>U</sub> will cause  $\overline{TC}_U$  to go Low.  $\overline{TC}_U$  will stay Low until CP<sub>U</sub> goes High again, duplicating the count up clock, although delayed by two gate delays. Likewise, the  $\overline{TC}_D$  output will go Low when the circuit is in the zero state and the CP<sub>D</sub> goes Low. The  $\overline{TC}$  outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms.

Multistage counters will not be fully synchronous since there is a two-gate delay time difference added for each stage that is added.

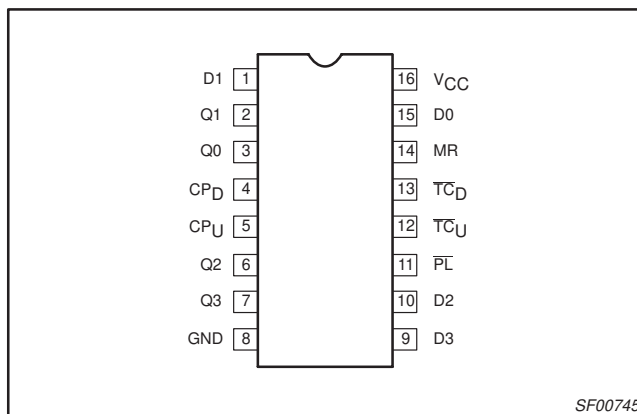
The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs (D0 - D3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs when the Parallel Load ( $\overline{PL}$ ) input is Low. A High level on the Master Reset (MR) input will disable the parallel load gates, override both clock inputs, and set all Q outputs Low. If one of the clock inputs is Low during and after a reset or load operation, the next Low-to-High transition of the clock will be interpreted as a legitimate signal and will be counted.

TYPE	TYPICAL f <sub>MAX</sub>	TYPICAL SUPPLY CURRENT (TOTAL)
74F193	125MHz	32mA

## ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V <sub>CC</sub> = 5V ±10%, T <sub>amb</sub> = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F193N	SOT38-4
16-pin plastic SO	N74F193D	SOT109-1

## PIN CONFIGURATION



## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

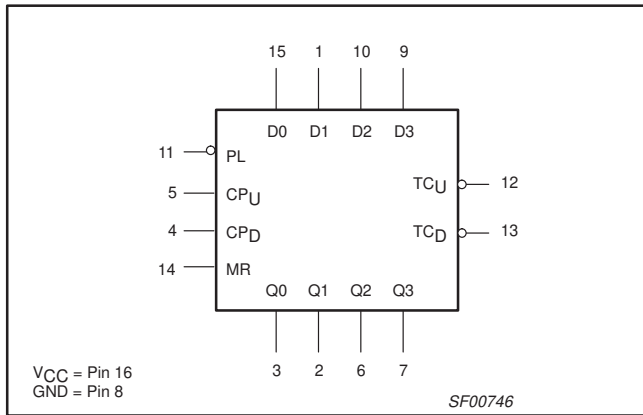
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D3	Data inputs	1.0/1.0	20µA/0.6mA
CP <sub>U</sub>	Count up clock input (active rising edge)	1.0/3.0	20µA/1.8mA
CP <sub>D</sub>	Count down clock input (active rising edge)	1.0/3.0	20µA/1.8mA
$\overline{PL}$	Asynchronous parallel load control input (active Low)	1.0/1.0	20µA/0.6mA
MR	Asynchronous master reset input	1.0/1.0	20µA/0.6mA
Q0 - Q3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}_U$	Terminal count up (carry) output (active Low)	50/33	1.0mA/20mA
$\overline{TC}_D$	Terminal count down (borrow) output (active Low)	50/33	1.0mA/20mA

**NOTE:** One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

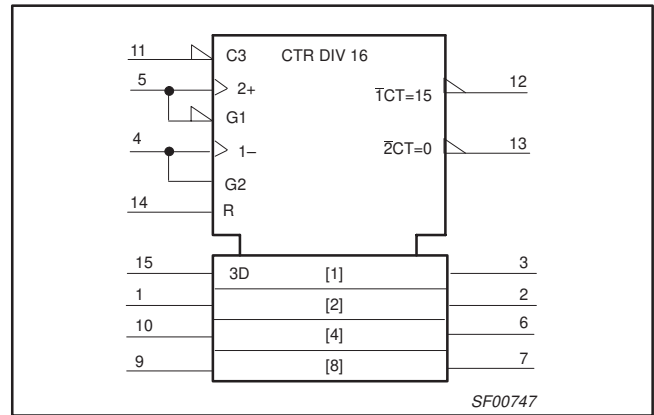
# Up/down binary counter with separate up/down clocks

74F193

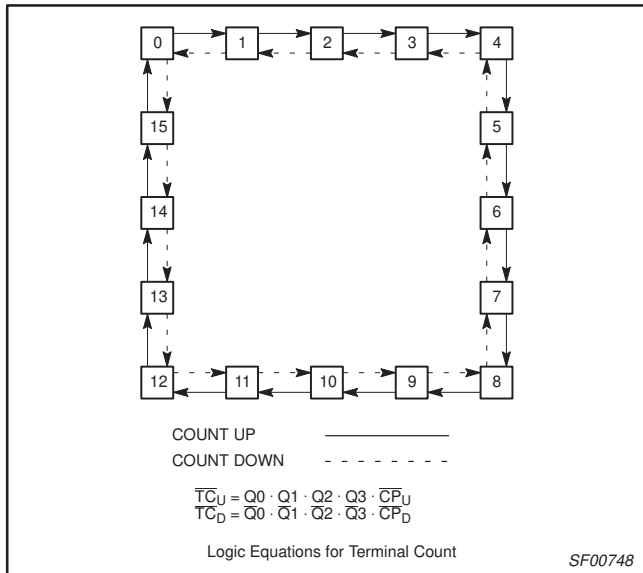
## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



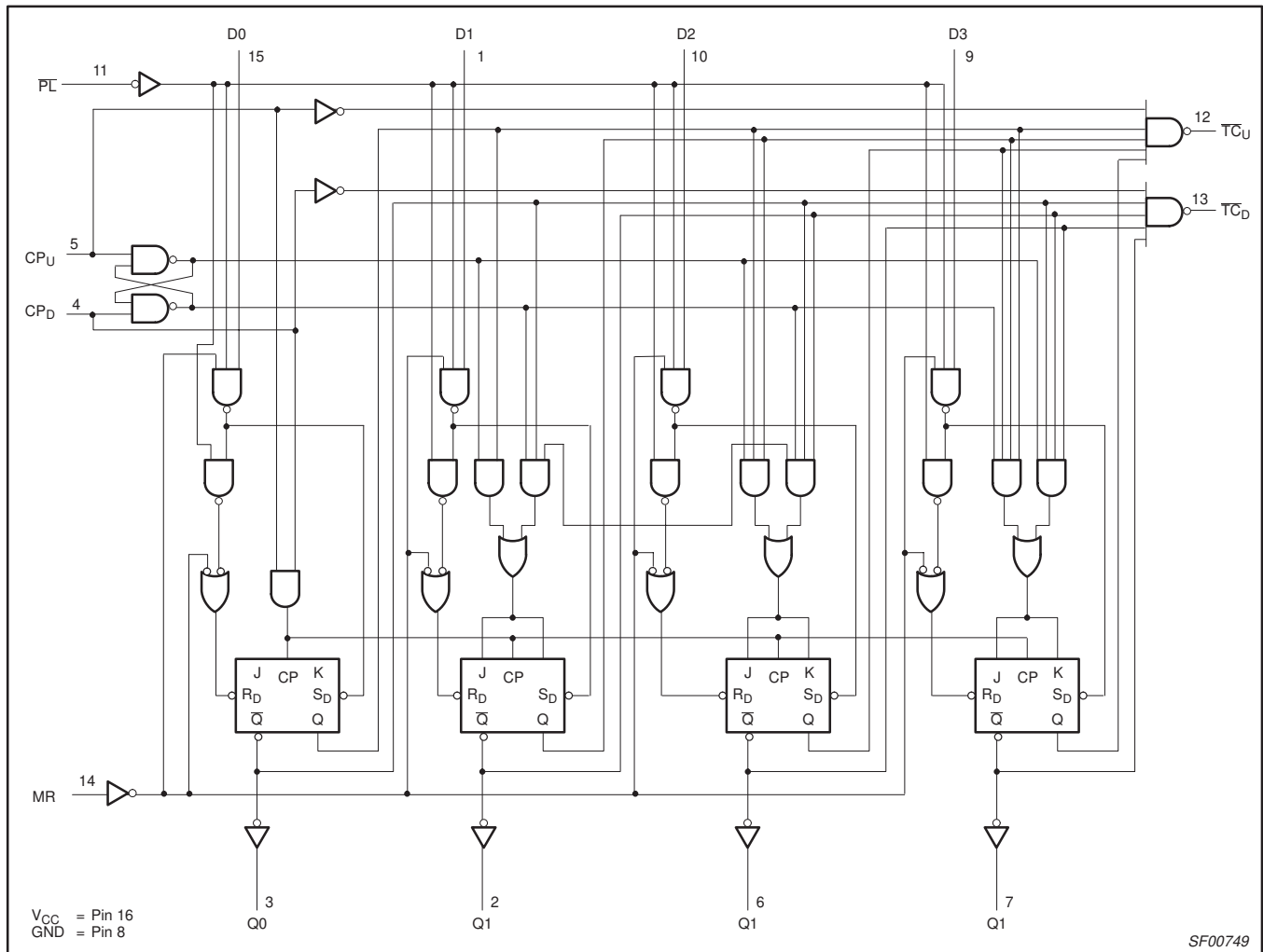
## STATE DIAGRAM



# Up/down binary counter with separate up/down clocks

74F193

## LOGIC DIAGRAM



SF00749

## FUNCTION TABLE

INPUTS								OUTPUTS						OPERATING MODE
MR	PL	CP <sub>U</sub>	CP <sub>D</sub>	D0	D1	D2	D3	Q0	Q1	Q2	Q3	TC <sub>U</sub>	TC <sub>D</sub>	
H	X	X	L	X	X	X	X	L	L	L	L	H	L	Reset (clear)
H	X	X	H	X	X	X	X	L	L	L	L	H	H	
L	L	X	L	L	L	L	L	L	L	L	L	H	L	Parallel load
L	L	X	H	L	L	L	L	L	L	L	L	H	H	
L	L	L	X	H	H	H	H	H	H	H	H	L	H	
L	L	H	X	H	H	H	H	H	H	H	H	H	H	
L	H	↑	H	X	X	X	X	Count up				H <sup>1</sup>	H	Count up
L	H	H	↑	X	X	X	X	Count down				H	H <sup>2</sup>	Count down

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 ↑ = Low-to-High clock transition

**NOTES:**  
 TC<sub>U</sub>=CP<sub>U</sub> at terminal count up (HHHH)  
 TC<sub>D</sub>=CP<sub>D</sub> at terminal count down (LLLL)

## Up/down binary counter with separate up/down clocks

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5.0	mA
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	40	mA
$T_{amb}$	Operating free-air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-1	mA
$I_{OL}$	Low-level output current			20	mA
$T_{amb}$	Operating free-air temperature range	0		+70	°C

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>NO TAG</sup>	LIMITS			UNIT
			MIN	TYP NO TAG	MAX	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}, V_{IH} = \text{MIN}$	$\pm 10\%V_{CC}$	2.5		V
			$\pm 5\%V_{CC}$	2.7	3.4	V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = \text{MAX}, V_{IH} = \text{MIN}$	$\pm 10\%V_{CC}$		0.35	0.50
			$\pm 5\%V_{CC}$		0.35	0.50
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			100	$\mu\text{A}$
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			20	$\mu\text{A}$
$I_{IL}$	Low-level input current	CP <sub>U</sub> , CP <sub>D</sub>			-1.8	mA
		Others			-0.6	mA
$I_{OS}$	Short-circuit output current <sup>NO TAG</sup>	$V_{CC} = \text{MAX}$	-60		-150	mA
$I_{CC}$	Supply current (total) <sup>4</sup>	$V_{CC} = \text{MAX}$		32	50	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}, T_{amb} = 25^\circ\text{C}$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.
- Measure  $I_{CC}$  with parallel load and Master reset inputs grounded, all other inputs at 4.5V and all outputs open.

## Up/down binary counter with separate up/down clocks

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f <sub>MAX</sub>	Maximum clock frequency	Waveform 1	100	125		90		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP <sub>U</sub> or CP <sub>D</sub> to TC <sub>U</sub> or TC <sub>D</sub>	Waveform 2	2.5 3.0	5.5 5.0	8.5 8.0	2.5 3.0	9.0 9.0	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP <sub>U</sub> or CP <sub>D</sub> to Q <sub>n</sub>	Waveform 1	2.5 5.0	5.5 8.5	8.5 12.0	2.5 5.0	9.0 13.0	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay D <sub>n</sub> to Q <sub>n</sub>	Waveform 4	2.0 6.0	4.0 9.5	7.0 13.5	1.5 6.0	8.0 15.0	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay PL to Q <sub>n</sub>	Waveform 3	4.5 5.5	6.5 8.5	10.0 12.0	4.0 5.0	11.0 13.0	ns ns
t <sub>PHL</sub>	Propagation delay MR to Q <sub>n</sub>	Waveform 5	5.0	7.5	11.0	5.0	12.0	ns
t <sub>PLH</sub>	Propagation delay MR to TC <sub>U</sub>	Waveform 5	6.0	8.5	12.0	5.5	13.0	ns
t <sub>PHL</sub>	Propagation delay MR to TC <sub>D</sub>	Waveform 5	5.0	7.5	11.0	5.0	12.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay PL to TC <sub>U</sub> or TC <sub>D</sub>	Waveform 3	6.0 6.0	9.5 9.0	13.5 12.0	6.0 6.0	15.0 13.0	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay D <sub>n</sub> to TC <sub>U</sub> or TC <sub>D</sub>	Waveform 4	5.5 4.5	9.0 8.5	13.0 12.5	5.0 4.5	14.0 13.5	ns ns

## AC SETUP REQUIREMENTS

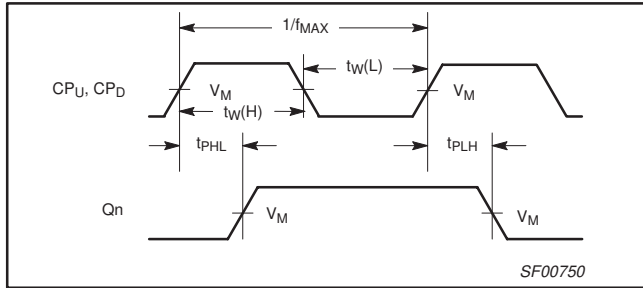
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, High or Low D <sub>n</sub> to PL	Waveform 6	4.5 4.5			5.0 5.0		ns ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low D <sub>n</sub> to PL	Waveform 6	2.0 2.0			2.0 2.0		ns ns
t <sub>w</sub> (L)	PL Pulse width Low	Waveform 3	6.0			6.0		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP <sub>U</sub> or CP <sub>D</sub> Pulse width High or Low	Waveform 1	3.5 5.0			3.5 5.0		ns ns
t <sub>w</sub> (L)	CP <sub>U</sub> or CP <sub>D</sub> Pulse width Low (Change of direction)	Waveform 1	10.0			10.0		ns
t <sub>w</sub> (H)	MR Pulse width High	Waveform 5	6.0			6.0		ns
t <sub>rec</sub>	Recovery time, PL to CP <sub>U</sub> or CP <sub>D</sub>	Waveform 3	6.0			6.0		ns
t <sub>rec</sub>	Recovery time MR to CP <sub>U</sub> or CP <sub>D</sub>	Waveform 5	4.0			4.0		ns

# Up/down binary counter with separate up/down clocks

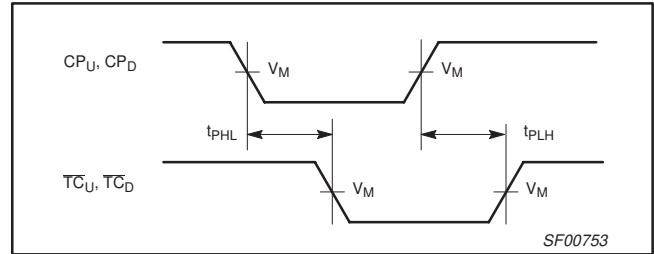
74F193

## AC WAVEFORMS

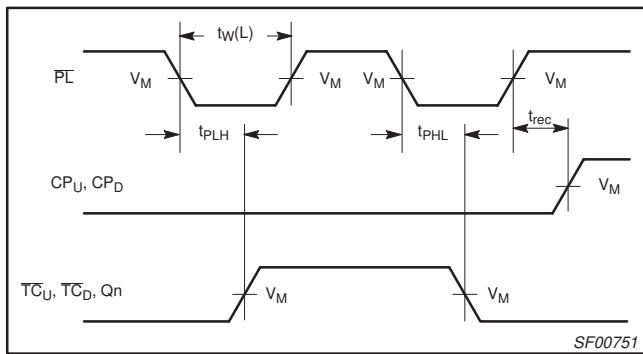
For all waveforms  $V_M = 1.5V$



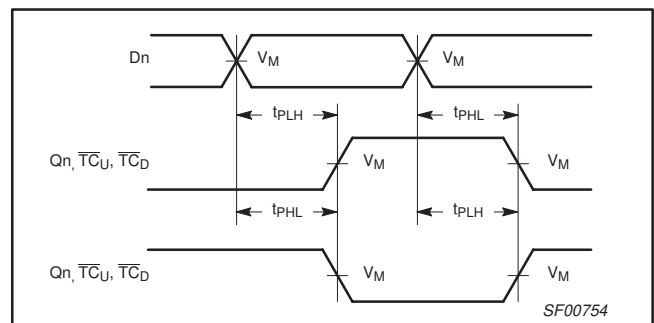
**Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency**



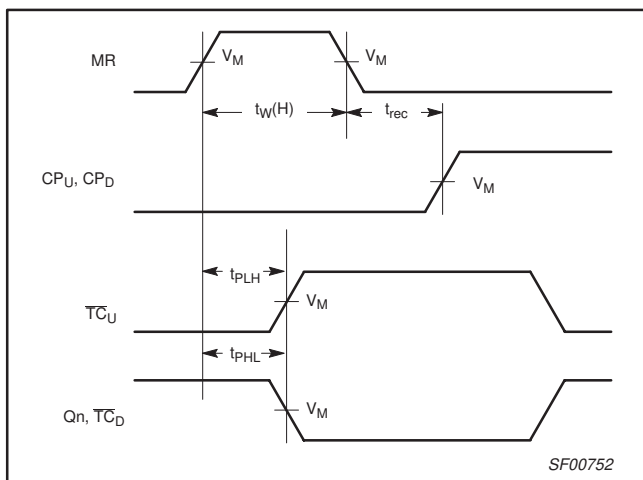
**Waveform 2. Propagation Delay, Clock to Terminal Count**



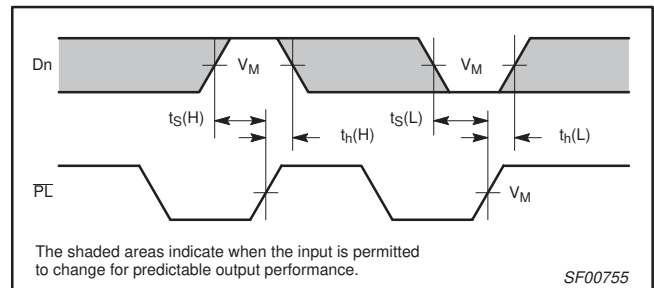
**Waveform 3. Parallel Pulse Width, Parallel Load to Output Delays, and Parallel Load to Clock Recovery Time**



**Waveform 4. Propagation Delay, Data to Flip-Flop Outputs, Terminal Count Up and Down Outputs**



**Waveform 5. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time**



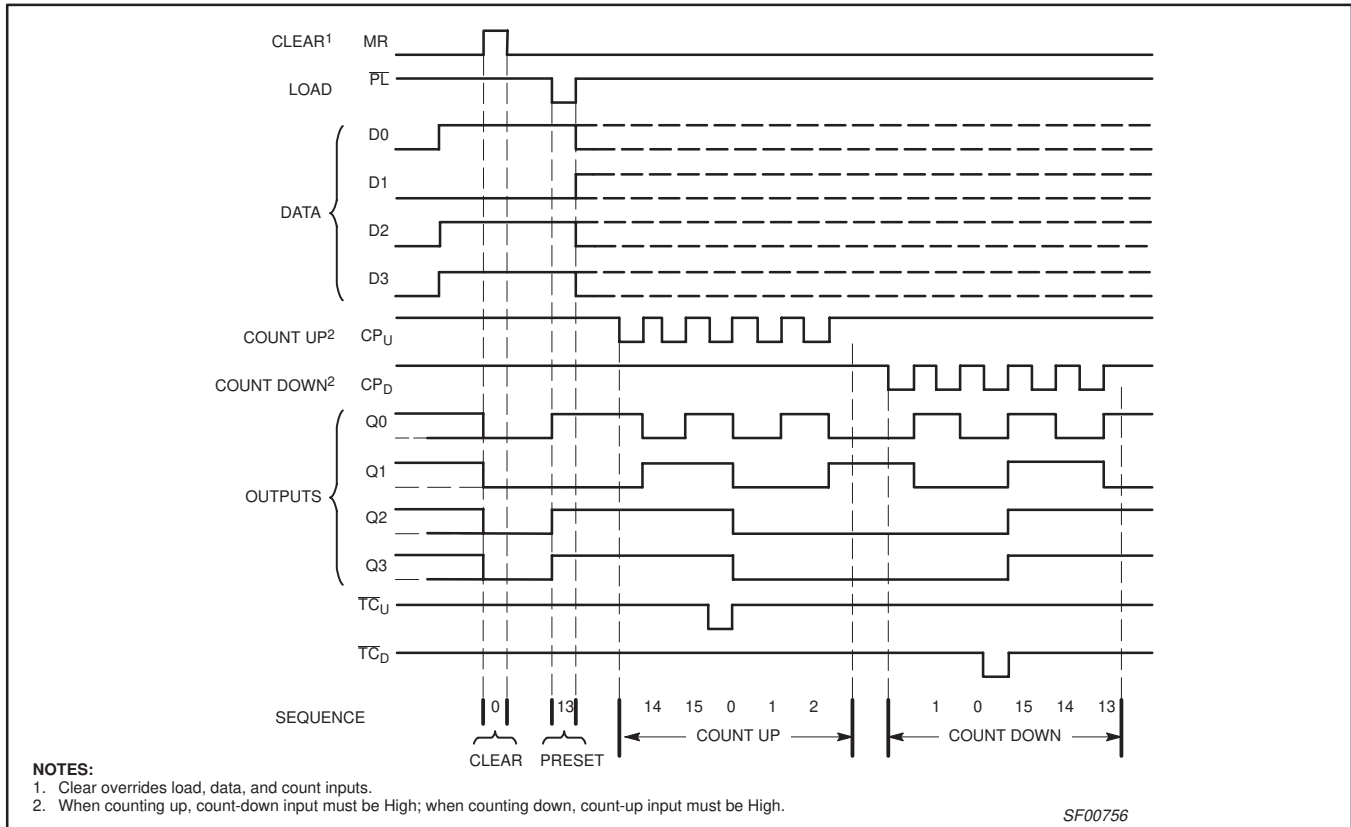
**Waveform 6. Data Setup and Hold Times**



# Up/down binary counter with separate up/down clocks

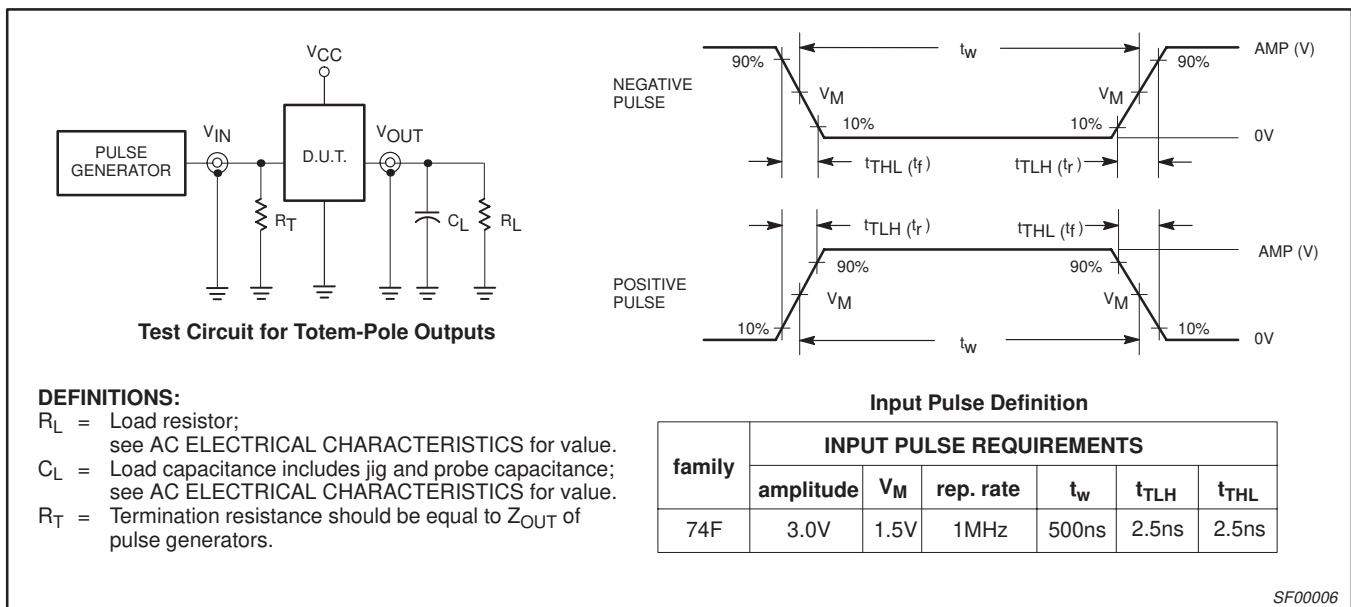
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## Timing Diagram (Typical clear, load, and count sequence)



### Binary Counter

## TEST CIRCUIT AND WAVEFORMS

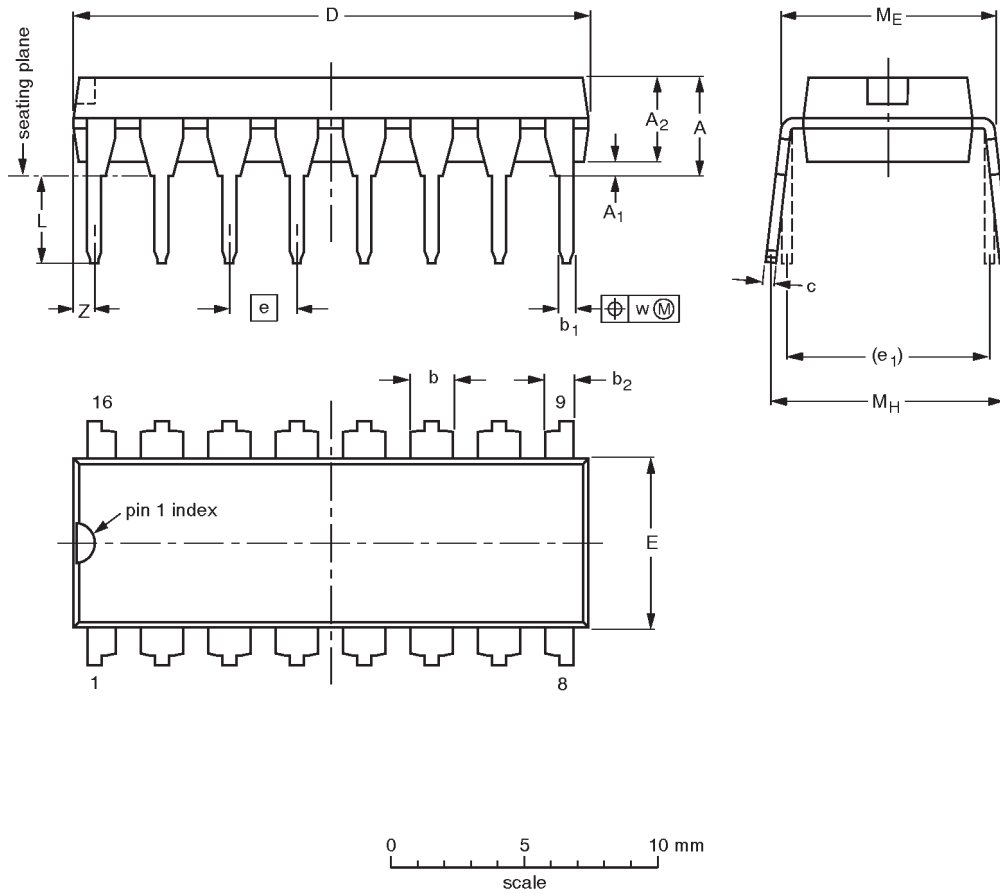


Up/down binary counter with separate up/down clocks

74F193

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

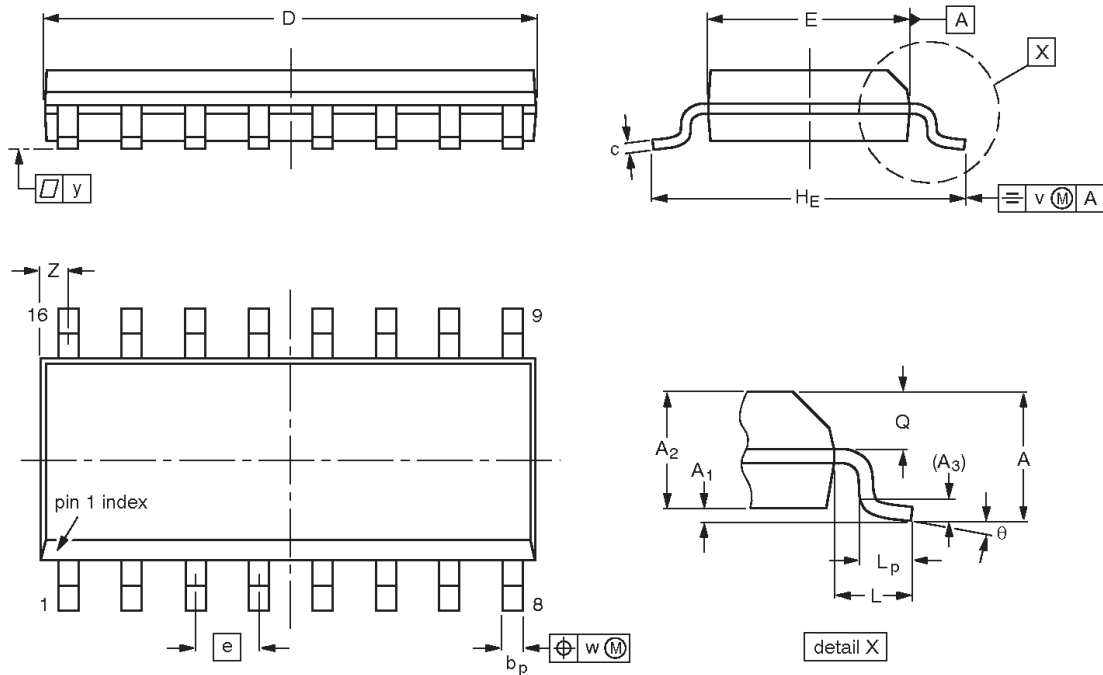
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

Up/down binary counter with separate up/down clocks

74F193

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

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Up/down binary counter with separate up/down clocks

74F193

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**NOTES**

## Up/down binary counter with separate up/down clocks

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**Data sheet status**

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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