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# DATA SHEET

## **74F827**

10-bit buffer/line driver, non-inverting  
(3-State)

Product data

2004 Jan 21

Replaces Product specification 74F827/74F828 of 1994 Dec 5

# 10-bit buffer/line driver, non-inverting (3-State)

# 74F827

## FEATURES

- High impedance NPN base inputs for reduced loading (20  $\mu$ A in HIGH and LOW states)
- $I_{IL}$  is 20  $\mu$ A vs FAST family spec of 600  $\mu$ A
- Ideal where high speed, light bus loading and increased fan-in are required
- Controlled rise and fall times to minimize ground bounce
- Glitch free power-up in 3-State
- Flow through pinout architecture for microprocessor oriented applications
- Outputs sink 64 mA
- 74F827 is available in SSOP type II package

## DESCRIPTION

The 74F827 10-Bit buffer provides high performance bus interface buffering for wide data/address paths or buses carrying parity. The device has NOR Output Enables ( $\overline{OE}0$ ,  $\overline{OE}1$ ) for maximum control flexibility.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F827	6.0ns	60 mA

## ORDERING INFORMATION

COMMERCIAL RANGE:  $V_{CC} = 5 V \pm 10\%$ ;  $T_{amb} = 0^{\circ}C$  to  $+70^{\circ}C$

Type number	Package		Version
	Name	Description	
N74F827N	DIP24	plastic dual in-line package; 24 leads (300 mil)	SOT222-1
N74F827D	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
N74F827DB	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

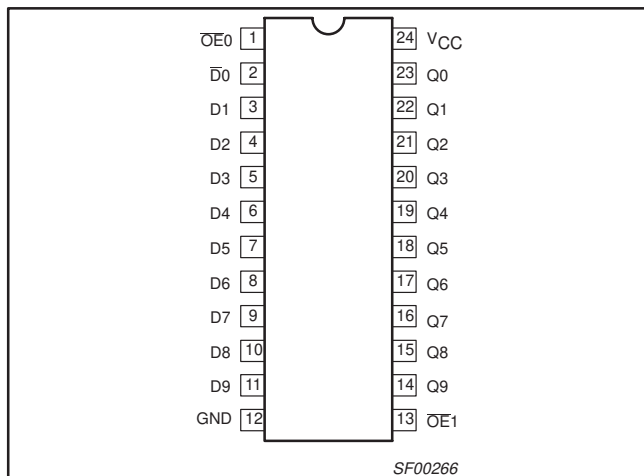
## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH / LOW
D0-D9	Data inputs	1.0/0.033	20 $\mu$ A / 20 $\mu$ A
$\overline{OE}0$ - $\overline{OE}1$	Output enable inputs (active-LOW)	1.0/0.033	20 $\mu$ A / 20 $\mu$ A
Q0-Q9	Data outputs	1200/106.7	24 mA / 64 mA

### NOTES:

One (1.0) FAST Unit Load is defined as: 20  $\mu$ A in the HIGH state and 0.6 mA in the LOW state.

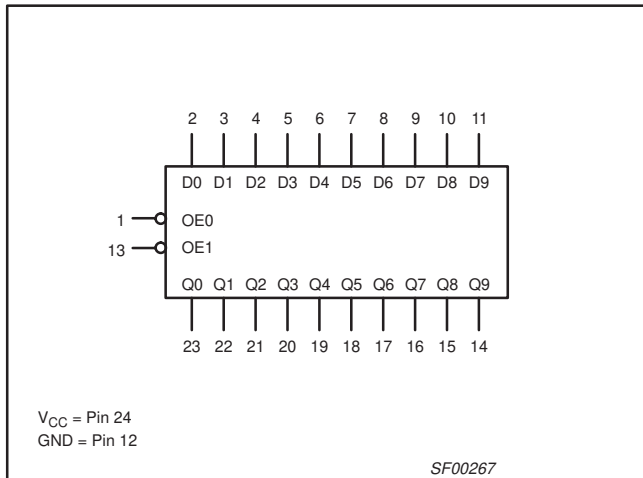
## PIN CONFIGURATION



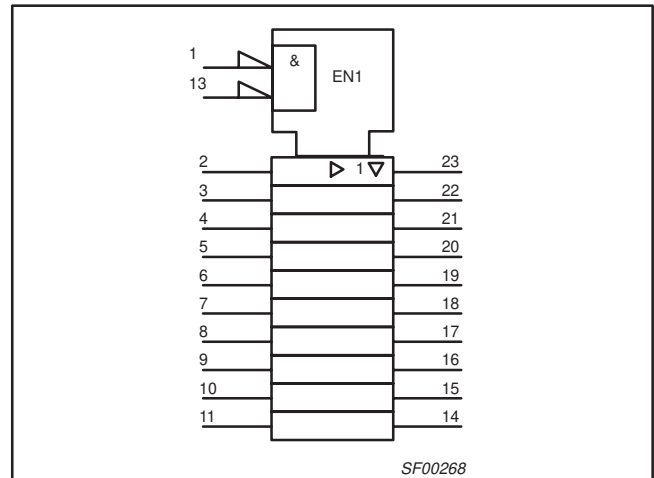
# 10-bit buffer/line driver, non-inverting (3-State)

74F827

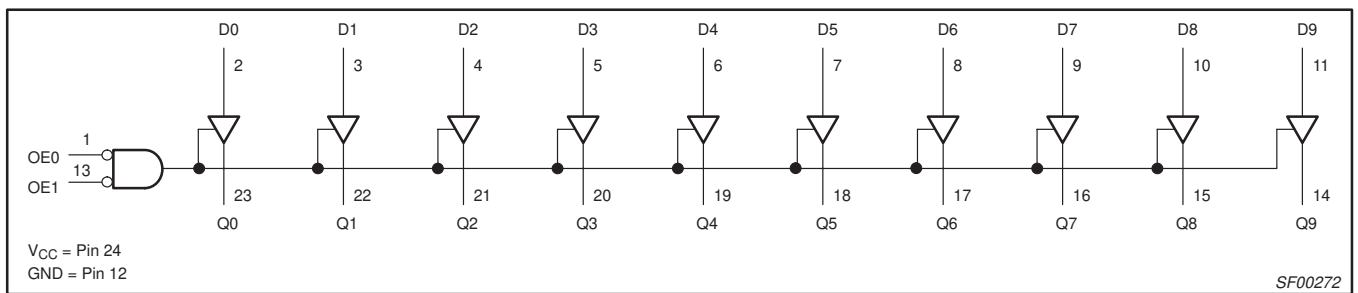
## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS		OUTPUTS	OPERATING MODE
OE <sub>n</sub>	D <sub>n</sub>	Q <sub>n</sub>	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

H = HIGH voltage level  
L = LOW voltage level  
X = Don't care  
Z = High impedance "off" state

## 10-bit buffer/line driver, non-inverting (3-State)

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**ABSOLUTE MAXIMUM RATINGS**

Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in HIGH output state	-0.5 to $+V_{CC}$	V
$I_{OUT}$	Current applied to output in LOW output state	128	mA
$T_{amb}$	Operating free-air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	HIGH-level input voltage	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	-	-	0.8	V
$I_{IK}$	Input clamp current	-	-	-18	mA
$I_{OH}$	HIGH-level output current	-	-	-24	mA
$I_{OL}$	LOW-level output current	-	-	64	mA
$T_{amb}$	Operating free-air temperature range	0	-	+70	°C



## 10-bit buffer/line driver, non-inverting (3-State)

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**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>			LIMITS			UNIT	
					MIN	TYP <sup>2</sup>	MAX		
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = -15 mA	± 10% V <sub>CC</sub>	2.4	-	-	V	
				± 5% V <sub>CC</sub>	2.4	3.3	-	V	
		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = -24 mA	± 10% V <sub>CC</sub>	2.0	-	-	V	
				± 5% V <sub>CC</sub>	2.0	-	-	V	
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OL</sub> = 64 mA	± 10% V <sub>CC</sub>	-	-	0.55	V	
				± 5% V <sub>CC</sub>	-	0.42	0.55	V	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN; I <sub>I</sub> = I <sub>IK</sub>			-	-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = 0 V; V <sub>I</sub> = 7.0 V			-	-	100	μA	
I <sub>IH</sub>	HIGH-level input current	V <sub>CC</sub> = MAX; V <sub>I</sub> = 2.7 V			-	-	20	μA	
I <sub>IL</sub>	LOW-level input current	V <sub>CC</sub> = MAX; V <sub>I</sub> = 0.5 V			-	-	-20	μA	
I <sub>OZH</sub>	Off-state output current, HIGH voltage applied	V <sub>CC</sub> = MAX; V <sub>O</sub> = 2.7 V			-	-	50	μA	
I <sub>OZL</sub>	Off-state output current, LOW voltage applied	V <sub>CC</sub> = MAX; V <sub>O</sub> = 0.5 V			-	-	-50	μA	
I <sub>OS</sub>	Short circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX			-100	-	-225	mA	
I <sub>CC</sub>	Supply current (total)	I <sub>CCH</sub>	V <sub>CC</sub> = MAX			-	50	70	mA
		I <sub>CCL</sub>				-	70	100	mA
		I <sub>CCZ</sub>				-	60	90	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5 V, T<sub>amb</sub> = 25 °C.
- Not more than one output should be shorted at one time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

## 10-bit buffer/line driver, non-inverting (3-State)

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## AC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25 °C V <sub>CC</sub> = 5 V C <sub>L</sub> = 50 pF; R <sub>L</sub> = 500 Ω			T <sub>amb</sub> = 0 °C to +70 °C V <sub>CC</sub> = 5 V ± 10% C <sub>L</sub> = 50 pF; R <sub>L</sub> = 500 Ω		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay D <sub>n</sub> to Q <sub>n</sub>	Waveform 1	2.0 2.0	5.5 4.5	8.5 8.5	2.0 2.0	9.0 9.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time OE <sub>n</sub> to Q <sub>n</sub>	Waveform 2 Waveform 3	5.0 4.0	8.0 6.0	12.0 10.5	4.5 4.0	14.0 11.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time OE <sub>n</sub> to Q <sub>n</sub>	Waveform 2 Waveform 3	2.5 2.5	5.0 5.0	8.0 8.0	2.0 2.0	8.5 8.5	ns

## AC CHARACTERISTICS

For 1 Output switching with C<sub>L</sub> = 300 pF and R<sub>L</sub> = 500 Ω load

SYMBOL	PARAMETER	CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25 °C V <sub>CC</sub> = 5 V C <sub>L</sub> = 300 pF; R <sub>L</sub> = 500 Ω			T <sub>amb</sub> = 0 °C to +70 °C V <sub>CC</sub> = 5 V ± 10% C <sub>L</sub> = 300 pF; R <sub>L</sub> = 500 Ω		
			MIN	Typ	Max	MIN	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay D <sub>n</sub> to Q <sub>n</sub>	Waveform 1	– –	9.5 7.5	13.0 10.0	– –	14.0 11.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time OE <sub>n</sub> to Q <sub>n</sub>	Waveform 2 Waveform 3	– –	15.0 9.5	20.0 13.0	– –	21.0 14.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time OE <sub>n</sub> to Q <sub>n</sub>	Waveform 2 Waveform 3	– –	15.0 9.5	19.0 13.5	– –	20.0 14.0	ns

## AC CHARACTERISTICS

For 10 Outputs switching with C<sub>L</sub> = 300 pF and R<sub>L</sub> = 500 Ω load

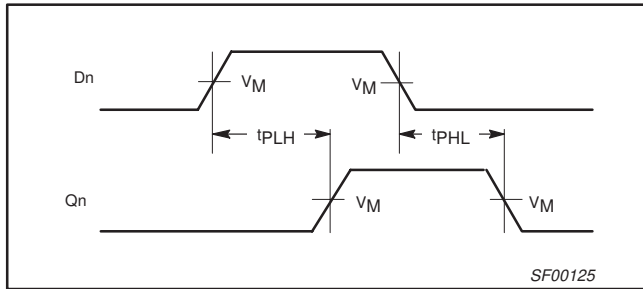
SYMBOL	PARAMETER	CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25 °C V <sub>CC</sub> = 5 V C <sub>L</sub> = 300 pF; R <sub>L</sub> = 500 Ω			T <sub>amb</sub> = 0 °C to +70 °C V <sub>CC</sub> = 5 V ± 10% C <sub>L</sub> = 300 pF; R <sub>L</sub> = 500 Ω		
			MIN	Typ	Max	MIN	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay D <sub>n</sub> to Q <sub>n</sub>	Waveform 1	– –	12.0 14.0	16.0 17.0	– –	17.0 18.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time OE <sub>n</sub> to Q <sub>n</sub>	Waveform 2 Waveform 3	– –	15.0 17.0	20.0 21.0	– –	21.0 21.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time OE <sub>n</sub> to Q <sub>n</sub>	Waveform 2 Waveform 3	– –	15.0 12.5	19.0 15.5	– –	20.0 16.0	ns

# 10-bit buffer/line driver, non-inverting (3-State)

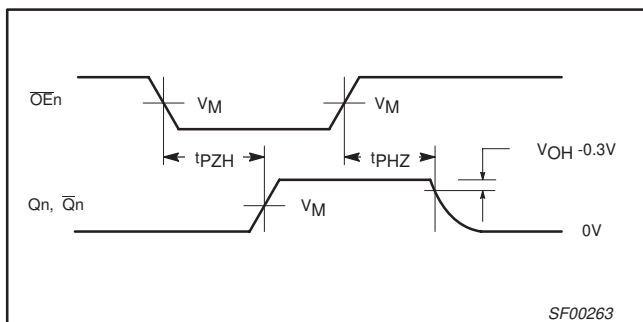
74F827

## AC WAVEFORMS

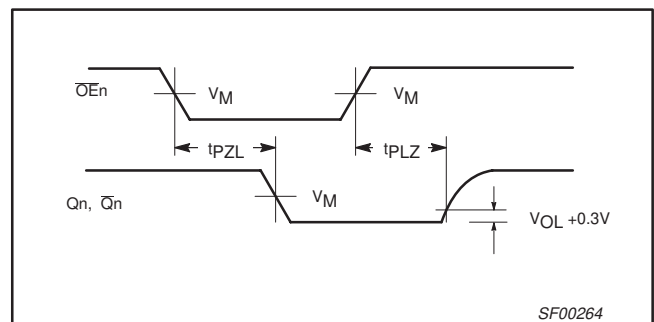
For all waveforms,  $V_M = 1.5\text{ V}$



Waveform 1. Propagation delay for non-inverting output



Waveform 2. 3-State Output Enable time to HIGH level and Output Disable time from HIGH level



Waveform 3. 3-State Output Enable time to LOW level and Output Disable time from LOW level

**Test Circuit for Open Collector Outputs**

**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

**DEFINITIONS:**

$R_L$  = Load resistor; see AC electrical characteristics for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

**Input Pulse Definition**

INPUT PULSE REQUIREMENTS						
family	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0 V	1.5 V	1 MHz	500 ns	2.5 ns	2.5 ns

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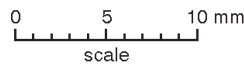
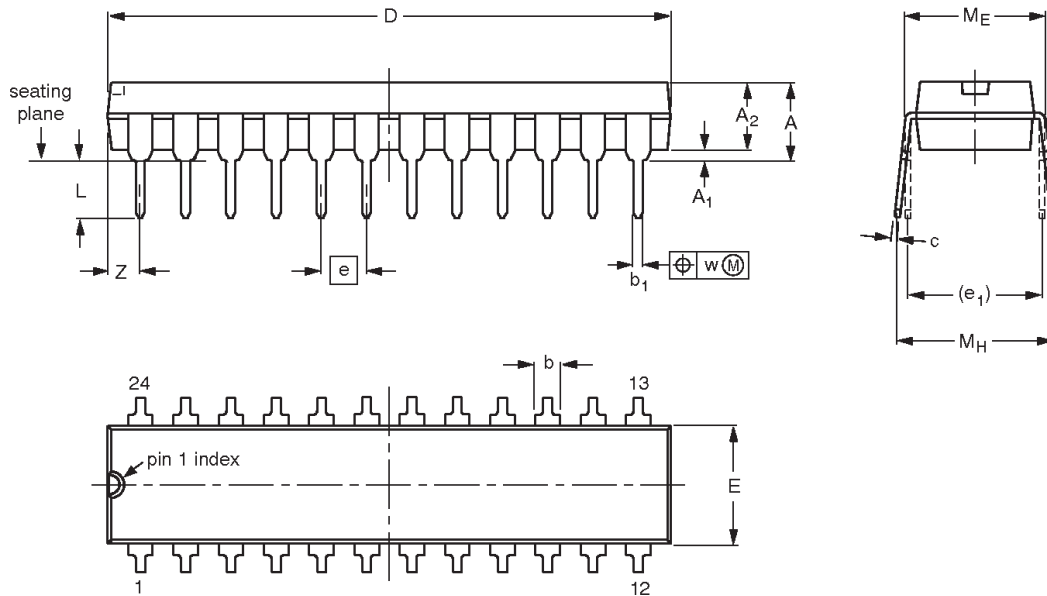


# 10-bit buffer/line driver, non-inverting (3-State)

74F827

DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



**DIMENSIONS (mm dimensions are derived from the original inch dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.7	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.25	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.246	0.1	0.3	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

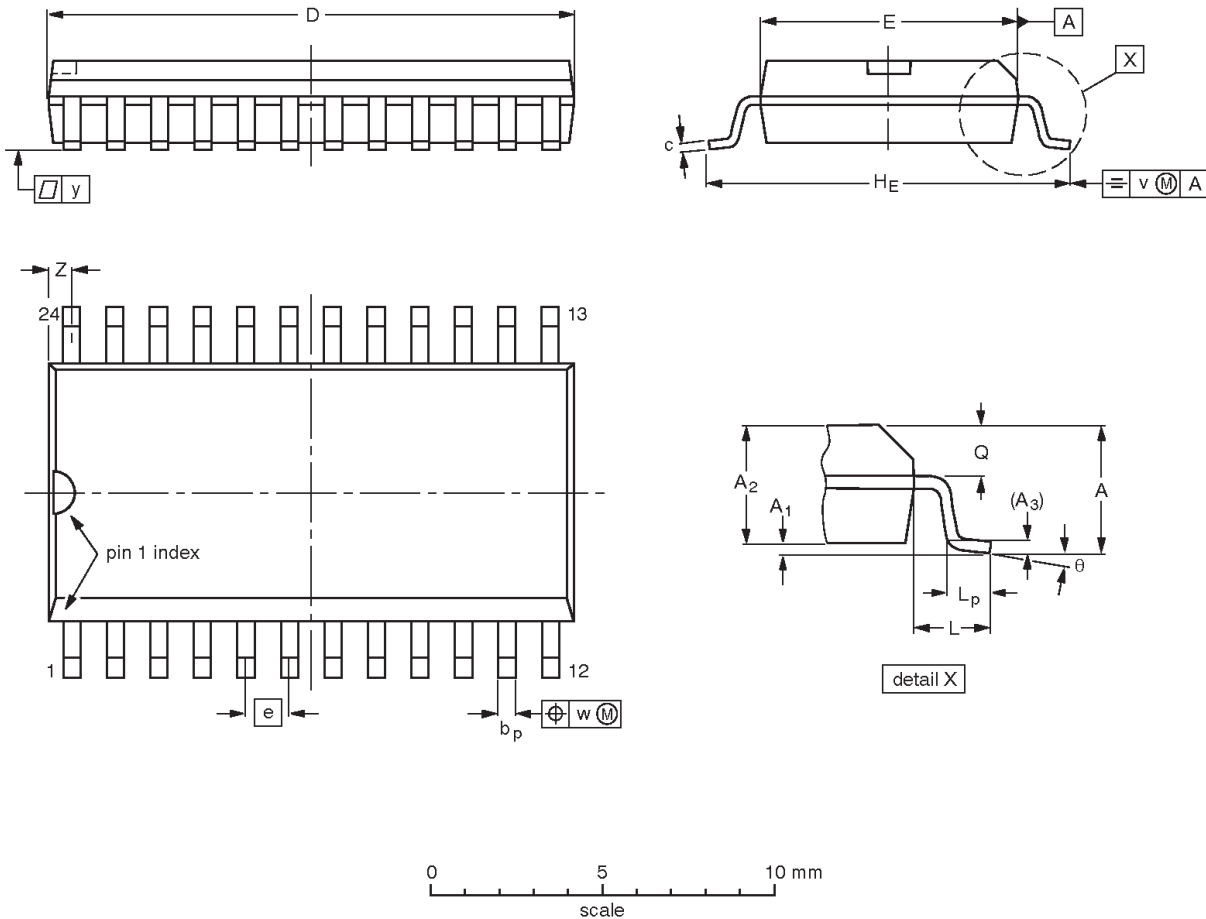
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT222-1		MS-001				<del>99-12-27</del> 03-03-12

# 10-bit buffer/line driver, non-inverting (3-State)

74F827

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

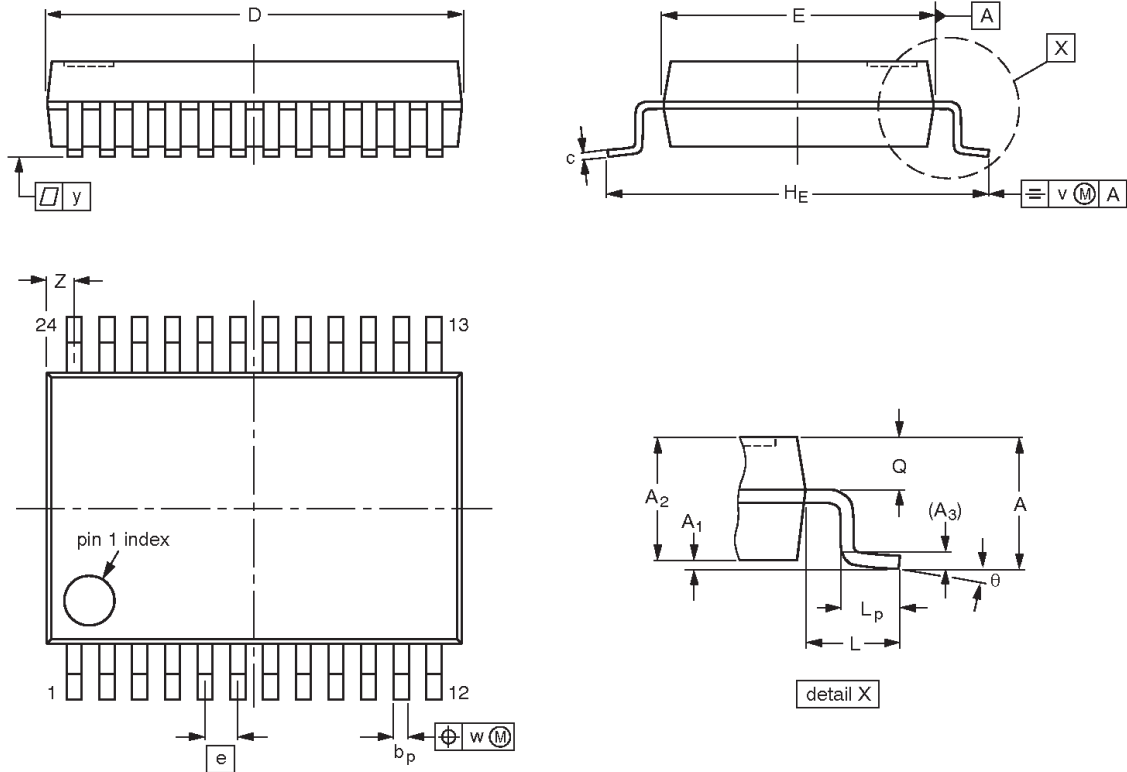
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				-99-12-27 03-02-19

10-bit buffer/line driver, non-inverting (3-State)

74F827

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	HE	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

**Note**

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				99-12-27 03-02-19

## 10-bit buffer/line driver, non-inverting (3-State)

74F827

## REVISION HISTORY

Rev	Date	Description
_3	20040121	<b>Product data (9397 750 12741). ECN 853-0880 A15336 of 21 January 2004.</b> <b>Replaces 74F827_74F828_2 dated 1994 Dec 5.</b> Modifications: <ul style="list-style-type: none"> <li>• Delete all references to 74F828 (product discontinued).</li> <li>• AC Characteristics table (for 10 outputs switching): change Limits columns' headings from <math>C_L = 50</math> pF to <math>C_L = 300</math> pF.</li> </ul>
_2	19941205	<b>Product specification. ECN 853-0880 14382 of 05 December 1994.</b>

## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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9397 750 12741

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