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DATA SHEET

74F862
Bus transceiver, inverting (3-State)

Product data
Replaces data sheet 74F862, 74F863 of 2000 Mar 24

2004 Jan 23

Philips
Semiconductors

PHILIPS

Bus transceiver, inverting (3-State) 74F862

FEATURES

- Provide high performance bus interface buffering for wide data/address paths or buses carrying parity
- High impedance NPN base inputs for reduced loading (20 μA in HIGH and LOW states)
- I_{IL} is 20 μA for minimum bus loading
- Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- Slim dual In-line (DIP) 300 mil package
- Broadside pinout
- Outputs sink 64 mA

DESCRIPTION

The 74F862 bus transceiver provides a high performance inverting bus interface for wide data/address paths of buses carrying parity.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F862	6.0 ns	150 mA

ORDERING INFORMATION

COMMERCIAL RANGE: V_{CC} = 5 V ± 10%; T_{amb} = 0 °C to +70 °C

Type number	Package		
	Name	Description	Version
N74F862N	DIP24	plastic dual in-line package; 24 leads (300 mil)	SOT222-1
N74F862D (see Note 1)	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

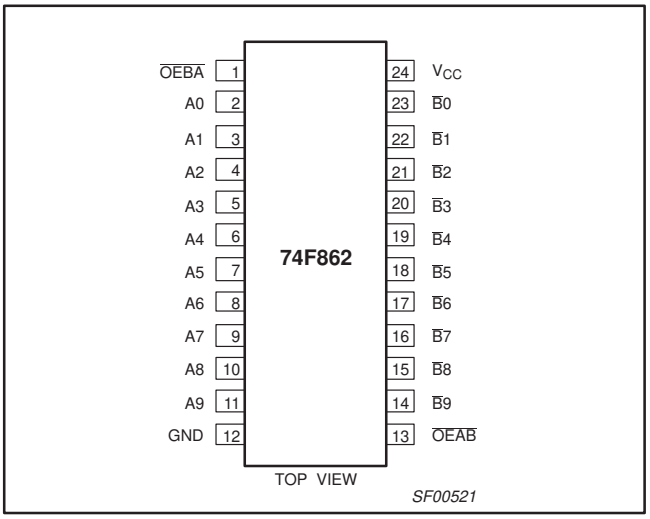
NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications for a discussion of thermal considerations for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

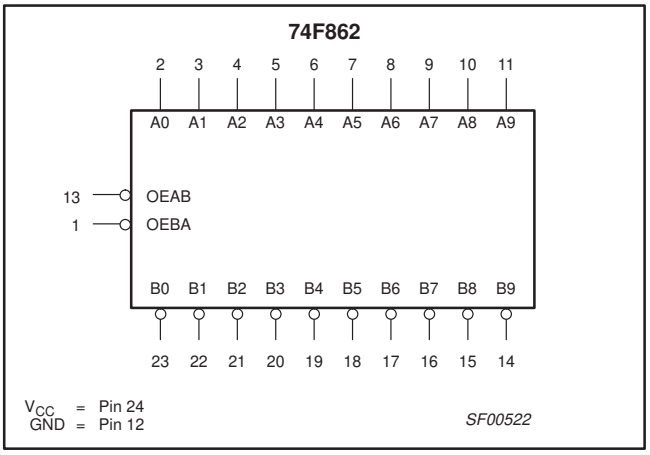
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A9	Data transmit inputs	1.0/0.033	20 μA / 20 μA
$\overline{B}0$ – $\overline{B}9$	Data receive inputs	1.0/0.033	20 μA / 20 μA
$\overline{OEBA}$	Transmit output enable input	1.0/0.033	20 μA / 20 μA
$\overline{OEAB}$	Receive output enable input	1.0/0.033	20 μA / 20 μA

NOTE: One (1.0) FAST Unit Load is defined as: 20 μA in the HiGH state and 0.6 mA in the LOW state.

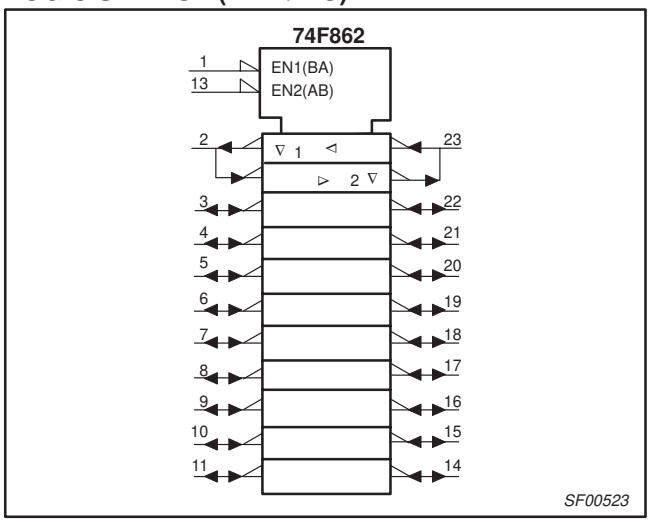
PIN CONFIGURATION



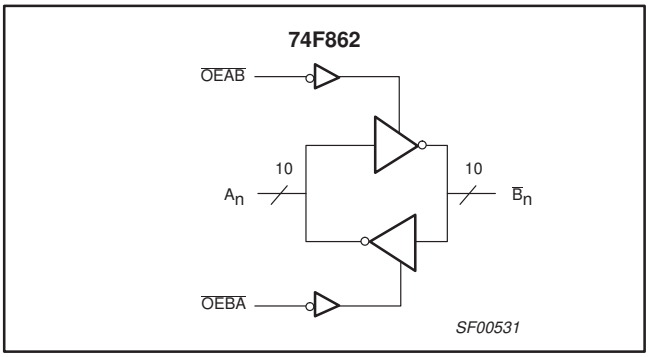
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OPERATING MODES
$\overline{OEAB}$	$\overline{OEBA}$	
L	H	A data to B bus, inverted
H	L	B bus to A data, inverted
H	H	Z

H = HIGH voltage level
L = LOW voltage level
Z = High impedance “off” state

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted, these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	–0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	128	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0	–	–	V
V_{IL}	LOW-level input voltage	–	–	0.8	V
I_{IK}	Input clamp current	–	–	–18	mA
I_{OH}	HIGH-level output current	–	–	–24	mA
I_{OL}	LOW-level output current	–	–	64	mA
T_{amb}	Operating free-air temperature range	0	–	70	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –1 mA	± 10% V_{CC}	2.4	–	–	V
					± 5% V_{CC}	2.4	3.3	–	V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –24 mA	± 10% V_{CC}	2.0	–	–	V
					± 5% V_{CC}	2.0	–	–	V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48 mA	± 10% V_{CC}	–	0.38	0.55	V
				I_{OL} = 64 mA	± 5% V_{CC}	–	0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–	–0.73	–1.2	V
I_I	Input current at maximum input voltage	$\overline{OEAB}$, $\overline{OEBA}$	V_{CC} = 0.0 V, V_I = 7.0 V			–	–	100	µA
		A_n, $\overline{B}_n$	V_{CC} = 5.5 V, V_I = 5.5 V			–	–	1	mA
I_{IH}	HIGH-level input current		V_{CC} = MAX, V_I = 2.7 V			–	–	20	µA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5 V			–	–	–20	µA
I_{IH} + I_{OZH}	Off-state output current HIGH-level voltage applied	A_n, $\overline{B}_n$	V_{CC} = MAX, V_O = 2.7 V			–	–	70	µA
I_{IL} + I_{OZL}	Off-state output current LOW-level voltage applied		V_{CC} = MAX, V_O = 0.5 V			–	–	–70	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			–100	–	–225	mA
I_{CC}	Supply current total	I_{CCH}	V_{CC} = MAX			–	90	130	mA
		I_{CCL}				–	120	170	mA
		I_{CCZ}				–	130	160	mA

NOTES:

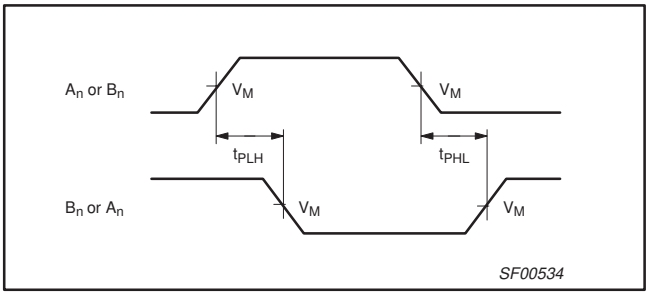
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

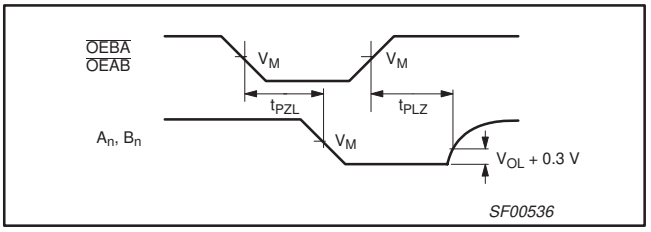
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25 °C V_{CC} = 5 V C_L = 50 pF; R_L = 500 Ω			T_{amb} = 0 °C to +70 °C V_{CC} = 5 V ± 10% C_L = 50 pF; R_L = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A_n or $\overline{B}_n$	Waveform 1	4.0 1.5	6.0 3.5	9.0 6.5	3.0 1.5	10.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ or A_n	Waveform 1	4.0 1.5	6.0 3.5	9.0 6.5	3.5 1.5	10.0 7.0	ns
t_{PZH} t_{PZL}	Output Enable time HIGH or LOW level $\overline{OEBA}$ to A_n	Waveform 2 Waveform 3	6.5 6.0	8.5 7.5	12.0 12.0	5.5 5.0	13.5 14.0	ns
t_{PZH} t_{PZL}	Output Enable time HIGH or LOW level $\overline{OEAB}$ to $\overline{B}_n$	Waveform 2 Waveform 3	6.5 6.0	8.5 7.5	12.0 12.0	5.5 5.0	13.5 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable time HIGH or LOW level $\overline{OEBA}$ to A_n	Waveform 2 Waveform 3	3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time HIGH or LOW level $\overline{OEAB}$ to $\overline{B}_n$	Waveform 2 Waveform 3	3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns

AC WAVEFORMS

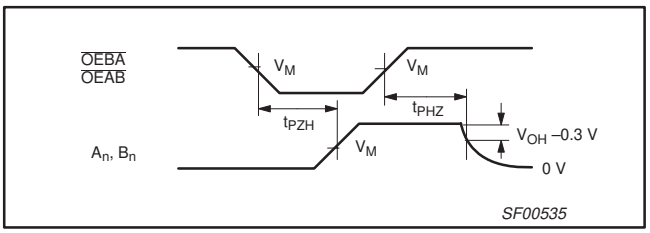
For all waveforms, V_M = 1.5 V.



Waveform 1. Propagation delay for inverting output

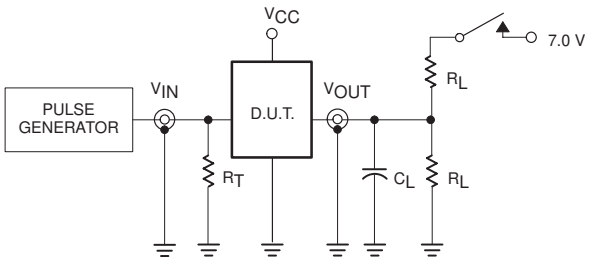


Waveform 3. 3-State Output Enable time to LOW level and Output Disable time from LOW level



Waveform 2. 3-State Output Enable time to HIGH level and Output Disable time from HIGH level

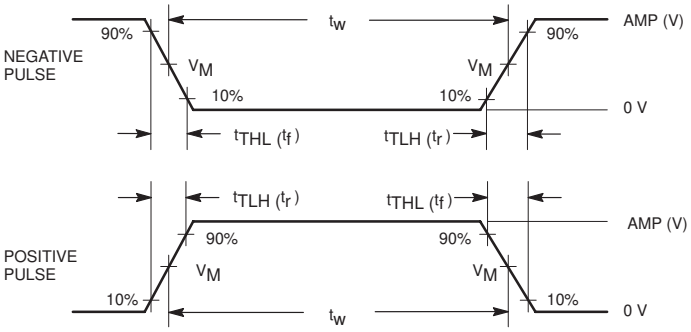
TEST CIRCUITS AND WAVEFORMS



Test Circuit for Open Collector Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open



Input Pulse Definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

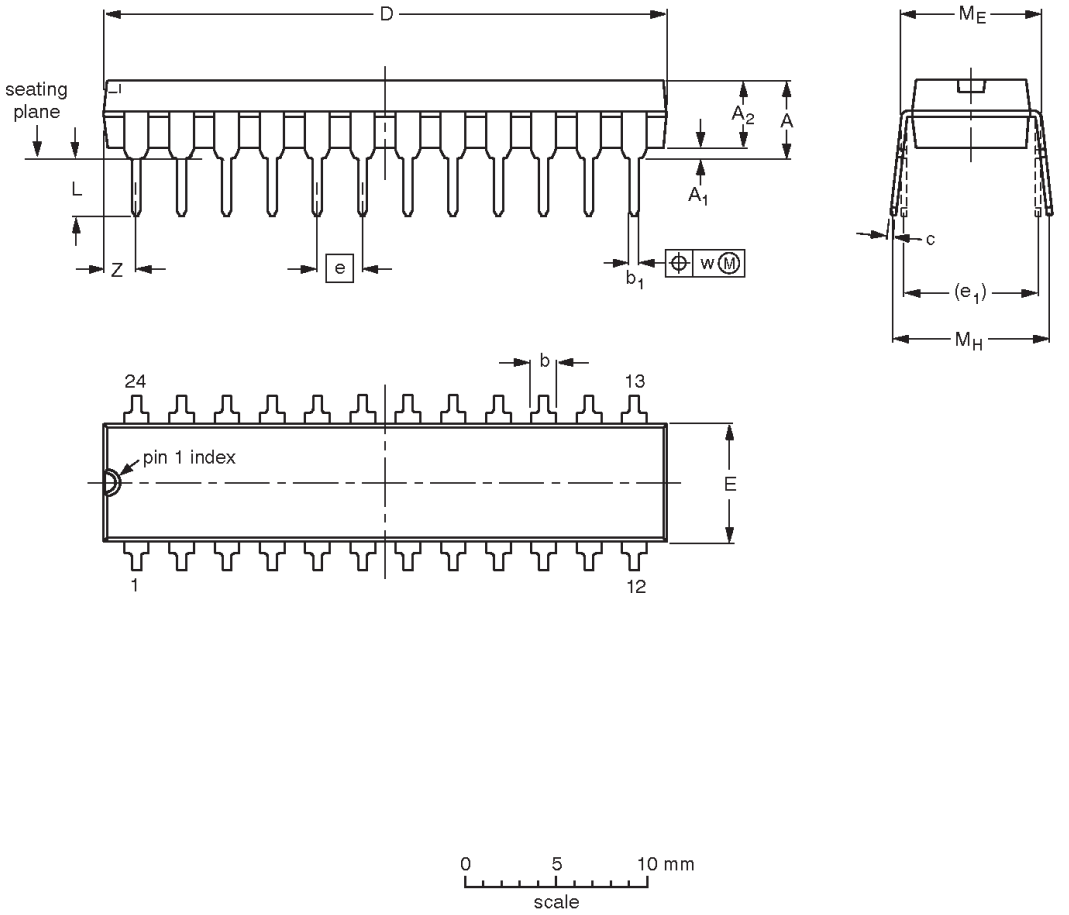
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0 V	1.5 V	1 MHz	500 ns	2.5 ns	2.5 ns

SF00128

DIP24: plastic dual in-line package; 24 leads (300 mil) **SOT222-1**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

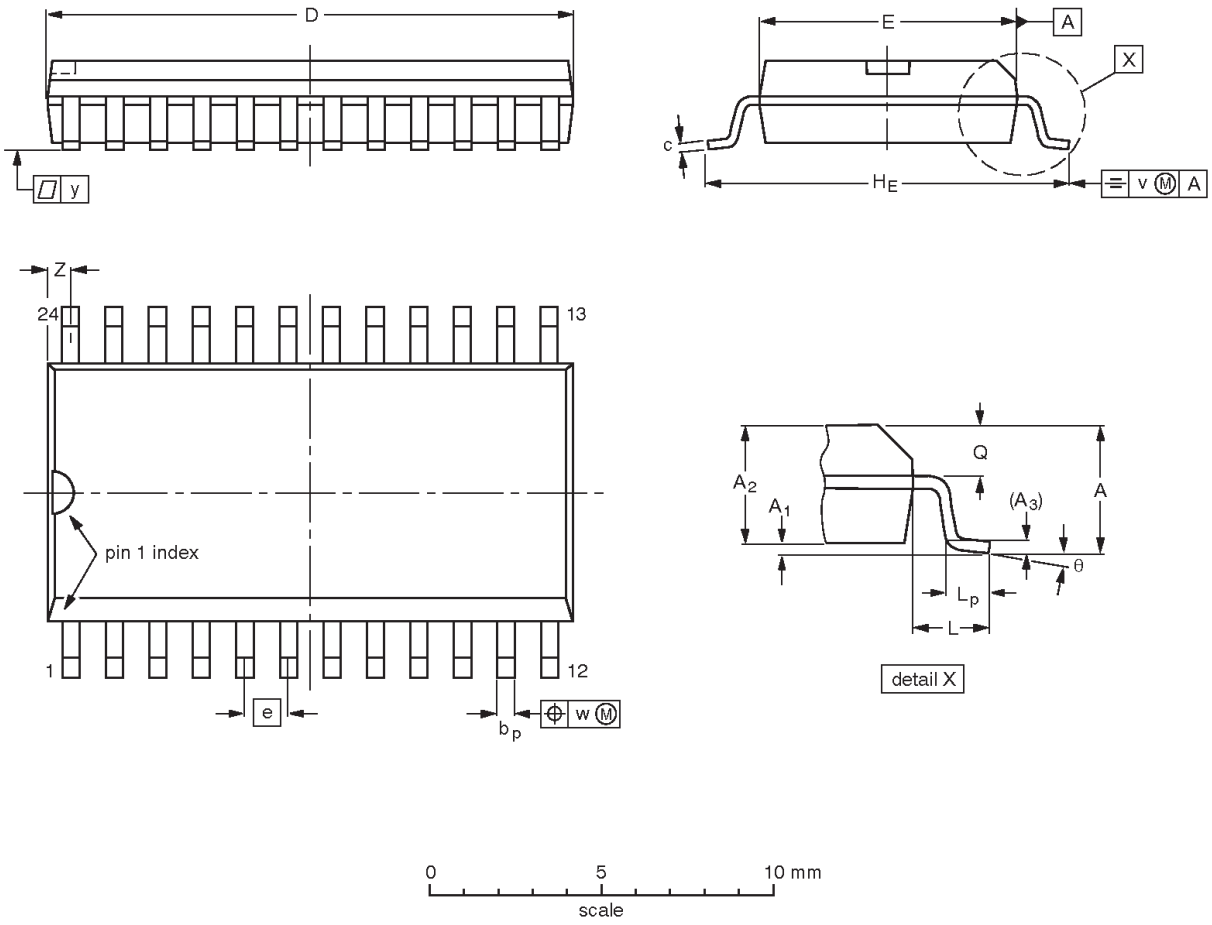
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.25	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.246	0.1	0.3	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT222-1		MS-001				~~99-12-27~~ 03-03-12

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

REVISION HISTORY

Rev	Date	Description
_5	20040123	**Product data (9397 750 12749). ECN 853-0881 A15378 of 22 January 2004. Replaces Product specification 74F862_74F863_4 dated 2000 Mar 24 (9397 750 06999).** Modifications: • Delete all references to 74F863 (product discontinued). • "Input and output loading and fan-out table" on page 2; for Pins A0 – A9 and $\overline{B}0$ – $\overline{B}9$: – change 74F(U.L.) HIGH/LOW from "3.5/0.117" to "1.0/0.033" – change Load value HIGH/LOW from "70 μA / 70 μA" to "20 μA / 20 μA" • "DC electrical characteristics" table on page 5; V_{OL} test condition, at ± 10% V_{CC}: change "I_{OL} = –48 mA" to "I_{OL} = 48 mA"
_4	20000324	**Product specification (9397 750 06999). ECN 853-0881 23378 of 24 March 2000. Supersedes data of 1999 Jan 08.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

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