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Nuvoton 1T 8051-based Microcontroller

N76E003

Datasheet

TABLE OF CONTENTS

1. GENERAL DESCRIPTION

The N76E003 is an embedded flash type, 8-bit high performance 1T 8051-based microcontroller. The instruction set is fully compatible with the standard 80C51 and performance enhanced.

The N76E003 contains a up to 18K Bytes of main Flash called APROM, in which the contents of User Code resides. The N76E003 Flash supports In-Application-Programming (IAP) function, which enables on-chip firmware updates. IAP also makes it possible to configure any block of User Code array to be used as non-volatile data storage, which is written by IAP and read by IAP or MOVC instruction. There is an additional Flash called LDROM, in which the Boot Code normally resides for carrying out In-System-Programming (ISP). The LDROM size is configurable with a maximum of 4K Bytes. To facilitate programming and verification, the Flash allows to be programmed and read electronically by parallel Writer or In-Circuit-Programming (ICP). Once the code is confirmed, user can lock the code for security.

The N76E003 provides rich peripherals including 256 Bytes of SRAM, 768 Bytes of auxiliary RAM (XRAM), Up to 18 general purpose I/O, two 16-bit Timers/Counters 0/1, one 16-bit Timer2 with three-channel input capture module, one Watchdog Timer (WDT), one Self Wake-up Timer (WKT), one 16-bit auto-reload Timer3 for general purpose or baud rate generator, two UARTs with frame error detection and automatic address recognition, one SPI, one I^2C, five enhanced PWM output channels, eight-channel shared pin interrupt for all I/O, and one 12-bit ADC. The peripherals are equipped with 18 sources with 4-level-priority interrupts capability.

The N76E003 is equipped with three clock sources and supports switching on-the-fly via software. The three clock sources include external clock input, 10 kHz internal oscillator, and one 16 MHz internal precise oscillator that is factory trimmed to ±1% at room temperature. The N76E003 provides additional power monitoring detection such as power-on reset and 4-level brown-out detection, which stabilizes the power-on/off sequence for a high reliability system design.

The N76E003 microcontroller operation consumes a very low power with two economic power modes to reduce power consumption — Idle and Power-down mode, which are software selectable. Idle mode turns off the CPU clock but allows continuing peripheral operation. Power-down mode stops the whole system clock for minimum power consumption. The system clock of the N76E003 can also be slowed down by software clock divider, which allows for a flexibility between execution performance and power consumption.

With high performance CPU core and rich well-designed peripherals, the N76E003 benefits to meet a general purpose, home appliances, or motor control system accomplishment.

2. FEATURES

- CPU:
  - Fully static design 8-bit high performance 1T 8051-based CMOS microcontroller.
  - Instruction set fully compatible with MCS-51.
  - 4-priority-level interrupts capability.
  - Dual Data Pointers (DPTRs).
- Operating:
  - Wide supply voltage from 2.4V to 5.5V.
  - Wide operating frequency up to 16 MHz.
  - Industrial temperature grade: -40℃ to +105℃.
- Memory:
  - Up to 18K Bytes of APROM for User Code.
  - Configurable 4K/3K/2K/1K/0K Bytes of LDROM, which provides flexibility to user developed Boot Code.
  - Flash Memory accumulated with pages of 128 Bytes each.
  - Built-in In-Application-Programmable (IAP).
  - Code lock for security.
  - 256 Bytes on-chip RAM.
  - Additional 768 Bytes on-chip auxiliary RAM (XRAM) accessed by MOVX instruction.
- Clock sources:
  - 16 MHz high-speed internal oscillator trimmed to ±1% when V_{DD} 5.0V, ±2% in all conditions.
  - 10 kHz low-speed internal oscillator.
  - External clock input.
  - On-the-fly clock source switch via software.
  - Programmable system clock divider up to 1/512.
- Peripherals:
  - Up to 17 general purpose I/O pins and one input-only pin. All output pins have individual 2-level slew rate control.
  - Standard interrupt pins $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$.

– Two 16-bit Timers/Counters 0 and 1 compatible with standard 8051.

– One 16-bit Timer 2 with three-channel input capture module and 9 input pin can be selected.

– One 16-bit auto-reload Timer 3, which can be the baud rate clock source of UARTs.

– One 16-bit PWM counter interrupt for timer.

– One programmable Watchdog Timer (WDT) clocked by dedicated 10 kHz internal source.

– One dedicated Self Wake-up Timer (WKT) for self-timed wake-up for power reduced modes.

– Two full-duplex UART ports with frame error detection and automatic address recognition. TXD and RXD pins of UART0 exchangeable via software.

– One SPI port with master and slave modes, up to 8 Mbps when system clock is 16 MHz.

– One I^2C bus with master and slave modes, up to 400 kbps data rate.

– Three pairs, six channels of pulse width modulator (PWM) output, 10 output pins can be selected., up to 16-bit resolution, with different modes and Fault Brake function for motor control.

– Eight channels of pin interrupt, shared for all I/O ports, with variable configuration of edge/level detection.

– One 12-bit ADC, up to 500 ksps converting rate, hardware triggered and conversion result compare facilitating motor control.

- Power management:

  – Two power reduced modes: Idle and Power-down mode.

- Power monitor:

  – Brown-out detection (BOD) with low power mode available, 4-level selection, interrupt or reset options.

  – Power-on reset (POR).

- Strong ESD and EFT immunity.

- Development Tools:

  – Nuvoton On-Chip-Debugger (OCD) with KEIL™ development environment.

  – Nuvoton In-Circuit-Programmer (ICP).

  – Nuvoton In-System-Programming (ISP) via UART.

- Part numbers and packages:

Part Number	APROM	LDROM	Package
N76E003AT20	18K Bytes shared with LDROM	Up to 4K Bytes	TSSOP 20
N76E003AQ20	18K Bytes shared with LDROM	Up to 4K Bytes	QFN 20
N76E003BQ20	18K Bytes shared with LDROM	Up to 4K Bytes	QFN 20

3. BLOCK DIAGRAM

Figure 3.1 shows the N76E003 functional block diagram and gives the outline of the device. User can find all the peripheral functions of the device in the diagram.

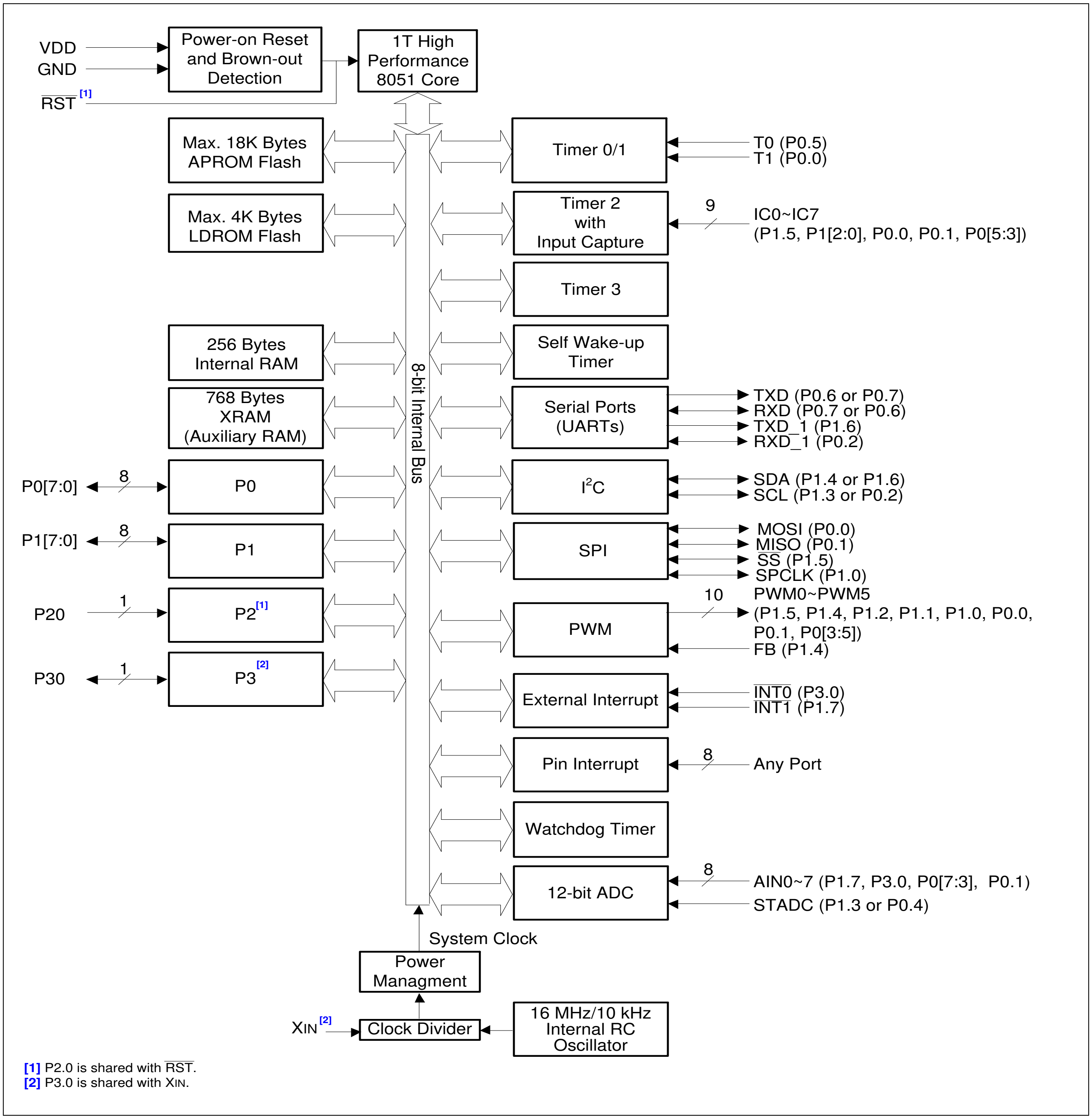
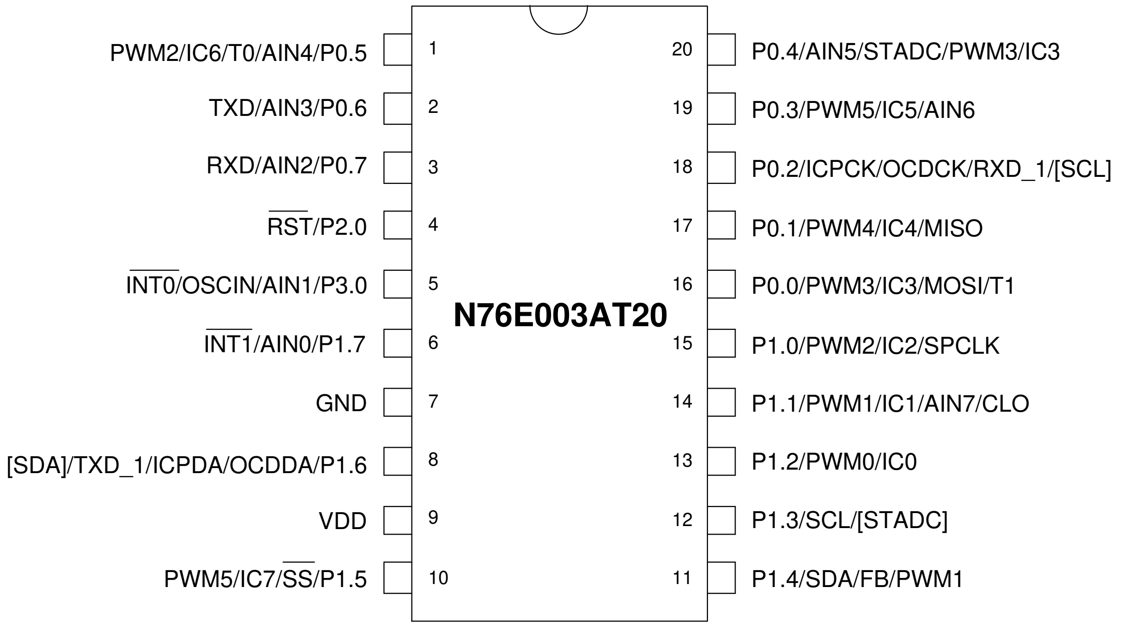


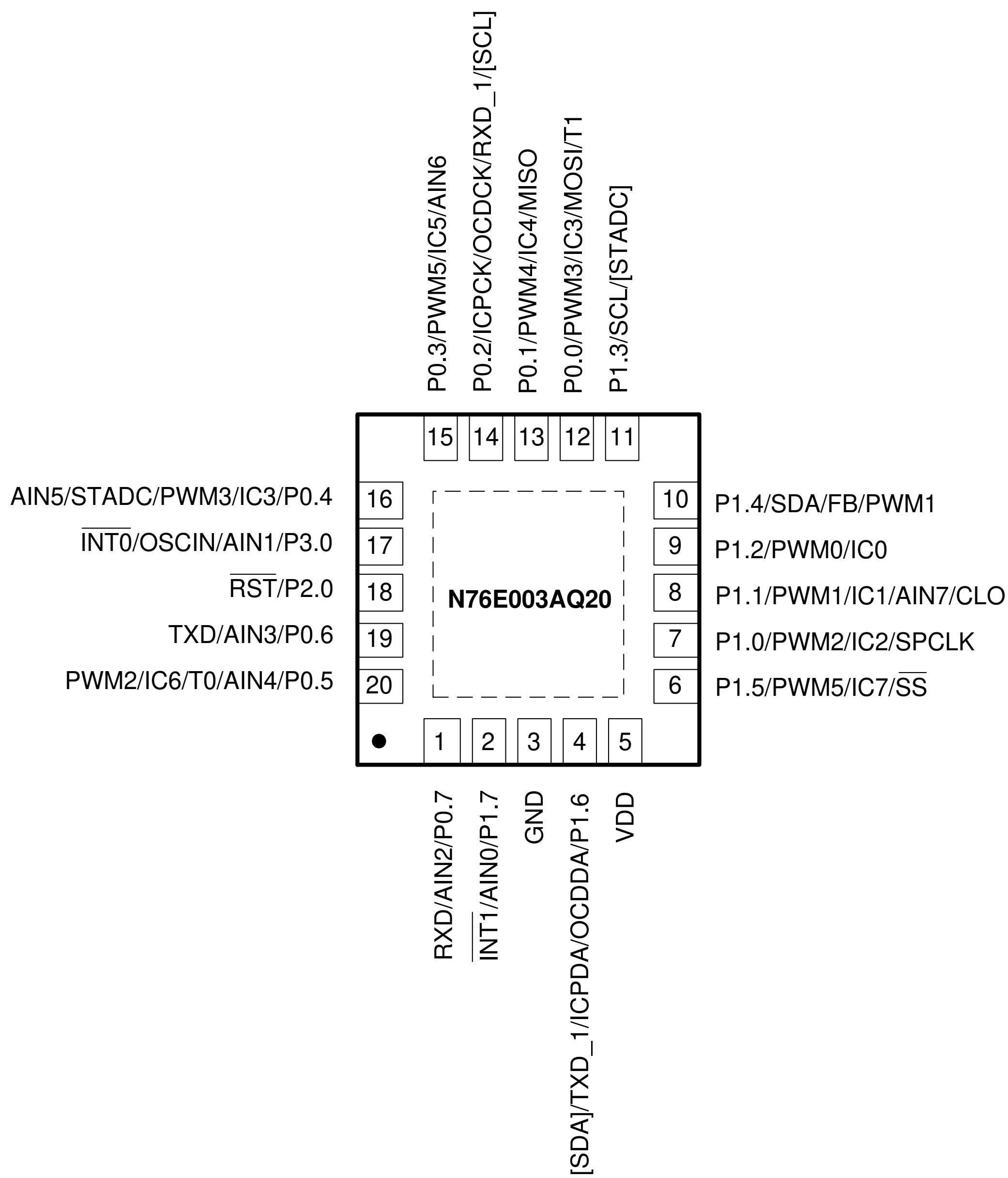
Figure 3.1. Functional Block Diagram

4. PIN CONFIGURATION



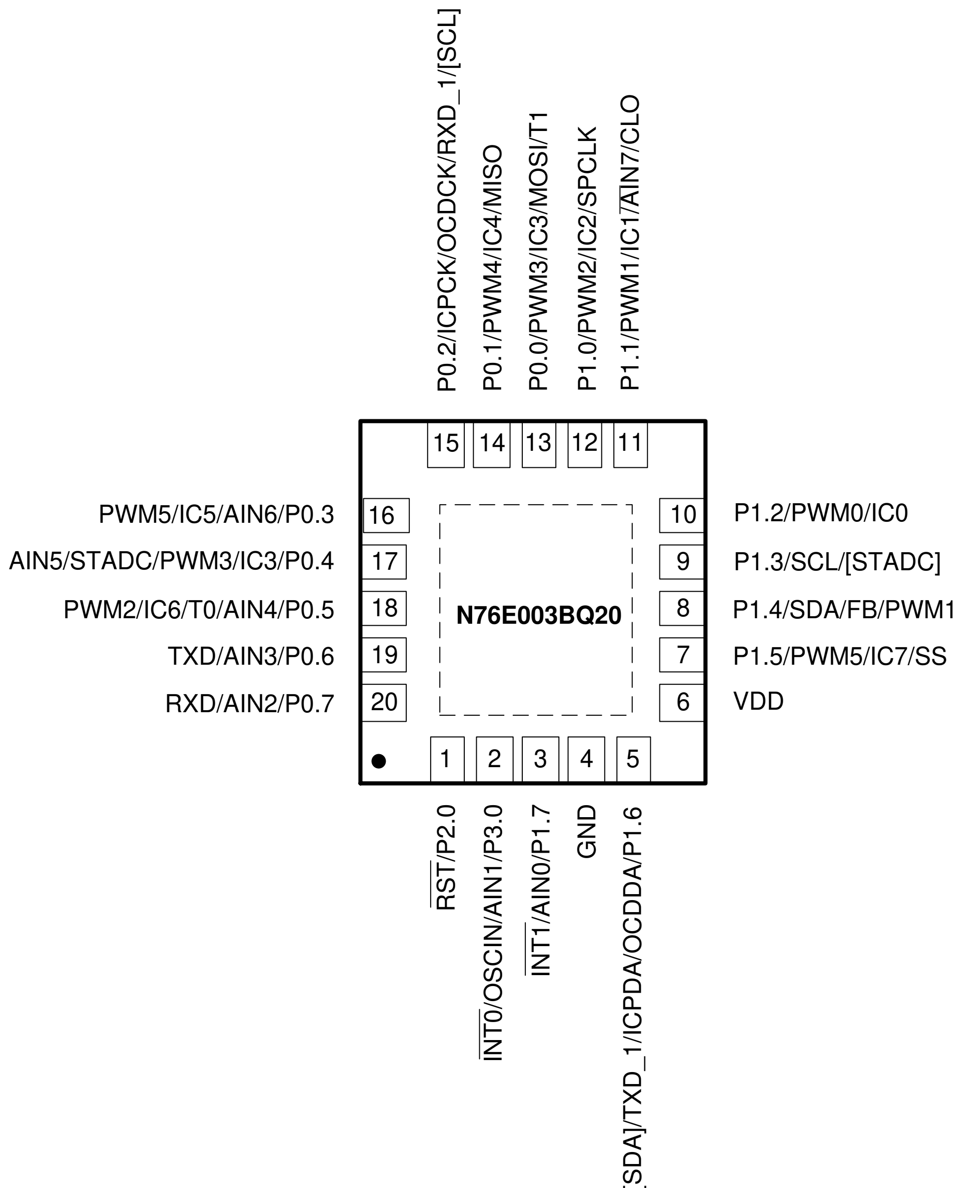
1. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Figure 4.1. Pin Assignment of TSSOP-20 Package



1. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Figure 4.2. Pin Assignment of QFN-20 Package for N76E003AQ20



1. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Figure 4.3. Pin Assignment of QFN-20 Package for N76E003BQ20

Pin Number			Symbol	Multi-Function Description[1]
N76E003AT20	N76E003AQ20	N76E003BQ20		
9	5	6	VDD	**POWER SUPPLY:** Supply voltage V_{DD} for operation.
7	3	4	GND	**GROUND:** Ground potential.
16	12	13	P0.0/PWM3/IC3/MOSI/T1	**P0.0:** Port 0 bit 0.
				PWM3: PWM output channel 3.
				MOSI: SPI master output/slave input.
				IC3: Input capture channel 3.
				T1: External count input to Timer/Counter 1 or its toggle output.
17	13	14	P0.1/PWM4/IC4/MISO	**P0.1:** Port 0 bit 1.
				PWM4: PWM output channel 4.
				IC4: Input capture channel 4.
				MISO: SPI master input/slave output.
18	14	15	P0.2/ICPCK/OCDCK/ RXD_1/[SCL]	**P0.2:** Port 0 bit 2.
				ICPCK: ICP clock input.
				OCDCK: OCD clock input.
				RXD_1: Serial port 1 receive input.
				[SCL] [3]: I^{2}C clock.
19	15	16	P0.3/PWM5/IC5/AIN6	**P0.3:** Port 0 bit 3.
				PWM5: PWM output channel
				IC5: Input capture channel 5.
				AIN6: ADC input channel 6.
20	16	17	P0.4/AIN5/STADC/ PWM3/IC3	**P0.4:** Port 0 bit 4.
				AIN5: ADC input channel 5.
				STADC: External start ADC trigger
				PWM3: PWM output channel 3.
				IC3: Input capture channel 3.
1	20	18	P0.5/PWM2/IC6/T0/AIN4	**P0.5:** Port 0 bit 5.
				PWM2: PWM output channel 2.
				IC6: Input capture channel 6.
				T0: External count input to Timer/Counter 0 or its toggle output.
2	19	19	P0.6/TXD/AIN3	**P0.6:** Port 0 bit 6.
				TXD[2]**:** Serial port 0 transmit data output.
				AIN3: ADC input channel 3.
3	1	20	P0.7/RXD/AIN2	**P0.7:** Port 0 bit 7.
				RXD: Serial port 0 receive input.
				AIN2: ADC input channel 2.
15	7	12	P1.0/PWM2/IC2/SPCLK	**P1.0:** Port 1 bit 0.
				PWM2: PWM output channel 2.
				IC2: Input capture channel 2.
				SPCLK: SPI clock.
14	8	11	P1.1/PWM1/IC1/AIN7/ CLO	**P1.1:** Port 1 bit 1
				PWM1: PWM output channel 1.
				IC1: Input capture channel 1.
				AIN7: ADC input channel 7.
				CLO: System clock output.
13	9	10	P1.2/PWM0/IC0	**P1.2:** Port 1 bit 2.
				PWM0: PWM output channel 0.

Pin Number			Symbol	Multi-Function Description[1]
N76E003AT20	N76E003AQ20	N76E003BQ20		
				IC0: Input capture channel 0.
12	11	9	P1.3/SCL/[STADC]	**P1.3:** Port 1 bit 3.
				SCL: I^{2}C clock.
				[STADC] [4]**:** External start ADC trigger
11	10	8	P1.4/SDA/FB/PWM1	**P1.4:** Port 1 bit 4.
				SDA: I^{2}C data.
				FB: Fault Brake input.
				PWM1: PWM output channel 1.
10	6	7	P1.5/PWM5/IC7/$\overline{SS}$	**P1.5:** Port 1 bit 5.
				PWM5: PWM output channel 5.
				IC7: Input capture channel 7.
				$\overline{SS}$: SPI slave select input.
8	4	5	P1.6/ICPDA/OCDDA/ TXD_1/[SDA]	**P1.6:** Port 1 bit 6.
				ICPDA: ICP data input or output.
				OCDAT: OCD data input or output.
				TXD_1: Serial port 1 transmit data output.
				[SDA] [3]**:** I^{2}C data.
6	2	3	P1.7/$\overline{INT1}$/AIN0	**P1.7:** Port 1 bit 7.
				$\overline{INT1}$: External interrupt 1 input.
				AIN0: ADC input channel 0.
4	18	1	P2.0/$\overline{RST}$	**P2.0:** Port 2 bit 0 input pin available when RPD (CONFIG0.2) is programmed as 0.
				$\overline{RST}$: $\overline{RST}$ pin is a Schmitt trigger input pin for hardware device reset. A low on this pin resets the device. $\overline{RST}$ pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
5	17	12	P3.0/$\overline{INT0}$/OSCIN/AIN1	**P3.0:** Port 3 bit 0 available when the internal oscillator is used as the system clock.
				$\overline{INT0}$: External interrupt 0 input.
				XIN: If the ECLK mode is enabled, XIN is the external clock input pin.
				AIN1: ADC input channel 1.

[1] All I/O pins can be configured as a interrupt pin. This feature is not listed in multi-function description. See Section 16. "Pin Interrupt".
[2] TXD and RXD pins of UART0 are software exchangeable by UART0PX (AUXR1.2).
[3] [I2C] alternate function remapping option. I2C pins is software switched by I2CPX (I2CON.0).
[4] [STADC] alternate function remapping option. STADC pin is software switched by STADCPX(ADCCON1.6).
[5] PIOx register decides which pins are PWM or GPIO.

5. MEMORY ORGANIZATION

A standard 80C51 based microcontroller divides the memory into two different sections, Program Memory and Data Memory. The Program Memory is used to store the instruction codes, whereas the Data Memory is used to store data or variations during the program execution.

The Data Memory occupies a separate address space from Program Memory. In N76E003, there are 256 Bytes of internal scratch-pad RAM. For many applications those need more internal RAM, the N76E003 provides another on-chip 768 Bytes of RAM, which is called XRAM, accessed by MOVX instruction.

The whole embedded flash, functioning as Program Memory, is divided into three blocks: Application ROM (APROM) normally for User Code, Loader ROM (LDROM) normally for Boot Code, and CONFIG bytes for hardware initialization. Actually, APROM and LDROM function in the same way but have different size. Each block is accumulated page by page and the page size is 128 Bytes. The flash control unit supports Erase, Program, and Read modes. The external writer tools though specific I/O pins, In-Application-Programming (IAP), or In-System-Programming (ISP) can both perform these modes.

5.1 Program Memory

The Program Memory stores the program codes to execute as shown in Figure 5.1. After any reset, the CPU begins execution from location 0000H.

To service the interrupts, the interrupt service locations (called interrupt vectors) should be located in the Program Memory. Each interrupt is assigned with a fixed location in the Program Memory. The interrupt causes the CPU to jump to that location with where it commences execution of the interrupt service routine (ISR). External Interrupt 0, for example, is assigned to location 0003H. If External Interrupt 0 is going to be used, its service routine should begin at location 0003H. If the interrupt is not going to be used, its service location is available as general purpose Program Memory.

The interrupt service locations are spaced at an interval of eight Bytes: 0003H for External Interrupt 0, 000BH for Timer 0, 0013H for External Interrupt 1, 001BH for Timer 1, etc. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within the 8-Byte interval. However longer service routines should use a JMP instruction to skip over subsequent interrupt locations if other interrupts are in use.

The N76E003 provides two internal Program Memory blocks APROM and LDROM. Although they both behave the same as the standard 8051 Program Memory, they play different rules according to their ROM size. The

APROM on N76E003 can be up to 18K Bytes. User Code is normally put inside. CPU fetches instructions here for execution. The MOVC instruction can also read this region.

The other individual Program Memory block is called LDROM. The normal function of LDROM is to store the Boot Code for ISP. It can update APROM space and CONFIG bytes. The code in APROM can also re-program LDROM. For ISP details and configuration bit setting related with APROM and LDROM, see Section 21.4 "In-System-Programming (ISP)" on page 225. Note that APROM and LDROM are hardware individual blocks, consequently if CPU re-boots from LDROM, CPU will automatically re-vector Program Counter 0000H to the LDROM start address. Therefore, CPU accounts the LDROM as an independent Program Memory and all interrupt vectors are independent from APROM.

CONFIG1

7	6	5	4	3	2	1	0
-	-	-	-	-	LDSIZE[2:0]		
-	-	-	-	-	R/W		

Factory default value: 1111 1111b

Bit	Name	Description
2:0	LDSIZE[2:0]	**LDROM size select** This field selects the size of LDROM. 111 = No LDROM. APROM is 18K Bytes. 110 = LDROM is 1K Bytes. APROM is 17K Bytes. 101 = LDROM is 2K Bytes. APROM is 16K Bytes. 100 = LDROM is 3K Bytes. APROM is 15K Bytes. 0xx = LDROM is 4K Bytes. APROM is 14K Bytes.

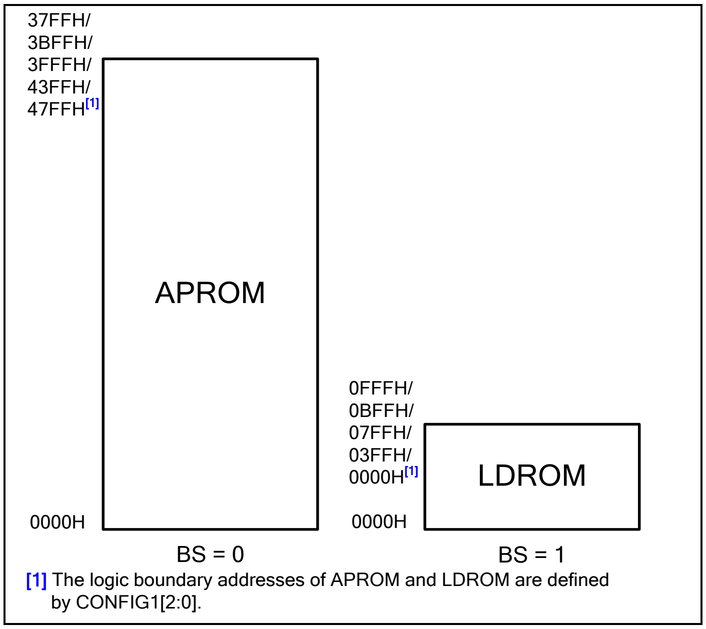


Figure 5.1. N76E003 Program Memory Map

5.2 Data Memory

Figure 5.2 shows the internal Data Memory spaces available on N76E003. Internal Data Memory occupies a separate address space from Program Memory. The internal Data Memory can be divided into three blocks. They are the lower 128 Bytes of RAM, the upper 128 Bytes of RAM, and the 128 Bytes of SFR space. Internal Data Memory addresses are always 8-bit wide, which implies an address space of only 256 Bytes. Direct addressing higher than 7FH will access the special function registers (SFRs) space and indirect addressing higher than 7FH will access the upper 128 Bytes of RAM. Although the SFR space and the upper 128 Bytes of RAM share the same logic address, 80H through FFH, actually they are physically separate entities. Direct addressing to distinguish with the higher 128 Bytes of RAM can only access these SFRs. Sixteen addresses in SFR space are either byte-addressable or bit-addressable. The bit-addressable SFRs are those whose addresses end in 0H or 8H.

The lower 128 Bytes of internal RAM are present in all 80C51 devices. The lowest 32 Bytes as general purpose registers are grouped into 4 banks of 8 registers. Program instructions call these registers as R0 to R7. Two bits RS0 and RS1 in the Program Status Word (PSW[3:4]) select which Register Bank is used. It benefits more efficiency of code space, since register instructions are shorter than instructions that use direct addressing. The next 16 Bytes above the general purpose registers (byte-address 20H through 2FH) form a block of bit-addressable memory space (bit-address 00H through 7FH). The 80C51 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

Either direct or indirect addressing can access the lower 128 Bytes space. But the upper 128 Bytes can only be accessed by indirect addressing.

Another application implemented with the whole block of internal 256 Bytes RAM is used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a JMP, CALL or interrupt is invoked, the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07H at reset. User can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

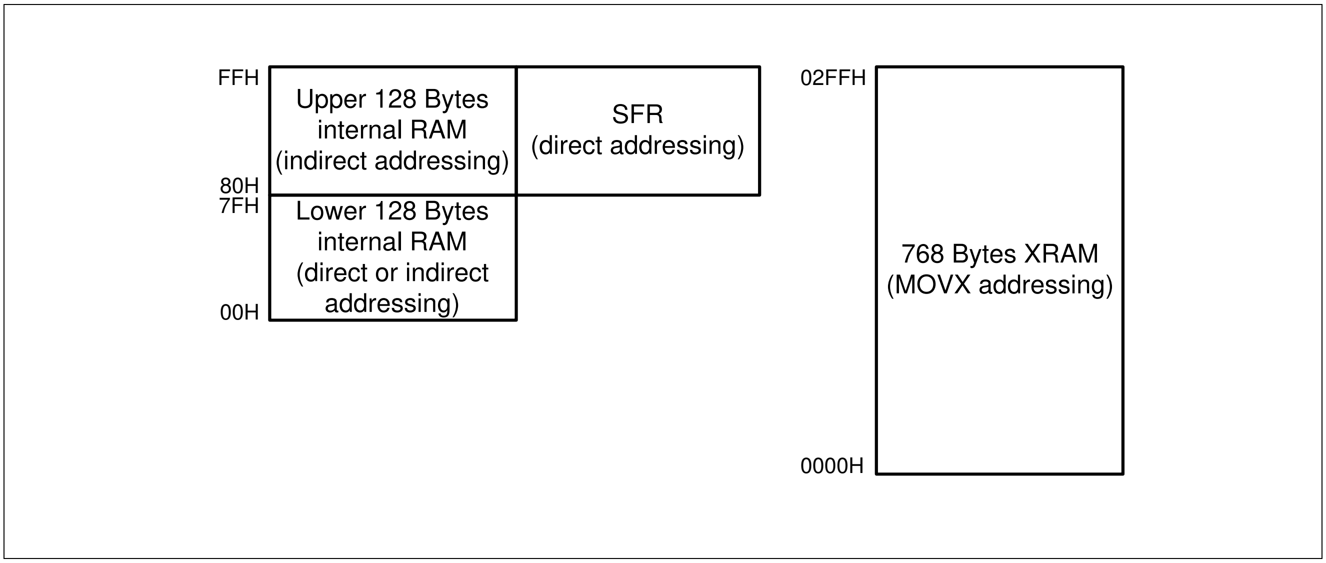


Figure 5.2. Data Memory Map

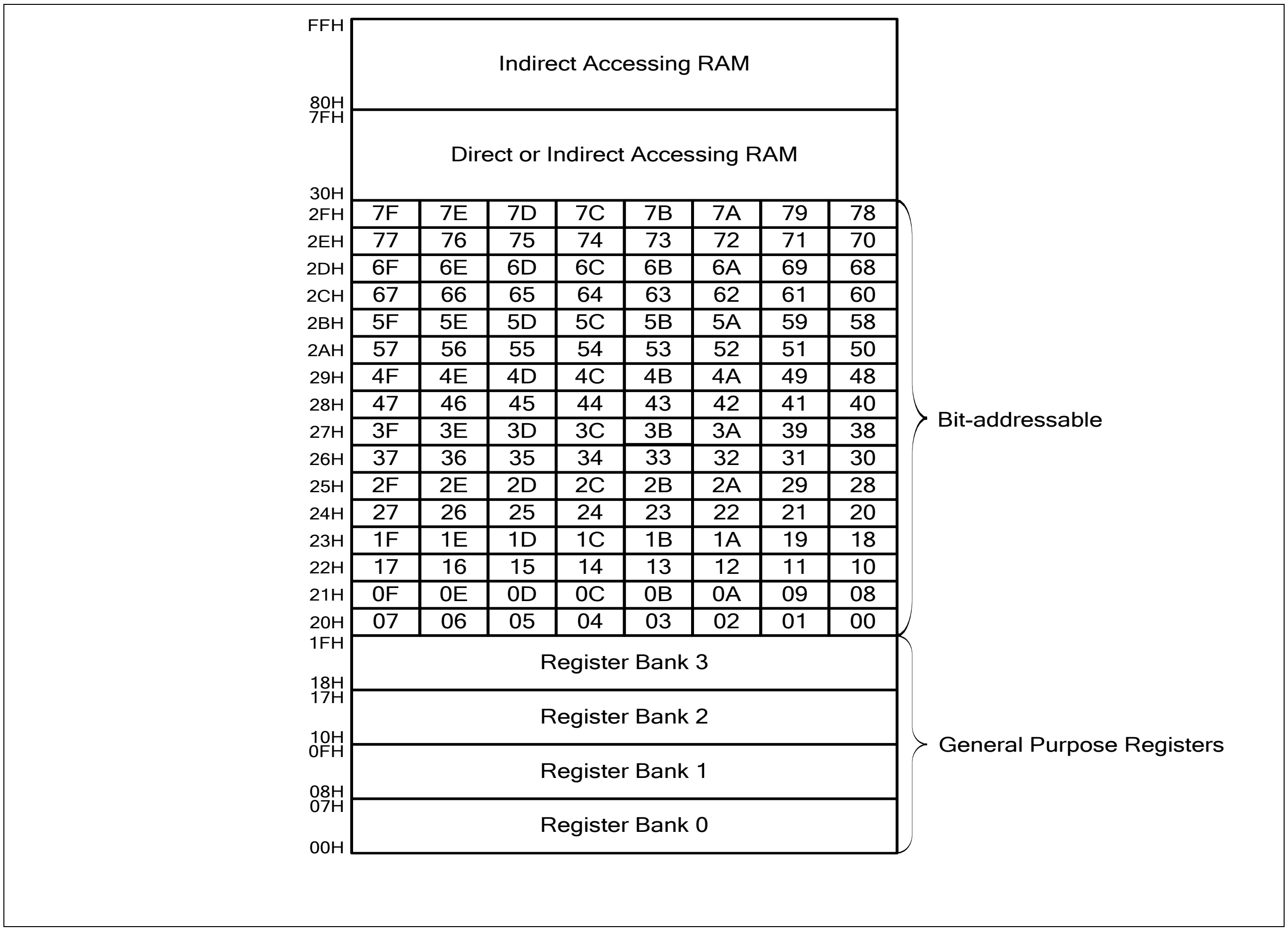


Figure 5.3. Internal 256 Bytes RAM Addressing

5.3 On-Chip XRAM

The N76E003 provides additional on-chip 768 bytes auxiliary RAM called XRAM to enlarge the RAM space. It occupies the address space from 00H through 2FFH. The 768 bytes of XRAM are indirectly accessed by move external instruction MOVX @DPTR or MOVX @Ri. (See the demo code below.) Note that the stack pointer cannot be located in any part of XRAM.

XRAM demo code:

```
MOV     R0,#23H             ;write #5AH to XRAM with address @23H
MOV     A,#5AH
MOVX    @R0,A
MOV     R1,#23H             ;read from XRAM with address @23H
MOVX    A,@R1
MOV     DPTR,#0023H         ;write #5BH to XRAM with address @0023H
MOV     A,#5BH
MOVX    @DPTR,A
MOV     DPTR,#0023H         ;read from XRAM with address @0023H
MOVX    A,@DPTR
```

5.4 Non-Volatile Data Storage

By applying IAP, any page of APROM or LDROM can be used as non-volatile data storage. For IAP details, please see Section 21. “In-Application-Programming (IAP)” on page 219.

6. SPECIAL FUNCTION REGISTER (SFR)

The N76E003 uses Special Function Registers (SFRs) to control and monitor peripherals and their modes. The SFRs reside in the register locations 80 to FFH and are accessed by direct addressing only. SFRs those end their addresses as 0H or 8H are bit-addressable. It is very useful in cases where user would like to modify a particular bit directly without changing other bits via bit-field instructions. All other SFRs are byte-addressable only. The N76E003 contains all the SFRs presenting in the standard 8051. However some additional SFRs are built in. Therefore, some of unused bytes in the original 8051 have been given new functions. The SFRs are listed below.

To accommodate more than 128 SFRs in the 0x80 to 0xFF address space, SFR paging has been implemented. By default, all SFR accesses target SFR page 0. During device initialization, some SFRs located on SFR page 1 may need to be accessed. The register SFRS is used to switch SFR addressing page. Note that this register has TA write protection. Most of SFRs are available on both SFR page 0 and 1.

SFRS – SFR Page Selection (TA protected)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	SFRPAGE
-	-	-	-	-	-	-	R/W

Address: 91H Reset value: 0000 0000b

Bit	Name	Description
0	SFRPAGE	**SFR page select** 0 = Instructions access SFR page 0. 1 = Instructions access SFR page 1.

Switch SFR page demo code:

```
MOV     TA,#0AAH            ;switch to SFR page 1
MOV     TA,#55H
ORL     SFRS,#01H

MOV     TA,#0AAH            ;switch to SFR page 0
MOV     TA,#55H
ANL     SFRS,#0FEH
```

Table 6-1. SFR Memory Map

SFR Page	Addr	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0 1	F8	**SCON_1**	PDTEN	PDTCNT	PMEN	PMD	PORDIS -	EIP1 -	EIPH1 -
0 1	F0	**B**	CAPCON3	CAPCON4	SPCR SPCR2	SPSR	SPDR -	AINDIDS -	EIPH -
0 1	E8	**ADCCON0**	PICON	PINEN	PIPEN	PIF	C2L	C2H	EIP -
0 1	E0	**ACC**	ADCCON1	ADCCON2	ADCDLY	C0L	C0H	C1L	C1H
0 1	D8	**PWMCON0**	PWMPL	PWM0L	PWM1L	PWM2L	PWM3L	PIOCON0	PWMCON1
0 1	D0	**PSW**	PWMPH	PWM0H	PWM1H	PWM2H	PWM3H	PNP	FBD
0 1	C8	**T2CON**	T2MOD	RCMP2L	RCMP2H	TL2 PWM4L	TH2 PWM5L	ADCMPL	ADCMPH
0 1	C0	**I2CON**	I2ADDR	ADCRL	ADCRH	T3CON PWM4H	RL3 PWM5H	RH3 PIOCON1	TA
0 1	B8	**IP**	SADEN	SADEN_1	SADDR_1	I2DAT	I2STAT	I2CLK	I2TOC
0 1	B0	**P3**	P0M1 P0S	P0M2 P0SR	P1M1 P1S	P1M2 P1SR	P2S	-	IPH PWMINTC
0 1	A8	**IE**	SADDR	WDCON	BODCON1	P3M1 P3S	P3M2 P3SR	IAPFD	IAPCN
0 1	A0	**P2**	-	AUXR1	BODCON0	IAPTRG	IAPUEN	IAPAL	IAPAH
0 1	98	**SCON**	SBUF	SBUF_1	EIE	EIE1	-	-	CHPCON
0 1	90	**P1**	SFRS	CAPCON0	CAPCON1	CAPCON2	CKDIV	CKSWT	CKEN
0 1	88	**TCON**	TMOD	TL0	TL1	TH0	TH1	CKCON	WKCON
0 1	80	**P0**	SP	DPL	DPH	RCTRIM0	RCTRIM1	RWK	PCON

Unoccupied addresses in the SFR space marked in "-" are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided.

Table 6-2. SFR Definitions and Reset Values

Symbol	Definition	Address /(Page)	MSB							LSB[1]	Reset Value[2]
EIPH1	Extensive interrupt priority high 1	FFH/(0)	-	-	-	-	-	PWKTH	PT3H	PSH_1	0000 0000b
EIP1	Extensive interrupt priority 1	FEH/(0)	-	-	-	-	-	PWKT	PT3	PS_1	0000 0000b
PMD	PWM mask data	FCH	-	-	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0	0000 0000b
PMEN	PWM mask enable	FBH	-	-	PMEN5	PMEN4	PMEN3	PMEN2	PMEN1	PMEN0	0000 0000b
PDTCNT[4]	PWM dead-time counter	FAH	PDTCNT[7:0]								0000 0000b
PDTEN[4]	PWM dead-time enable	F9H	-	-	-	PDTCNT.8	-	PDT45EN	PDT23EN	PDT01EN	0000 0000b
SCON_1	Serial port 1 control	F8H	(FF) SM0_1/ FE_1	(FE) SM1_1	(FD) SM2_1	(FC) REN_1	(FB) TB8_1	(FA) RB8_1	(F9) TI_1	(F8) RI_1	0000 0000b
EIPH	Extensive interrupt priority high	F7H	PT2H	PSPIH	PFBH	PWDTH	PPWMH	PCAPH	PPIH	PI2CH	0000 0000b
AINDIDS	ADC channel digital input disable	F6H	P11DIDS	P03DIDS	P04DIDS	P05DIDS	P06DIDS	P07DIDS	P30DIDS	P17DIDS	0000 0000b
SPDR	SPI data	F5H(0)	SPDR[7:0]								0000 0000b
SPSR	SPI status	F4H	SPIF	WCOL	SPIOVF	MODF	DISMODF	TXBUF	-	-	0000 0000b
SPCR	SPI control	F3H(0)	SSOE	SPIEN	LSBFE	MSTR	CPOL	CPHA	SPR[1:0]		0000 0000b
SPCR2	SPI control 2	F3H(1)	-	-	-	-	-	-	SPIS[1:0]		0000 0000b
CAPCON4	Input capture control 4	F2H	-	-	-	-	CAP23	CAP22	CAP21	CAP20	0000 0000b
CAPCON3	Input capture control 3	F1H	CAP13	CAP12	CAP11	CAP10	CAP03	CAP02	CAP01	CAP00	0000 0000b
B	B register	F0H	(F7) B.7	(F6) B.6	(F5) B.5	(F4) B.4	(F3) B.3	(F2) B.2	(F1) B.1	(F0) B.0	0000 0000b
EIP	Extensive interrupt priority	EFH	PT2	PSPI	PFB	PWDT	PPWM	PCAP	PPI	PI2C	0000 0000b
C2H	Input capture 2 high byte	EEH	C2H[7:0]								0000 0000b
C2L	Input capture 2 low byte	EDH	C2L[7:0]								0000 0000b
PIF	Pin interrupt flag	ECH	PIF7	PIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	0000 0000b
PIPEN	Pin interrupt high level/rising edge enable	EBH	PIPEN7	PIPEN6	PIPEN5	PIPEN4	PIPEN3	PIPEN2	PIPEN1	PIPEN0	0000 0000b
PINEN	Pin interrupt low level/falling edge enable	EAH	PINEN7	PINEN6	PINEN5	PINEN4	PINEN3	PINEN2	PINEN1	PINEN0	0000 0000b
PICON	Pin interrupt control	E9H	PIT67	PIT45	PIT3	PIT2	PIT1	PIT0	PIPS[1:0]		0000 0000b
ADCCON0	ADC control 0	E8H	(EF) ADCF	(EE) ADCS	(ED) ETGSEL1	(EC) ETGSEL0	(EB) ADCHS3	(EA) ADCHS2	(E9) ADCHS1	(E8) ADCHS0	0000 0000b
C1H	Input capture 1 high byte	E7H	C1H[7:0]								0000 0000b
C1L	Input capture 1 low byte	E6H	C1L[7:0]								0000 0000b
C0H	Input capture 0 high byte	E5H	C0H[7:0]								0000 0000b
C0L	Input capture 0 low byte	E4H	C0L[7:0]								0000 0000b
ADCDLY	ADC trigger delay	E3H	ADCDLY[7:0]								0000 0000b
ADCCON2	ADC control 2	E2H	ADFBEN	ADCMPOP	ADCMPEN	ADCMPO	-	-	-	ADCDLY.8	0000 0000b
ADCCON1	ADC control 1	E1H	-	STADCPX	-	-	ETGTYP[1:0]		ADCEX	ADCEN	0000 0000b
ACC	Accumulator	E0H	(E7) ACC.7	(E6) ACC.6	(E5) ACC.5	(E4) ACC.4	(E3) ACC.3	(E2) ACC.2	(E1) ACC.1	(E0) ACC.0	0000 0000b
PWMCON1	PWM control 1	DFH	PWMMOD[1:0]		GP	PWMTYP	FBINEN	PWMDIV[2:0]			0000 0000b
PIOCON0	PWM I/O switch 0	DEH	-	-	PIO05	PIO04	PIO03	PIO02	PIO01	PIO00	0000 0000b
PWM3L	PWM3 duty low byte	DDH	PWM3[7:0]								0000 0000b
PWM2L	PWM2 duty low byte	DCH	PWM2[7:0]								0000 0000b
PWM1L	PWM1 duty low byte	DBH	PWM1[7:0]								0000 0000b
PWM0L	PWM0 duty low byte	DAH	PWM0[7:0]								0000 0000b
PWMPL	PWM period low byte	D9H	PWMP[7:0]								0000 0000b
PWMCON0	PWM control 0	D8H	(DF) PWMRUN	(DE) LOAD	(DD) PWMF	(DC) CLRPWM	(DB) -	(DA) -	(D9) -	(D8) -	0000 0000b
FBD	Brake data	D7H	FBF	FBINLS	FBD5	FBD4	FBD3	FBD2	FBD1	FBD0	0000 0000b
PNP	PWM negative polarity	D6H	-	-	PNP5	PNP4	PNP3	PNP2	PNP1	PNP0	0000 0000b
PWM3H	PWM3 duty high byte	D5H	PWM3[15:8]								0000 0000b
PWM2H	PWM2 duty high byte	D4H	PWM2[15:8]								0000 0000b
PWM1H	PWM1 duty high byte	D3H	PWM1[15:8]								0000 0000b
PWM0H	PWM0 duty high byte	D2H	PWM0[15:8]								0000 0000b
PWMPH	PWM period high byte	D1H	PWMP[15:8]								0000 0000b
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) -	(D0) P	0000 0000b
ADCMPH	ADC compare high byte	CFH	ADCMP[11:4]								0000 0000b
ADCMPL	ADC compare low byte	CEH	-	-	-	-	ADCMP[3:0]				0000 0000b
PWM5L	PWM5 duty low byte	CDH(1)	PWM5[7:0]								0000 0000b

Table 6-2. SFR Definitions and Reset Values

Symbol	Definition	Address /(Page)	MSB							LSB[1]	Reset Value[2]
TH2	Timer 2 high byte	CDH(0)	TH2[7:0]								0000 0000b
PWM4L	PWM4 duty low byte	CCH(1)	PWM4[7:0]								0000 0000b
TL2	Timer 2 low byte	CCH(0)	TL2[7:0]								0000 0000b
RCMP2H	Timer 2 compare high byte	CBH	RCMP2H[7:0]								0000 0000b
RCMP2L	Timer 2 compare low byte	CAH(0)	RCMP2L[7:0]								0000 0000b
T2MOD	Timer 2 mode	C9H	LDEN	T2DIV[2:0]			CAPCR	CMPCR	LDTS[1:0]		0000 0000b
T2CON	Timer 2 control	C8H	(CF) TF2	(CE) -	(CD) -	(CC) -	(CB) -	(CA) TR2	(C9) -	(C8) CM/RL2	0000 0000b
TA	Timed access protection	C7H	TA[7:0]								0000 0000b
PIOCON1	PWM I/O switch 1	C6H(1)	-	-	PIO15	-	PIO13	PIO12	PIO11	-	0000 0000b
RH3	Timer 3 reload high byte	C6H(0)	RH3[7:0]								0000 0000b
PWM5H	PWM5 duty high byte	C5H(1)	PWM5[15:8]								0000 0000b
RL3	Timer 3 reload low byte	C5H(0)	RL3[7:0]								0000 0000b
PWM4H	PWM4 duty high byte	C4H(1)	PWM4[15:8]								0000 0000b
T3CON	Timer 3 control	C4H(0)	SMOD_1	SMOD0_1	BRCK	TF3	TR3	T3PS[2:0]			0000 0000b
ADCRH	ADC result high byte	C3H	ADCR[11:4]								0000 0000b
ADCRL	ADC result low byte	C2H	-	-	-	-	ADCR[3:0]				0000 0000b
I2ADDR	I^2C own slave address	C1H	I2ADDR[7:1]							GC	0000 0000b
I2CON	I^2C control	C0H	(C7) -	(C6) I2CEN	(C4) STA	(C4) STO	(C3) SI	(C2) AA	(C1) -	(C0) I2CPX	0000 0000b
I2TOC	I^2C time-out counter	BFH	-	-	-	-	-	I2TOCEN	DIV	I2TOF	0000 0000b
I2CLK	I^2C clock	BEH	I2CLK[7:0]								0000 1001b
I2STAT	I^2C status	BDH	I2STAT[7:3]					0	0	0	1111 1000b
I2DAT	I^2C data	BCH	I2DAT[7:0]								0000 0000b
SADDR_1	Slave 1 address	BBH	SADDR_1[7:0]								0000 0000b
SADEN_1	Slave 1 address mask	BAH	SADEN_1[7:0]								0000 0000b
SADEN	Slave 0 address mask	B9H	SADEN[7:0]								0000 0000b
IP	Interrupt priority	B8H	(BF) -	(BE) PADC	(BD) PBOD	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	0000 0000b
PWMINTC	PWM Interrupt Control	B7H(1)	-	-	INTTYP1	INTTYP0	-	INTSEL2	INTSEL1	INTSEL0	0000 0000b
IPH	Interrupt priority high	B7H(0)	-	PADCH	PBODH	PSH	PT1H	PX1H	PT0H	PX0H	0000 0000b
P2S	P20 Setting and Timer0/1 Output Enable	B5H	P20UP	-	-	-	T1OE	T0OE	-	P2S.0	0000 0000b
P1SR	P1 slew rate	B4H/(1)	P1SR.7	P1SR.6	P1SR.5	P1SR.4	P1SR.3	P1SR.2	P1SR.1	P1SR.0	0000 0000b
P1M2	P1 mode select 2	B4H/(0)	P1M2.7	P1M2.6	P1M2.5	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0	0000 0000b
P1S	P1 Schmitt trigger input	B3H/(1)	P1S.7	P1S.6	P1S.5	P1S.4	P1S.3	P1S.2	P1S.1	P1S.0	0000 0000b
P1M1	P1 mode select 1	B3H/(0)	P1M1.7	P1M1.6	P1M1.5	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0	1111 1111b
P0SR	P0 slew rate	B2H/(1)	P0SR.7	P0SR.6	P0SR.5	P0SR.4	P0SR.3	P0SR.2	P0SR.1	P0SR.0	0000 0000b
P0M2	P0 mode select 2	B2H/(0)	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0	0000 0000b
P0S	P0 Schmitt trigger input	B1H/(1)	P0S.7	P0S.6	P0S.5	P0S.4	P0S.3	P0S.2	P0S.1	P0S.0	0000 0000b
P0M1	P0 mode select 1	B1H/(0)	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0	1111 1111b
P3	Port 3	B0H	(B7) 0	(B6) 0	(B5) 0	(B4) 0	(B3) 0	(B2) 0	(B1) 0	(B0) P3.0	Output latch, 0000 0001b Input, 0000 000Xb[3]
IAPCN	IAP control	AFH	IAPA[17:16]		FOEN	FCEN	FCTRL[3:0]				0011 0000b
IAPFD	IAP flash data	AEH	IAPFD[7:0]								0000 0000b
P3SR	P3 slew rate	ADH/(1)	-	-	-	-	-	-	-	P3SR.0	0000 0000b
P3M2	P3 mode select 2	ADH/(0)	-	-	-	-	-	-	-	P3M2.0	0000 0000b
P3S	P3 Schmitt trigger input	ACH/(1)	-	-	-	-	-	-	-	P3S.0	0000 0000b
P3M1	P3 mode select 1	ACH/(0)	-	-	-	-	-	-	-	P3M1.0	0000 0001b
BODCON1[4]	Brown-out detection control 1	ABH	-	-	-	-	-	LPBOD[1:0]		BODFLT	POR, 0000 0001b Others, 0000 0UUUb
WDCON[4]	Watchdog Timer control	AAH	WDTR	WDCLR	WDTF	WIDPD	WDTRF	WDPS[2:0]			POR, 0000 0111b WDT, 0000 1UUUb Others, 0000 UUUUb

Table 6-2. SFR Definitions and Reset Values

Symbol	Definition	Address /(Page)	MSB							LSB[1]	Reset Value[2]
SADDR	Slave 0 address	A9H	SADDR[7:0]								0000 0000b
IE	Interrupt enable	A8H	(AF) EA	(AE) EADC	(AD) EBOD	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000b
IAPAH	IAP address high byte	A7H	IAPA[15:8]								0000 0000b
IAPAL	IAP address low byte	A6H	IAPA[7:0]								0000 0000b
IAPUEN[4]	IAP update enable	A5H	-	-	-	-	-	CFUEN	LDUEN	APUEN	0000 0000b
IAPTRG[4]	IAP trigger	A4H	-	-	-	-	-	-	-	IAPGO	0000 0000b
BODCON0[4]	Brown-out detection control 0	A3H	BODEN[5]	-	BOV[1:0][5]		BOF[6]	BORST[5]	BORF	BOS[7]	POR, CCCC XC0Xb BOD, UUUU XU1Xb Others, UUUU XUUXb
AUXR1	Auxiliary register 1	A2H	SWRF	RSTPINF	HardF	-	GF2	UART0PX	0	DPS	POR, 0000 0000b Software, 1U00 0000b $\overline{RST}$ pin, U100 0000b Others, UUU0 0000b
P2	Port 2	A0H	(A7) 0	(A6) 0	(A5) 0	(A4) 0	(A3) 0	(A2) 0	(A1) 0	(A0) P2.0	Output latch, 0000 000Xb Input, 0000 000Xb[3]
CHPCON[4]	Chip control	9FH	SWRST	IAPFF	-	-	-	-	BS[5]	IAPEN	Software, 0000 00U0b Others, 0000 00C0b
EIE1	Extensive interrupt enable 1	9CH	-	-	-	-	-	EWKT	ET3	ES_1	0000 0000b
EIE	Extensive interrupt enable	9BH	ET2	ESPI	EFB	EWDT	EPWM	ECAP	EPI	EI2C	0000 0000b
SBUF_1	Serial port 1 data buffer	9AH	SBUF_1[7:0]								0000 0000b
SBUF	Serial port 0 data buffer	99H	SBUF[7:0]								0000 0000b
SCON	Serial port 0 control	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000b
CKEN[4]	Clock enable	97H	EXTEN[1:0]		HIRCEN	-	-	-	-	CKSWTF	0011 0000b
CKSWT[4]	Clock switch	96H	-	-	HIRCST	-	ECLKST	OSC[1:0]		-	0011 0000b
CKDIV	Clock divider	95H	CKDIV[7:0]								0000 0000b
CAPCON2	Input capture control 2	94H	-	ENF2	ENF1	ENF0	-	-	-	-	0000 0000b
CAPCON1	Input capture control 1	93H	-	-	CAP2LS[1:0]		CAP1LS[1:0]		CAP0LS[1:0]		0000 0000b
CAPCON0	Input capture control 0	92H	-	CAPEN2	CAPEN1	CAPEN0	-	CAPF2	CAPF1	CAPF0	0000 0000b
SFRS[4]	SFR page selection	91H	-	-	-	-	-	-	-	SFRPSEL	0000 0000b
P1	Port 1	90H	(97) P1.7	(96) P1.6	(95) P1.5	(94) P1.4	(93) P1.3	(92) P1.2	(91) P1.1	(90) P1.0	Output latch, 1111 1111b Input, XXXX XXXXb[3]
WKCON	Self Wake-up Timer control	8FH	-	-	-	WKTF	WKTR	WKPS[2:0]			0000 0000b
CKCON	Clock control	8EH	-	PWMCKS	-	T1M	T0M	-	CLOEN	-	0000 0000b
TH1	Timer 1 high byte	8DH	TH1[7:0]								0000 0000b
TH0	Timer 0 high byte	8CH	TH0[7:0]								0000 0000b
TL1	Timer 1 low byte	8BH	TL1[7:0]								0000 0000b
TL0	Timer 0 low byte	8AH	TL0[7:0]								0000 0000b
TMOD	Timer 0 and 1 mode	89H	GATE	$C/\overline{T}$	M1	M0	GATE	$C/\overline{T}$	M1	M0	0000 0000b
TCON	Timer 0 and 1control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0000 0000b
PCON	Power control	87H	SMOD	SMOD0	-	POF	GF1	GF0	PD	IDL	POR, 0001 0000b Others, 000U 0000b
RWK	Self Wake-up Timer reload byte	86H	RWK[7:0]								0000 0000b