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Nuvoton 8-bit 8051-based Microcontroller

N78E059A/N78E055A

Data Sheet

CONTENTS

1. DESCRIPTION

N78E059A/N78E055A is an 8-bit microcontroller, which has an in-system programmable Flash supported. The instruction set of N78E059A/N78E055A is fully compatible with the standard 8051. N78E059A/N78E055A contains 32k/16k bytes of main Flash APROM, in which the contents of the main program code can be updated by parallel Programmer/Writer or In System Programming (ISP) method which enables on-chip firmware updating. There is an additional 2.5k bytes called LDROM for ISP function. N78E059A/N78E055A has 4k bytes of Data Flash which is accessed with ISP. N78E059A/N78E055A provides 256 bytes of SRAM, 1k bytes of auxiliary RAM (XRAM), four 8-bit bi-directional and bit-addressable I/O ports, an additional 8-bit bi-directional and bit-addressable port P4 for LQPF-48 package (PLCC-44 and PQFP-44 just have low nibble 4 bits of P4 and DIP-40 does not have this additional P4), three 16-bit Timers/Counters, one UART, five PWM output channels, and one SPI. These peripherals equip with 11-source with 4-level priority interrupts capability. To facilitate programming and verification, the Flash inside the N78E059A/N78E055A allows the Program Memory to be programmed and read electronically. Once the code confirms, the user can lock the code for security.

N78E059A/N78E055A is built in a precise on-chip RC oscillator of 22.1184MHz/11.0592MHz selected by CONFIG setting, factory trimmed to ±1% at room temperature. N78E059A/N78E055A provides additional power monitoring detection such as power-on and Brown-out detection. It stabilizes the power-on/off sequence for a high reliability system design.

N78E059A/N78E055A microcontroller operation consumes a very low power. Two economic power modes to reduce power consumption, Idle mode and Power Down mode. Both of them are software selectable. The Idle mode turns off the CPU clock but allows continuing peripheral operation. The Power Down mode stops the whole system clock for minimum power consumption.

2. FEATURES

- Fully static design 8-bit CMOS microcontroller.

- Wide supply voltage of 2.4V to 5.5V and wide frequency from 4MHz to 40MHz.

- 12T mode compatible with the tradition 8051 timing.

- 6T mode supported for double performance.

- On-chip RC oscillator of 22.1184MHz/11.0592MHz, trimmed to ±1% at room temperature for the precise system clock.

- 32k/16k bytes Flash APROM for the application program.

- 2.5k bytes Flash LDROM for ISP code.

- 4k bytes Data Flash.

- In-System-Programmable (ISP) built in. ISP Erasing or programming supports wide operating voltage 3.0V~5.5V.

- Flash 10,000 writing cycle endurance. Greater than 10 years data retention under 85℃.

- 256 bytes of on-chip RAM.

- 1024 bytes of on-chip auxiliary RAM (XRAM).

- 64k bytes Program Memory address space and 64k bytes Data Memory address space.

- Maximum five 8-bit general purpose I/O ports pin-to-pin compatible with standard 8051, additional $\overline{INT2}$ and $\overline{INT3}$ on packages except DIP-40.

- Three 16-bit Timers/Counters.

- One dedicate timer for Power Down mode waking-up.

- One full-duplex UART port.

- Five pulse width modulated (PWM) output channels.

- One SPI communication port.

- 11-source, 4-priority-level interrupts capability.

- Programmable Watchdog Timer.

- Power-on reset.

- Brown-out detection interrupt and reset, 4-level selected.

- Supports software reset function.

- Built-in power management with Idle mode and Power Down mode.

- Code lock for data security.

- Much lower power consumption than other standard 8051 productions.

- Industrial temperature grade, -40℃~85℃.

- Strong ESD, EFT immunity.

- Development Tool:

    – Parallel Programmer/Writer.

    – Nuvoton 8-bit Microcontroller ISP Writer.

- Package:

Part Number	APROM	Data Flash	Package
N78E059ADG	32k bytes	4k bytes	40-pin DIP
N78E059APG			44-pin PLCC
N78E059AFG			44-pin PQFP
N78E059ALG			48-pin LQFP
N78E055ADG	16k bytes	4k bytes	40-pin DIP
N78E055APG			44-pin PLCC
N78E055AFG			44-pin PQFP
N78E055ALG			48-pin LQFP

3. BLOCK DIAGRAM

Figure 3–1 shows the functional block diagram of N78E059A/N78E055A. It gives the outline of the device. The user can find all the device's peripheral functions in the diagram.
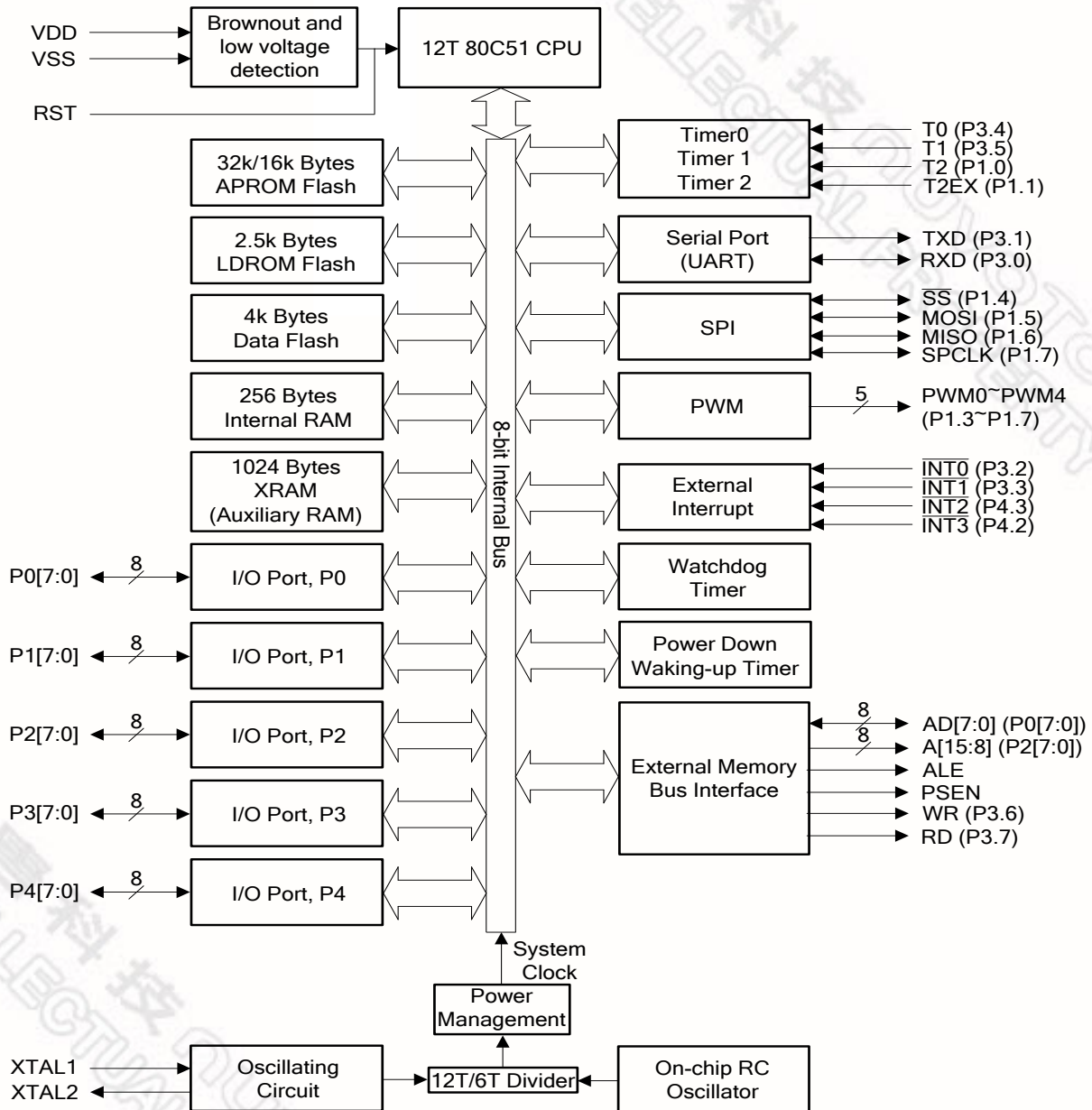

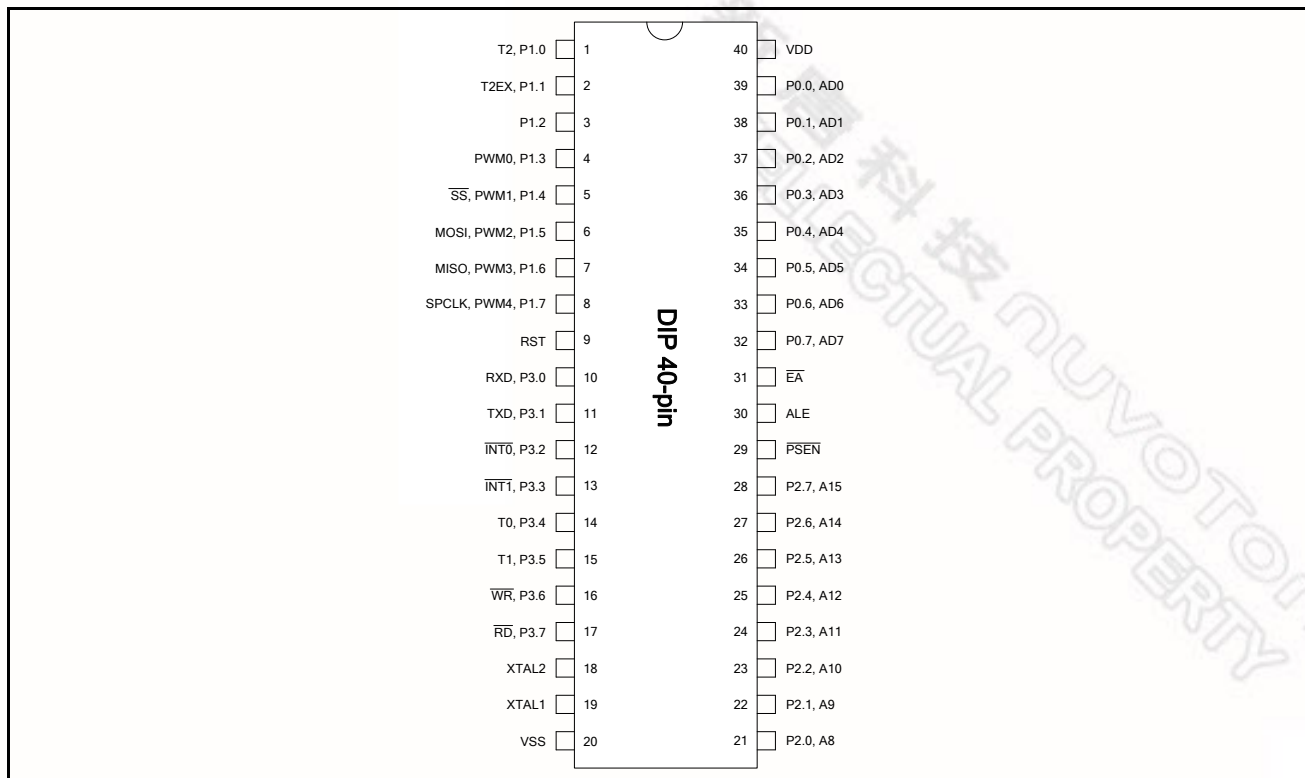**Figure 3–1. N78E059A/N78E055A Function Block Diagram**

4. PIN CONFIGURATIONS

Figure 4–1. Pin Assignment of DIP 40-Pin
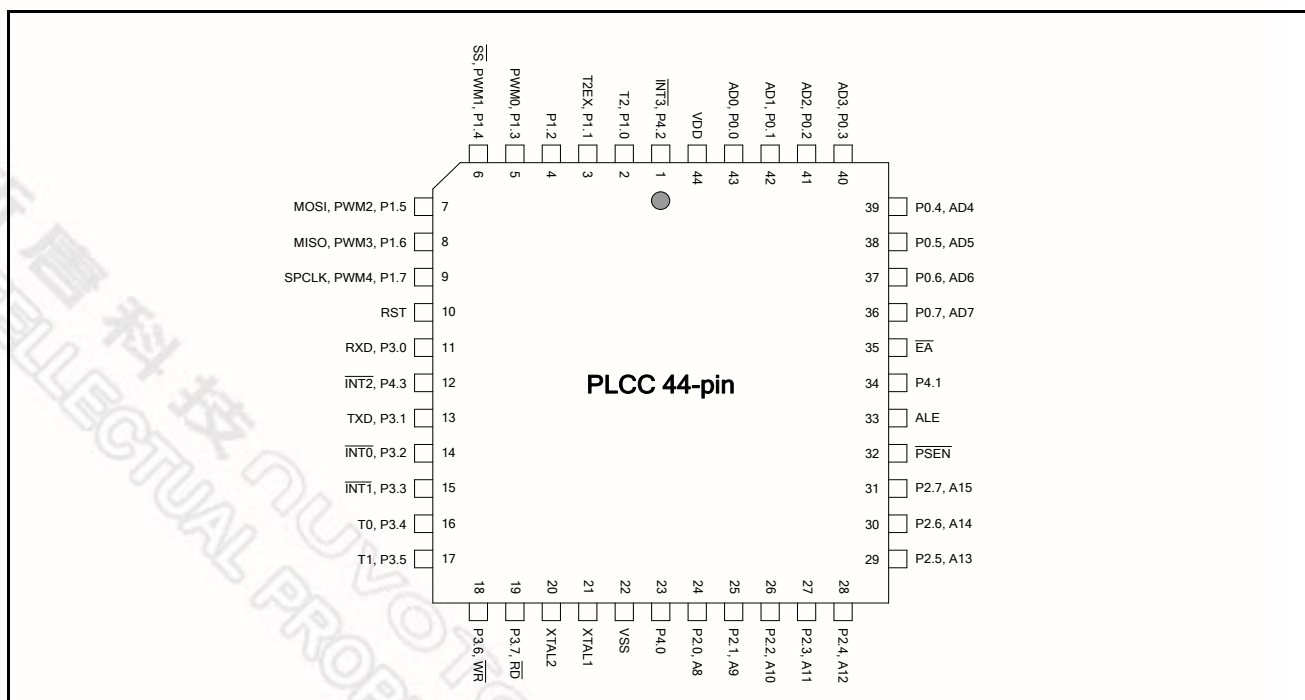
Figure 4–2. Pin Assignment of PLCC 44-Pin
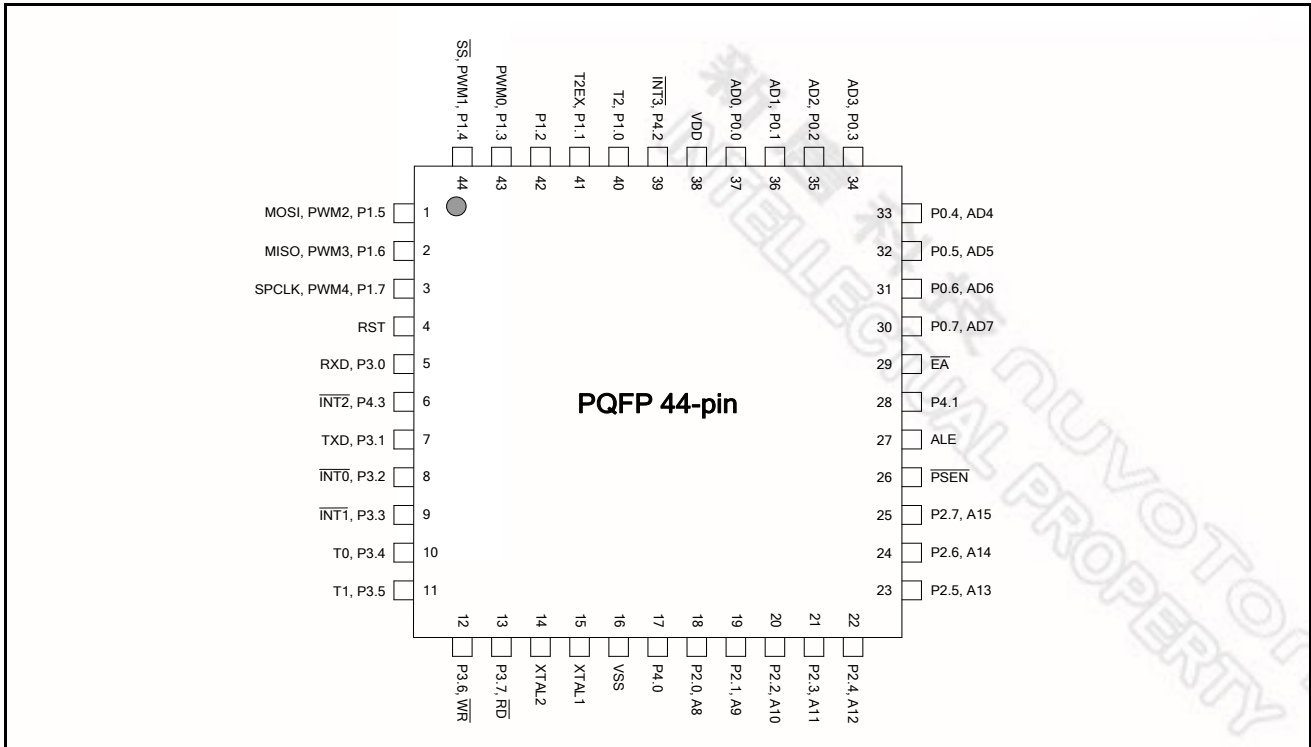
Figure 4–3. Pin Assignment of PQFP 44-Pin
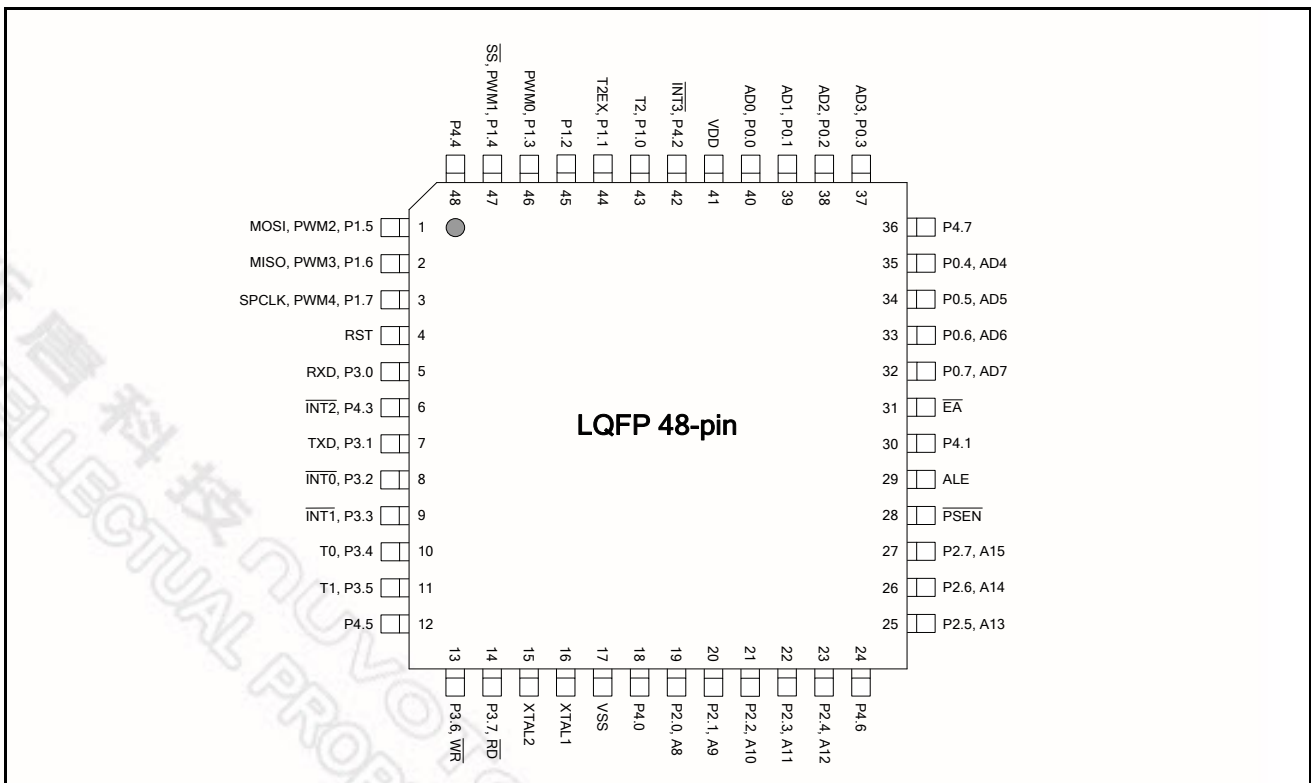
Figure 4–4. Pin Assignment of LQFP 48-Pin

Table 4–1. Pin Description

DIP	PLCC	PQFP	LQFP	Symbol	Alternate Function 1	Alternate Function 2	Type[1]	Description
19	21	15	16	XTAL1			I (ST)	**CRYSTAL1:** This is the input pin to the internal inverting amplifier. The system clock is from external crystal or resonator when FOSC (CONFIG3.1) is logic 1 by default. *A 0.1µF capacitor is recommended to be added on XTAL1 pin to gain the more precise frequency of the internal RC oscillator frequency if it is selected as the system clock source.*
18	20	14	15	XTAL2			O	**CRYSTAL2:** This is the output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1. While on-chip RC oscillator is used, float XTAL2 pin always.
40	44	38	41	VDD			P	**POWER SUPPLY:** Supply voltage V_{DD} for operation.
20	22	16	17	VSS			P	**GROUND:** Ground potential.
31	35	29	31	$\overline{EA}$			I	**EXTERNAL ACCESS ENABLE:** To force $\overline{EA}$ low will make the CPU execute the external Program Memory. The address and data will be presented on the bus P0 and P2. If the $\overline{EA}$ pin is high, CPU will fetch internal code unless the Program Counter addresses the area out of the internal Program Memory. This will make CPU run external Program Memory continuously. $\overline{EA}$ possesses reset lock. After all reset, the $\overline{EA}$ state will be latched and any state change of this pin after reset will not switch between internal and external Program Memory execution. *The user should take care of this pin from floating but connecting to V_{DD} directly if internal Program Memory is used.*
30	33	27	29	ALE			O	**ADDRESS LATCH ENABLE:** ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6 of the Fosc[2]. An ALE pulse is omitted always. The user can turn ALE off by setting ALEOFF (AUXR.0) to reduce EMI. Setting ALEOFF will just make ALE activating only during external memory access through a MOVC or MOVX instruction. ALE will stay high in other conditions.
29	32	26	28	$\overline{PSEN}$			O	**PROGRAM STORE ENABLE:** $\overline{PSEN}$ strobes the external Program Memory. When internal Program Memory access is performed, there will be no $\overline{PSEN}$ strobe signal output from this pin.
9	10	4	4	RST			I (ST)	**RESET:** RST pin is a Schmitt trigger input pin for hardware device reset. A high on this pin for two machine-cycles while the system clock is running will reset the device. RST pin has an internal pull-down resistor allowing power-on reset by simply connecting

Table 4–1. Pin Description

Pin number				Symbol	Alternate Function		Type[1]	Description
DIP	PLCC	PQFP	LQFP		1	2		
								an external capacitor to V_{DD}.
39	43	37	40	P0.0		AD0	D, I/O	**PORT0:** Port 0 is an 8-bit open-drain port by default. Via setting P0UP (P0OR.0), P0 will switch as weakly pulled up internally. P0 has an alternative function as AD[7:0] while external memory accessing. During the external memory access, P0 will output high will be internal strong pulled-up rather than weak pull-up in order to drive out high byte address for external devices.
38	42	36	39	P0.1		AD1	D, I/O	
37	41	35	38	P0.2		AD2	D, I/O	
36	40	34	37	P0.3		AD3	D, I/O	
35	39	33	35	P0.4		AD4	D, I/O	
34	38	32	34	P0.5		AD5	D, I/O	
33	37	31	33	P0.6		AD6	D, I/O	
32	36	30	32	P0.7		AD7	D, I/O	
1	2	40	43	P1.0	T2		I/O	**PORT1:** Port 1 is an 8-bit quasi bi-directional I/O port. Its multifunction pins are for T2, T2EX, PWM0~PWM4, $\overline{SS}$, MOSI, MISO, and SPCLK.
2	3	41	44	P1.1	T2EX		I/O	
3	4	42	45	P1.2			I/O	
4	5	43	46	P1.3	PWM0		I/O	
5	6	44	47	P1.4	PWM1	$\overline{SS}$	I/O	
6	7	1	1	P1.5	PWM2	MOSI	I/O	
7	8	2	2	P1.6	PWM3	MISO	I/O	
8	9	3	3	P1.7	PWM4	SPCLK	I/O	
21	24	18	19	P2.0		A8	I/O	**PORT2:** Port 2 is an 8-bit quasi bi-directional I/O port. It has an alternative function as A[15:8] while external memory accessing. During the external memory access, P2 will output high will be internal strong pulled-up rather than weak pull-up in order to drive out high byte address for external devices.
22	25	19	20	P2.1		A9	I/O	
23	26	20	21	P2.2		A10	I/O	
24	27	21	22	P2.3		A11	I/O	
25	28	22	23	P2.4		A12	I/O	
26	29	23	25	P2.5		A13	I/O	
27	30	24	26	P2.6		A14	I/O	
28	31	25	27	P2.7		A15	I/O	

Table 4–1. Pin Description

Pin number				Symbol	Alternate Function		Type[1]	Description
DIP	PLCC	PQFP	LQFP		1	2		
10	11	5	5	P3.0	RXD		I/O	**PORT3:** Port 3 is an 8-bit quasi bi-directional I/O port. Its multifunction pins are for RXD, TXD, $\overline{INT0}$, $\overline{INT1}$, T0, T1, $\overline{WR}$, and $\overline{RD}$.
11	13	7	7	P3.1	TXD		I/O	
12	14	8	8	P3.2	$\overline{INT0}$		I/O	
13	15	9	9	P3.3	$\overline{INT1}$		I/O	
14	16	10	10	P3.4	T0		I/O	
15	17	11	11	P3.5	T1		I/O	
16	18	12	13	P3.6	$\overline{WR}$		I/O	
17	19	13	14	P3.7	$\overline{RD}$		I/O	
-	23	17	18	P4.0			I/O	**PORT4[3]:** Port 4 is an 8-bit quasi bi-directional I/O port. It also possesses bit-addressable feature as P0~P3. P4.2 and P4.3 are alternative function pins of $\overline{INT3}$ and $\overline{INT2}$.
-	34	28	30	P4.1			I/O	
-	1	39	42	P4.2	$\overline{INT3}$		I/O	
-	12	6	6	P4.3	$\overline{INT2}$		I/O	
-	-	-	48	P4.4			I/O	
-	-	-	12	P4.5			I/O	
-	-	-	24	P4.6			I/O	
-	-	-	36	P4.7			I/O	

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pins, ST: Schmitt trigger.
[2] While switching to 6T mode, ALE will run at 1/3 of Fosc.
[3] A full 8-bit P4 is just on LQPF-48 package. PLCC-44 and PQFP-44 just have low nibble 4 bits of P4. DIP-40 does not have this additional P4.

The application circuit is shown below. The user is recommended follow the circuit enclosed by gray blocks to achieve the most stable and reliable operation of MCU especially in a noisy power environment for a healthy EMS immunity. If internal RC oscillator is used as the system clock, a 0.1μF capacitor should be added to gain a precise RC frequency.

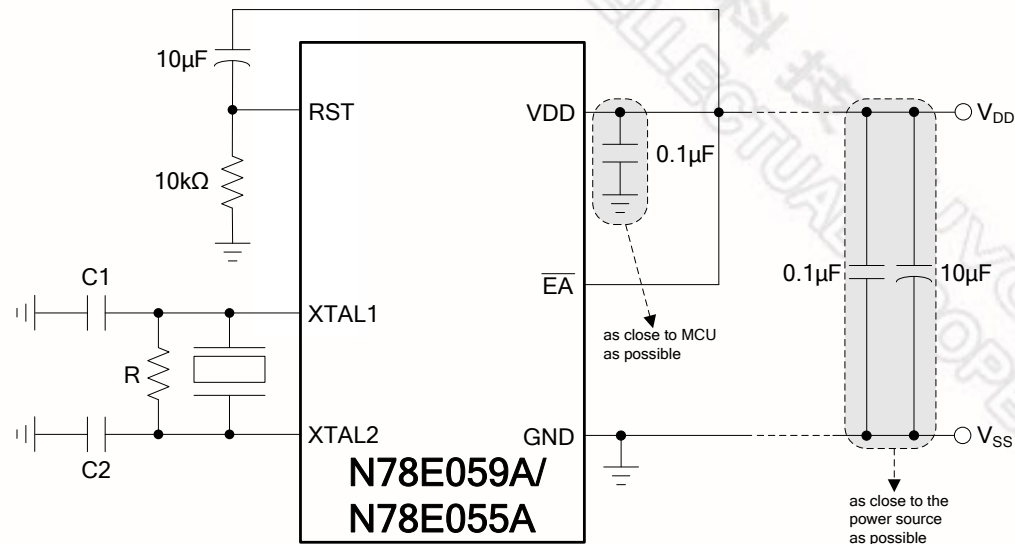**Figure 4–5. Application Circuit for Execution of Internal Program Code with External Crystal**

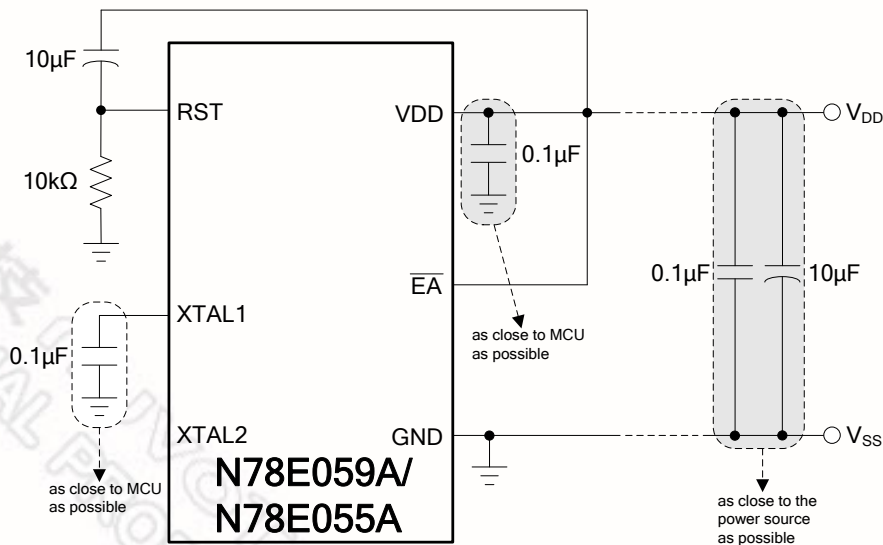| Crystal Frequency	R	C1	C2
4MHz~33MHz	Without	Depend on crystal specifications	
33MHZ~40MHz	5kΩ~10kΩ		

Figure 4–6. Application Circuit for Execution of Internal Program Code with Internal RC Oscillator

5. MEMORY ORGANIZATION

A standard 8051 based MCU divides the memory into two different sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction codes, whereas the Data Memory is used to store data or variations during the program execution.

Data Memory occupies a separate address space from Program Memory. In N78E059A/N78E055A, there are 256 bytes of internal scratch-pad RAM and up to 64k bytes of memory space for external Data Memory. The MCU generates the 16-bit or 8-bit addresses, read and write strobe signals ($\overline{RD}$ and $\overline{WR}$, respectively) during external Data Memory access. For many applications which need more internal RAM, N78E059A/N78E055A possesses on-chip 1k bytes of RAM (called XRAM) accessed by MOVX instruction.

The whole embedded flash is divided into 4 banks, APROM for storage of user's program code, Data Flash for parameter data storage, LDROM for ISP program and CONFIG bytes. Each bank is accumulated page by page and the page size is 256 bytes. The flash control unit supports Page Erase, Byte Program, and Byte Read modes. The external writer tools though specific I/O pins and the internal ISP (In System Programming) function both can perform these modes.

5.1 Internal Program Memory

Program Memory is the one, which stores the program codes to execute, as shown in . While $\overline{EA}$ pin is pulled high and after any reset, the CPU begins execution from location 0000H where should be the starting point of the user's application code. To service the interrupts, the interrupt service locations (called interrupt vectors) should be located in the Program Memory. Each interrupt is assigned with a fixed location in the Program Memory. The interrupt causes the CPU to jump to that location with where it commences execution of the interrupt service routine (ISR). External Interrupt 0, for example, is assigned to location 0003H. If External Interrupt 0 is going to be used, its service routine must begin at location 0003H. If the interrupt is not going to be used, its service location is available as general purpose Program Memory.

The interrupt service locations are spaced at an interval of 8 bytes: 0003H for External Interrupt 0, 000BH for Timer 0, 0013H for External Interrupt 1, 001BH for Timer 1, etc. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within that 8-byte interval. However longer service routines should use a JMP instruction to skip over subsequent interrupt locations if other interrupts are in use.

N78E059A/N78E055A provides two internal Program Memory bank APROM and LDROM. Although they both behave the same as the standard 8051 Program Memory, they play different rules according to their ROM

size. The APROM on N78E059A/N78E055A is 32k/16k-byte size. The user's main program code is normally put inside. All instructions are fetched for execution from this area. The MOVC instruction can also read this flash memory region.

N78E059A/N78E055A supports the other individual Program Memory bank called LDROM besides APROM. The main function of LDROM is to store the ISP application program. User may develop the ISP in LDROM for updating APROM content. The program in APROM can also re-program LDROM. For ISP details and configuration bit setting related with APROM and LDROM, see Section 18. "IN SYSTEM PROGRAMMING (ISP)" on page 91. Note that because APROM and LDROM are hardware individual blocks, consequently if CPU reboots from LDROM, CPU will automatically re-vectors Program Counter 0000H to the LDROM start address. Therefore, CPU accounts the LDROM as an independent Program Memory and all interrupt vectors are independent from APROM.
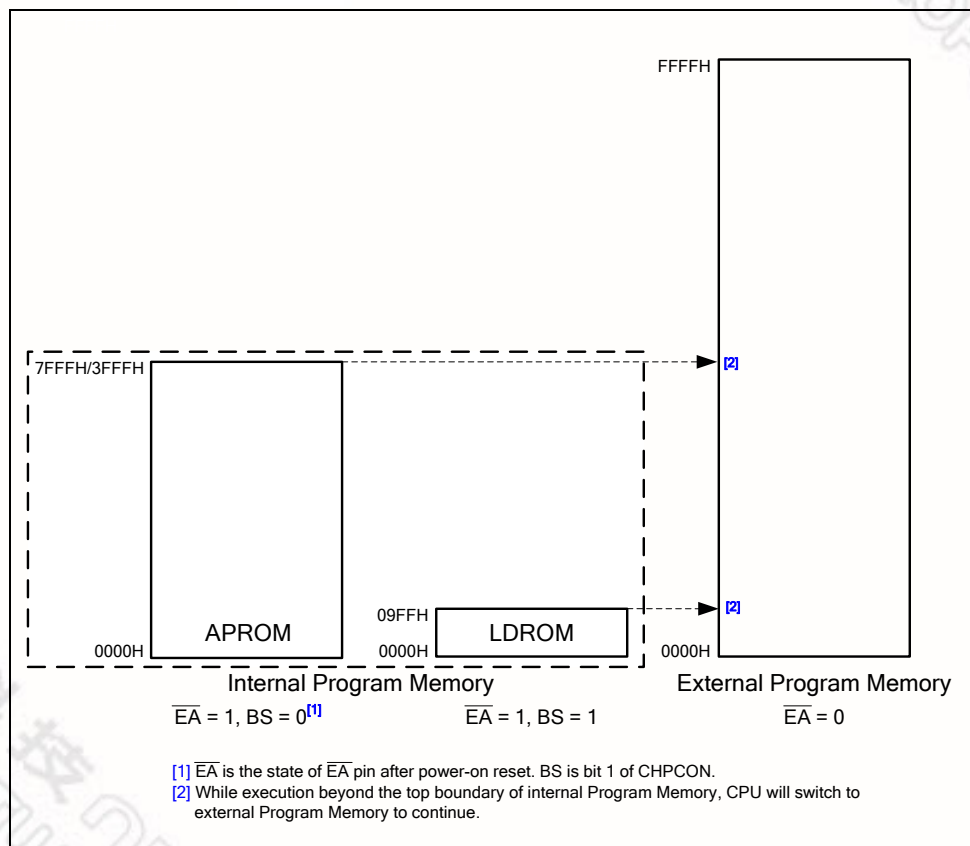
Figure 5–1. N78E059A/N78E055A Program Memory Structure

5.2 External Program Memory

N78E059A/N78E055A is a 16-bit address-width CPU. It can address 64k-byte program code. Besides the internal Program Memory, the external additional Program Memory is also can be used. The external program addressing will be executed under cases below,

1. The PC (Program Counter) value is beyond the boundary size address of APROM or LDROM while $\overline{EA}$ pin is pulled high during power on. The CPU will continue to fetch the external Program Memory.

2. While $\overline{EA}$ pin is pulled low during power on period, The CPU will run totally 64k-byte code externally.

While the external mode is running, the P0 and P2 will produce address and data signals to fetching external Program Memory. In this case, P0 and P2 cannot be general purpose I/O anymore. $\overline{PSEN}$ will also toggle out to strobe the external Program Memory. For the hardware circuit for external program execution, see Figure 5–2. Program Memory Interface.

For security $\overline{EA}$ pin state will be locked after power on. The user cannot switch the program running internally or externally by $\overline{EA}$ after power on. The other design for data security is MOVC lock enable (MOVCL, CONFIG0.2). While this bit is set 0, The external Program Memory code is inhibited to read internal APROM or LDROM contents through MOVC instruction.
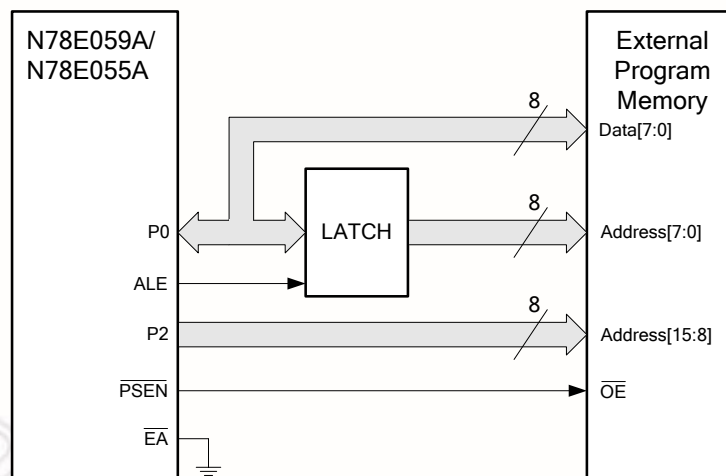
Figure 5–2. Program Memory Interface

5.3 Internal Data Memory

Figure 5–3 shows the internal and external Data Memory spaces available on N78E059A/N78E055A. Internal Data Memory can be divided into three blocks. They are the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128 bytes of SFR space. Internal Data Memory addresses are always 8-bit wide, which implies an address space of only 256 bytes. Direct addressing higher than 7FH will access the special function registers (SFRs) space and indirect addressing higher than 7FH will access the upper 128 bytes of RAM. Although the SFR space and the upper 128 bytes of RAM share the same logic address, 80H through FFH, actually they are physically separate entities. Direct addressing to distinguish with the higher 128 bytes of RAM can only access these SFRs. Sixteen addresses in SFR space are both byte and bit-addressable. The bit-addressable SFRs are those whose addresses end in 0H or 8H.

The lower 128 bytes of internal RAM are present in all 8051 devices. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call these registers as R0 through R7. Two bits RS0 and RS1 in the Program Status Word (PSW[3:4]) select which Register Bank is used. This benefits more efficiency of code space, since register instructions are shorter than instructions that use direct addressing. The next 16 bytes above the Register Banks (byte-address 20H through 2FH) form a block of bit-addressable memory space (bit-address 00H through 7FH). The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All bytes in the lower 128-byte space can be accessed by either direct or indirect addressing. Indirect addressing can only access the upper 128.

Another application implemented with the whole block of internal 256-byte RAM is for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a JMP, CALL or interrupt is invoked, the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07H at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.
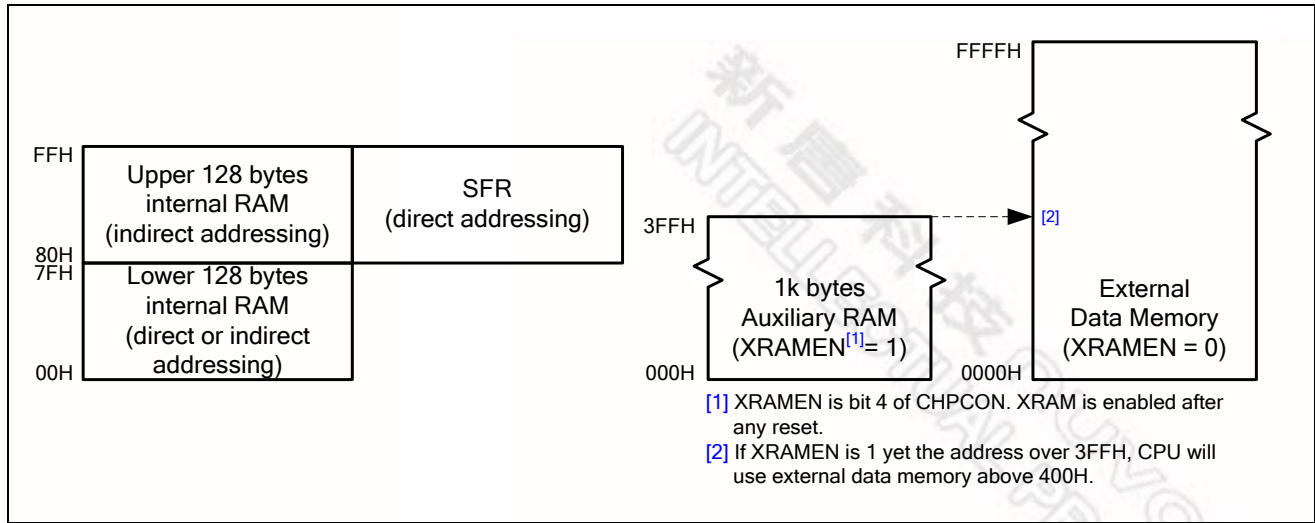
Figure 5–3. N78E059A/N78E055A Data Memory Structure

In the figure:

- FFH / 80H: Upper 128 bytes internal RAM (indirect addressing)
- SFR (direct addressing)
- 7FH / 00H: Lower 128 bytes internal RAM (direct or indirect addressing)
- 3FFH / 000H: 1k bytes Auxiliary RAM (XRAMEN[1] = 1)
- FFFFH / 0000H: External Data Memory (XRAMEN = 0)

[1] XRAMEN is bit 4 of CHPCON. XRAM is enabled after any reset.
[2] If XRAMEN is 1 yet the address over 3FFH, CPU will use external data memory above 400H.

Figure 5–4. 256 bytes Internal RAM Addressing

In the figure (bit addresses table):

FFH – 80H	Indirect Accessing RAM						
7FH – 30H	Direct or Indirect Accessing RAM						
2FH	7F	7E	7D	7C	7B	7A	79	78
2EH	77	76	75	74	73	72	71	70
2DH	6F	6E	6D	6C	6B	6A	69	68
2CH	67	66	65	64	63	62	61	60
2BH	5F	5E	5D	5C	5B	5A	59	58
2AH	57	56	55	54	53	52	51	50
29H	4F	4E	4D	4C	4B	4A	49	48
28H	47	46	45	44	43	42	41	40
27H	3F	3E	3D	3C	3B	3A	39	38
26H	37	36	35	34	33	32	31	30
25H	2F	2E	2D	2C	2B	2A	29	28
24H	27	26	25	24	23	22	21	20
23H	1F	1E	1D	1C	1B	1A	19	18
22H	17	16	15	14	13	12	11	10
21H	0F	0E	0D	0C	0B	0A	09	08
20H	07	06	05	04	03	02	01	00

- 1FH – 18H: Register Bank 3
- 17H – 10H: Register Bank 2
- 0FH – 08H: Register Bank 1
- 07H – 00H: Register Bank 0

5.4 On-chip XRAM

N78E059A/N78E055A provides additional on-chip auxiliary RAM called XRAM to enlarge RAM space. The 1024 bytes of XRAM (000H to 3FFH) are indirectly accessed by move external instruction MOVX. For details, see Section 8. "AUXILIARY RAM (XRAM)" on page 29.

5.5 External Data Memory

Access to external Data Memory can use either a 16-bit address (using 'MOVX @DPTR') or an 8-bit address (using 'MOVX @Ri', i = 0 or 1). For another 1k-byte XRAM exists, remember the bit XRAMEN (CHPCON.4) should be cleared as logic 0 in order to access the range of 000H to 3FFH address of the external Data Memory.

16-bit addresses are often used to access up to 64k bytes of external RAM. Whenever a 16-bit address is used, P0, P2, P3.7 and P3.6 serve as the low byte address/data, the high byte address, $\overline{RD}$ strobe and $\overline{WR}$ strobe signals respectively. Meanwhile the pins listed above cannot be used as general purpose I/O during external Data Memory access.

8-bit addresses are often used in conjunction with one or more other I/O lines to page the RAM. For example, if a 1k-byte external RAM is used, Port 0 serves as a multiplexed address/data bus to the RAM, and 2 pins of Port 2 are used to page the RAM. The CPU generates $\overline{RD}$ and $\overline{WR}$ (alternate functions of P3.7 and P3.6) to strobe the memory. In 8-bit addressing mode, P2 pins other than the two pins for RAM paging are free for general purpose I/O usage. This will facilitate P2 application. Of course, the user may use any other I/O lines instead of P2 to page the RAM.

In all cases, the low byte of the address is time-multiplexed with the data byte on Port 0. ALE (Address Latch Enable) should be used to capture the address byte into an external latch. The address byte is valid at the negative transition of ALE. Then, in a write cycle, the data byte to be written appears on Port 0 just before $\overline{WR}$ is activated, and remains there until after $\overline{WR}$ is deactivated. In a read cycle, the incoming byte is accepted at Port 0 just before the read strobe is deactivated. During any access to external memory, the CPU writes 0FFH to the Port 0 latch (P0 in SFRs), thus obliterating whatever information the Port 0 SFR may have been holding.
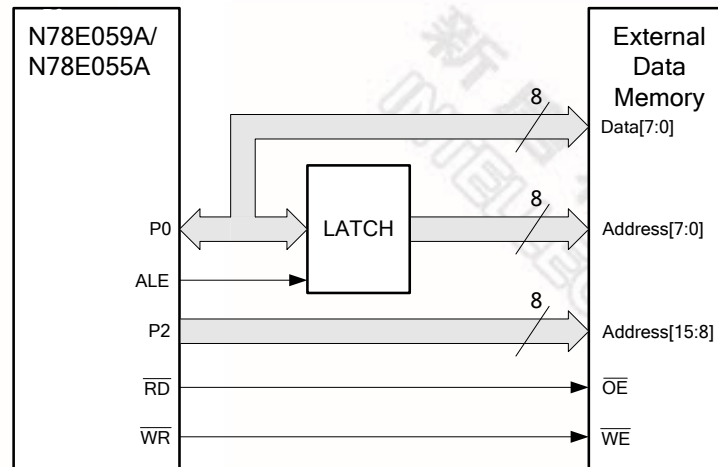
Figure 5–5. Data Memory Interface

5.6 On-chip Non-volatile Data Flash

N78E059A/N78E055A additionally has Data Flash. The Data Flash is non-volatile so that it remains its content even after the power is off. Therefore, in general application the user can write or read data which rules as parameters or constants. Be aware of Data Flash writing endurance of 10,000 cycles. By the software path, the Data Flash can be accessed only through ISP mode. Note that the erasing or writing of Data Flash should not operates under V_{DD} 3.0V for ISP limitation. For Data Flash accessing with ISP, please see Section 18. "IN SYSTEM PROGRAMMING (ISP)" on page 91 for details. For the design for security, ISP is invalid while external Program Memory executes. The Data Flash, therefore, cannot be accessed with external memory code. Of course the Data Flash can be accessed via hardware with parallel Programmer/Writer.

The Data Flash size is fixed as 4k-byte size on N78E059A/N78E055A.
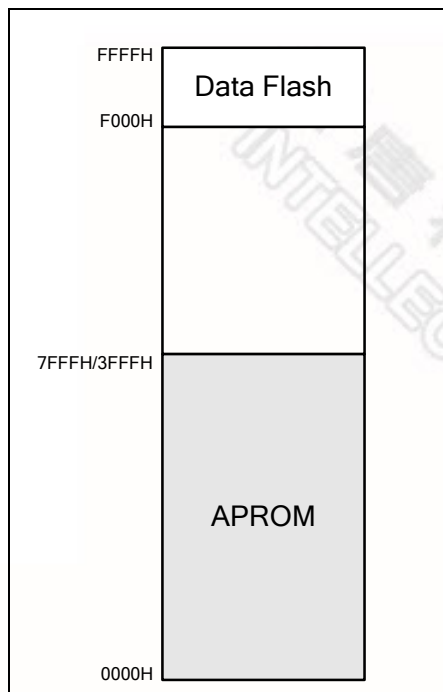
Figure 5–6. N78E059A/N78E055A Data Flash

6. SPECIAL FUNCTION REGISTER (SFR)

The N78E059A/N78E055A uses Special Function Registers (SFRs) to control and monitor peripherals and their modes. The SFRs reside in the register locations 80~FFH and are accessed by direct addressing only. Some of the SFRs are bit-addressable. This is very useful in cases where users would like to modify a particular bit directly without changing other bits. Those which are bit-addressable SFRs end their addresses as 0H or 8H. N78E059A/N78E055A contains all the SFRs presenting in the standard 8051. However some additional SFRs are built in. Therefore, some of unused bytes in the original 8051 have been given new functions. The SFRs is listed as below.

Table 6–1. N78E059A/N78E055A Special Function Registers Mapping

F8	-	-	-	-	-	-	-	-	FF
F0	**B**	-	-	SPCR	SPSR	SPDR	-	-	F7
E8	-	-	-	-	-	-	-	-	EF
E0	**ACC**	-	-	-	-	-	-	-	E7
D8	**P4**	PWMP	PWM0	PWM1	PWMCON0	PWM2	PWM3	-	DF
D0	**PSW**	-	-	-	-	-	-	-	D7
C8	**T2CON**	T2MOD	RCAP2L	RCAP2H	TL2	TH2	PWMCON1	PWM4	CF
C0	**XICON**	-	-	-	-	-	-	TA	C7
B8	**IP**	-	IPH	EIPH	EIP	EIE	-	-	BF
B0	**P3**	-	-	-	-	-	-	-	B7
A8	**IE**	-	WDCON	PDCON	PMC	-	ISPFD	ISPCN	AF
A0	**P2**	XRAMAH	-	-	ISPTRG	-	ISPAL	ISPAH	A7
98	**SCON**	SBUF	-	-	-	-	-	CHPCON	9F
90	**P1**	-	-	-	-	-	RSR	-	97
88	**TCON**	TMOD	TL0	TL1	TH0	TH1	AUXR	-	8F
80	**P0**	SP	DPL	DPH	-	-	P0OR	PCON	87

In Bold	bit-addressable
-	reserved

Note that the reserved SFR addresses must be kept in their own initial states. Users should never change their values.

Table 6–2. N78E059A/N78E055A SFR Descriptions and Reset Values

Symbol	Definition	Address	MSB							LSB[1]	Reset Value[2]
SPDR	SPI data	F5H									0000 0000b
SPSR	SPI status	F4H	SPIF	WCOL	SPIOVF	MODF	DISMODF	-	-	-	0000 0000b
SPCR	SPI control	F3H	SSOE	SPIEN	LSBFE	MSTR	CPOL	CPHA	SPR1	SPR0	0000 0000b
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	0000 0000b
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	0000 0000b
PWM3	PWM3 duty	DEH									0000 0000b
PWM2	PWM2 duty	DDH									0000 0000b
PWMCON0	PWM control 0	DCH	PWM3OE	PWM2OE	PWM3EN	PWM2EN	PWM1OE	PWM0OE	PWM1EN	PWM0EN	0000 0000b
PWM1	PWM1 duty	DBH									0000 0000b
PWM0	PWM0 duty	DAH									0000 0000b
PWMP	PWM period	D9H									0000 0000b
P4	Port 4	D8H	(DF)	(DE)	(DD)	(DC)	(DB) $\overline{INT2}$	(DA) $\overline{INT3}$	(D9)	(D8)	1111 1111b
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	0000 0000b
PWM4	PWM4 duty	CFH									0000 0000b
PWMCON1	PWM control 1	CEH	-	-	-	-	-	PWM4OE	-	PWM4EN	0000 0000b
TH2	Timer 2 high byte	CDH									0000 0000b
TL2	Timer 2 low byte	CCH									0000 0000b
RCAP2H	Timer 2 reload/capture high byte	CBH									0000 0000b
RCAP2L	Timer 2 reload/capture low byte	CAH									0000 0000b
T2MOD	Timer 2 mode	C9H	-	-	-	-	-	-	T2OE	-	0000 0000b
T2CON	Timer 2 control	C8H	(CF) TF2	(CE) EXF2	(CD) RCLK	(CC) TCLK	(CB) EXEN2	(CA) TR2	(C9) $C/\overline{T2}$	(C8) $\overline{CP/RL2}$	0000 0000b
TA	Timed access protection	C7H									0000 0000b
XICON	External interrupt control	C0H	(C7) PX3	(C6) EX3	(C4) IE3	(C4) IT3	(C3) PX2	(C2) EX2	(C1) IE2	(C0) 1IT2	0000 0000b
EIE	Extensive interrupt enable	BDH	-	-	-	-	-	EBOD	EPDT	ESPI	0000 0000b
EIP	Extensive interrupt priority	BCH	-	-	-	-	-	PBOV	PPDT	PSPI	0000 0000b
EIPH	Extensive interrupt priority high	BBH	-	-	-	-	-	PBODH	PPDTH	PSPIH	0000 0000b
IPH	Interrupt priority high	BAH	PX3H	PX2H	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	0000 0000b
IP	Interrupt priority	B8H	(BF) -	(BE) -	(BD) PT2	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	0000 0000b
P3	Port 3	B0H	(B7) $\overline{RD}$	(B6) $\overline{WR}$	(B5) T1	(B4) T0	(B3) $\overline{INT1}$	(B2) $\overline{INT0}$	(B1) TXD	(B0) RXD	1111 1111b
ISPCN	ISP flash control	AFH	ISPA17	ISPA16	FOEN	FCEN	FCTRL3	FCTRL2	FCTRL1	FCTRL0	0000 0000b
ISPFD	ISP flash data	AEH									0000 0000b
PMC[3]	Power monitoring control	ACH	BODEN	-	-	BORST	BOF[4]	LPBOD	-	BOS[5]	Power-on[6], XXXX X00Xb Brown-out, XXXX 100Xb Others, XXXX 000Xb
PDCON	Power Down waking-up timer control	ABH	PDTEN	PDTCK	PDTF	-	-	PPS2	PPS1	PPS0	0000 0000b
WDCON[3]	Watchdog Timer control	AAH	WDTEN	WDCLR	-	WIDPD	WDTRF	WPS2	WPS1	WPS0	Power-on[6], X000 0000b Watchdog, X00U 1UUUb Others, X00U UUUUb
IE	Interrupt enable	A8H	(AF) EA	(AE) -	(AD) ET2	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000b
ISPAH	ISP address high byte	A7H									0000 0000b
ISPAL	ISP address low byte	A6H									0000 0000b
ISPTRG[3]	ISP trigger	A4H	-	-	-	-	-	-	-	ISPGO	0000 0000b
XRAMAH	Auxiliary RAM address high byte	A1H	-	-	-	-	-	-	XRAMAH.1	XRAMAH.0	0000 0000b
P2	Port 2	A0H	(A7) A15	(A6) A14	(A5) A13	(A4) A12	(A3) A11	(A2) A10	(A1) A9	(A0) A8	1111 1111b

Table 6–2. N78E059A/N78E055A SFR Descriptions and Reset Values

Symbol	Definition	Address	MSB							LSB[1]	Reset Value[2]
CHPCON[3]	Chip control	9FH	SWRST	ISPF	LDUEN	XRAMEN	-	-	BS	ISPEN	Software[6], 0 0 0 1　0 0 U 0 b Others, 0 0 0 1　0 0 X 0 b
SBUF	Serial buffer	99H									0 0 0 0　0 0 0 0 b
SCON	Serial control	98H	(9F) SM0	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0 0 0 0　0 0 0 0 b
RSR	Reset status register	96H	-	-	-	-	-	BORF	-	SWRF	Power-on, 0 0 0 0　0 0 0 0 b Brown-out, 0 0 0 0　0 1 0 U b Software, 0 0 0 0　0 U 0 1 b Others, 0 0 0 0　0 U 0 U b
P1	Port 1	90H	(97) PWM4 SPCLK	(96) PWM3 MISO	(95) PWM2 MOSI	(94) PWM1 __ SS	(93) PWM0	(92)	(91) T2EX	(90) T2	1 1 1 1　1 1 1 1 b
AUXR	Auxiliary register	8EH	-	-	-	-	-	-	-	ALEOFF	0 0 0 0　0 0 0 0 b
TH1	Timer 1 high byte	8DH									0 0 0 0　0 0 0 0 b
TH0	Timer 0 high byte	8CH									0 0 0 0　0 0 0 0 b
TL1	Timer 1 low byte	8BH									0 0 0 0　0 0 0 0 b
TL0	Timer 0 low byte	8AH									0 0 0 0　0 0 0 0 b
TMOD	Timer 0 and 1 mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	0 0 0 0　0 0 0 0 b
TCON	Timer 0 and 1control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0 0 0 0　0 0 0 0 b
PCON	Power control	87H	SMOD	-	-	POF	GF1	GF0	PD	IDL	Power-on, 0 0 0 1　0 0 0 0 b Others, 0 0 0 U　0 0 0 0 b
P0OR	P0 option register	86H	-	-	-	-	-	-	-	P0UP	0 0 0 0　0 0 0 0 b
DPH	Data pointer high byte	83H									0 0 0 0　0 0 0 0 b
DPL	Data pointer low byte	82H									0 0 0 0　0 0 0 0 b
SP	Stack pointer	81H									0 0 0 0　0 1 1 1 b
P0	Port 0	80H	(87) A7	(86) A6	(85) A5	(84) A4	(83) A3	(82) A2	(81) A1	(80) A0	1 1 1 1　1 1 1 1 b

[1] ( ) item means the bit address in bit-addressable SFRs.
[2] Reset value symbol description. 0: logic 0, 1: logic 1, U: unchanged, X: see **[4]** ~ **[7]**.
[3] These SFRs have TA protected writing.
[4] BOF has different power-on reset value according to CBODEN (CONFIG2.7) and CBORST (CONFIG2.4). See Table 21–1. BOF Reset Value.
[5] BOS is a read-only flag decided by V_{DD} level while Brown-out detection is enabled.
[6] These SFRs have bits which are initialized after specified reset by loading certain bits in CONFIG bytes. See Section 24. "CONFIG BYTES" on page 116 for details.

Note that bits marked in "-" must be kept in their own initial states. Users should never change their values.

7. GENERAL 80C51 SYSTEM CONTROL

A or ACC – Accumulator (bit-addressable)

7	6	5	4	3	2	1	0
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: E0H   reset value: 0000 0000b

Bit	Name	Description
7:0	ACC[7:0]	**Accumulator.** The A or ACC register is the standard 8051 accumulator for arithmetic operation.

B – B Register (bit-addressable)

7	6	5	4	3	2	1	0
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: F0H   reset value: 0000 0000b

Bit	Name	Description
7:0	B[7:0]	**B register.** The B register is the other accumulator of the standard 8051. It is used mainly for MUL and DIV operations.

SP – Stack Pointer

7	6	5	4	3	2	1	0
			SP[7:0]				
			r/w				

Address: 81H   reset value: 0000 0111b

Bit	Name	Description
7:0	SP[7:0]	**Stack pointer.** The Stack Pointer stores the scratch-pad RAM address where the stack begins. It is incremented before data is stored during PUSH or CALL instructions. Note that the default value of SP is 07H. It causes the stack to begin at location 08H.

DPL – Data Pointer Low Byte

7	6	5	4	3	2	1	0
			DPL[7:0]				
			r/w				

Address: 82H   reset value: 0000 0000b

Bit	Name	Description
7:0	DPL[7:0]	**Data pointer low byte.** This is the low byte of the standard 8051 16-bit data pointer. DPL combined with DPH serve as a 16-bit data pointer DPTR to address non-scratch-pad memory or Program Memory.