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8-BIT MICROCONTROLLER

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1. GENERAL DESCRIPTION

The N79E352(R) is an 8-bit Turbo 51 microcontroller which has Flash EPROM programmable hardware writer. The instruction set of the N79E352(R) is fully compatible with the standard 8052. The N79E352(R) contains a 8Kbytes of main Flash EPROM; a 256 bytes of RAM; 128 bytes NVM Data Flash EPROM; three 16-bit timer/counters; 2-channel 8-bit PWM; 1-channel UART and 1 additional input capture. These peripherals are supported by 11 interrupt sources four-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the N79E352(R) allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security. N79E352(R) is designed for cost effective applications which can serve industrial devices, and other low power applications.

2. FEATURES

- Fully static design 8-bit Turbo 51 CMOS microcontroller up to 24MHz when VDD=4.5V to 5.5V, 12MHz when VDD=2.7V to 5.5V, and 4MHz when VDD=2.4V to 5.5V.
- 8K bytes of AP Flash EPROM, with external writer programmable mode.
- 256 bytes of on-chip RAM.
- 128 bytes NVM Data Flash EPROM for customer data storage used and 10k writer cycles.
- Instruction-set compatible with MCS-51.
- On-chip configurable RC oscillator: 22.1184MHz/11.0592MHz (selectable by config bit) with ±2% accuracy, at 5V voltage and 25°C condition. (±2% accuracy is only for N79E352R.)
- Three 16-bit timer/counters.
- One input capture.
- 11 interrupt source with four levels of priority.
- One enhanced full duplex serial port with framing error detection and automatic address recognition.
- 4 outputs mode and TTL/Schmitt trigger selectable Port.
- Programmable Watchdog Timer with 20KHz internal RC clock can wake-up the power down mode, and have very low power under 10uA at 5V.
- Two-channel 8-bit PWM.
- One I2C communication port.
- Dual 16-bit Data Pointers.
- Software programmable access cycle to external RAM/peripherals.
- Eight keypads interrupt inputs with sharing the same interrupt source.
- LED drive capability (20mA) on all port pins, total 100mA.
- Low Voltage (3 levels) Detection interrupt and reset.
- Industrial temperature grade -40°C~85°C.
- Packages:
  - ■Lead Free (RoHS) DIP40: N79E352RADG
  - ■Lead Free (RoHS) PLCC44: N79E352RAPG
  - ■Lead Free (RoHS) PQFP44: N79E352RAFG
  - ■Lead Free (RoHS) LQFP48: N79E352RALG
  - ■Lead Free (RoHS) DIP40: N79E352ADG
  - ■Lead Free (RoHS) PLCC44: N79E352APG
  - ■Lead Free (RoHS) PQFP44: N79E352AFG
  - ■Lead Free (RoHS) LQFP48: N79E352ALG
  - -

3. PARTS INFORMATION LIST

3.1 Lead Free (RoHS) Parts information list

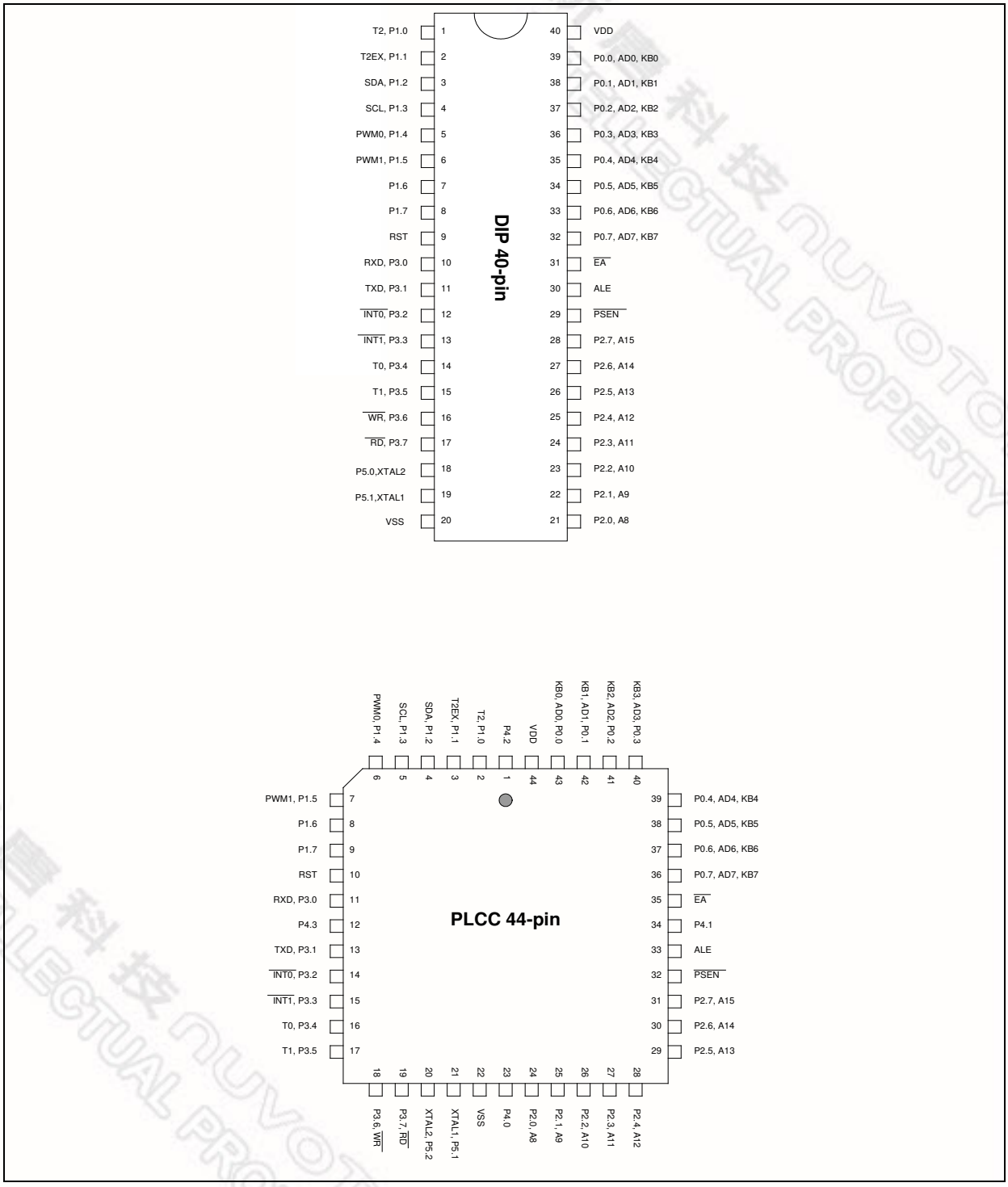
PART NO.	EPROM FLASH SIZE	RAM	NVM FLASH EPROM	INTERNAL RC OSCILLATOR ACCURACY[1]	PACKAGE
N79E352RADG	8KB	256B	128B	22.1184MHz ± 2%	DIP-40 Pin
N79E352RAPG	8KB	256B	128B	22.1184MHz ± 2%	PLCC-44 Pin
N79E352RAFG	8KB	256B	128B	22.1184MHz ± 2%	PQFP-44 Pin
N79E352RALG	8KB	256B	128B	22.1184MHz ± 2%	LQFP-48 Pin
N79E352ADG	8KB	256B	128B	22MHz ± 25%	DIP-40 Pin
N79E352APG	8KB	256B	128B	22MHz ± 25%	PLCC-44 Pin
N79E352AFG	8KB	256B	128B	22MHz ± 25%	PQFP-44 Pin
N79E352ALG	8KB	256B	128B	22MHz ± 25%	LQFP-48 Pin

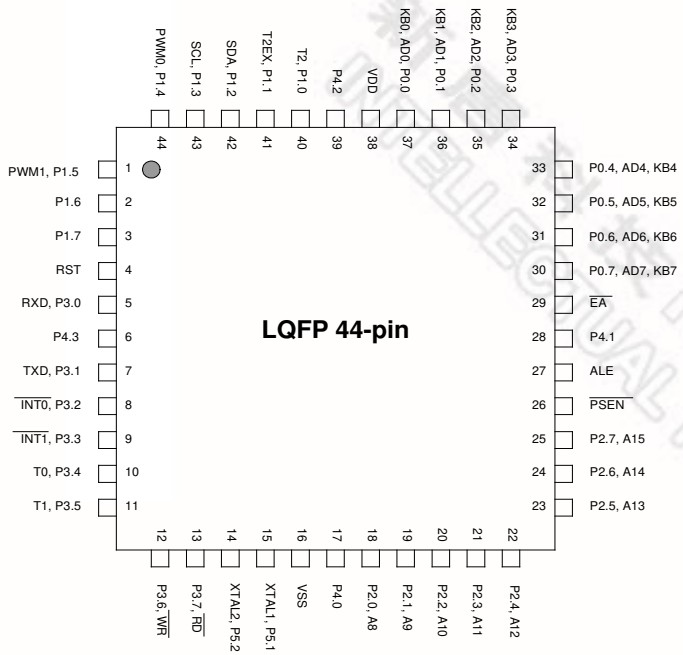
Table 3-1: Lead Free (RoHS) Parts information list

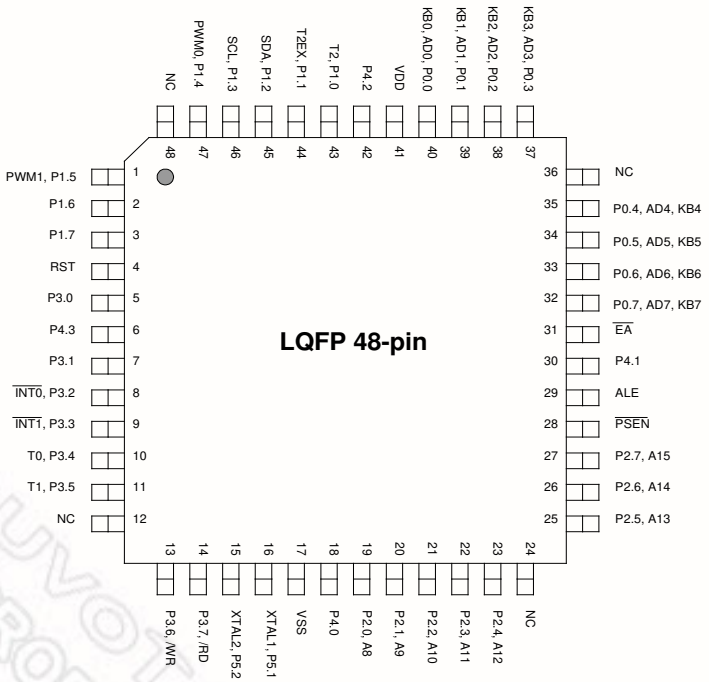
Note:

1. Factory calibration condition: V_{DD}=5.0V±10%, TA = 25°C

4. PIN CONFIGURATIONS




LQFP 44-pin
1 PWM1, P1.5
2 P1.6
3 P1.7
4 RST
5 RXD, P3.0
6 P4.3
7 TXD, P3.1
8 INT0, P3.2
9 INT1, P3.3
10 T0, P3.4
11 T1, P3.5
12 P3.6, WR
13 P3.7, RD
14 XTAL2, P5.2
15 XTAL1, P5.1
16 VSS
17 P4.0
18 P2.0, A8
19 P2.1, A9
20 P2.2, A10
21 P2.3, A11
22 P2.4, A12
23 P2.5, A13
24 P2.6, A14
25 P2.7, A15
26 PSEN
27 ALE
28 P4.1
29 EA
30 P0.7, AD7, KB7
31 P0.6, AD6, KB6
32 P0.5, AD5, KB5
33 P0.4, AD4, KB4
34 KB3, AD3, P0.3
35 KB2, AD2, P0.2
36 KB1, AD1, P0.1
37 KB0, AD0, P0.0
38 VDD
39 P4.2
40 T2, P1.0
41 T2EX, P1.1
42 SDA, P1.2
43 SCL, P1.3
44 PWM0, P1.4


LQFP 48-pin
1 PWM1, P1.5
2 P1.6
3 P1.7
4 RST
5 P3.0
6 P4.3
7 P3.1
8 INT0, P3.2
9 INT1, P3.3
10 T0, P3.4
11 T1, P3.5
12 NC
13 P3.6, /WR
14 P3.7, /RD
15 XTAL2, P5.2
16 XTAL1, P5.1
17 VSS
18 P4.0
19 P2.0, A8
20 P2.1, A9
21 P2.2, A10
22 P2.3, A11
23 P2.4, A12
24 NC
25 P2.5, A13
26 P2.6, A14
27 P2.7, A15
28 PSEN
29 ALE
30 P4.1
31 EA
32 P0.7, AD7, KB7
33 P0.6, AD6, KB6
34 P0.5, AD5, KB5
35 P0.4, AD4, KB4
36 NC
37 KB3, AD3, P0.3
38 KB2, AD2, P0.2
39 KB1, AD1, P0.1
40 KB0, AD0, P0.0
41 VDD
42 P4.2
43 T2, P1.0
44 T2EX, P1.1
45 SDA, P1.2
46 SCL, P1.3
47 PWM0, P1.4
48 NC

5. PIN DESCRIPTIONS

SYMBOL	Alternate Function 1	Alternate function 2	Type	DESCRIPTIONS
$\overline{EA}$			I	**EXTERNAL ACCESS ENABLE**: This pin forces the processor to execute out of external ROM. It should be kept high to access internal ROM. The ROM address and data will not be present on the bus if $\overline{EA}$ pin is high and the program counter is within internal ROM area. Otherwise they will be present on the bus.
$\overline{PSEN}$			O	**PROGRAM STORE ENABLE**: $\overline{PSEN}$ enables the external ROM data onto the Port 0 address/data bus during fetch and MOVC operations. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs from this pin.
ALE			O	**ADDRESS LATCH ENABLE**: ALE is used to enable the address latch that separates the address from the data on Port 0.
XTAL1	P5.1		I/O	**CRYSTAL1**: This is the crystal oscillator input. This pin may be driven by an external clock or configurable i/o pin, P5.1.
XTAL2	P5.0		I/O	**CRYSTAL2**: This is the crystal oscillator output. It is the inversion of XTAL1. Also a configurable i/o pin, P5.0.
VDD			P	**POWER SUPPLY**: Supply voltage for operation.
VSS			P	**GROUND**: Ground potential.
RST				**RESET:** A high on this pin for two machine cycles while the oscillator is running resets the device.
P0.0	KB0	AD0	I/O	**PORT0:** Support 4 mode output and 2 mode input. Multifunction pins for AD0-7and KB0-7.
P0.1	KB1	AD1	I/O	
P0.2	KB2	AD2	I/O	
P0.3	KB3	AD3	I/O	
P0.4	KB4	AD4	I/O	
P0.5	KB5	AD5	I/O	
P0.6	KB6	AD6	I/O	
P0.7	KB7	AD7	I/O	
P1.0		T2	I/O	**PORT1:** Support 4 mode output and 2 mode input. Multifunction pins for SDA & SCL (I2C), T2, T2EX and PWM0-1.
P1.1		T2EX	I/O	
P1.2		SDA	I/O	
P1.3		SCL	I/O	
P1.4		PWM0	I/O	
P1.5		PWM1	I/O	
P1.6	ICPDAT		I/O	
P1.7	ICPCLK		I/O	

P2.0		A8	I/O	**PORT2:** Support 4 mode output and 2 mode input. Multifunction pins for A8-A15,.
P2.1		A9	I/O	
P2.2		A10	I/O	
P2.3		A11	I/O	
P2.4		A12	I/O	
P2.5		A13	I/O	
P2.6		A14	I/O	
P2.7		A15	I/O	
P3.0		RXD	I/O	**PORT3:** Support 4 mode output and 2 mode input. Multifunction pins for RXD & TXD (uart), /INT0, /INT1, T0, T1, /WR and /RD.
P3.1		TXD	I/O	
P3.2		/INT0	I/O	
P3.3		/INT1	I/O	
P3.4		T0	I/O	
P3.5		T1	I/O	
P3.6		/WR	I/O	
P3.7		/RD	I/O	
P4.0			I/O	**PORT4:** Quasi output with internal pull up.
P4.1			I/O	
P4.2			I/O	
P4.3			I/O	

* Note: TYPE I: input, O: output, I/O: bi-directional.

In application if any pins need external pull-up, it is recommended to add a pull-up resistor (10kΩ) between pin and power (V_{DD}) instead of directly wiring pin to V_{DD} for enhancing EMC.

6. FUNCTIONAL DESCRIPTION

N79E352(R) architecture consist of a 4T 8051 core controller surrounded by various registers, 8K bytes Flash EPROM, 256 bytes of RAM, 128 bytes NVM Data Flash EPROM; three timer/counters, one UART serial port, one I2C serial port, eight keyboard interrupt input, 2-channel PWM with 8-bit counter and Flash EPROM program by Writer.

6.1 On-Chip Flash EPROM

N79E352(R) includes one 8K bytes of main Flash EPROM for application program which need Writer to program the Flash EPROM.

6.2 I/O Ports

N79E352(R) has four 8-bit, one 4-bit port and one 2-bit port, with at least 36 I/O pins. All ports (except port 4) can be used as four outputs mode when it may set by PxM1.y and PxM2.y registers, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as general I/O port as open drain circuit. All ports can be used bi-directional and these are as I/O ports. These ports are not true I/O, but rather are pseudo-I/O ports. This is because these ports have strong pull-downs and weak pull-ups.

6.3 Serial I/O

N79E352(R) has one UART serial port that is functionally similar to the serial port of the original 8052 family. However the serial port on N79E352(R) can operate in different modes in order to obtain timing similarity as well. The Serial port has the enhanced features of Automatic Address recognition and Frame Error detection.

6.4 Timers

The device has total three 16-bit timers; two 16-bit timers that have functions similar to the timers of the 8052 family, and third timer is capable to function as timer and also provide capture support. When used as timers, user has a choice to set 12 or 4 clocks per count that emulates the timing of the original 8052. Each timer's count value is stored in two SFR locations that can be written or read by software. There are also some other SFRs associated with the timers that control their mode and operation.

6.5 Interrupts

The Interrupt structure in N79E352(R) is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased.

6.6 Data Pointers

The original 8052 had only one 16-bit Data Pointer (DPL, DPH). In the N79E352(R), there is an additional 16-bit Data Pointer (DPL1, DPH1). This new Data Pointer uses two SFR locations which were unused in the original 8052. In addition there is an added instruction, DEC DPTR (op-code A5H), which helps in improving programming flexibility for the user.

6.7 Architecture

N79E352(R) is based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

6.7.1 ALU

The ALU is the heart of the N79E352(R). It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used in Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

6.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in N79E352(R). Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

6.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

6.7.4 Program Status Word:

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

6.7.5 Scratch-pad RAM

N79E352(R) has a 256 bytes on-chip scratch-pad RAM. These can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

6.7.6 Stack Pointer

N79E352(R) has an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM. Hence the size of the stack is limited by the size of this RAM.

6.8 Power Management

Like the standard 80C52, the N79E352(R) also has IDLE and POWER DOWN modes of operation. The N79E352(R) provides a new Economy mode which allow user to switch the internal clock rate divided by either 4, 64 or 1024. In the IDLE mode, the clock to the CPU core is stopped while the timers, serial ports and interrupts clock continue to operate. In the POWER DOWN mode, all the clock are stopped and the chip operation is completely stopped. This is the lowest power consumption state.

7. MEMORY ORGANIZATION

N79E352(R) separates the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

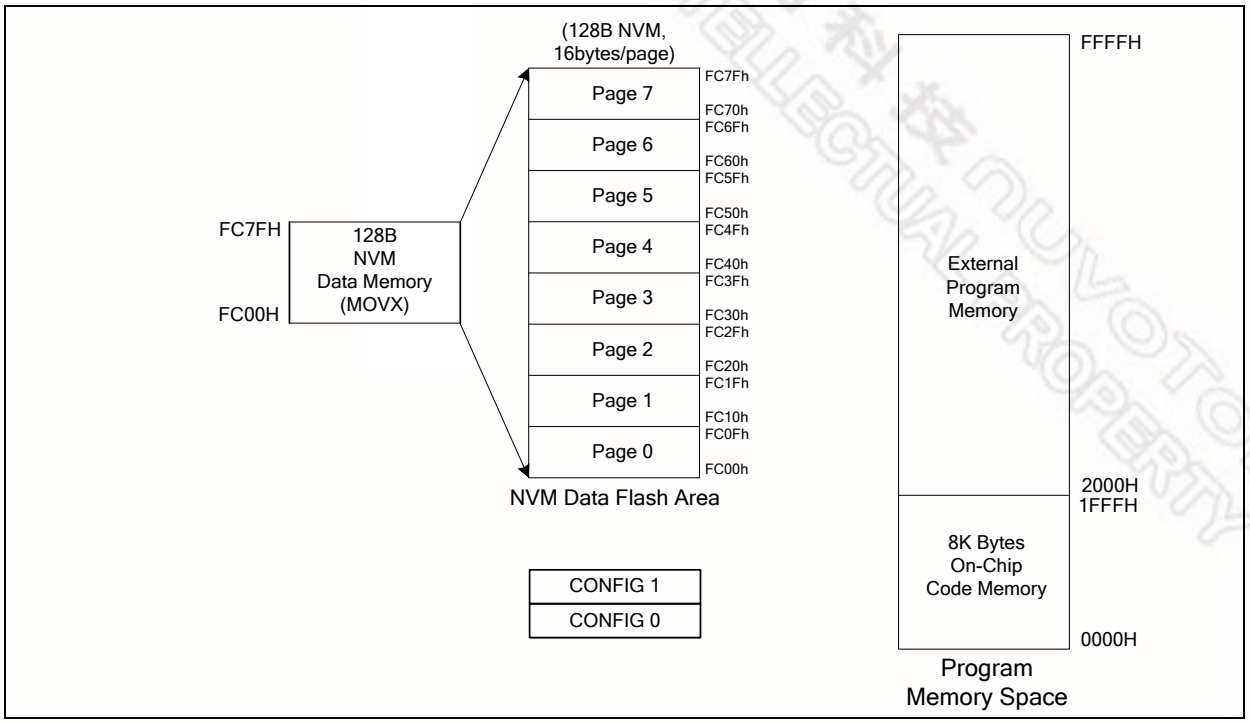


Figure 7-1: N79E352(R) Memory Map

7.1 Program Memory (on-chip Flash)

The Program Memory on N79E352(R) can be up to 8K bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

7.2 Data Memory

The N79E352(R) has NVM data memory of 128 bytes for customer's data store used. The NVM data memory has 8 pages area and each page has 16 bytes. The N79E352(R) can access up to 64Kbytes of external Data Memory. This memory region is accessed by the MOVX instructions. For NVM s/w read access, user require to set EnNVM bit, otherwise, the access will goes to external data memory. N79E352(R) has the standard 256 bytes of on-chip Scratchpad RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing. Since the Scratchpad RAM is only 256 bytes, it can be used only when data contents are small.

7.3 Scratch-pad RAM and Register Map

As mentioned before, N79E352(R) has separate Program and Data Memory areas. The on-chip 256 bytes scratch pad RAM is in addition to the external memory. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

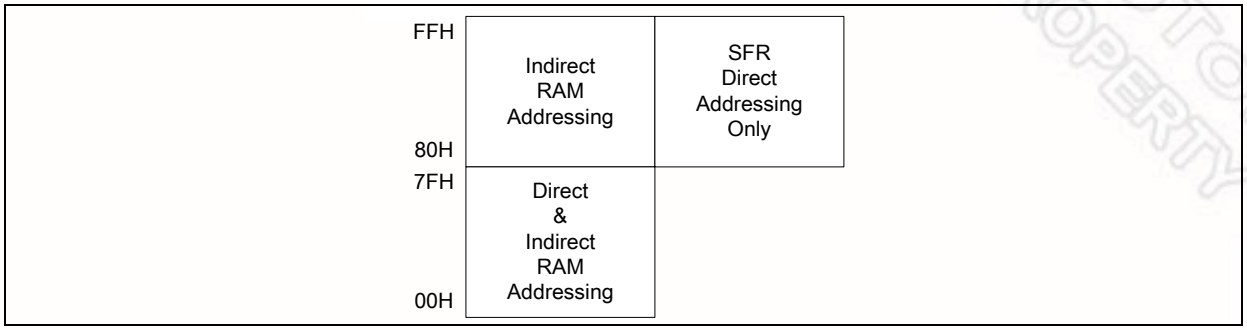


Figure 7-2: N79E352(R) RAM and SFR Memory Map

Since the scratch-pad RAM is only 256 bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are illustrated in next figure.

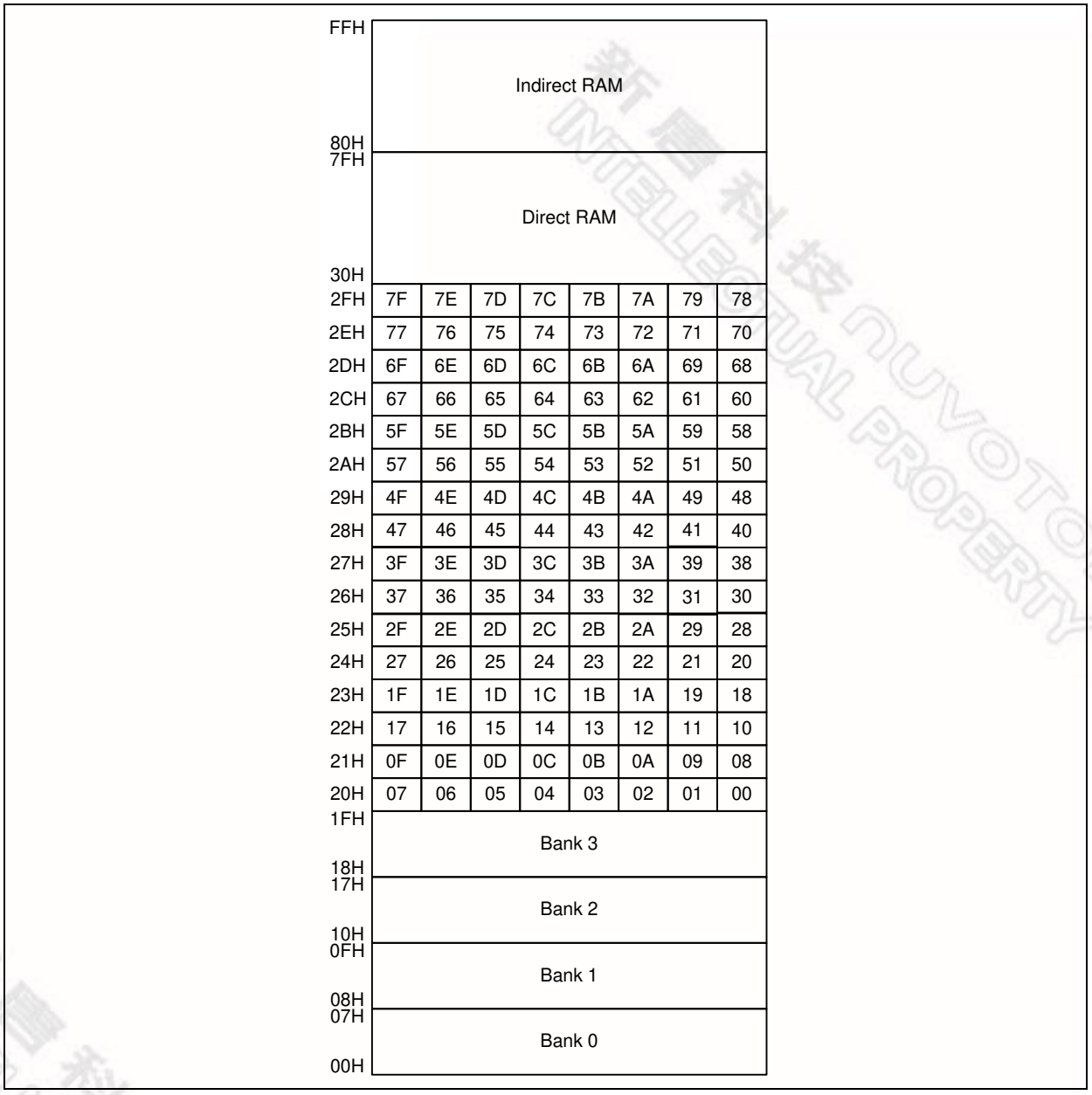


Figure 7-3: Scratch-pad RAM

7.3.1 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at any one time N79E352 can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

7.3.2 Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

7.3.3 Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

8. SPECIAL FUNCTION REGISTERS

The N79E352(R) uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes.

The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where one wishes to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The N79E352(R) contains all the SFRs present in the standard 8052. However, some additional SFRs have been added. In some cases unused bits in the original 8052 have been given new functions. The list of SFRs is as follows. The table is condensed with eight locations per row. Empty locations indicate that there are no registers at these addresses. When a bit or register is not implemented, it will read high.

8.1 SFR Location Table

F8	IP1								FF
F0	B							IP1H	F7
E8	EIE	KBL			PORTS	P5M1	P5M2		EF
E0	ACC				CCL0	CCH0			E7
D8	WDCON		PWM0L	PWM1L	PWMCON1				DF
D0	PSW							PWMCON3	D7
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	NVMCON	NVMDAT	CF
C0	I2CON	I2ADDR	ROMMAP		PMR	STATUS	NVMADDR	TA	C7
B8	IP0	SADEN			I2DATA	I2STATUS	I2CLK	I2TIMER	BF
B0	P3	P0M1	P0M2	P1M1	P1M2	P2M1	P2M2	IP0H	B7
A8	IE	SADDR							AF
A0	P2	KBI	AUXR1	CAPCON0	CAPCON1	P4			A7
98	SCON	SBUF					P3M1	P3M2	9F
90	P1				P5				97
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON		8F
80	P0	SP	DPL	DPH	DPL1	DPH1	DPS	PCON	87

Note: The SFRs in the column with dark borders are bit-addressable.

Table 8- 1: Special Function Register Location Table

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
IP1	INTERRUPT PRIORITY 1	F8H	PCAP	PBO	-	PWDI	-	-	PKB	PI2	00x0 xx00B
IP1H	INTERRUPT HIGH PRIORITY 1	F7H	PCAPH	PBOH	-	PWDIH	-	-	PKBH	PI2H	00x0 xx00B
B	B REGISTER	F0H	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	0000 0000B
P5M2	PORT 5 OUTPUT MODE 2	EEH	-	-	-	-	-	-	P5M2.1	P5M2.0	CONFIG0.PMODE=1; Xxxx xx00B CONFIG0.PMODE=0; Xxxx xx11B
P5M1	PORT 5 OUTPUT MODE 1	EDH	-	-	-	-	-	ENCLK	P5M1.1	P5M1.0	CONFIG0.PMODE=1; Xxxx x000B CONFIG0.PMODE=0; Xxxx x011B
PORTS	PORT SHMITT REGISTER	ECH	-	-	P5S	-	P3S	P2S	P1S	P0S	xx0x 0000B
KBL	KEYBOARD LEVEL REGISTER	E9H	KBL.7	KBL.6	KBL.5	KBL.4	KBL.3	KBL.2	KBL.1	KBL.0	0000 0000B
EIE	INTERRUPT ENABLE 1	E8H	ECPTF	EBO	-	EWDI	-	-	EKB	EI2	00x0 xx00B
CCH0	INPUT CAPTURE 0 HIGH	E5H	CCH0.7	CCH0.6	CCH0.5	CCH0.4	CCH0.3	CCH0.2	CCH0.1	CCH0.0	0000 0000B
CCL0	INPUT CAPTURE 0 LOW	E4H	CCL0.7	CCL0.6	CCL0.5	CCL0.4	CCL0.3	CCL0.2	CCL0.1	CCL0.0	0000 0000B
ACC	ACCUMULATOR	E0H	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	0000 0000B
PWMCON1	PWM CONTROL REGISTER 1	DCH	PWMRUN	-	-	CLRPWM	-	-	-	-	0xx0 xxxxB
PWM1L	PWM 1 LOW BITS REGISTER	DBH	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0	0000 0000B
PWM0L	PWM 0 LOW BITS REGISTER	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	0000 0000B
WDCON	WATCH-DOG CONTROL	D8H	WDRUN	POR	-	-	WDIF	WTRF	EWRST	WDCLR	POR: X1xx 0000B External reset: Xxxx 0xx0B Watchdog reset: Xxxx 01x0B
PWMCON3	PWM CONTROL REGISTER 3	D7H	-	-	PWM1OE	PWM0OE	PCLK.1	PCLK.0	FP1	FP0	Xx00 0000B
PSW	PROGRAM STATUS WORD	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	0000 0000B
NVMDATA	NVM DATA	CFH	NVMDATA.7	NVMDATA.6	NVMDATA.5	NVMDATA.4	NVMDATA.3	NVMDATA.2	NVMDATA.1	NVMDATA.0	0000 0000B
NVMCON	NVM CONTROL	CEH	EER	EWR	EnNVM	-	-	-	-	-	000x xxxxB
TH2	TIMER 2 MSB	CDH	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0	0000 0000B
TL2	TIMER 2 LSB	CCH	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0	0000 0000B
RCAP2H	TIMER 2 RELOAD MSB	CBH	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0	0000 0000B
RCAP2L	TIMER 2 RELOAD LSB	CAH	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0	0000 0000B
T2MOD	TIMER 2 MODE	C9H	-	-	-	ICEN0	T2CR	1	T2OE	DCEN	Xxx0 0100B
T2CON	TIMER 2 CONTROL	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL	0000 0000B
TA	TIMED ACCESS PROTECTION	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	0000 0000B
NVMADDR	NVM LOW BYTE ADDRESS	C6H	NVMADDR.7	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0	0000 0000B
STATUS	STATUS REGISTER	C5H	-	-	-	-	-	-	SPTA0	SPRA0	Xxxx xx00B
PMR	POWER MANAGEMENT REGISTER	C4H	CD1	CD0	SWB	-	-	ALE-OFF	-	-	010x xxxxB
ROMMAP	ROMMAP REGISTER	C2H	WS	1	-	-	-	1	1	0	01xxx110B
I2ADDR	I2C ADDRESS1	C1H	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	xxxxxxx0B

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
I2CON	I2C CONTROL REGISTER	C0H	-	ENSI	STA	STO	SI	AA	-	-	x00000xxB
I2TIMER	I2C TIMER COUNTER REGISTER	BFH	-	-	-	-	-	ENTI	DIV4	TIF	Xxxx x000B
I2CLK	I2C CLOCK RATE	BEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	0000 0000B
I2STATUS	I2C STATUS	BDH	I2STATUS.7	I2STATUS.6	I2STATUS.5	I2STATUS.4	I2STATUS.3	I2STATUS.2	I2STATUS.1	I2STATUS.0	1111 1000B
I2DAT	I2C DATA	BCH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	xxxxxxxxB
SADEN	SLAVE ADDRESS MASK	B9H	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0	00000000B
IP0	INTERRUPT PRIORITY	B8H	-	-	PT2	PS	PT1	PX1	PT0	PX0	Xx00 0000B
IP0H	INTERRUPT HIGH PRIORITY	B7H	-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	Xx00 0000B
P2M2	PORT 2 OUTPUT MODE 2	B6H	P2M2.7	P2M2.6	P2M2.5	P2M2.4	P2M2.3	P2M2.2	P2M2.1	P2M2.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B
P2M1	PORT 2 OUTPUT MODE 1	B5H	P2M1.7	P2M1.6	P2M1.5	P2M1.4	P2M1.3	P2M1.2	P2M1.1	P2M1.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B
P1M2	PORT 1 OUTPUT MODE 2	B4H	P1M2.7	P1M2.6	P1M2.5	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B
P1M1	PORT 1 OUTPUT MODE 1	B3H	P1M1.7	P1M1.6	P1M1.5	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B
P0M2	PORT 0 OUTPUT MODE 2	B2H	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0	1111 1111B
P0M1	PORT 0 OUTPUT MODE 1	B1H	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0	1111 1111B
P3	PORT3	B0H	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	1111 1111B
			/RD	/WR	T1	T0	/INT1	/INT0	TXD	RXD	
SADDR	SLAVE ADDRESS	A9H	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0	0000 0000B
IE	INTERRUPT ENABLE	A8H	EA	-	ET2	ES	ET1	EX1	ET0	EX0	0x00 0000B
P4	PORT4	A5H	-	-	-	-	P4.3	P4.2	P4.1	P4.0	Xxxx 1111B
CAPCON1	CAPTURE CONTROL 1	A4H	0	T0CC	-	-	ENF0	-	-	CPTF0	00xx 0xx0B
CAPCON0	CAPTURE CONTROL 0	A3H	-	-	-	-	CCT0.1	CCT0.0	-	-	Xxxx 00xxB
AUXR1	AUX FUNCTION REGISTER 1	A2H	KBF	BOD	BOI	LPBOV	SRST	BOV1	BOV0	BOS	0000 0000B
KBI	KEYBOARD INTERRUPT	A1H	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0	0000 0000B
P2	PORT 2	A0H	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	1111 1111B
			A15	A14	A13	A12	A11	A10	A9	A8	
P3M2	PORT 3 OUTPUT MODE 2	9FH	P3M2.7	P3M2.6	P3M2.5	P3M2.4	P3M2.3	P3M2.2	P3M2.1	P3M2.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
P3M1	PORT 3 OUTPUT MODE 1	9EH	P3M1.7	P3M1.6	P3M1.5	P3M1.4	P3M1.3	P3M1.2	P3M1.1	P3M1.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B
SBUF	SERIAL BUFFER	99H	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0	Xxxx xxxxB
SCON	SERIAL CONTROL	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	0000 0000B
P5	PORT5	94H	-	-	-	-	-	-	P5.1	P5.0	Xxxx xx11B
			-	-	-	-	-	-	XTAL1	XTAL2	
			-	-	-	-	-	-	-	CLKOUT	
P1	PORT 1	90H	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	1111 1111B
			-	-	PWM1	PWM0	SCL	SDA	T2EX	T2	
CKCON	CLOCK CONTROL	8EH	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	0000 0001B
TH1	TIMER HIGH 1	8DH	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0	0000 0000B
TH0	TIMER HIGH 0	8CH	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0	0000 0000B
TL1	TIMER LOW 1	8BH	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0	0000 0000B
TL0	TIMER LOW 0	8AH	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0	0000 0000B
TMOD	TIMER MODE	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	0000 0000B
TCON	TIMER CONTROL	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0000 0000B
PCON	POWER CONTROL	87H	SM0D	SMOD0	BOF	-	GF1	GF0	PD	IDL	001x 0000B
DPS	DATA POINTER SELECT	86H	-	-	-	-	-	-	-	DPS.0	Xxxx xxx0B
DPH1	DATA POINTER HIGH 1	85H	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0	0000 0000B
DPL1	DATA POINTER LOW 1	84H	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0	0000 0000B
DPH	DATA POINTER HIGH	83H	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0	0000 0000B
DPL	DATA POINTER LOW	82H	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0	0000 0000B
SP	STACK POINTER	81H	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0	0000 0111B
P0	PORT 0	80H	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	1111 1111B
			AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	
			KB7	KB6	KB5	KB4	KB3	KB2	KB1	KB0	

8.2 SFR Detail Bit Descriptions

PORT 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

Port 0 is an open-drain bi-directional I/O port. This port provides a multiplexed low order address/data bus during accesses to external memory. The ports also support alternate input function for Keyboard pins (KB0-7).

BIT	NAME	FUNCTION
7	P0.7	AD7 or KB7 or I/O pin by alternative.
6	P0.6	AD6 or KB6 or I/O pin by alternative.
5	P0.5	AD5 or KB5 or I/O pin by alternative.
4	P0.4	AD4 or KB4 or I/O pin by alternative.
3	P0.3	AD3 or KB3 or I/O pin by alternative.
2	P0.2	AD2 or KB2 or I/O pin by alternative.
1	P0.1	AD1 or KB1 or I/O pin by alternative.
0	P0.0	AD0 or KB0 or I/O pin by alternative.

Note: The initial value of the port is set by CONFIG0.PRHI bit. The default setting for CONFIG0.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG0.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

BIT	NAME	FUNCTION
7-0	SP.[7:0]	The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

BIT	NAME	FUNCTION
7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0

DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

BIT	NAME	FUNCTION
7-0	DPH.[7:0]	This is the high byte of the standard 8052 16-bit data pointer. This is the high byte of the DPTR 16-bit data pointer.

DATA POINTER LOW 1

Bit: 7 6 5 4 3 2 1 0

DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0

Mnemonic: DPL1 Address: 84h

BIT	NAME	FUNCTION
7-0	DPL1.[7:0]	This is the low byte of the new additional 16-bit data pointer that has been added to the N79E352(R). The user can switch between DPL, DPH and DPL1, DPH1 simply by setting register DPS = 1. The instructions that use DPTR will now access DPL1 and DPH1 in place of DPL and DPH. If they are not required they can be used as conventional register locations by the user.

DATA POINTER HIGH 1

Bit: 7 6 5 4 3 2 1 0

DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0

Mnemonic: DPH1 Address: 85h

BIT	NAME	FUNCTION
7-0	DPH1.[7:0]	This is the high byte of the new additional 16-bit data pointer that has been added to the N79E352(R). The user can switch between DPL, DPH and DPL1, DPH1 simply by setting register DPS = 1. The instructions that use DPTR will now access DPL1 and DPH1 in place of DPL and DPH. If they are not required they can be used as conventional register locations by the user.

DATA POINTER SELECT

Bit: 7 6 5 4 3 2 1 0

-	-	-	-	-	-	-	DPS.0

Mnemonic: DPS Address: 86h

BIT	NAME	FUNCTION
7-1	-	Reserved.
0	DPS	This bit is used to select either the DPL,DPH pair or the DPL1,DPH1 pair as the active Data Pointer. When set to 1, DPL1, DPH1 will be selected, otherwise DPL, DPH will be selected.

POWER CONTROL

Bit: 7 6 5 4 3 2 1 0

SMOD	SMOD0	BOF	-	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3.
6	SMOD0	0: Framing Error Detection Disable. SCON.7 (SM0/FE) bit is used as SM0 (standard 8052 function). 1: Framing Error Detection Enable. SCON.7 (SM0/FE) bit is used to reflect as Frame Error (FE) status flag.
5	BOF	0: Cleared by software. 1: Set automatically when a brownout reset or interrupt has occurred. Also set at power on.
4	-	Reserved.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: The CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.
0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

TIMER CONTROL

Bit:

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on

		$\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1) Timer/Counter 1 is stopped.

TIMER 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

BIT	NAME	FUNCTION
7-0	TL0.[7:0]	Timer 0 LSB.

TIMER 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

BIT	NAME	FUNCTION
7-0	TL1.[7:0]	Timer 1 LSB.

TIMER 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

BIT	NAME	FUNCTION
7-0	TH0.[7:0]	Timer 0 MSB.

TIMER 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

BIT	NAME	FUNCTION
7-0	TH1.[7:0]	Timer 1 MSB.

CLOCK CONTROL

Bit:	7	6	5	4	3	2	1	0
	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7-5	WD1~0	Watchdog timer mode select bits: These bits determine the time-out period for the watchdog timer. In all four time-out options the reset time-out is 512 clocks more than the interrupt time-out period.

WD1	WD0	Interrupt time-out	Reset time-out
0	0	2^6	$2^6 + 512$
0	1	2^9	$2^9 + 512$
1	0	2^{13}	$2^{13} + 512$
1	1	2^{15}	$2^{15} + 512$