Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Nuvoton 8051-based Microcontroller

N79E845
N79E844
N79E8432

Data Sheet

Version: A2.6

Table of Contents

1 General Description

The N79E845/844/8432 8-bit Turbo 51 (4T Mode) microcontroller is embedded with 16K[1]/8K/4K bytes Flash EPROM which can be programmed through universal hardware writer, serial ICP (In Circuit Program) programmer, software ISP function. The instruction sets of the N79E845/844/8432 is fully compatible with the standard 8052. The N79E845/844/8432 contains 16K/8K/4K bytes Application Flash EPROM (APROM) memory, 4 Kbytes Data Flash memory, and 2 Kbytes Load Flash EPROM (LDROM) memory; 256 bytes direct and indirect RAM, 256 bytes XRAM; 17 I/O with bit-addressable I/O ports; two 16-bit timers/counters; 7-channel multiplexed 10-bit A/D converter; 4-channel 10-bit PWM; three serial ports including a SPI, I^2C and an enhanced full duplex serial port; 2-level BOD voltage detection/reset, and power-on reset (POR). The N79E845/844/8432 also supports internal RC oscillator at the nominal frequency of 22.1184 MHz. The accuracy of RC oscillator (22.1184 MHz) is trimmed as ±1% under the condition of room temperature and V_{DD} = 5V before shipping from by factory trimming mechanism, which peripherals are supported by 14 sources of four-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the N79E845/844/8432 allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

The N79E845/844/8432 microcontroller, featuring wide operating voltage range, built-in rich analog and digital peripherals and non-volatile Flash memory, is widely suitable for general control and home appliances.

[1] For N79E845, Data Flash and APROM share 16 Kbytes space.

2 Features

- Core
  - Fully static design 8-bit Turbo 51 (4T) CMOS microcontroller
  - Instruction sets fully compatible with the MCS-51
- Operating voltage range
  - V_{DD} = 4.5V to 5.5V at F_{OSC} up to 24MHz
  - V_{DD} = 3.0V to 5.5V at Internal RC 22.1184MHz
  - V_{DD} = 2.4V to 5.5V at F_{OSC} = 4~12MHz or Internal RC 11.0592MHz
- Operating temperature range
  - -40°C ~85°C
- Clock Source
  - High-speed external oscillator:
    - Up to 24 MHz Crystal and resonator (enabled by CONFIG-bits)
  - Internal RC oscillator: 22.1184MHz/11.0592MHz (selectable by CONFIG-bits)
    - ±1% at V_{DD} = 5V and 25°C
    - ±3% at V_{DD} = 2.7V ~ 5.5V and 25°C
    - ±5% at V_{DD} = 2.7V ~ 5.5V and -10°C~+70°C
    - ±8% at V_{DD} = 2.7V ~ 5.5V and -40°C ~ 85°C
  - Flexible CPU clock source configurable by CONFIG-bits and software
  - 8-bit Programmable CPU clock divider(DIVM)
- On-chip Memory
  - 100,000 erase/write cycles
  - N79E845: 16 Kbytes shared by APROM and Data Flash depending on CONFIG-bits definitions
  - N79E844: 8 Kbytes APROM, 4 Kbytes Data Flash
  - N79E8432: 4 Kbytes APROM, 4 Kbytes Data Flash
  - APROM, LDROM and Data Flash security protection
  - Flash page size as 128 bytes
  - 256 bytes of on-chip direct/indirect RAM
  - 256 bytes of XRAM, accessed by MOVX instruction
  - On-chip Flash programmed through
    - Parallel H/W Writer mode
    - Serial In-Circuit-Program mode (ICP)
    - Software Implemented ISP (In-System-Program)
- I/O Ports
  - Maximum 17 I/O pins
  - All I/O pin besides P1.2 and P1.3 support 4 software configurable output modes
  - Software selectable TTL or Schmitt trigger input type per port
  - 14 interrupt sources with four levels of priority
  - LED drive capability 38mA on P10, P11, P14, P16, P17
  - LED drive capability 20mA on port 0 and port 3
- Timer/Counter
  - Two sets 16-bit Timers/Counters

- One 16-bit Timer with two channel of input captures

- Watchdog Timer
  - Programmable Watchdog Timer
  - Clock source supported by internal 10kHz ±50% accuracy RC oscillator
- Serial ports (UART, SPI, I^2C)
  - One set of enhanced full duplex UART port with framing error detection and automatic address recognition.
  - One set SPI with master/slave capability.
  - One set I^2C with master/slave capability
- PWM
  - 4 channels 10-bit PWM outputs with one brake/fault input
- KBI
  - 8-keypad interrupt inputs(KBI) with 8 falling/rising/both-edge detection pins selected by software
- ADC
  - 10-bit A/D converter
  - Up to 150 Ksps.(sample per second)
  - 7 analog input channels
- Brown-out Detector
  - 2-level (3.8V/2.7V) BOD detector
  - Supports interrupt and reset options
- POR (Power on Reset)
  - Threshold voltage levels as 2.0V
- Built-in power management.
  - Idle mode
  - Power-down mode with optionally enabled WDT functions
- Development Tools
  - Hardware writer
  - ICP programmer
  - ISP update APROM by UART port

3 Parts Information List

Table 3-1 Lead Free (RoHS) Parts Information List

PART NO.	APROM	LDROM	RAM	DATA FLASH	PACKAGE
N79E845AWG	16KB	2KB	512B	Share APROM	TSSOP-20 Pin
N79E844AWG	8KB	2KB	512B	4KB	TSSOP-20 Pin
N79E8432ASG	4KB	2KB	512B	4KB	SOP-16 Pin

4 Block Diagram

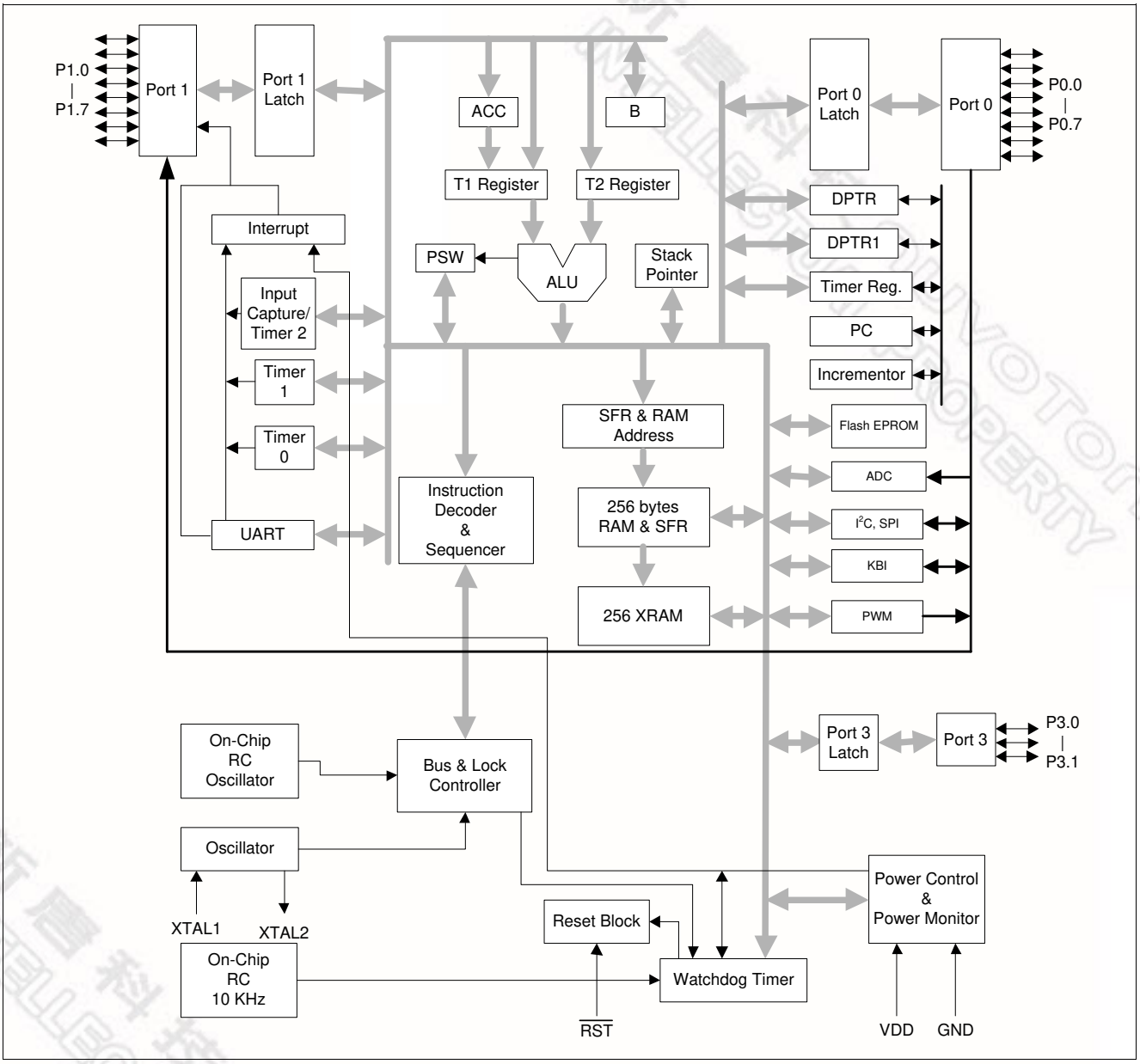

Figure 4–1 N79E845/844/8432 Function Block Diagram

5 Pin Configuration

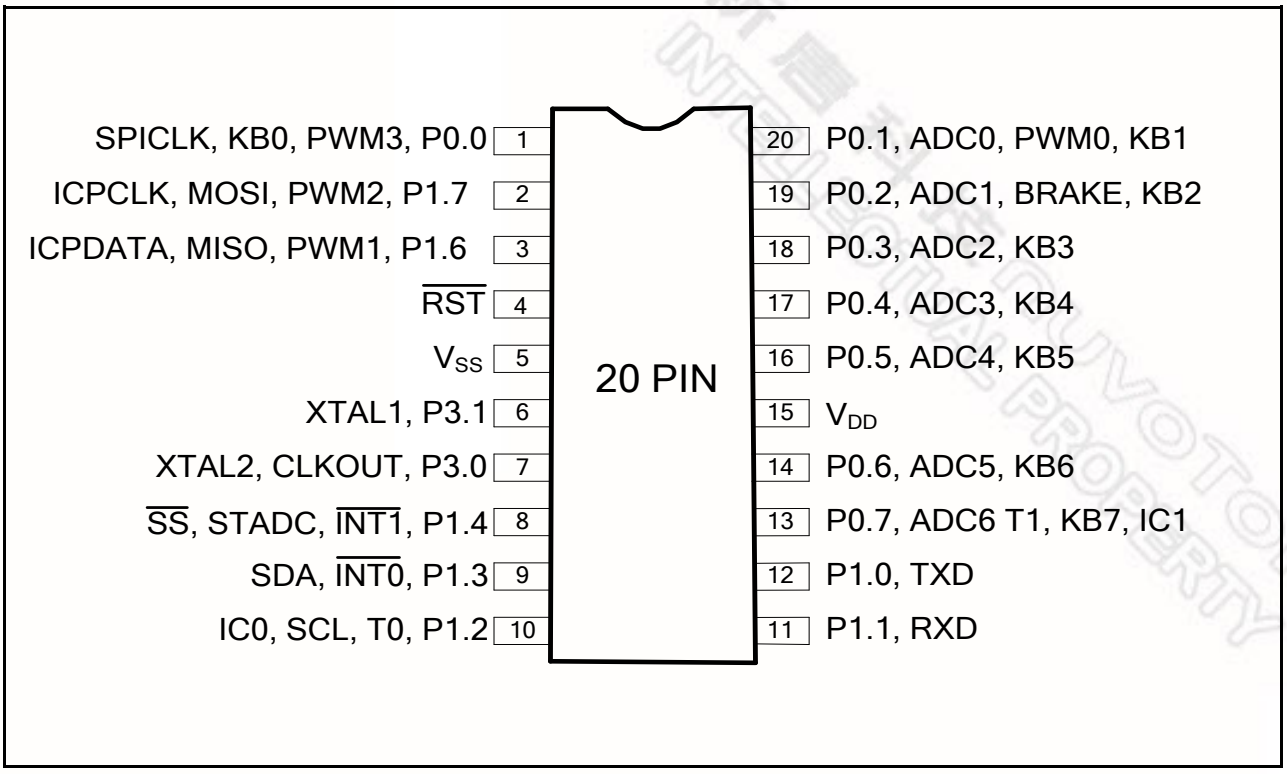

Figure 5–2 TSSOP/SOP 20- pin Assignment

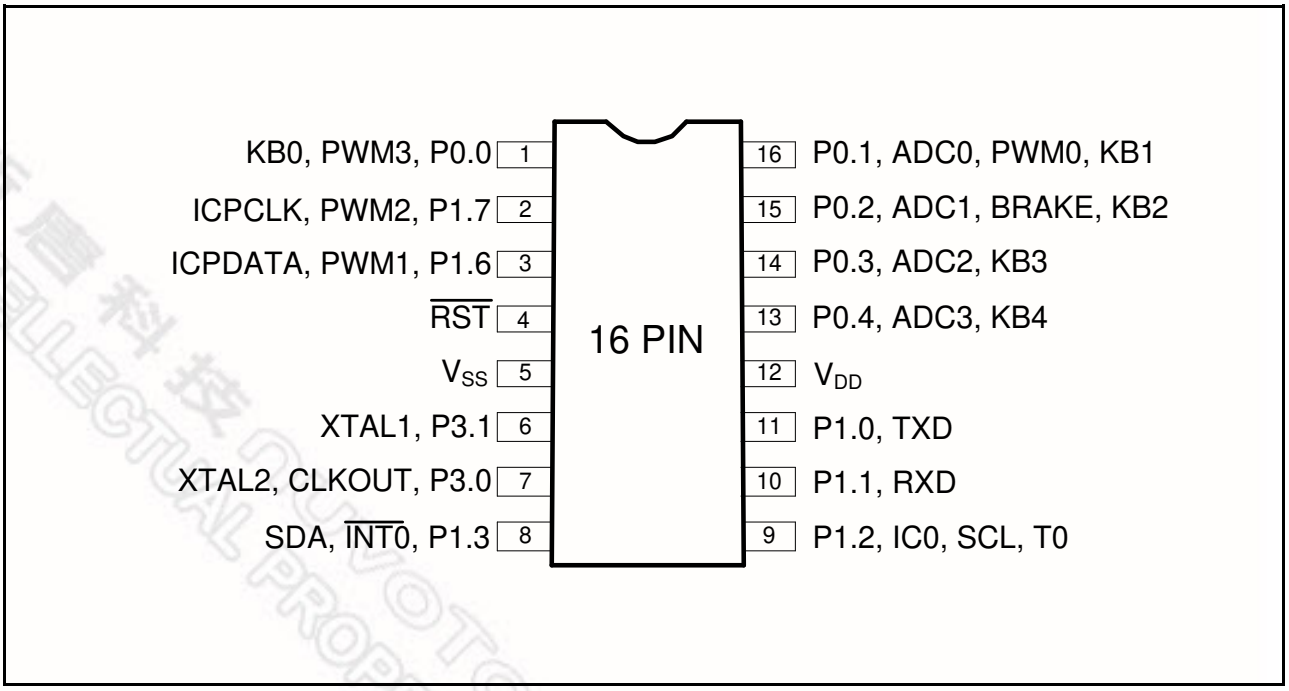

Figure 5–3 SOP 16- pin Assignment

Table 5–1 Pin Description

Pin number		Sym-	Alternate Function				Type	Description
SOP16	SOP20 TSSOP20		1	2	3			
12	15	V_{DD}					P	**POWER SUPPLY:** Supply voltage V_{DD} for operation.
5	5	V_{SS}					P	**GROUND:** Ground potential
4	4	/RST					I (ST)	**RESET:** Chip reset pin that is low active. Because reset pin has internal pull-up resistor (about 200 KΩ at V_{DD} = 5V), this pin can-not be floating. Reset pin should be connected to 100Ω pull-up resistor and 10uF pull-low capacitor.
1	1	P0.0	PWM3		KB0	SPICLK	I/O	**PORT0:** Port 0 has 4-type I/O port. Its multifunction pins are for PWM0, PWM3, T1, BRAKE, SPICLK, ADC0~ADC6 and KB0~KB7. ADC0 ~ADC6: ADC channel input. KB0 ~ KB7: Key Board Input The PWM0 and PWM3 is PWM output channel. T1: Timer 1 External Input SPICLK: SPI-1 clock pin
16	20	P0.1	PWM0	ADC0	KB1		I/O	
15	19	P0.2	BRAKE	ADC1	KB2		I/O	
14	18	P0.3		ADC2	KB3		I/O	
13	17	P0.4		ADC3	KB4		I/O	
-	16	P0.5		ADC4	KB5		I/O	
-	14	P0.6		ADC5	KB6		I/O	
-	13	P0.7	T1	ADC6	KB7	IC1	I/O	
11	12	P1.0	TXD				I/O	**PORT1:** Port 1 has 4-type I/O port. Its multifunction pins are for TXD, RXD, T0, /INT0, /INT1, SCL, SDA, STADC, ICPDAT, ICPCLK and /SS, MISO, MOSI. The TXD and RXD are UART port The SCL and SDA are I^2C function with open-drain port. The ICPDAT and ICPCLK are ICP (In Circuit Programming) function pin. The /SS, MISO, MOSI are SPI-1 function pins. The PWM1 and PWM2 are PWM output channel T0: Timer 0 External Input IC0/1: Input Capture pin
10	11	P1.1	RXD				I/O	
9	10	P1.2	T0		SCL	IC0	D	
8	9	P1.3	/INT0		SDA		D	

Table 5–1 Pin Description

Pin number		Sym-	Alternate Function				Type	Description
SOP16	SOP20 TSSOP20		1	2	3			
-	8	P1.4	/INT1	STADC		/SS	I/O	STADC: ADC trigger by external pin
3	3	P1.6	PWM1		ICPDAT	MISO	I/O	
2	2	P1.7	PWM2		ICPCLK	MOSI	I/O	
7	7	P3.0	XTAL2	CLKOUT			I/O	**PORT3:** Port 3 has 4-type I/O port. Its multifunction pins are for XTAL1, XTAL2 and CLKOUT, **CLKOUT:** Internal RC OSC/4 output pin.
6	6	P3.1	XTAL1				I/O	**XTAL2:** This is the output pin from the internal inverting amplifier. It emits the inverted signal of XTAL2. **XTAL1:** This is the output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.

[1] I/O type description I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pins, ST: Schmitt trigger.

6 Memory Organization

The N79E845/844/8432 has embedded Flash EPROM including 16K/8K/4K bytes Application Program Flash memory (APROM), fixed 4K bytes Data Flash (except the device with 16K APROM), fixed 2K bytes Load ROM Flash memory (LDROM) and CONFIG-bits. The N79E845/844/8432 also provides 256 bytes of on-chip direct/indirect RAM and 256 bytes of XRAM accessed by MOVX instruction.

For the device of 16K-bytes APROM, the APROM block and Data Flash block comprise the 16K bytes embedded Flash. The block size is CONFIG-bits/software configurable.

The N79E845/844/8432 is built with a CMOS page-erase. The page-erase operation erases all bytes within a page of 128 bytes.

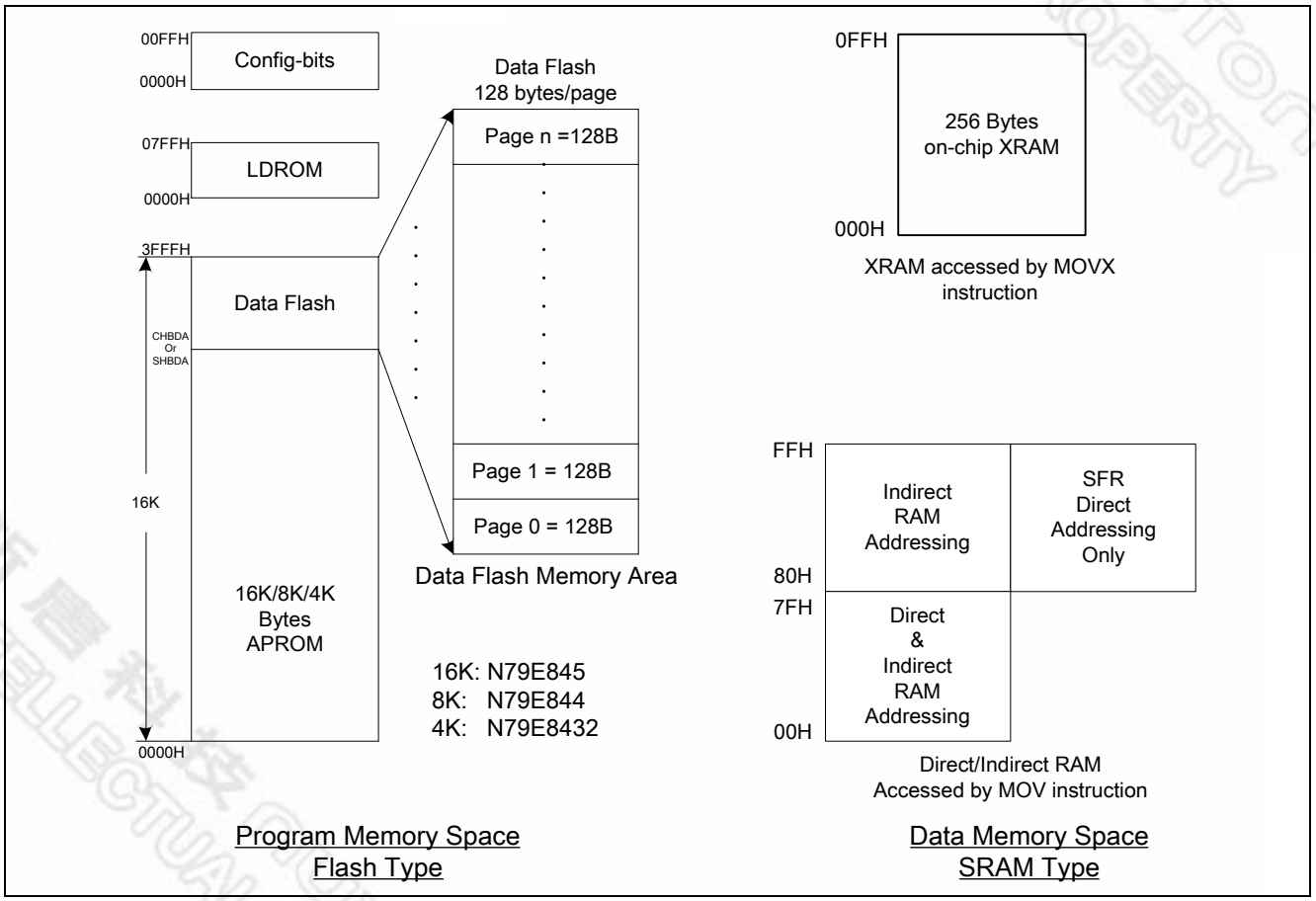

Figure 6-1 N79E845/844/8432 Memory Map

6.1 APROM Flash memory

The N79E845/844/8432 has **16K/8K/4K** Program Memory. All instructions are fetched for execution from this memory area. The MOVC instruction can also read this memory region.

The user application program is located in APROM. When CPU boots from APROM (CHPCON.BS=0), CPU starts executing the program from address 0000H. If the value of program counter (PC) is over the space of APROM, CPU will execute NOP operand and program counter increases one by one until PC reaches 3FFFH then it wraparounds to address 0000H of APROM, the CPU executes the application program again.

6.2 LDROM Flash Memory

Each device of the N79E845/844/8432 is equipped with 2 Kbytes LDROM stored the ISP application program. User may develop the ISP function in LDROM for updating application program or Data Flash. Similarly, APROM can also reprogram LDROM and Data Flash. The start address of LDROM is at 0000H corresponding to the physical address of the Flash memory. However, when CPU runs in LDROM, CPU automatically re-vectors the LDROM start address to 0000H, therefore user program regards the LDROM as an independent program memory, meanwhile, with all interrupt vectors that CPU provides.

6.3 CONFIG-bits

There are several bytes of CONFIG-bits located CONFIG-bits block. The CONFIG-bits define the CPU initial setting after power up or reset. Only hardware parallel writer or hardware ICP writer can erase/program CONFIG-bits. ISP program in LDROM can also erase/program CONFIG-bits.

6.4 On-chip Non-volatile Data Flash

The N79E845/844/8432 additionally has non-volatile Data Flash, which is non-volatile so that it remains its content even after the power is off. Therefore, in general application the user can write or read data which rules as parameters or constants. By the software path, SP mode can erase, written, or read the Data Flash only . Of course, hardware with parallel Programmer/Writer or ICP programmer can also access the Data Flash.

The Data Flash size is software adjustable in N79E845 (16KB) by updating the content of SHBDA. SHBDA[7:0] represents the high byte of 16-bit Data Flash start address and the low byte is hardware set to 00H. The value of SHBDA is loaded from the content of CONFIG1 (CHBDA) after all resets. The application program can dynamically adjust the Data Flash size by resetting SHBDA value. Once the Data Flash size is changed the APROM size is changed accordingly. SHBDA has time access protection while a write to SHBDA is required. The Data Flash size will be 15.75k bytes and there will is 256 bytes APROM.

The Data Flash size is fixed as 4 Kbytes from address 3000H through 3FFFH in N79E844/8432. SHBDA affects nothing.

The CONFIG bit DFEN (CONFIG0.0) should be programmed as 0 before accessing the Data Flash block. If DFEN remains its un-programmed value 1, APROM will occupy whole 16K-bytes block in N79E845 DFEN.

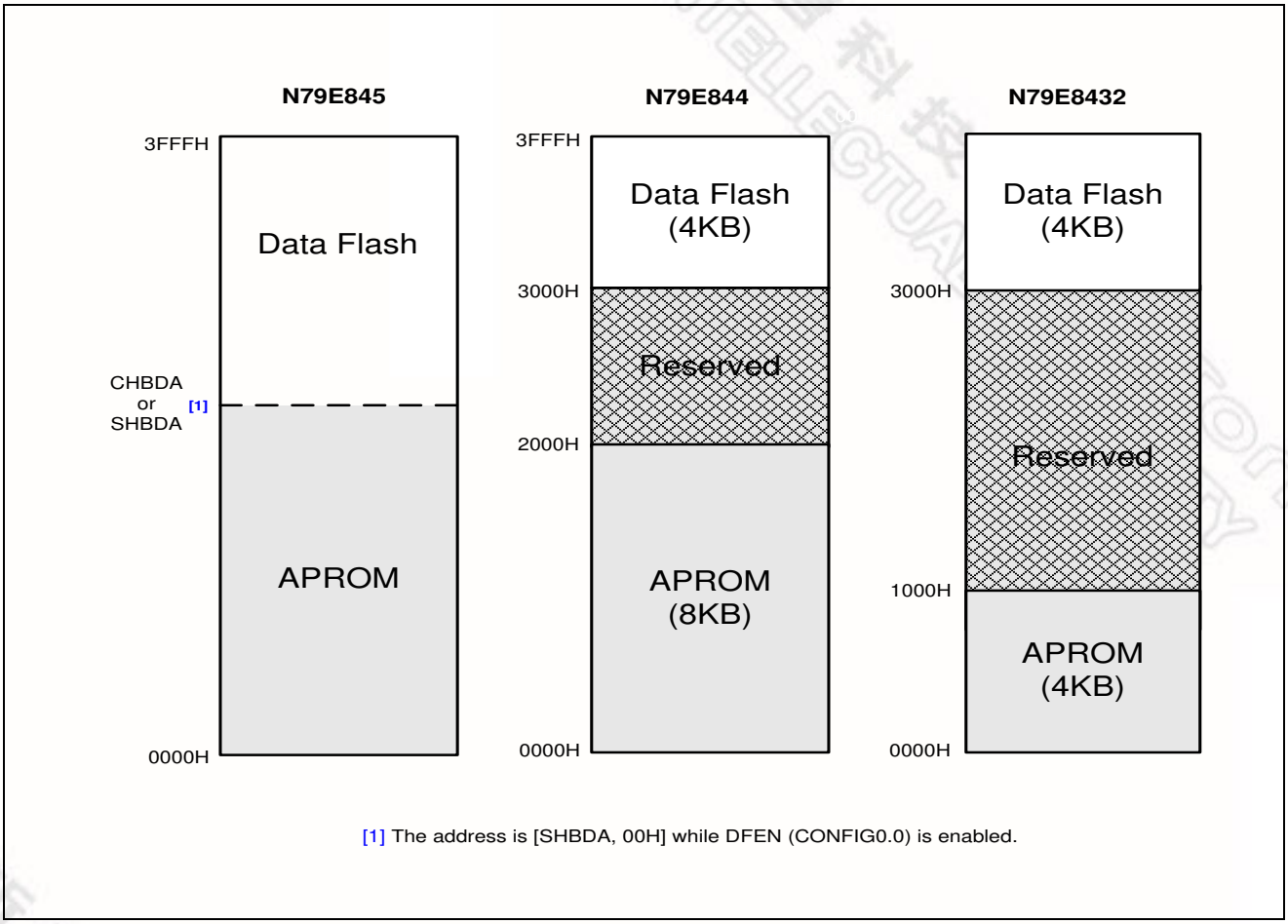

Figure 6–2 N79E845/844/8432 Data Flash

SHBDA – SFR High Byte of Data Flash Starting Address (TA protected, N79E845 Only)

7	6	5	4	3	2	1	0
SHBDA[7:0] [1]							
R/W							

Address: 9CH Reset value: see Table 7–2 N79E845/844/8432 SFR Description and Reset Values

Bit	Name	Description
7:0	SHBDA[7:0]	**SFR high byte of Data Flash starting address** This byte is valid only when DFEN (CONFIG0.0) being 0 condition. It is used to dynamic adjust the starting address of the Data Flash when the application program is executing.

[1] SHBDA is loaded from CONFIG1 after all resets.

6.5 On-chip XRAM

The N79E845/844/8432 provides additional on-chip 256 bytes auxiliary RAM called XRAM to enlarge the RAM space. It occupies the address space from 00H through FFH. The 256 bytes of XRAM are indirectly accessed by move external instruction MOVX @DPTR or MOVX @Ri. (See the demo code below.) Note that the stack pointer may not be located in any part of XRAM. Figure 6-1 shows the memory map for this product series.

XRAM demo code:

```
MOV    R0,#23H              ;write #5AH to XRAM with address @23H
MOV    A,#5AH
MOVX   @R0,A

MOV    R1,#23H             ;read from XRAM with address @23H
MOVX   A,@R1

MOV    DPTR,#0023H         ;write #5BH to XRAM with address @0023H
MOV    A,#5BH
MOVX   @DPTR,A

MOV    DPTR,#0023H         ;read from XRAM with address @0023H
MOVX   A,@DPTR
```

6.6 On-chip scratch-pad RAM and SFR

The N79E845/844/8432 provides the on-chip 256 bytes scratch pad RAM and Special Function Registers (SFRs) which be accessed by software. The SFRs be accessed only by direct addressing, while the on-chip RAM be accessed by either direct or indirect addressing.

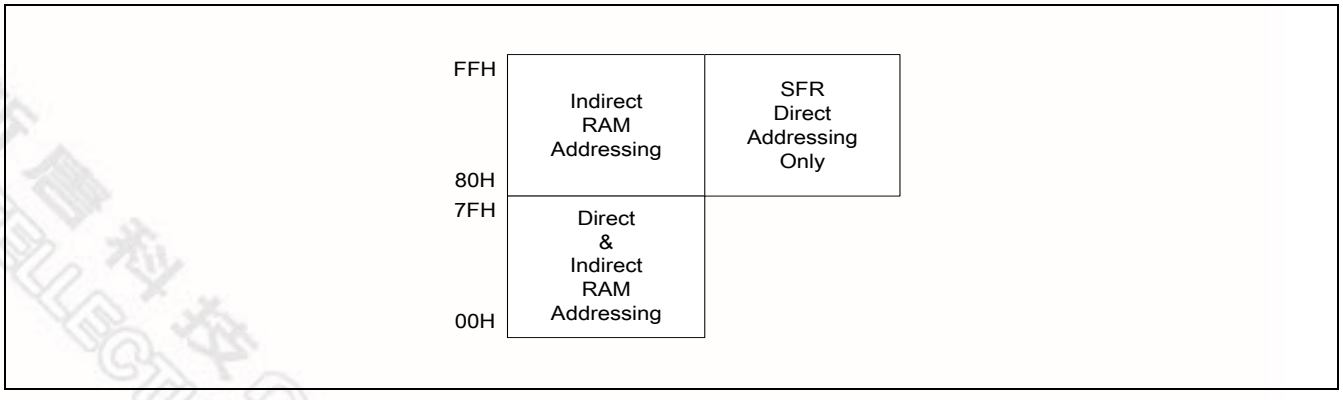

Figure 6-3 256 bytes RAM and SFR

Since the scratch-pad RAM is only 256 byte it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM, which are described as follows.

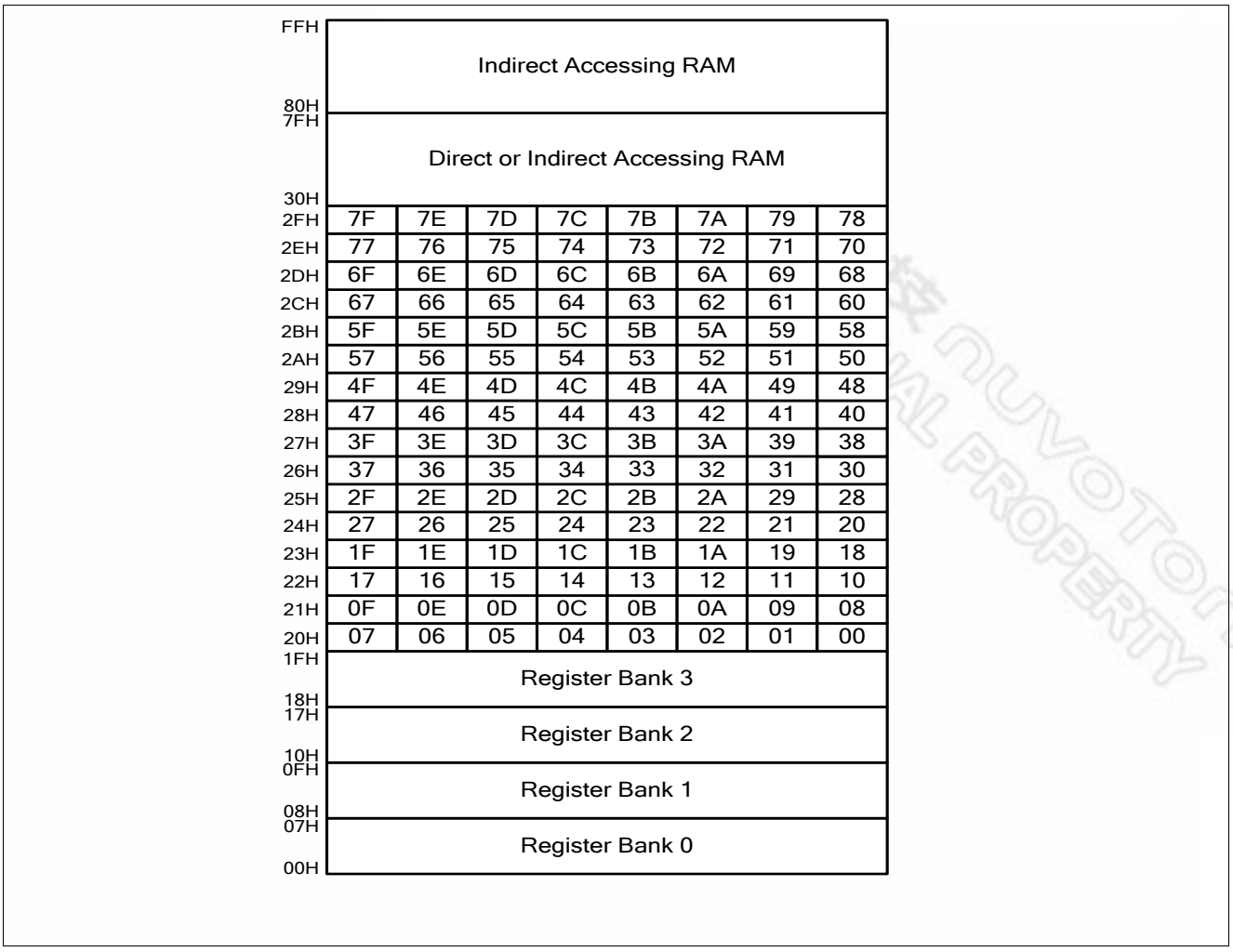

Figure 6-4 Data Memory and Bit-addressable Region

6.7 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers, which are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions, which individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the N79E845/844/8432 can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

6.8 Bit-addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit-addressable. This means that a bit in this area can be individually addressed. In addition, some of the SFRs are also bit-addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in 0 or 8 is bit-addressable.

6.9 Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

7 Special Function Register (SFR)

The N79E845/844/8432 uses Special Function Registers (SFRs) to control and monitor peripherals and their modes. The SFRs reside in the register locations 80~FFH and are accessed by direct addressing only. Some of the SFRs are bit-addressable. This is very useful in cases where user would like to modify a particular bit directly without changing other bits. Those which are bit-addressable SFRs end their addresses as 0H or 8H. The N79E845/844/8432 contains all the SFRs presenting in the standard 8051. However some additional SFRs are built in. Therefore, some of unused bytes in the original 8051 have been given new functions. The SFRs are listed as follows.

Table 7–1 N79E845/844/8432 Special Function Registers (SFR) Mapping

F8	**ADCCON0**	-	-	-	-	-	-	EIP	FF
F0	**B**	-	-	SPCR	SPSR	SPDR	P0DIDS	EIPH	F7
E8	**EIE**	KBIE	KBIF	KBLS0	KBLS1	C2L	C2H	-	EF
E0	**ACC**	ADCCON1	ADCH	-	C0L	C0H	C1L	C1H	E7
D8	**WDCON0***	PWMPL	PWM0L	PWM1L	PWMCON0	PWM2L	PWM3L	PWMCON1	DF
D0	**PSW**	PWMPH	PWM0H	PWM1H	-	PWM2H	PWM3H	PWMCON2	D7
C8	**T2CON**	T2MOD	RCOMP2L	RCOM2H	TL2	TH2	-	-	CF
C0	**I2CON**	I2ADDR	-	-	-	-	-	TA	C7
B8	**IP**	SADEN	-	-	I2DAT	I2STA	I2CLK	I2TOC	BF
B0	**P3**	P0M1	P0M2	P1M1	P1M2			IPH	B7
A8	**IE**	SADDR	-	WDCON1*	-	-	ISPFD	ISPCN	AF
A0	**-**	-	AUXR1	PMCR*	ISPTRG*	-	ISPAL	ISPAH	A7
98	**SCON**	SBUF	-	-	SHBDA*	-	-	CHPCON*	9F
90	**P1**	-	CAPCON0	CAPCON1	CAPCON2	DIVM	P3M1	P3M2	97
88	**TCON**	TMOD	TL0	TL1	TH0	TH1	CKCON	-	8F
80	**P0**	SP	DPL	DPH	-	-	-	PCON	87

In Bold	bit-addressable
-	reserved

Note:

1. The reserved SFR addresses should be kept in their own initial states. User should never change their values.
2. The SFRs in the column with dark borders are bit-addressable

* With TA-Protection. (Time Access Protection)

Table 7–2 N79E845/844/8432 SFR Description and Reset Values

Symbol	Definition	Address	MSB							LSB	Reset Value[1]
EIP	Interrupt Priority 1	FFH	PT2	PSPI	PPWM	PWDI	-	-	PKB	PI2	0000 0000B
ADCCON0	ADC control register 0	F8H	(FF) ADC.1	(FE) ADC.0	(FD) ADCEX	(FC) ADCI	(FB) ADCS	(FA) AADR2	(F9) AADR1	(F8) AADR0	0000 0000B
EIPH	Interrupt High Priority 1	F7H	PT2H	PSPIH	PPWMH	PWDIH	-	-	PKBH	PI2H	0000 0000B
P0DIDS	Port 0 Digital Input Disable	F6H	P0DIDS[7:0]								0000 0000B
SPDR	Serial Peripheral Data Register	F5H	SPDR[7:0]								0000 0000B
SPSR	Serial Peripheral Status Register	F4H	SPIF	WCOL	SPIOVF	MODF	DISMODF	-	-	-	0000 0000B
SPCR	Serial Peripheral Control Register	F3H	SSOE	SPIEN	LSBFE	MSTR	CPOL	CPHA	SPR1	SPR0	0000 0100B
B	B register	F0H	(F7) B.7	(F6) B.6	(F5) B.5	(F4) B.4	(F3) B.3	(F2) B.2	(F1) B.1	(F0) B.0	0000 0000B
C2H	Input Capture 2 High	EEH	C2H[7:0]								0000 0000B
C2L	Input Capture 2 Low	EDH	C2L[7:0]								0000 0000B
KBLS1	Keyboard level select 1	ECH	KBLS1[7:0]								0000 0000B
KBLS0	Keyboard level select 0	EBH	KBLS0[7:0]								0000 0000B
KBIF	KBI Interrupt Flag	EAH	KBIF[7:0]								0000 0000B
KBIE	Keyboard Interrupt Enable	E9H	KBIE[7:0]								0000 0000B
EIE	Interrupt enable 1	E8H	(EF) ET2	(EE) ESPI	(ED) EPWM	(EC) EWDI	(E7)	(E8) ECPTF	(E9) EKB	(E8) EI2C	0000 0000B
C1H	Input Capture 1 High	E7H	C1H[7:0]								0000 0000B
C1L	Input Capture 1 Low	E6H	C1L[7:0]								0000 0000B
C0H	Input Capture 0 High	E5H	C0H[7:0]								0000 0000B
C0L	Input Capture 0 Low	E4H	C0L[7:0]								0000 0000B
ADCH	ADC converter result	E2H	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	0000 0000B
ADCCON1	ADC control register1	E1H	ADCEN	-	-	-	-	-	RCCLK	ADC0SEL	0000 0000B
ACC	Accumulator	E0H	(E7) ACC.7	(E6) ACC.6	(E5) ACC.5	(E4) ACC.4	(E3) ACC.3	(E2) ACC.2	(E1) ACC.1	(E0) ACC.0	0000 0000B
PWMCON1	PWM control register 1	DFH	BKCH	BKPS	BPEN	BKEN	PWM3B	PWM2B	PWM1B	PWM0B	0000 0000B
PWM3L	PWM 3 low bits register	DEH	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0	0000 0000B
PWM2L	PWM 2 low bits register	DDH	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0	0000 0000B
PWMCON0	PWM control register 0	DCH	PWMRUN	LOAD	CF	CLRPWM	PWM3I	PWM2I	PWM1I	PWM0I	0000 0000B
PWM1L	PWM 1 low bits register	DBH	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0	0000 0000B
PWM0L	PWM 0 low bits register	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	0000 0000B
PWMPL	PWM counter low register	D9H	PWMP0.7	PWMP0.6	PWMP0.5	PWMP0.4	PWMP0.3	PWMP0.2	PWMP0.1	PWMP0.0	0000 0000B
WDCON0[4] [3]	Watch-Dog control 0	D8H	(DF) WDTEN	(DE) WDCLR	(DD) WDTF	(DC) WIDPD	(DB) WDTRF	(DA) WPS2	(D9) WPS1	(D8) WPS0	Power-ON C000 0000B Watch reset C0UU 1UUUB Other reset C0UU UUUUB
PWMCON2	PWM control register 2	D7H	-	-	-	-	FP1	FP0	-	BKF	0000 0000B
PWM3H	PWM 3 high bits register	D6H	-	-	-	-	-	-	PWM3.9	PWM3.8	0000 0000B
PWM2H	PWM 2 high bits register	D5H	-	-	-	-	-	-	PWM2.9	PWM2.8	0000 0000B
PWM1H	PWM 1 high bits register	D3H	-	-	-	-	-	-	PWM1.9	PWM1.8	0000 0000B
PWM0H	PWM 0 high bits register	D2H	-	-	-	-	-	-	PWM0.9	PWM0.8	0000 0000B
PWMPH	PWM counter high register	D1H	-	-	-	-	-	-	PWMP0.9	PWMP0.8	0000 0000B
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	0000 0000B
TH2	Timer 2 MSB	CDH	TH2[7:0]								0000 0000B

Table 7–2 N79E845/844/8432 SFR Description and Reset Values

Symbol	Definition	Address	MSB							LSB	Reset Value[1]
TL2	Timer 2 LSB	CCH	TL2[7:0]								0000 0000B
RCOMP2H	Timer 2 Reload MSB	CBH	RCOMP2H[7:0]								0000 0000B
RCOMP2L	Timer 2 Reload LSB	CAH	RCOMPL2[7:0]								0000 0000B
T2MOD	Timer 2 Mode	C9H	LDEN	T2DIV[2:0]			CAPCR	COMPCR	LDTS[1:0]		0000 0000B
T2CON	Timer 2 Control	C8H	(CF) TF2	-	-	-	-	(CA) TR2	-	(C8) CP/$\overline{RL2}$	0000 0000B
TA	Timed Access Protection	C7H									1111 1111B
I2ADDR	I2C address	C1H	ADDR[7:1]							GC	0000 0000B
I2CON	I2C Control register	C0H	(C7) -	(C6) I2CEN	(C5) STA	(C4) STO	(C3) SI	(C2) AA	(C1) -	(C0) -	0000 0000B
I2TOC	I2C Time-out Counter register	BFH	-	-	-	-	-	I2TOCEN	DIV	I2TOF	0000 0000B
I2CLK	I2C Clock Rate	BEH	I2CLK[7:0]								0000 0000B
I2STA	I2C Status Register	BDH	I2STA[7:3]					0	0	0	1111 1000B
I2DAT	I2C Data Register	BCH	I2DAT[7:0]								0000 0000B
SADEN	Slave address mask	B9H	SADEN[7:0]								0000 0000B
IP	Interrupt priority	B8H	(BF) PCAP	(BE) PADC	(BD) PBOD	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	0000 0000B
IPH	Interrupt high priority	B7H	PCAPH	PADCH	PBODH	PSH	PT1H	PX1H	PT0H	PX0H	0000 0000B
P1M2	Port 1 output mode 2	B4H	P1M2.7	P1M2.6	-	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0	0000 0000B
P1M1	Port 1 output mode 1	B3H	P1M1.7	P1M1.6	-	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0	0000 0000B
P0M2	Port 0 output mode 2	B2H	P0M2[7:0]								0000 0000B
P0M1	Port 0 output mode 1	B1H	P0M1[7:0]								0000 0000b
P3	Port3	B0H	-	-	-	-	-	-	(B1) X1	(B0) X2 CLKOUT	0000 0011B
ISPCN	ISP Control Register	AFH	ISPA17	ISPA16	FOEN	FCEN	FCTRL3	FCTRL2	FCTRL1	FCTRL0	0011 0000B
ISPFD	ISP Flash Data Register	AEH	ISPFD[7:0]								0000 0000B
WDCON1[4]	Watch-Dog control1	ABH	-	-	-	-	-	-	-	EWRST	0000 0000B
SADDR	Slave address	A9H	SADDR[7:0]								00000000B
IE	Interrupt enable	A8H	(AF) EA	(AE) EADC	(AD) EBOD	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000B
ISPAH	ISP Flash Address High-byte	A7H	ISPAH[7:0]								0000 0000B
ISPAL	ISP Flash Address Low-byte	A6H	ISPAL[7:0]								0000 0000B
ISPTRG[4]	ISP Trigger Register	A4H	-	-	-	-	-	-	-	ISPGO	0000 0000B
PMCR[2][4]	Power Monitor Control Register	A3H	BODEN	BOV	-	BORST	BOF	-	-	-	Power-on CC0C 100XB BOR reset UU0U 100XB Other reset UU0U 000XB
AUXR1	AUX function register	A2H	-	-	-	-	-	-	0	DPS	0000 0000B
CHPCON[4]	Chip Control	9FH	SWRST	ISPF (Read only)	LDUE	-	-	-	BS[3]	ISPEN	Power-ON 0000 00C0B Other reset 0000 00C0B
SHBDA[4]	High-byte Data Flash Start Address	9CH	SHBDA[7:0], SHBDA Initial by CHBDA								Power ON CCCC CCCCB Other Reset UUUU UUUUB
SBUF	Serial buffer	99H	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0	0000 0000B

Table 7–2 N79E845/844/8432 SFR Description and Reset Values

Symbol	Definition	Address	MSB							LSB	Reset Value[1]
SCON	Serial control	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000B
P3M2	Port 3 output mode 2	97H	-	-	-	-	-	ENCLK	P3M2.1	P3M2.0	00000000B
P3M1	Port 3 output mode 1	96H	P3S	-	P1S	P0S	T1OE	T0OE	P3M1.1	P3M1.0	00000000B
DIVM	CPU Clock Divide Register	95H	DIVM[7:0]								0000 0000B
CAPCON2	Input capture control 2	94H	-	-	ENF1	ENF0	-	-	-	-	0000 0000B
CAPCON1	Input capture control 1	93H	-	-			CAP1LS1[2:0]		CAP1LS1[2:0]		0000 0000B
CAPCON0	Input capture control 0	92H	-	-	CAPEN1	CAPEN0	-	-	CAPF1	CAPF0	0000 0000B
P1	Port 1	90H	(97) P17	(96) P16	-	(94) P14	(93) P13	(92) P12	(91) P11	(90) P10	1111 1111B
CKCON	Clock control	8EH	-	-	-	T1M	T0M	-	-	-	0000 0000B
TH1	Timer high 1	8DH	TH1[7:0]								0000 0000B
TH0	Timer high 0	8CH	TH0[7:0]								0000 0000B
TL1	Timer low 1	8BH	TL1[7:0]								0000 0000B
TL0	Timer low 0	8AH	TL0[7:0]								0000 0000B
TMOD	Timer mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	0000 0000B
TCON	Timer control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0000 0000B
PCON	Power control	87H	SMOD	SMOD0	-	POF	GF1	GF0	PD	IDL	Power-on 0001 0000B Other reset 000u 0000B
DPH	Data pointer high	83H	DPH[7:0]								0000 0000B
DPL	Data pointer low	82H	DPL[7:0]								0000 0000B
SP	Stack pointer	81H	SP[7:0]								0000 0111B
P0	Port 0	80H	(87) P07	(86) P06	(85) P05	(84) P04	(83) P03	(82) P02	(81) P01	(80) P00	1111 1111B

Note: Bits marked in "-" should be kept in their own initial states. User should never change their values.

Note:

[1.] ( ) item means the bit address in bit-addressable SFRs.

[2.] BODEN, BOV and BORST are initialized by CONFIG2 at power-on reset, and keep unchanged at any other resets. If BODEN=1, BOF will be automatically set by hardware at power-on reset, and keeps unchanged at any other resets.

[3.] Initialized by power-on reset. WDTEN=/CWDTEN; BS=/CBS;

[4.] With TA-Protection. (Time Access Protection)

[5.] Notation “C” means the bit is defined by CONFIG-bits; “U” means the bit is unchanged after any reset except power-on reset.

[6.] Reset value symbol description. 0: logic 0, 1: logic 1, U: unchanged, X:, C: initial by CONFIG.

8 General 80C51 System Control

A or ACC – Accumulator (Bit-addressable)

7	6	5	4	3	2	1	0
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: E0H Reset value: 0000 0000B

Bit	Name	Description
7:0	ACC[7:0]	**Accumulator.** The A or ACC register is the standard 8051 accumulator for arithmetic operation.

B – B Register (Bit-addressable)

7	6	5	4	3	2	1	0
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: F0H Reset value: 0000 0000B

Bit	Name	Description
7:0	B[7:0]	**B Register** The B register is the other accumulator of the standard 8051. It is used mainly for MUL and DIV operations.

SP – Stack Pointer

7	6	5	4	3	2	1	0
SP[7:0]							
R/W							

Address: 81H Reset value: 0000 0111B

Bit	Name	Description
7:0	SP[7:0]	**Stack Pointer** The Stack Pointer stores the scratch-pad RAM address where the stack begins. It is incremented before data is stored during PUSH or CALL instructions. Note that the default value of SP is 07H. It causes the stack to begin at location 08H.

DPL – Data Pointer Low Byte

7	6	5	4	3	2	1	0
DPL[7:0]							
R/W							

Address: 82H Reset value: 0000 0000B

Bit	Name	Description
7:0	DPL[7:0]	**Data Pointer Low Byte** This is the low byte of the standard 8051 16-bit data pointer. DPL combined with DPH serve as 16-bit data pointer DPTR to address non-scratch-pad memory or Program Memory.

DPH – Data Pointer High Byte

7	6	5	4	3	2	1	0
DPH[7:0]							
R/W							

Address: 83H Reset value: 0000 0000B

Bit	Name	Description
7:0	DPH[7:0]	**Data pointer high byte** This is the high byte of the standard 8051 16-bit data pointer. DPH combined with DPL serve as 16-bit data pointer DPTR to address non-scratch-pad memory or Program Memory.

PSW – Program Status Word (Bit-addressable)

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Address: D0H Reset value: 0000 0000B

Bit	Name	Description
7	CY	**Carry Flag** For a adding or subtracting operation, CY will be set when the previous operation resulted in a carry-out from or a borrow-in to the Most Significant bit, otherwise cleared. If the previous operation is MUL or DIV, CY is always 0. CY is affected by DA A instruction which indicates that if the original BCD sum is greater than 100. For a CJNE branch, CY will be set if the first unsigned integer value is less than the second one. Otherwise, CY will be cleared.
6	AC	**Auxiliary Carry** Set when the previous operation resulted in a carry-out from or a borrow-in to the 4th bit of the low order nibble, otherwise cleared.