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8-BIT MICROCONTROLLER

Table of Contents-

1 GENERAL DESCRIPTION

N79E875 series are 8-bit Turbo 51 microcontrollers which have embedded Flash that can be programmed by ICP (In Circuit Program) or by writer. The instruction sets of the N79E875 series are fully compatible with the standard 8052. N79E875 series contain a **16K** bytes of main Flash EPROM; a **256** bytes of RAM; **256** bytes AUX-RAM; **128** bytes NVM Data Flash EPROM support; **two** 16-bit timer/counters; **one** 16-bit timer with 3 capture inputs; **one** 12-bit capture/compare/auto-reload timer; **8**-channel multiplexed 10-bit A/D converter; **8**-channel 12-bit PWM that includes 6-channel for 3 pairs complementary PWM; **three** serial ports that includes a SPI, an I2C and an enhanced full duplex serial port; **one** OP amplifier; **two** analog comparators; 3-level selectable Brownout detector. These peripherals are supported by **17** sources of four-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside N79E875 series allow the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

N79E875 series, built-in efficient PWM generator and Input capture/timer, are designed for motor control applications such as E-bike, inverters of DC/BLDC/AC induction/Stepping motor and home appliance, etc. The built-in rich functions and peripheral also suit to general application.

2 FEATURES

- Fully static design 8-bit Turbo 51 CMOS microcontroller;
  - V_{DD} = 4.5V to 5.5V @40MHz
  - V_{DD} = 3.0V to 5.5V @24MHz
  - V_{DD} = 2.4V to 5.5V @8MHz
- Operating temperature range
  - N79**E**875A/N79**E**875RA series: -40°C ~85°C
- Flexible CPU clock source configurable by config-bit and software:
  - High speed external oscillator: Up to 40MHz Crystal and resonator (enabled by config-bit).
  - Internal oscillator: Nominal 22MHz/11MHz (selected by config-bit)
    N79E875**A** series: 22MHz/11MHz with ±25% accuracy
    N79E875**RA** series: 22.1184MHz/11.0592MHz with ±2% accuracy, at 3.3V/25°C
- On-chip Memory
  - 16K bytes of Application Program Flash memory, with ICP and External Writer programmable mode.
  - 128 bytes (8 pages x 16 bytes) Data Flash for customer data storage used and 10K writer cycles; Data Flash program/erase V_{DD}=3.0V to 5.5V
  - 256 bytes of on-chip scratch-pad RAM.
  - 256 bytes of auxiliary RAM, software-selectable, accessed by MOVX instruction.
- Maximum 36 I/O pins.
  - Four outputs mode and TTL/Schmitt trigger selectable Port.
- 17 interrupts source with four levels of priority.
- Four timer/counters.
  - Two 16-bit timer/counters
  - One 16-bit timer supports 3 capture inputs capability for hall sensor feedback.
  - One 12-bit timer supports 12-bit auto reload timer, capture and compare mode.
- Three serial ports
  - One enhanced full duplex UART port with framing error detection and automatic address recognition.
  - One SPI with master/slave capability.
  - One I2C with master/slave capability.
- Four independent 12-bit PWM duty control units with maximum 8 port pins:
  - Six PWM output channels with mask control for BLDC application.
  - Three pairs complementary PWM with programmable dead-time insertion
  - Independent polarity setting for each channel
  - Two brake/fault input pins

- Up to two channels PWM independent from paired PWM channels.

- One build-in OP amplifier.
- Eight-channel multiplexed with 10-bits A/D converter.
  - Support synchronized trigger with PWM period.
  - Support OP amplifier output conversion.
  - Support digital compare function.
- Two analog comparators with optional internal reference voltage input at negative end.
- Eight-keypad interrupt inputs.
- Built-in power management.
  - Idle mode
  - Power down mode
- LED drive capability (20mA) on all port pins.
- Config-bits selectable 3 levels(4.5V/3.8V/2.6V) Brown-Out voltage detect interrupt and reset.
- Independent Programmable Watchdog Timer.
- Program and Data Flash security protection.
- Development Tools:
  - JTAG ICE(In Circuit Emulation) tool
  - ICP(In Circuit Programming) writer
- Packages:
  - Lead Free (RoHS) LQFP 48: N79E875ALG series (-40°C ~85°C)
  - Lead Free (RoHS) LQFP 48: N79E875RALG series (-40°C ~85°C)

3 PARTS INFORMATION LIST

3.1 Lead Free (RoHS) Parts information list

Table 3-1 Lead Free (RoHS) Parts information list

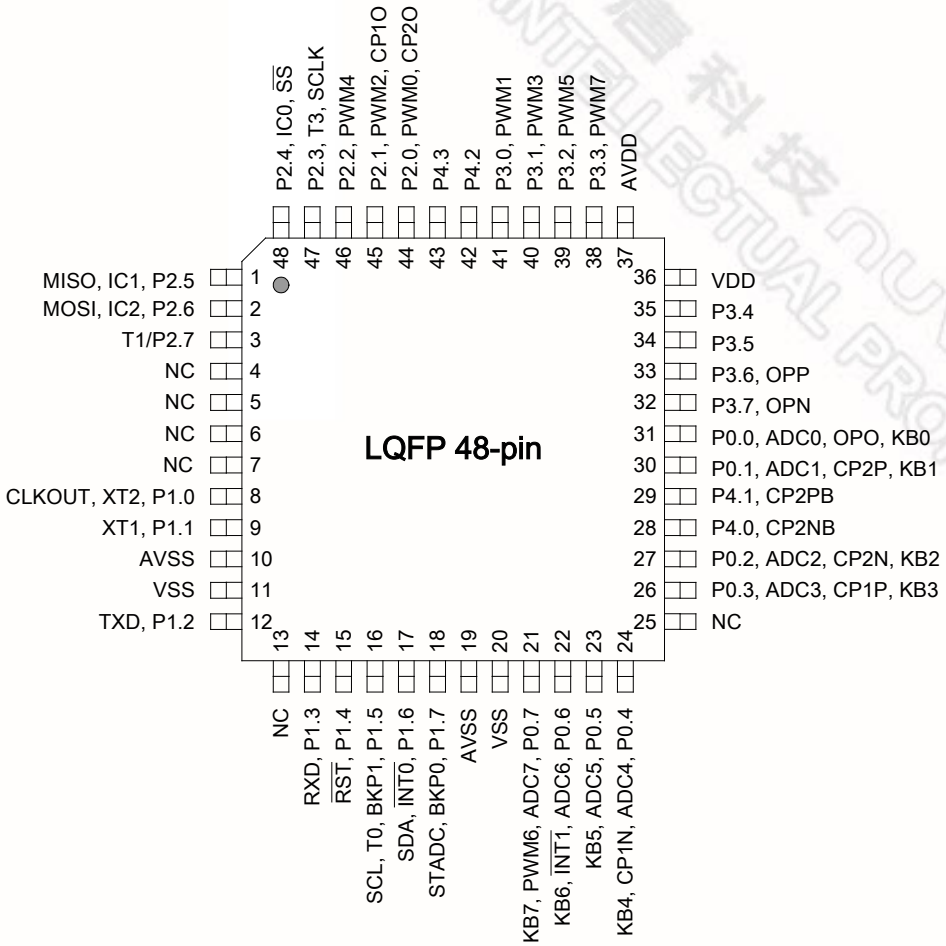
PART NO.	PROGRAM FLASH EPROM	RAM	DATA FLASH EPROM	TEMP °C	INTERNAL RC OSC[1]	PACKAGE
N79E875ALG	16KB	256B+256B	128B	-40~85°C	22MHz ± 25%	LQFP-48
N79E875RALG	16KB	256B+256B	128B	-40~85°C	22.1184MHz ± 2%	LQFP-48

Note:

1. Factory calibration condition: V_{DD}=3.3V, TA = 25°C

4 PIN CONFIGURATION

N79E875ALG/N79E875RALG



5 PIN DESCRIPTION

SYMBOL	Alternate Function 1	Alternate function 2	Alternate function 3	Type	DESCRIPTIONS
VDD				P	POWER SUPPLY: Supply voltage for operation.
VSS				P	GROUND: Ground potential.
AVDD				P	ANALOG Power Supply
AVSS				P	ANALOG GROUND.
P0.0	ADC0	OPO	KB0	I/O	Port0: Support 4 mode output and 2 mode input. Multifunction pins.
P0.1	ADC1	CP2PA	KB1	I/O	
P0.2	ADC2	CP2NA	KB2	I/O	
P0.3	ADC3	CP1P	KB3	I/O	
P0.4	ADC4	CP1N	KB4	I/O	
P0.5	ADC5		KB5	I/O	
P0.6	ADC6	/INT1	KB6	I/O	
P0.7	ADC7	PWM6	KB7	I/O	
P1.0	XT2	CLKOUT		I/O	Port1: Support 4 mode output and 2 mode input. Multifunction pins. P1.5 and P1.6 are permanently in Open-Drain type.
P1.1	XT1			I/O	
P1.2	TXD			I/O	
P1.3	RXD			I/O	
P1.4	/RST			I, H(rst)	
P1.5	T0	SCL	BKP1	D	
P1.6	/INT0	SDA		D	
P1.7		STADC	BKP0	I/O	
P2.0	PWM0	CP2O		I/O	Port2: Support 4 mode output and 2 mode input. Multifunction pins.
P2.1	PWM2	CP1O		I/O	
P2.2	PWM4			I/O	
P2.3	T3	SCLK		I/O	
P2.4	IC0	/SS		I/O	

SYMBOL	Alternate Function 1	Alternate function 2	Alternate function 3	Type	DESCRIPTIONS
P2.5	IC1	MISO		I/O	
P2.6	IC2	MOSI		I/O	
P2.7	T1			I/O	
P3.0	PWM1			I/O	Port3: Support 4 modes output and 2 modes input. Multifunction pins.
P3.1	PWM3			I/O	
P3.2	PWM5			I/O	
P3.3	PWM7			I/O	
P3.4				I/O	
P3.5				I/O	
P3.6	OPP			I/O	
P3.7	OPN			I/O	
P4.0		CP2NB		I/O	Support 4 modes output and 2 modes input.
P4.1		CP2PB		I/O	
P4.2				I/O	
P4.3				I/O	

TYPE: P: power, I: input, O: output, I/O: bi-directional with 4-type I/O modes,, H: Internal pull-up, L: Internal pull low, D: Open Drain

Notes:

- During Power-on-reset, all port pins are in tri-stated.
- After power-on-reset, all port pins state will follow CONFIG0.PRHI bit definition.
- All digital input pins support software enabled schmitt trigger buffer which is selected by SFR PORTS (ECH)

In application if MCU pins need external pull-up, it is recommended to add a pull-up resistor (10KΩ) between pin and power(V_{DD}) instead of directly wiring pin to V_{DD} for enhancing EMC.

6 MEMORY ORGANIZATION

N79E875 series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

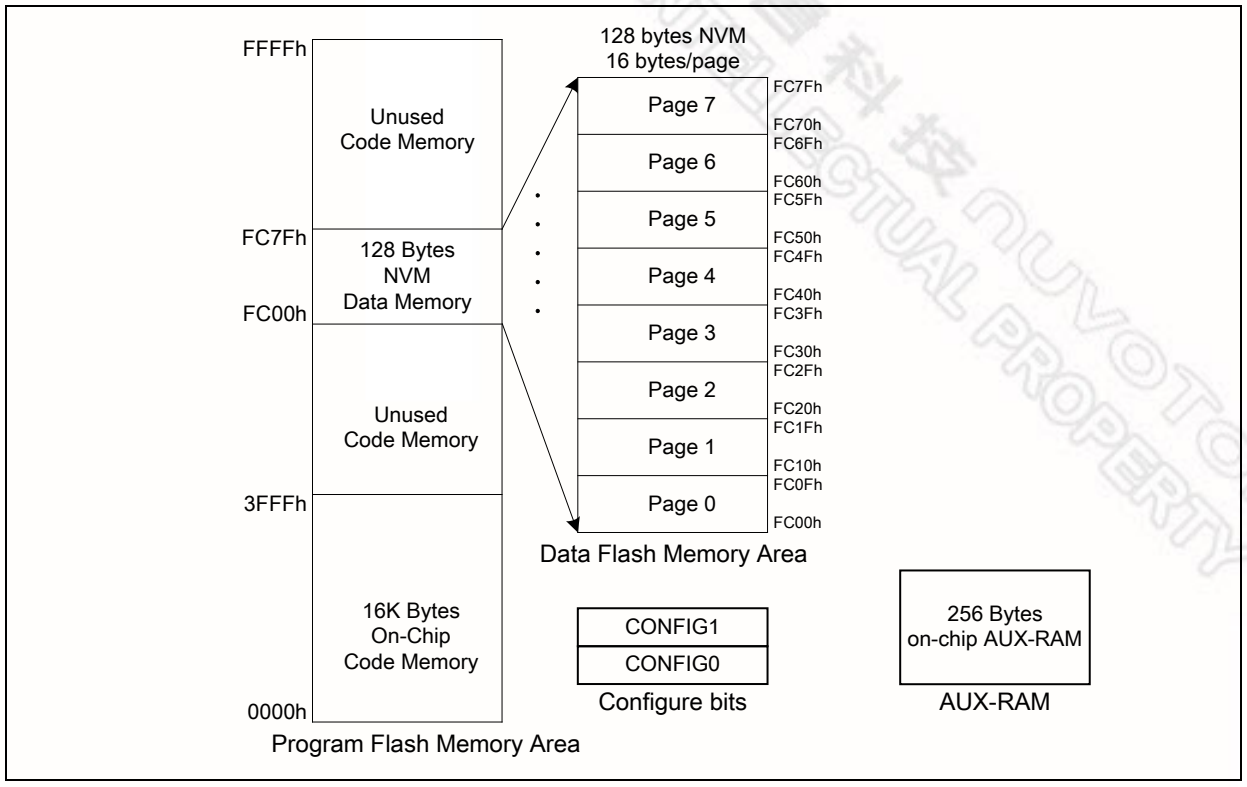


Figure 6-1 N79E875 series Memory Map

6.1 Program Flash Memory

The Program Memory on N79E875 series can be up to **16K** bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

6.2 Data Flash Memory

The NVM Data Memory of Flash EPROM on the N79E875 series is **128** bytes long, with page size of 16 bytes. The N79E875 series read the content of data memory by using “MOVC A, @A+DPTR”. To write data is by NVMADDRL, NVMDAT and NVMCON SFR’s registers.

6.3 Data Memory (accessed by MOVX)

N79E875 provides 256 bytes AUX RAM accessed by the MOVX instruction. The data memory region is from 0000H to 00FFH. Figure 6-1 shows the memory map for this product series.

6.4 Scratch-pad RAM and Register Map

As mentioned before, N79E875 series have separate Program and Data Memory areas. The on-chip 256 bytes scratch pad RAM is in addition to the external memory. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

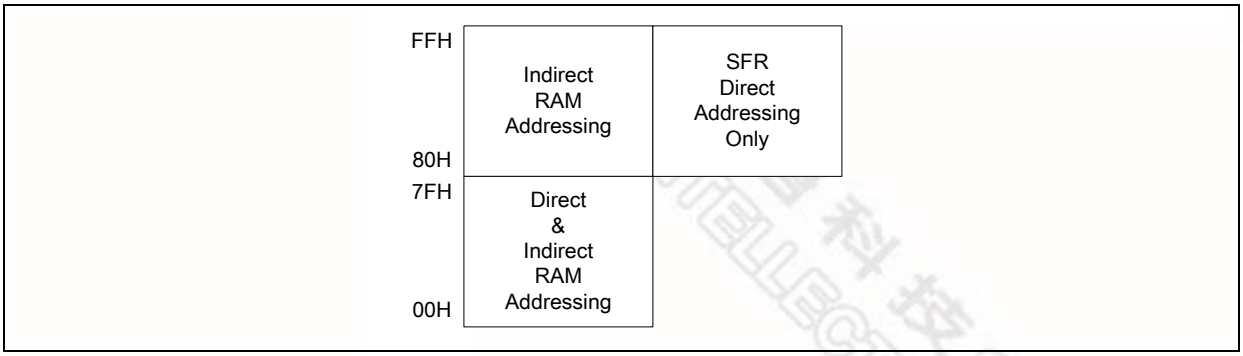


Figure 6-2 N79E875 series RAM and SFR Memory Map

Since the scratch-pad RAM is only 256 bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are illustrated in next figure.

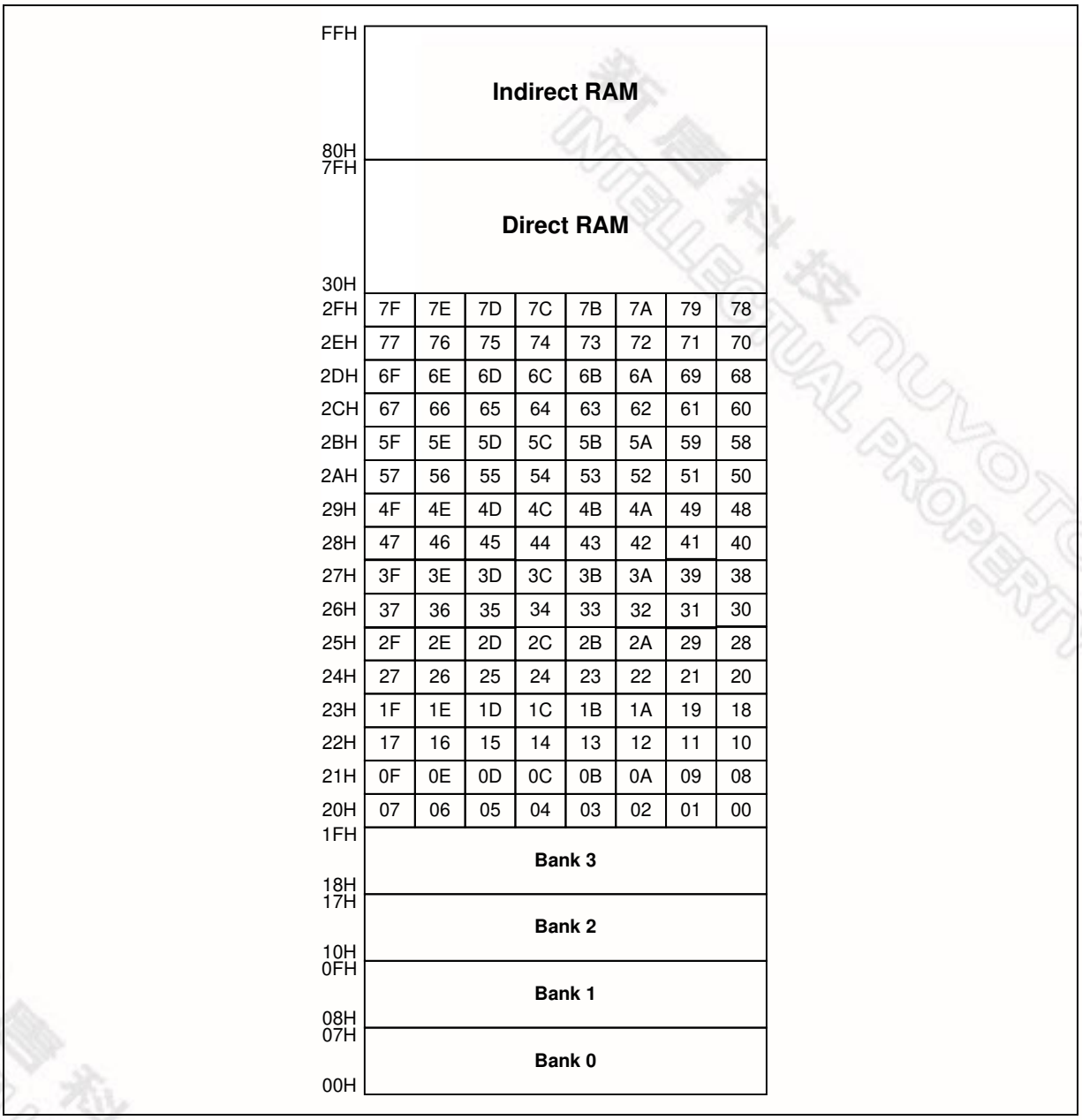


Figure 6-3 Scratch-pad RAM

6.5 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed ads Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at any one time N79E875 series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

6.6 Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

6.7 Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

7 SPECIAL FUNCTION REGISTERS

N79E875 series use Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where we wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. N79E875 series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

7.1 SFR Location Table

F8	**IP1**		P4M1	P4M2	PWMCON4	PWM6L	PWM6H	AUXR2
F0	**B**			SPCR	SPSR	SPDR	PADIDS	IP1H
E8	**EIE1**				PORTS	PME	PMD	IP2H
E0	**ACC**	ADCCON	ADCH	ADCCON1	CCL0	CCH0	CCL1	CCH1
D8	**WDCON**(3)	PWMPL	PWM0L		PWMCON1	PWM2L		PWMB
D0	**PSW**	PWMPH	PWM0H		EIE2	PWM2H		PWMCON3
C8	**T2CON**	T2MOD	RCAP2L	RCAP2H	TL2	TH2	NVMCON	NVMDAT
C0	**I2CON**	I2ADDR	T3CON	PNP			NVMADDRL	TA
B8	**IP0**	SADEN			I2DATA	I2STATUS	I2CLK	I2TIMER
B0	**P3**	P0M1	P0M2	P1M1	P1M2	P2M1	P2M2	IP0H
A8	**IE**	SADDR		DTCNT(3)	CMP1	CMP2	PDTC0(3)	ADCDLY
A0	**P2**	KBI	AUXR1	CAPCON0	CAPCON1	P4	CCL2	CCH2
98	**SCON**	SBUF	IP2	PIO	ADCRL	ADCRH	P3M1	P3M2
90	**P1**	T3L	RCAP3L	RCAP3HT3H			PWM4L	PWM4H
88	**TCON**	TMOD	TL0	TL1	TH0	TH1	CKCON	
80	**P0**	SP	DPL	DPH			DIV	PCON

Table 7- 1 Special Function Register Location Table

Note:

1. The SFRs in the column with dark borders are bit-addressable
2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses.
3. With Timed Access Protection on write operation.

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
AUXR2	AUXR2 CONTROL REGISTER	FFH	T1OE	T0OE	PCMP2DIDS.1	PCMP2DIDS.0	POPDIDS	ENCLK	ADC1SEL	ENOP	0000 0000b
PWM6H	PWM 6 HIGH BITS REGISTER	FEH		-			PWM6.11	WM6.10	PWM6.9	PWM6.8	XXXX 0000b
PWM6L	PWM 6 LOW BITS REGISTER	FDH	PWM6.7	PWM6.6	PWM6.5	PWM6.4	PWM6.3	PWM6.2	PWM6.1	PWM6.0	0000 0000b
PWMCON4	PWM CONTROL REGISTER 4	FCH	BK1FILT.1	BK1FILT.0	BK0FILT.1	BK0FILT.0	AUTOBK1	-	BKEN1	BKEN0	0000 0X00b
P4M2	PORT 4 OUTPUT MODE 2	FBH	-	-	-	-	P4M2.3	P4M2.2	P4M2.1	P4M2.0	XXXX 0000b
P4M1	PORT 4 OUTPUT MODE 1	FAH	-	-	-	-	P4M1.3	P4M1.2	P4M1.1	P4M1.0	XXXX 0000b
IP1	INTERRUPT PRIORITY 1	F8H	(FF) PCAP	(FE) PPWM	(FD) PBRK	(FC) PWDI	(FB) -	(FA) PCI	(F9) PKB	(F8) PI2	0000 X000b
IP1H	INTERRUPT HIGH PRIORITY 1	F7H	PCAPH	PPWMH	PBRKH	PWDIH	-	PCIH	PKBH	PI2H	0000 X000b
PADIDS	PORT ADC DIGITAL INPUTS DISABLE	F6H	PADIDS.7	PADIDS.6	PADIDS.5	PADIDS.4	PADIDS.3	PADIDS.2	PADIDS.1	PADIDS.0	0000 0000b
SPDR	SERIAL PERIPHERAL DATA REGISTER	F5H	SPD.7	SPD.6	SPD.5	SPD.4	SPD.3	SPD.2	SPD.1	SPD.0	XXXX XXXXb
SPSR	SERIAL PERIPHERAL STATUS REGISTER	F4H	SPIF	WCOL	SPIOVF	MODF	DRSS	-	-	-	0000 0XXXb
SPCR	SERIAL PERIPHERAL CONTROL REGISTER	F3H	SSOE	SPE	LSBFE	MSTR	CPOL	CPHA	SPR1	SPR0	0000 0100b
PCH	PC COUNTER HIGH REGISTER	F2H									0000 0000b
PCL	PC COUNTER LOW REGISTER	F1H									0000 0000b
B	B REGISTER	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	0000 0000b
IP2H	INTERRUPT HIGH PRIORITY 2	EFH	-	PT2H	-	-	PSPIH	-	-	PET3H	X0XX 0XX0b
PMD	PWM MASK DATA REGISTER	EEH	-	-	PMD.5	PMD.4	PMD.3	PMD.2	PMD.1	PMD.0	XX00 0000b
PME	PWM MASK ENABLE REGISTER	EDH	-	-	PME.5	PME.4	PME.3	PME.2	PME.1	PME.0	XX00 0000b
PORTS	PORT SHMITT REGISTER	ECH	-	-	-	P4S	P3S	P2S	P1S	P0S	XXX0 0000b
EIE1	INTERRUPT ENABLE 1	E8H	(EF) ECPTF	(EE) EPWM	(ED) EBRK	(EC) EWDI	(EB) -	(EA) ECI	(E9) EKB	(E8) EI2C	0000 X000b
CCH1	INPUT CAPTURE 1 HIGH	E7H	CCH1.7	CCH1.6	CCH1.5	CCH1.4	CCH1.3	CCH1.2	CCH1.1	CCH1.0	0000 0000b
CCL1	INPUT CAPTURE 1 LOW	E6H	CCL1.7	CCL1.6	CCL1.5	CCL1.4	CCL1.3	CCL1.2	CCL1.1	CCL1.0	0000 0000b
CCH0	INPUT CAPTURE 0 HIGH	E5H	CCH0.7	CCH0.6	CCH0.5	CCH0.4	CCH0.3	CCH0.2	CCH0.1	CCH0.0	0000 0000b
CCL0	INPUT CAPTURE 0 LOW	E4H	CCL0.7	CCL0.6	CCL0.5	CCL0.4	CCL0.3	CCL0.2	CCL0.1	CCL0.0	0000 0000b
ADCCON1	ADC CONTROL REGISTER 1	E3H	ADCLK.1	ADCLK.0	STADCT.1	STADCT.0	DLYDIV	ADCCM	PWMSRC.1	PWMSRC.0	0000 0000b
ADCH	ADC CONVERTER RESULT	E2H	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	XXXX XXXXb
ADCCON	ADC CONTROL REGISTER	E1H	ADC.1	ADC.0	ADCEX	ADCI	ADCS	AADR2	AADR1	AADR0	XX00 0000b
ACC	ACCUMULATOR	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	0000 0000b
PWMB	PWM BRAKE OUTPUT	DFH	-	-	PWM5B	PWM4B	PWM3B	PWM2B	PWM1B	PWM0B	XX00 0000b
PWM2L	PWM 2 LOW BITS REGISTER	DDH	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0	0000 0000b
PWMCON1	PWM CONTROL REGISTER 1	DCH	PWMRUN	LOAD	PWMF	CLRPWM	FBK1	FBK0	PMOD.1	PMOD.0	0000 0000b
PWM0L	PWM 0 LOW BITS REGISTER	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	0000 0000b
PWMPL	PWM COUNTER LOW REGISTER	D9H	PWMP0.7	PWMP0.6	PWMP0.5	PWMP0.4	PWMP0.3	PWMP0.2	PWMP0.1	PWMP0.0	0000 0000b
WDCON	WATCH-DOG CONTROL	D8H	(DF) WDRUN	(DE) -	(DD) WD1	(DC) WD0	(DB) WDIF	(DA) WTRF	(D9) EWRST	(D8) WDCLR	EXTERNAL RESET: 0X00 0X00b WATCHDOG RESET: 0X000100b POWER ON RESET 0X00 0000b
PWMCON3	PWM CONTROL REGISTER 3	D7H	HZ_Even	HZ_Odd	GRP	PWMTYPE	-	-	P6CTRL	INT_TYPE	XX00 XX00b
PWM2H	PWM 2 HIGH BITS REGISTER	D5H	-	-	-	-	PWM2.11	PWM2.10	PWM2.9	PWM2.8	XXXX 0000b

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
EIE2	INTERRUPT ENABLE 2	D4H	-	ET2	-	-	ESPI	-	EADCP	ET3	X0XX 0X00b
PWM0H	PWM 0 HIGH BITS REGISTER	D2H	-	-	-	-	PWM0.11	PWM0.10	PWM0.9	PWM0.8	XXXX 0000b
PWMPH	PWM COUNTER HIGH REGISTER	D1H	-	-	-	-	PWMP.11	PWMP.10	PWMP.9	PWMP.8	XXXX 0000b
PSW	PROGRAM STATUS WORD	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	0000 0000b
NVMDATA	NVM DATA	CFH	NVMDATA.7	NVMDATA.6	NVMDATA.5	NVMDATA.4	NVMDATA.3	NVMDATA.2	NVMDATA.1	NVMDATA.0	0000 0000b
NVMCON	NVM CONTROL	CEH	EER	EWR	-	-	-	-	-	-	00XX XXXXb
TH2	TIMER 2 MSB	CDH	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0	0000 0000b
TL2	TIMER 2 LSB	CCH	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0	0000 0000b
RCAP2H	TIMER 2 RELOAD MSB	CBH	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0	0000 0000b
RCAP2L	TIMER 2 RELOAD LSB	CAH	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0	0000 0000b
T2MOD	TIMER 2 MODE	C9H	ENLD	ICEN2	ICEN1	ICEN0	T2CR	CMPCR	-	-	0000 00XXb
T2CON	TIMER 2 CONTROL	C8H	TF2	-	-	-	-	TR2	-	CMP/RL2	0XXX X0X0b
TA	TIMED ACCESS PROTECTION	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	0000 0000b
NVMADDRL	NVM LOW BYTE ADDRESS	C6H	NVMADDR.7	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0	0000 0000b
NVMADDRH	NVM HIGH BYTE ADDRESS	C5H	-	-	-	-	-	-	-	NVMADDR.8	XXXX XXX0b
PNP	PWM NEGATIVE POLRARITY	C3H	-	-	PNP.5	PNP.4	PNP.3	PNP.2	PNP.1	PNP.0	XX00 0000b
T3CON	TIMER 3 CONTOL	C2H	TF3	EXF3	T3CNTE	T3OE	T3RST	TR3	T3MOD.1	T3MOD.0	0000 0000b
I2ADDR	I2C ADDRESS1	C1H	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	XXXX XXX0b
I2CON	I2C CONTROL REGISTER	C0H	(C7) -	(C6) ENSI	(C5) STA	(C4) STO	(C3) SI	(C2) AA	(C1) -	(C0) -	X00000XXb
I2TOC	I2C TIMER-OUT COUNTER REGISTER	BFH	-	-	-	-	-	ENTI	DIV4	TIF	XXXX X000b
I2CLK	I2C CLOCK RATE	BEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	00000000b
I2STATUS	I2C STATUS REGISTER	BDH	B7	B6	B5	B4	B3	B2	B1	B0	1111 1000b
I2DAT	I2C DATA REGISTER	BCH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	XXXX XXXXb
SADEN	SLAVE ADDRESS MASK	B9H	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0	0000 0000b
IP0	INTERRUPT PRIORITY	B8H	(BF) -	(BE) PADC	(BD) PBO	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	X000 0000b
IP0H	INTERRUPT HIGH PRIORITY	B7H	-	PADCH	PBOH	PSH	PT1H	PX1H	PT0H	PX0H	X000 0000b
P2M2	PORT 2 OUTPUT MODE 2	B6H	P2M2.7	P2M2.6	P2M2.5	P2M2.4	P2M2.3	P2M2.2	P2M2.1	P2M2.0	0000 0000b
P2M1	PORT 2 OUTPUT MODE 1	B5H	P2M1.7	P2M1.6	P2M1.5	P2M1.4	P2M1.3	P2M1.2	P2M1.1	P2M1.0	0000 0000b
P1M2	PORT 1 OUTPUT MODE 2	B4H	P1M2.7	-	-	-	P1M2.3	P1M2.2	P1M2.1	P1M2.0	000X 0000b
P1M1	PORT 1 OUTPUT MODE 1	B3H	P1M1.7	-	-	-	P1M1.3	P1M1.2	P1M1.1	P1M1.0	000X 0000b
P0M2	PORT 0 OUTPUT MODE 2	B2H	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0	0000 0000b
P0M1	PORT 0 OUTPUT MODE 1	B1H	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0	0000 0000b
P3	PORT 3	B0H	(B7) P3.7 OPN	(B6) P3.6 OPP	(B5) P3.5	(B4) P3.4	(B3) P3.3 PWM7	(B2) P3.2 PWM5	(B1) P3.1 PWM3	(B0) P3.0 PWM1	1111 1111b[1] 0000 0000b
ADCDLY	ADC DELAY START REGISTER	AFH	ADCDLY.7	ADCDLY.6	ADCDLY.5	ADCDLY.4	ADCDLY.3	ADCDLY.2	ADCDLY.1	ADCDLY.0	0000 0000b
PDTC0	PWM DEAD TIME CONTROL 0 REGISTER	AEH	-	-	-	-	-	DTENB4	DTENB2	DTENB0	XXXX X000b
CMP2	COMPARATOR 1 CONTROL REGISTER	ADH	-	HYSEN2	CMPEN2	CP2	CN2	COE2	CO2	CMF2	XX0X 0000b
CMP1	COMPARATOR 1 CONTROL REGISTER	ACH	-	HYSEN1	CMPEN1	-	CN1	COE1	CO1	CMF1	XX0X 0000b
DTCNT	PWM DEAD TIME COUNTER REGISTER	ABH	DTCNT.7	DTCNT.6	DTCNT.5	DTCNT.4	DTCNT.3	DTCNT.2	DTCNT.1	DTCNT.0	0000 0000b
SADDR	SLAVE ADDRESS	A9H	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0	0000 0000b
IE	INTERRUPT ENABLE	A8H	(AF) EA	(AE) EADC	(AD) EBO	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000b
CCH2	INPUT CAPTURE 2 HIGH	A7H	CCH2.7	CCH2.6	CCH2.5	CCH2.4	CCH2.3	CCH2.2	CCH2.1	CCH2.0	0000 0000b

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
CCL2	INPUT CAPTURE 2 LOW	A6H	CCL2.7	CCL2.6	CCL2.5	CCL2.4	CCL2.3	CCL2.2	CCL2.1	CCL2.0	0000 0000b
P4	PORT 4	A5H	-	-	-	-	P4.3	P4.2	P4.1 CP2PB	P4.0 CP2NB	XXXX 1111b(1) XXXX 0000b
CAPCON1	CAPTURE CONTROL 1	A4H	-	IC0SS	ENF2	ENF1	ENF0	CPTF2	CPTF1	CPTF0	X000 0000b
CAPCON0	CAPTURE CONTROL 0	A3H	CCT2.1	CCT2.0	CCT1.1	CCT1.0	CCT0.1	CCT0.0	CCLD.1	CCLD.0	0000 0000b
AUXR1	AUX FUNCTION REGISTER 1	A2H	KBF	BOD	BOI	LPBOD	SRST	ADCEN	RCCLK	BOS	0X00 0000b
KBI	KEYBOARD INTERRUPT	A1H	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0	0000 0000b
P2	PORT 2	A0H	(A7) P2.7 T1	(A6) P2.6 IC2 MOSI	(A5) P2.5 IC1 MISO	(A4) P2.4 IC0 /SS	(A3) P2.3 T3 SCLK	(A2) P2.2 PWM4	(A1) P2.1 PWM2 CP1O	(A0) P2.0 PWM0 CP2O	1111 1111b(1) 0000 0000b
P3M2	PORT 3 OUTPUT MODE 2	9FH	P3M2.7	P3M2.6	P3M2.5	P3M2.4	P3M2.3	P3M2.2	P3M2.1	P3M2.0	0000 0000b
P3M1	PORT 3 OUTPUT MODE 1	9EH	P3M1.7	P3M1.6	P3M1.5	P3M1.4	P3M1.3	P3M1.2	P3M1.1	P3M1.0	0000 0000b
ADCRH	ADC COMPARE REFERENCE HIGH DATA REGISTER	9DH	ADCR.9	ADCR.8	ADCR.7	ADCR.6	ADCR.5	ADCR.4	ADCR.3	ADCR.2	XXXX XXXXb
ADCRL	ADC COMPARE REFERENCE LOW DATA/COMPARE REGISTER	9CH	ADCR.1	ADCR.0	ADCPO	ADCPI	-	-	T3CSS	ENADCP	XX10 XX00b
PIO	PWM IO REGISTER	9BH	PIO.7	PIO.6	PIO.5	PIO.4	PIO.3	PIO.2	PIO.1	PIO.0	0000 0000b
IP2	INTERRUPT PRIORITY 2	9AH	-	PT2	-	-	PSPI	-	-	PET3	X0XX 0XX0b
SBUF	SERIAL BUFFER	99H	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0	XXXX XXXXb
SCON	SERIAL CONTROL	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000b
PWM4H	PWM 4 HIGH BITS REGISTER	97H	-	-	-	-	PWM4.11	PWM4.10	PWM4.9	PWM4.8	XXXX 0000b
PWM4L	PWM 4 LOW BITS REGISTER	96H	PWM4.7	PWM4.6	PWM4.5	PWM4.4	PWM4.3	PWM4.2	PWM4.1	PWM4.0	0000 0000b
RCAP3HT3H	TIMER 3 RELOAD MSB	93H	RCAP3.11	RCAP3.10	RCAP3.9	RCAP3.8	T3.11	T3.10	T3.9	T3.8	0000 0000b
RCAP3L	TIMER 3 RELOAD LSB	92H	RCAP3.7	RCAP3.6	RCAP3.5	RCAP3.4	RCAP3.3	RCAP3.2	RCAP3.1	RCAP3.0	0000 0000b
TL3	TIMER 3 LSB	91H	T3.7	T3.6	T3.5	T3.4	T3.3	T3.2	T3.1	T3.0	0000 0000b
P1	PORT 1	90H	(97) P1.7 STADC BKP0	(96) P1.6 /INT0 SDA	(95) P1.5 T0 SCL BKP1	(94) P1.4 /RST	(93) P1.3 RXD	(92) P1.2 TXD	(91) P1.1 XT1	(90) P1.0 XT2 CLKOUT	1111 1111b(1) 0000 0000b
CKCON	CLOCK CONTROL	8EH	-	-	-	T1M	T0M	-	-	-	XXX0 0XXXb
TH1	TIMER HIGH 1	8DH	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0	0000 0000b
TH0	TIMER HIGH 0	8CH	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0	0000 0000b
TL1	TIMER LOW 1	8BH	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0	0000 0000b
TL0	TIMER LOW 0	8AH	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0	0000 0000b
TMOD	TIMER MODE	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	0000 0000b
TCON	TIMER CONTROL	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0000 0000b
PCON	POWER CONTROL	87H	SMOD	SMOD0	BOF	POR	GF1	GF0	PD	IDL	00XX 0000b
DIV	DIVIDER	86H	CCDIV.1	CCDIV.0	PWMDIV.1	PWMDIV.0	T3DIV.1	T3DIV.0	T0DIV.1	T0DIV.0	0000 0000b
DPH	DATA POINTER HIGH	83H	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0	0000 0000b
DPL	DATA POINTER LOW	82H	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0	0000 0000b
SP	STACK POINTER	81H	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0	0000 0111b
P0	PORT 0	80H	(87) P0.7 ADC7 PWM6 KB7	(86) P0.6 ADC6 /INT1 KB6	(85) P0.5 ADC5 KB5	(84) P0.4 ADC4 CP1N KB4	(83) P0.3 ADC3 CP1P KB3	(82) P0.2 ADC2 CP2NA KB2	(81) P0.1 ADC1 CP2PA KB1	(80) P0.0 ADC0 OPO KB0	1111 1111b(1) 0000 0000b

Note: 1. If config0.PRHI=1, the initial value is FFh at reset. If config0.PRHI=0, the initial value is 00h at reset

7.2 SFR Detail Bit Descriptions

PORT 0 **Initial=1111_1111b/0000_0000b**

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

P0.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. If config0.PRHI=1, the initial value is FFh at reset. If config0.PRHI=0, the initial value is 00h at reset. These alternate functions are described below.

BIT	NAME	FUNCTION
7	P0.7	ADC7 or PWM6 or KB7 pin or I/O pin by alternative.
6	P0.6	ADC6 or /INT1 or KB6 or I/O pin by alternative.
5	P0.5	ADC5 or KB5 or Clock (ICP function) pin or I/O pin by alternative.
4	P0.4	ADC4 or CP1N or KB4 or Data (ICP function) pin or I/O pin by alternative.
3	P0.3	ADC3 or CP1P or KB3 pin or I/O pin by alternative.
2	P0.2	ADC2 or CP2NA or KB2 pin or I/O pin by alternative.
1	P0.1	ADC1 or CP2PA or KB1 pin or I/O pin by alternative.
0	P0.0	ADC0 or OPO or KB0 pin or I/O pin by alternative.

Note: The initial value of the port is set by CONFIG0.PRHI bit. The default setting for CONFIG0.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG0.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

STACK POINTER **Initial=0000 0111b**

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

BIT	NAME	FUNCTION
7-0	SP.[7:0]	The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

DATA POINTER LOW **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

BIT	NAME	FUNCTION

7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH **Initial=0000 0000b**

Bit: 7 6 5 4 3 2 1 0

DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

BIT	NAME	FUNCTION
7-0	DPH.[7:0]	This is the high byte of the standard 8052 16-bit data pointer. This is the high byte of the DPTR 16-bit data pointer.

DIVIDER **Initial=0000 0000b**

Bit: 7 6 5 4 3 2 1 0

CCDIV.1	CCDIV.0	PWMDIV.1	PWMDIV.0	T3DIV.1	T3DIV.0	T0DIV.1	T0DIV.0

Mnemonic: DIV Address: 86h

BIT	NAME	FUNCTION
7~6	CCDIV.1~0	Timer 2 clock select: CCDIV.1 / CCDIV.0 0 / 0 : Timer 2 clock = Fcpu 0 / 1 : Timer 2 clock = Fcpu/4 1 / 0 : Timer 2 clock = Fcpu/16 1 / 1 : Timer 2 clock = Fcpu/32
5~4	PWMDIV.1~0	PWM clock select: PWMDIV.1 / PWMDIV.0 0 / 0 : PWM clock = Fcpu 0 / 1 : PWM clock = Fcpu/2 1 / 0 : PWM clock = Fcpu/4 1 / 1 : PWM clock = Fcpu/16
3~2	T3DIV.1~0	Timer 3 clock select: T3DIV.1 / T3DIV.0 0 / 0 : Timer 3 clock = Fcpu/4 0 / 1 : Timer 3 clock = Fcpu/16 1 / 0 : Timer 3 clock = Fcpu/32

		1	1	Timer 3 clock = Fcpu/128	
1~0	T0DIV.1~0	Timer 2 clock select:			
		T0DIV.1	T0DIV.0		
		0	0	Timer 0 clock = Fcpu/4	
		0	1	Timer 0 clock = Fcpu/16	
		1	0	Timer 0 clock = Fcpu/32	
		1	1	Timer 0 clock = Fcpu/128	

POWER CONTROL **Initial=00xx 0000b**

Bit: 7 6 5 4 3 2 1 0

SMOD	SMOD0	BOF	POR	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3.
6	SMOD0	0: Framing Error Detection Disable. SCON.7 (SM0/FE) bit is used as SM0 (standard 8052 function). 1: Framing Error Detection Enable. SCON.7 (SM0/FE) bit is used to reflect as Frame Error (FE) status flag.
5	BOF	0: Cleared by software. 1: Set automatically when a brownout reset or interrupt has occurred. Also set at power on.
4	POR	0: Cleared by software. 1: Set automatically when a power-on reset has occurred.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: The CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.
0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

TIMER CONTROL **Initial=0000 0000b**

Bit: 7 6 5 4 3 2 1 0

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared

		automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.

2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1) Timer/Counter 1 is stopped.

TIMER 0 LSB **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

BIT	NAME	FUNCTION
7-0	TL0.[7:0]	Timer 0 LSB.

TIMER 1 LSB **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

BIT	NAME	FUNCTION
7-0	TL1.[7:0]	Timer 1 LSB.

TIMER 0 MSB **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

BIT	NAME	FUNCTION
7-0	TH0.[7:0]	Timer 0 MSB.

TIMER 1 MSB **Initial=0000 0000b**

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

BIT	NAME	FUNCTION
7-0	TH1.[7:0]	Timer 1 MSB.

CLOCK CONTROL **Initial=xxx0 0xxxb**

Bit:	7	6	5	4	3	2	1	0
	-	-	-	T1M	T0M	-	-	-

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7-5	-	Reserved.
4	T1M	Timer 1 clock select: 0: Timer 1 uses a divide by 12 clocks. 1: Timer 1 uses a divide by 4clocks.
3	T0M	Timer 0 clock select: 0: Timer 0 uses a divide by 12 clocks. 1: Timer 0 uses a divide by 4 clocks. 4/16/32/128 clocks. The divider selection bits are located in SFR DIV.T0DIV[1:0].
2~0	-	Reserved.

PORT 1 **Initial=1111_1111b/0000_0000b**

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. If config0.PRHI=1, the initial value is FFh at reset. If config0.PRHI=0, the initial value is 00h at reset. These alternate functions are described below.

BIT	NAME	FUNCTION
7	P1.7	BKP1 or STADC or I/O pin by alternative.
6	P1.6[(1)]	$\overline{INT0}$ interrupt or SDA or I/O pin by alternative.
5	P1.5[(1)]	BKP0 or T0 or SCL or Input Pin by alternative.
4	P1.4	$\overline{RST}$ pin or digital input pin by alternative.