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We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

NAND01G-B2B
NAND02G-B2C

1-Gbit, 2-Gbit,
2112-byte/1056-word page, 1.8 V/3 V, NAND flash memory

Features

- High density NAND flash memories
  – Up to 2 Gbits of memory array
  – Cost effective solutions for mass storage applications
- NAND interface
  – x8 or x16 bus width
  – Multiplexed address/ data
  – Pinout compatibility for all densities
- Supply voltage: 1.8 V/3.0 V
- Page size
  – x8 device: (2048 + 64 spare) bytes
  – x16 device: (1024 + 32 spare) words
- Block size
  – x8 device: (128 K + 4 K spare) bytes
  – x16 device: (64 K + 2 K spare) words
- Page read/program
  – Random access: 25 μs (max)
  – Sequential access: 30 ns (min)
  – Page program time: 200 μs (typ)
- Copy back program mode
- Cache program and cache read modes
- Fast block erase: 2 ms (typ)
- Status register
- Electronic signature
- Chip enable 'don't care'

TSOP48 12 x 20 mm

VFBGA63 9.5 x 12 x 1 mm
VFBGA63 9 x 11 x 1 mm
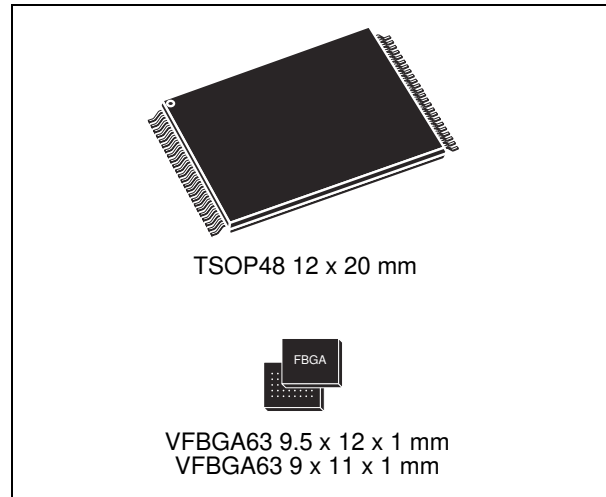
- Serial number option
- Data protection
  – Hardware block locking
  – Hardware program/erase locked during power transitions
- Data integrity
  – 100 000 program/erase cycles per block (with ECC)
  – 10 years data retention
- ECOPACK® packages
- Development tools
  – Error correction code models
  – Bad blocks management and wear leveling algorithms
  – Hardware simulation models

Table 1.   Device summary

Reference	Part number
NAND01G-B2B	NAND01GR3B2B, NAND01GW3B2B
	NAND01GR4B2B, NAND01GW4B2B[1]
NAND02G-B2C	NAND02GR3B2C, NAND02GW3B2C
	NAND02GR4B2C, NAND02GW4B2C[1]

1. x16 organization only available for MCP products.

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1 Description

NAND01G-B2B and NAND02G-B2C flash 2112-byte/1056-word page is a family of non-volatile flash memories that uses NAND cell technology. The devices range from 1 Gbit to 2 Gbits and operate with either a 1.8 V or 3 V voltage supply. The size of a page is either 2112 bytes (2048 + 64 spare) or 1056 words (1024 + 32 spare) depending on whether the device has a x8 or x16 bus width.

The address lines are multiplexed with the Data Input/Output signals on a multiplexed x8 or x16 input/output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased over 100 000 cycles (with ECC on). To extend the lifetime of NAND flash devices it is strongly recommended to implement an error correction code (ECC).

The devices feature a write protect pin that allows performing hardware protection against program and erase operations.

The devices feature an open-drain ready/busy output that can be used to identify if the program/erase/read (P/E/R) controller is currently active. The use of an open-drain output allows the ready/busy pins from several memories to be connected to a single pull-up resistor.

A Copy Back Program command is available to optimize the management of defective blocks. When a page program operation fails, the data can be programmed in another page without having to resend the data to be programmed.

Each device has cache program and cache read features which improve the program and read throughputs for large files. During cache programming, the device loads the data in a cache register while the previous data is transferred to the page buffer and programmed into the memory array. During cache reading, the device loads the data in a cache register while the previous data is transferred to the I/O buffers to be read.

All devices have the chip enable don't care feature, which allows code to be directly downloaded by a microcontroller, as chip enable transitions during the latency time do not stop the read operation.

All devices have the option of a unique identifier (serial number), which allows each device to be uniquely identified.

The unique identifier options is subject to an NDA (non disclosure agreement) and so not described in the datasheet. For more details of this option contact your nearest Numonyx sales office.

The devices are available in the following packages:
● TSOP48 (12 x 20 mm)
● VFBGA63 (9.5 x 12 x 1 mm, 0.8 mm pitch) for NAND02G-B2C devices
● VFBGA63 (9 x 11 x 1 mm, 0.8 mm pitch) for NAND01G-B2B devices.

For information on how to order these options refer to *Table 29: Ordering information scheme*. Devices are shipped from the factory with Block 0 always valid and the memory content bits, in valid blocks, erased to '1'.

See *Table 2: Product description*, for all the devices available in the family.

Table 2. **Product description**

Reference	Part number	Density	Bus width	Page size	Block size	Memory array	Operating voltage	Timings				Package
								Random access time (max)	Sequential access time (min)	Page Program time (typ)	Block erase (typ)	
NAND01G -B2B	NAND01GR3B2B	1Gbit	x8	2048 +64 bytes	128K +4K bytes	64 pages x 1024 blocks	1.7 to 1.95 V	25 µs	50 ns	200 µs	2 ms	VFBGA63 9 x 11 mm
	NAND01GW3B2B						2.7 to 3.6 V	25 µs	30 ns			TSOP48
	NAND01GR4B2B		x16	1024 +32 words	64K+ 2K words		1.7 to 1.95 V	25 µs	50 ns			(1)
	NAND01GW4B2B						2.7 to 3.6 V	25 µs	30 ns			(1)
NAND02G -B2C	NAND02GR3B2C	2Gbits	x8	2048 +64 bytes	128K +4K bytes	64 pages x 2048 blocks	1.7 to 1.95 V	25 µs	50 ns		2 ms	VFBGA63 9.5 x 12 mm
	NAND02GW3B2C						2.7 to 3.6 V	25 µs	30 ns			TSOP48
	NAND02GR4B2C		x16	1024 +32 words	64K+ 2K words		1.7 to 1.95 V	25 µs	50 ns			(1)
	NAND02GW4B2C						2.7 to 3.6 V	25 µs	30 ns			(1)

1. x16 organization only available for MCP.

Figure 1. **Logic block diagram**

AI12799
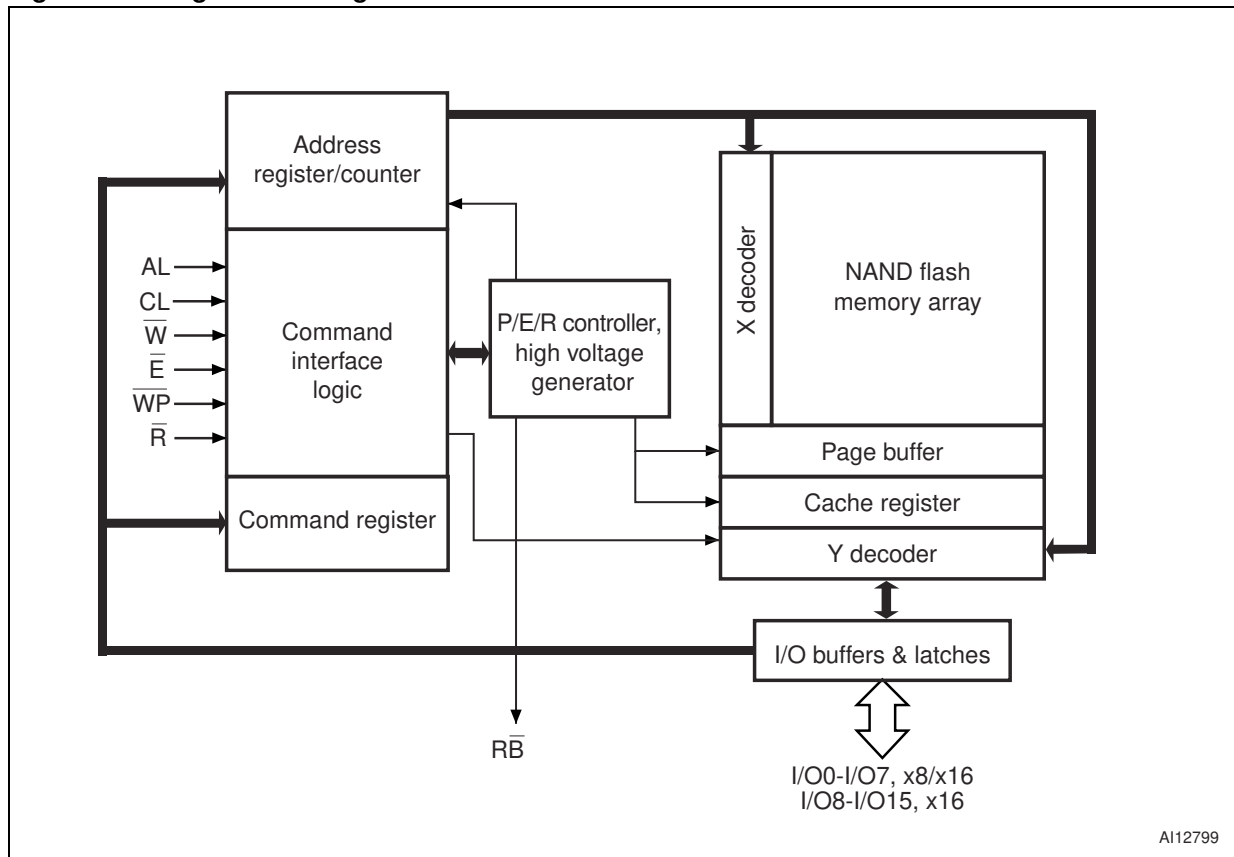
Figure 2.   Logic diagram
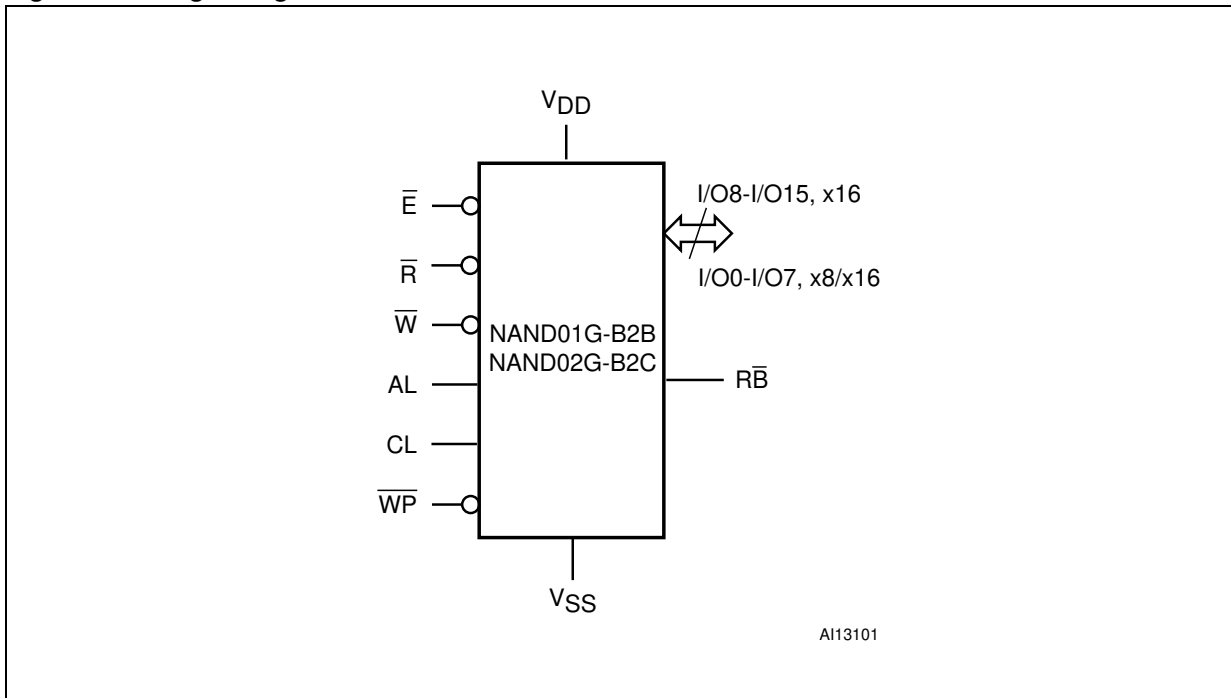
1.   x16 organization only available for MCP.

Table 3.   Signal names

Signal	Function	Direction
I/O8-15	Data input/outputs for x16 devices	I/O
I/O0-7	Data input/outputs, address inputs, or command inputs for x8 and x16 devices	I/O
AL	Address Latch Enable	Input
CL	Command Latch Enable	Input
$\overline{E}$	Chip Enable	Input
$\overline{R}$	Read Enable	Input
$R\overline{B}$	Ready/Busy (open-drain output)	Output
$\overline{W}$	Write Enable	Input
$\overline{WP}$	Write Protect	Input
V_{DD}	Supply voltage	Supply
V_{SS}	Ground	Supply
NC	Not connected internally	–
DU	Do not use	–

Figure 3.   TSOP48 connections

NC	①	48	NC
NC			NC
NC			NC
NC			NC
NC			I/O7
NC			I/O6
R$\overline{\text{B}}$			I/O5
$\overline{\text{R}}$			I/O4
$\overline{\text{E}}$			NC
NC			NC
NC			NC
V$_{DD}$	12 NAND01GW3B2B	37	V$_{DD}$
V$_{SS}$	13 NAND02GW3B2C	36	V$_{SS}$
NC			NC
NC			NC
CL			NC
AL			I/O3
$\overline{\text{W}}$			I/O2
$\overline{\text{WP}}$			I/O1
NC			I/O0
NC			NC
NC			NC
NC			NC
NC	24	25	NC
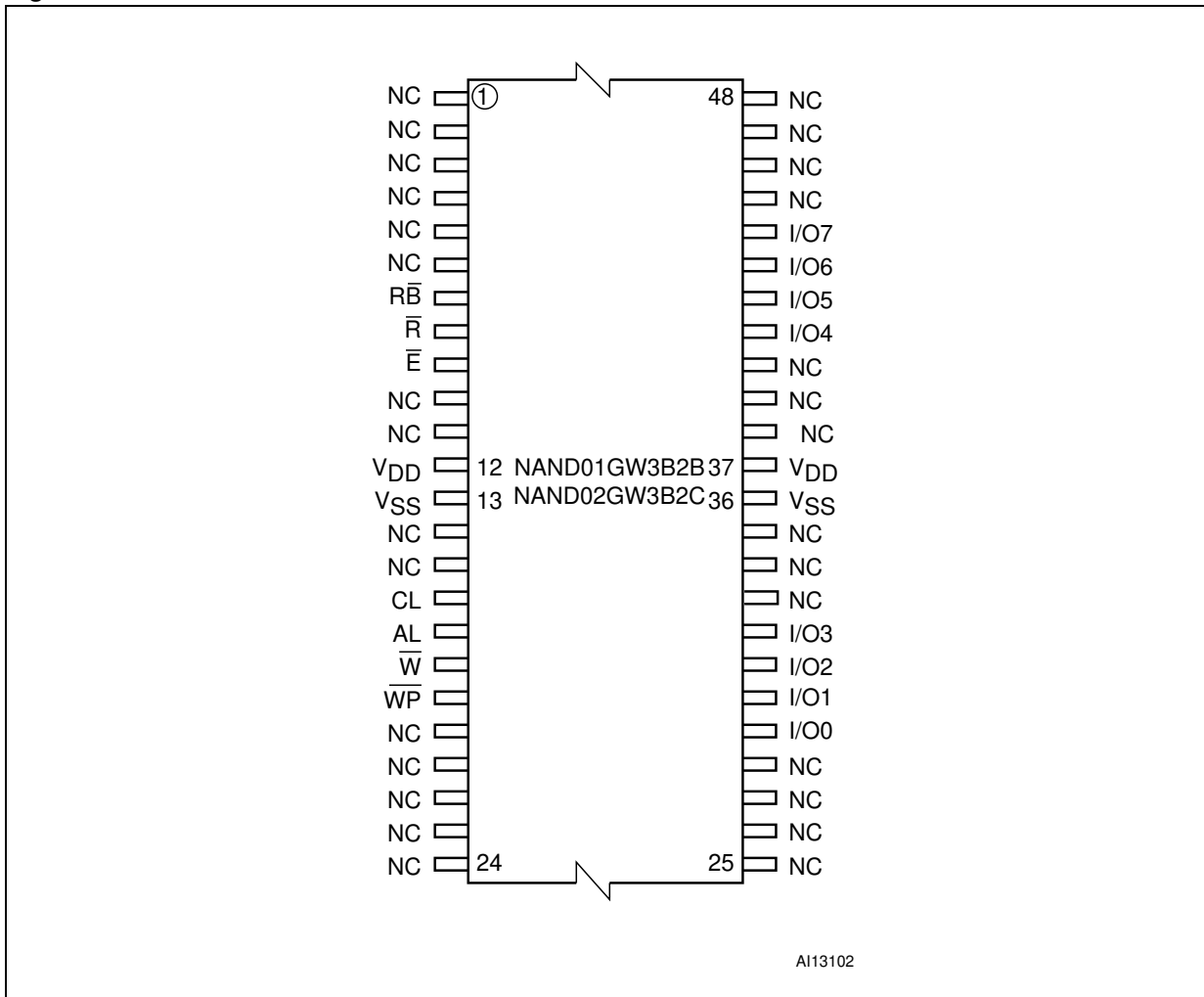
AI13102

1.   Available only for NAND01GW3B2B and NAND02GW3B2C 8-bit devices.

Figure 4.   VFBGA63 connections (top view through package)
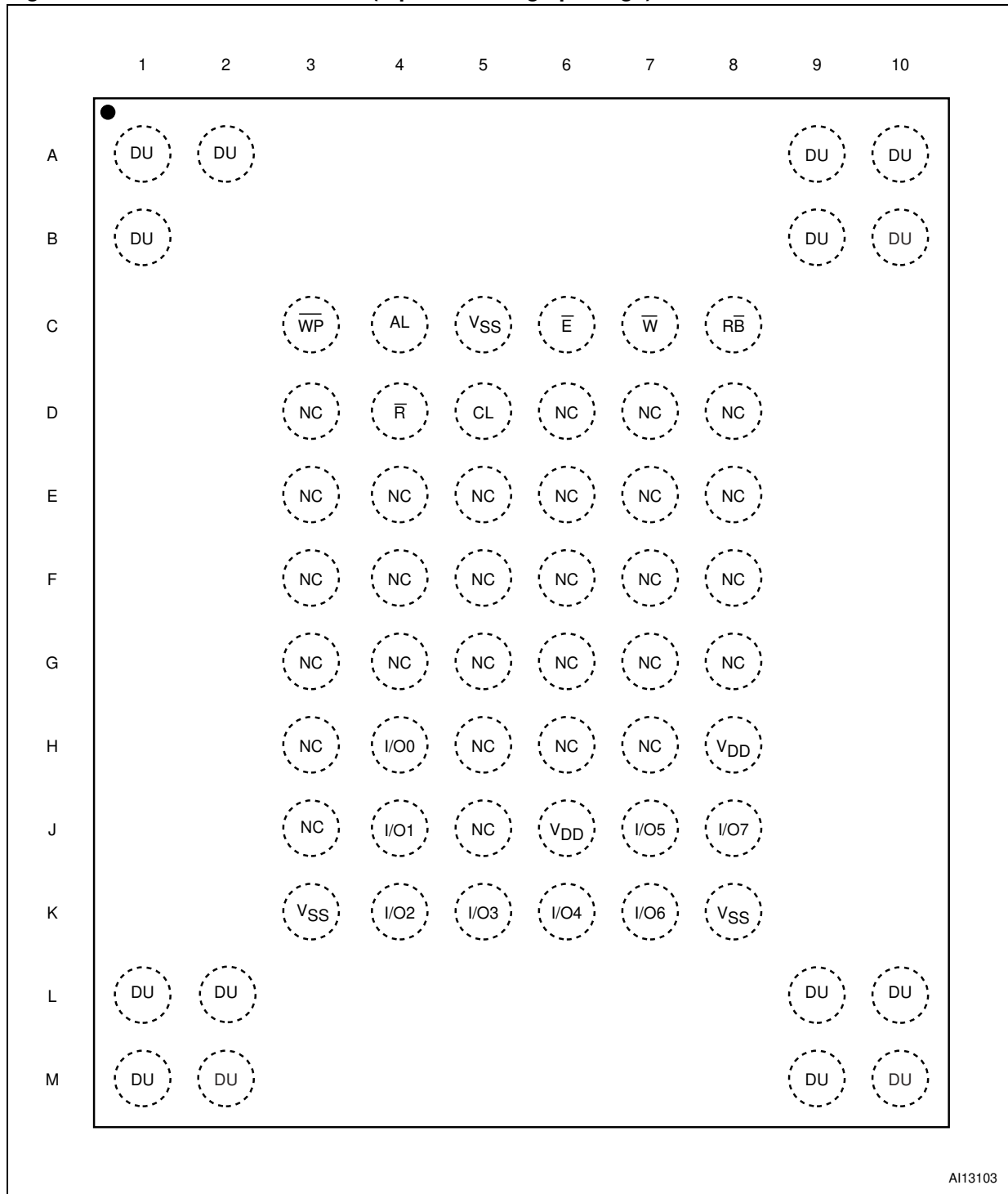
1.   Available only for NAND01GR3B2B and NAND02GR3B2C 8-bit devices.

2   Memory array organization

The memory array is made up of NAND structures where 32 cells are connected in series.

The memory array is organized in blocks where each block contains 64 pages. The array is split into two areas, the main area and the spare area. The main area of the array is used to store data whereas the spare area is typically used to store error correction codes, software flags or bad block identification.

In x8 devices the pages are split into a 2048-byte main area and a spare area of 64 bytes. In the x16 devices the pages are split into a 1,024-word main area and a 32-word spare area. Refer to *Figure 5: Memory array organization*.

2.1   Bad blocks

The NAND flash 2112-byte/1056-word page devices may contain bad blocks, that is blocks that contain one or more invalid bits whose reliability is not guaranteed. Additional bad blocks may develop during the lifetime of the device.

The bad block Information is written prior to shipping (refer to *Section 8.1: Bad block management* for more details).

Table 4: Valid blocks shows the minimum number of valid blocks in each device. The values shown include both the bad blocks that are present when the device is shipped and the bad blocks that could develop later on.

These blocks need to be managed using bad blocks management, block replacement or error correction codes (refer to *Section 8: Software algorithms*).

Table 4.   Valid blocks

Density of device	Min	Max
2 Gbits	2008	2048
1 Gbit	1004	1024

Figure 5.   **Memory array organization**
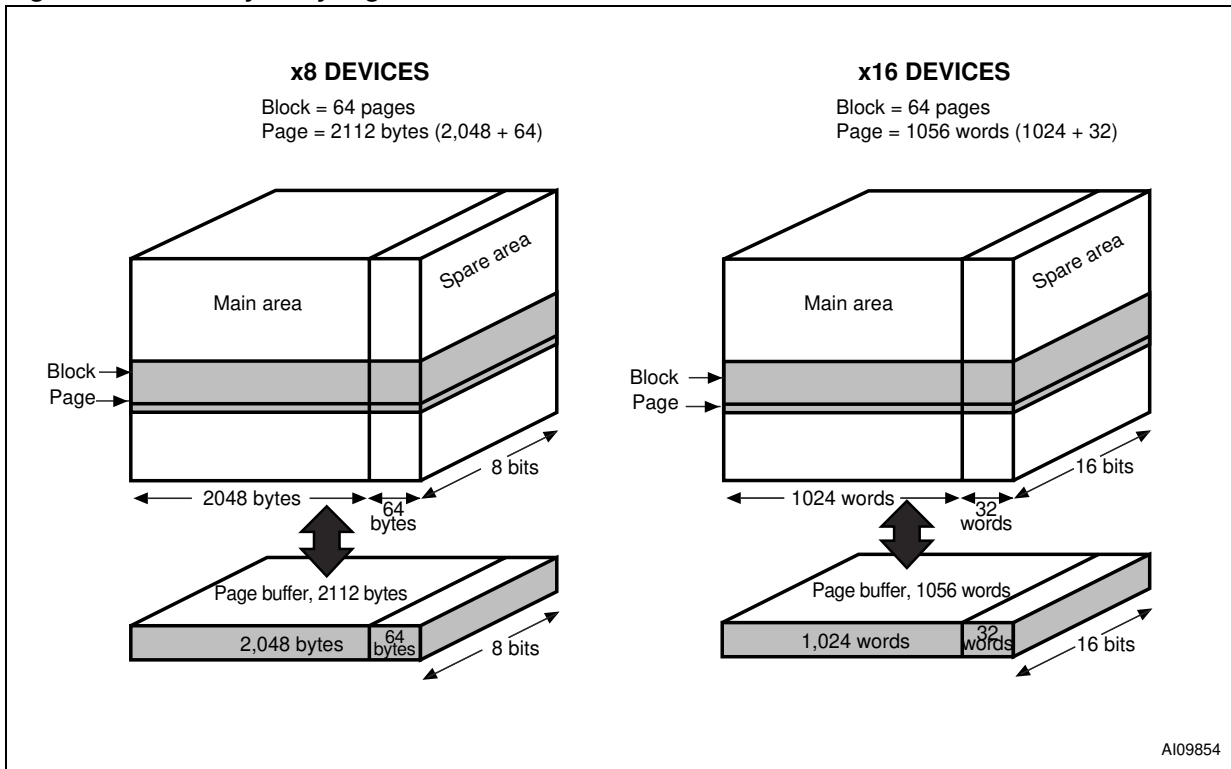
3   Signals description

See *Figure 2: Logic diagram*, and *Table 3: Signal names*, for a brief overview of the signals connected to this device.

3.1   Inputs/outputs (I/O0-I/O7)

Input/outputs 0 to 7 are used to input the selected address, output the data during a read operation or input a command or data during a write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

3.2   Inputs/outputs (I/O8-I/O15)

Input/outputs 8 to 15 are only available in x16 devices. They are used to output the data during a read operation or input data during a write operation. Command and address Inputs only require I/O0 to I/O7.

The inputs are latched on the rising edge of Write Enable. I/O8-I/O15 are left floating when the device is deselected or the outputs are disabled.

3.3   Address Latch Enable (AL)

The Address Latch Enable activates the latching of the address inputs in the command interface. When AL is High, the inputs are latched on the rising edge of Write Enable.

3.4   Command Latch Enable (CL)

The Command Latch Enable activates the latching of the command inputs in the command interface. When CL is High, the inputs are latched on the rising edge of Write Enable.

3.5   Chip Enable ($\overline{\text{E}}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is Low, V_{IL}, the device is selected. If Chip Enable goes High, v_{IH}, while the device is busy, the device remains selected and does not go into standby mode.

3.6   Read Enable ($\overline{\text{R}}$)

The Read Enable pin, $\overline{\text{R}}$, controls the sequential data output during read operations. Data is valid t_{RLQV} after the falling edge of $\overline{\text{R}}$. The falling edge of $\overline{\text{R}}$ also increments the internal column address counter by one.

3.7 Write Enable ($\overline{\text{W}}$)

The Write Enable input, $\overline{\text{W}}$, controls writing to the command interface, input address and data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 10 μs (min) is required before the command interface is ready to accept a command. It is recommended to keep Write Enable High during the recovery time.

3.8 Write Protect ($\overline{\text{WP}}$)

The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

3.9 Ready/Busy ($R\overline{B}$)

The Ready/Busy output, $R\overline{B}$, is an open-drain output that can be used to identify if the P/E/R controller is currently active. When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

Refer to the *Section 11.1: Ready/Busy signal electrical characteristics* for details on how to calculate the value of the pull-up resistor.

During power-up and power-down a minimum recovery time of 10 μs is required before the command interface is ready to accept a command. During this period the $R\overline{B}$ signal is Low, V_{OL}.

3.10 V_{DD} supply voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

An internal voltage detector disables all functions whenever V_{DD} is below V_{LKO} (see *Table 22* and *Table 23*) to protect the device from any involuntary program/erase during power-transitions.

Each device in a system should have V_{DD} decoupled with a 0.1 μF capacitor. The PCB track widths should be sufficient to carry the required program and erase currents.

3.11 V_{SS} ground

Ground, V_{SS}, is the reference for the power supply. It must be connected to the system ground.

4   Bus operations

There are six standard bus operations that control the memory. Each of these is described in this section, see *Table 5: Bus operations*, for a summary.

Typically, glitches of less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

4.1   Command input

Command input bus operations are used to give commands to the memory. Commands are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O0 to I/O7 are used to input commands.

See *Figure 19* and *Table 24* for details of the timings requirements.

4.2   Address input

Address input bus operations are used to input the memory addresses. Four bus cycles are required to input the addresses for 1-Gbit devices whereas five bus cycles are required for the 2-Gbit device (refer to *Table 6* and *Table 7*, Address insertion).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal. Only I/O0 to I/O7 are used to input addresses.

See *Figure 20* and *Table 24* for details of the timings requirements.

4.3   Data input

Data input bus operations are used to input the data to be programmed.

Data is accepted only when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low and Read Enable is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

See *Figure 21* and *Table 24* and *Table 25* for details of the timings requirements.

4.4   Data output

Data output bus operations are used to read: the data in the memory array, the status register, the lock status, the electronic signature and the unique identifier.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low. The data is output sequentially using the Read Enable signal.

See *Figure 22* and *Table 25* for details of the timings requirements.

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4.5 Write Protect

Write Protect bus operations are used to protect the memory against program or erase operations. When the Write Protect signal is Low the device will not accept program or erase operations and so the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection even during power-up.

4.6 Standby

When Chip Enable is High the memory enters standby mode, the device is deselected, outputs are disabled and power consumption is reduced.

Table 5.   Bus operations

Bus operation	$\overline{E}$	AL	CL	$\overline{R}$	$\overline{W}$	$\overline{WP}$	I/O0 - I/O7	I/O8 - I/O15[1]
Command input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X[2]	Command	X
Address input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address	X
Data input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	V_{IH}	Data input	Data input
Data output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data output	Data output
Write Protect	X	X	X	X	X	V_{IL}	X	X
Standby	V_{IH}	X	X	X	X	V_{IL}/V_{DD}	X	X

1. Only for x16 devices.

2. $\overline{WP}$ must be V_{IH} when issuing a program or erase command.

Table 6.   Address insertion, x8 devices

Bus cycle[1]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A11	A10	A9	A8
3rd	A19	A18	A17	A16	A15	A14	A13	A12
4th	A27	A26	A25	A24	A23	A22	A21	A20
5th[2]	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A28

1. Any additional address input cycles will be ignored.

2. The fifth cycle is valid for 2-Gbit devices. A28 is for 2-Gbit devices only.

Table 7.   Address insertion, x16 devices

Bus cycle[1]	I/O8-I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	X	A7	A6	A5	A4	A3	A2	A1	A0
2nd	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A10	A9	A8
3rd	X	A18	A17	A16	A15	A14	A13	A12	A11
4th	X	A26	A25	A24	A23	A22	A21	A20	A19
5th[2]	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A27

1. Any additional address input cycles will be ignored.

2. The fifth cycle is valid for 2-Gbit devices. A27 is for 2-Gbit devices only.

Table 8.   Address definitions, x8

Address	Definition	
A0 - A11	Column address	
A12 - A17	Page address	
A18 - A27	Block address	1-Gbit device
A18 - A28	Block address	2-Gbit device

Table 9.   Address definitions, x16

Address	Definition	
A0 - A10	Column address	
A11 - A16	Page address	
A17 - A26	Block address	1-Gbit device
A17 - A27	Block address	2-Gbit device

5   Command set

All bus write operations to the device are interpreted by the command interface. The commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is High. Device operations are selected by writing specific commands to the command register. The two-step command sequences for program and erase operations are imposed to maximize data security.

The commands are summarized in *Table 10: Commands*.

Table 10.   Commands

Command	Bus write operations[1]				Commands accepted during busy
	1st cycle	2nd cycle	3rd cycle	4th cycle	
Read	00h	30h	–	–	
Random Data Output	05h	E0h	–	–	
Cache Read	00h	31h	–	–	
Exit Cache Read	34h	–	–	–	Yes[2]
Page Program (Sequential Input default)	80h	10h	–	–	
Random Data Input	85h	–	–	–	
Copy Back Program	00h	35h	85h	10h	
Cache Program	80h	15h	–	–	
Block Erase	60h	D0h	–	–	
Reset	FFh	–	–	–	Yes
Read Electronic Signature	90h	–	–	–	
Read Status Register	70h	–	–	–	Yes

1. The bus cycles are only shown for issuing the codes. The cycles required to input the addresses or input/output data are not shown.

2. Only during Cache Read busy.

6   Device operations

The following section gives the details of the device operations.

6.1   Read memory array

At power-up the device defaults to read mode. To enter read mode from another mode the Read command must be issued, see *Table 10: Commands*.

Once a Read command is issued two types of operations are available: random read and page read.

6.1.1   Random read

Each time the Read command is issued the first read is random read.

6.1.2   Page read

After the first random read access, the page data (2112 bytes or 1056 words) is transferred to the page buffer in a time of t_{WHBH} (refer to *Table 25* for value). Once the transfer is complete the Ready/Busy signal goes High. The data can then be read out sequentially (from selected column address to last column address) by pulsing the Read Enable signal.

The device can output random data in a page, instead of the consecutive sequential data, by issuing a Random Data Output command.

The Random Data Output command can be used to skip some data during a sequential data output.

The sequential operation can be resumed by changing the column address of the next data to be output, to the address which follows the Random Data Output command.

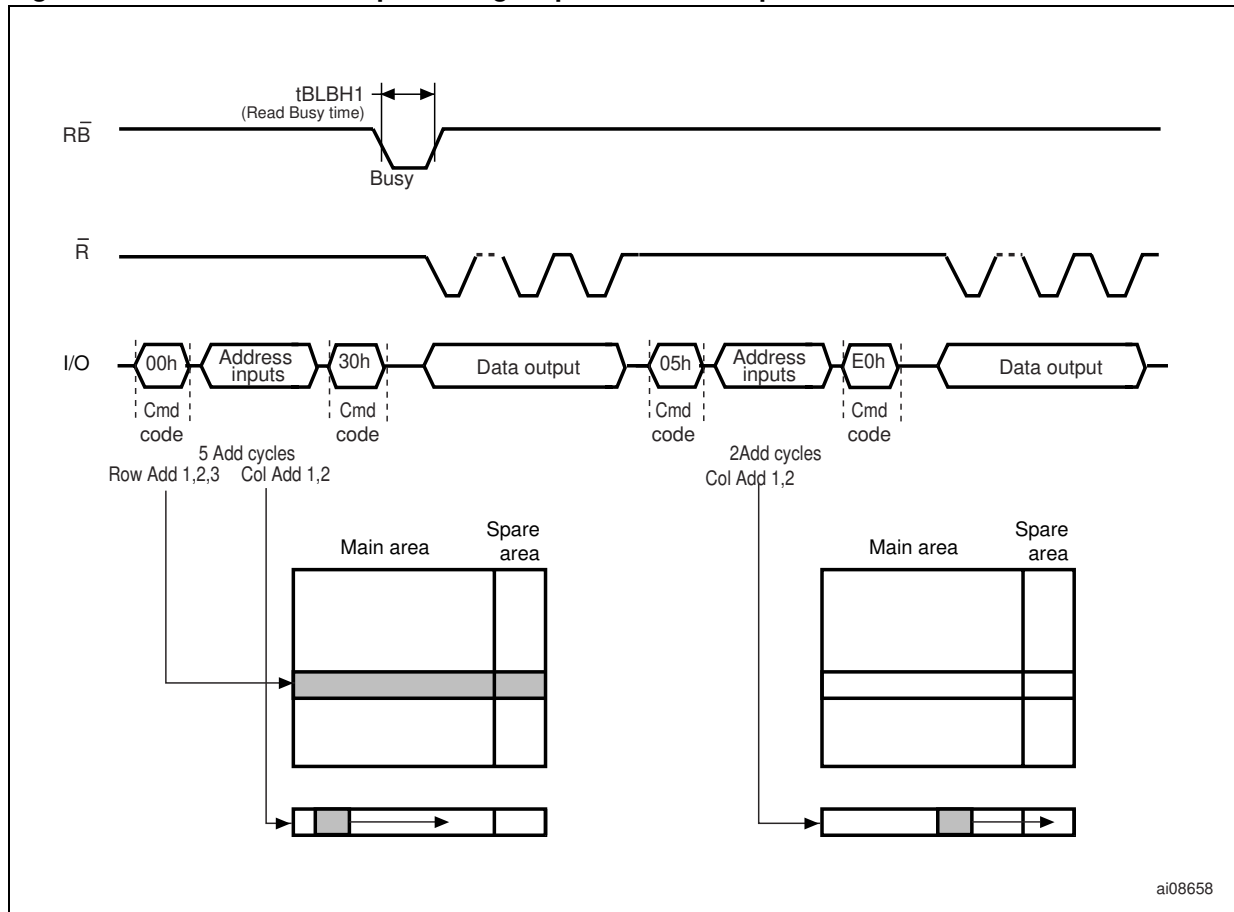The Random Data Output command can be issued as many times as required within a page.

The Random Data Output command is not accepted during cache read operations.

Figure 6.   **Read operations**
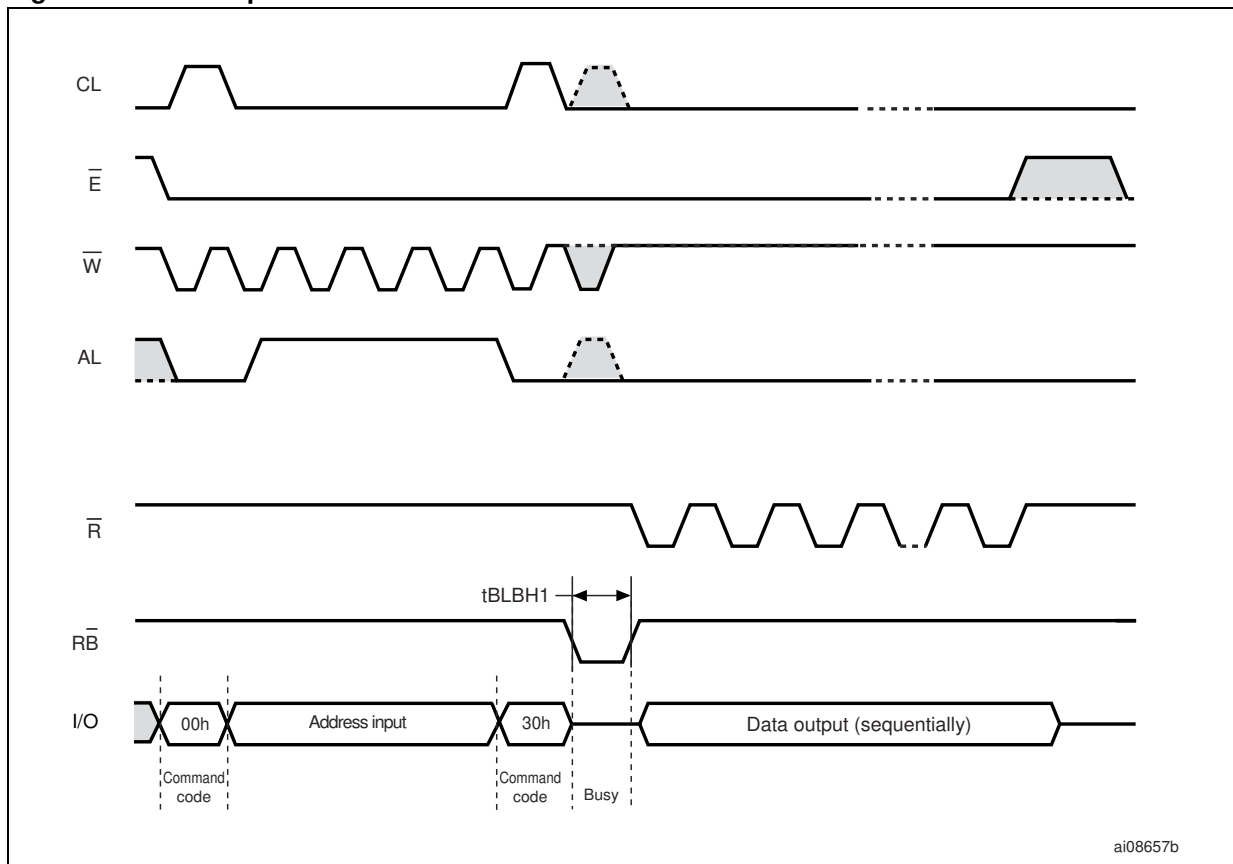
1. Highest address depends on device density.

Figure 7.   Random data output during sequential data output

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6.2   Cache read

The cache read operation is used to improve the read throughput by reading data using the cache register. As soon as the user starts to read one page, the device automatically loads the next page into the cache register.

A cache read operation consists of three steps (see *Table 10: Commands*):

1. One bus cycle is required to setup the Cache Read command (the same as the standard Read command)

2. Four or five (refer to *Table 6* and *Table 7*) bus cycles are then required to input the start address

3. One bus cycle is required to issue the Cache Read Confirm command to start the P/E/R controller.

The start address must be at the beginning of a page (column address = 00h, see *Table 8* and *Table 9*). This allows the data to be output uninterrupted after the latency time (t_{BLBH1}), see *Figure 8*.

The Ready/Busy signal can be used to monitor the start of the operation. During the latency period the Ready/Busy signal goes Low, after this the Ready/Busy signal goes High, even if the device is internally downloading page n+1.

Once the cache read operation has started, the status register can be read using the Read Status Register command.

During the operation, SR5 can be read, to find out whether the internal reading is ongoing (SR5 = '0'), or has completed (SR5 = '1'), while SR6 indicates whether the cache register is ready to download new data.

To exit the cache read operation an Exit Cache Read command must be issued (see *Table 10*).

If the Exit Cache Read command is issued while the device is internally reading page n+1, pages n and n+1 will not be output.

Figure 8.   Cache read operation
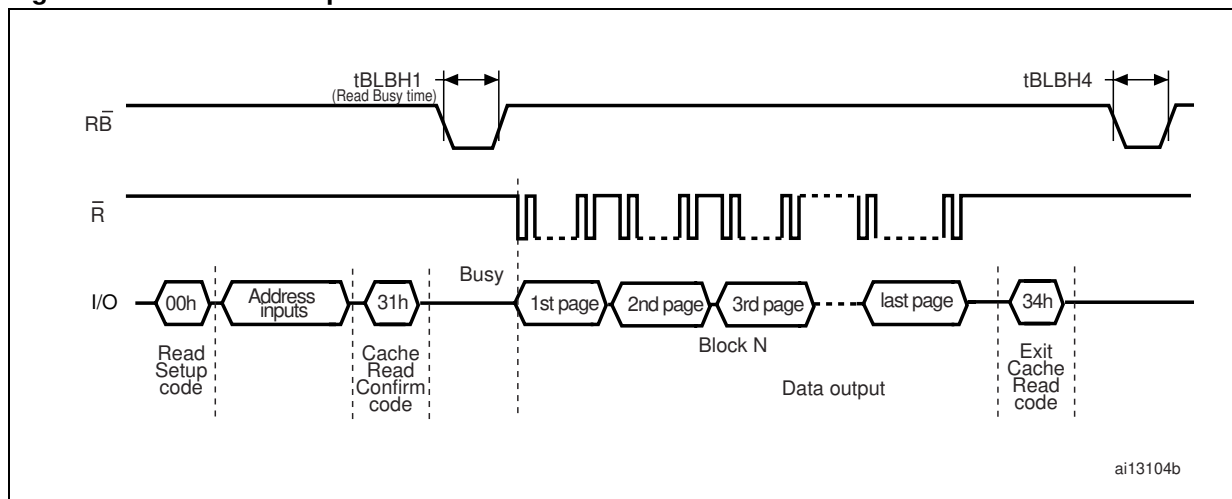
6.3 Page program

The page program operation is the standard operation to program data to the memory array. Generally, the page is programmed sequentially, however the device does support random input within a page. It is recommended to address pages sequentially within a given block.

The memory array is programmed by page, however partial page programming is allowed where any number of bytes (1 to 2112) or words (1 to 1056) can be programmed.

The maximum number of consecutive partial page program operations allowed in the same page is four. After exceeding this a Block Erase command must be issued before any further program operations can take place in that page.

6.3.1 Sequential input

To input data sequentially the addresses must be sequential and remain in one block.

For sequential input each page program operation consists of five steps (see *Figure 9*):

1. one bus cycle is required to setup the Page Program (sequential input) command (see *Table 10*)
2. four or five bus cycles are then required to input the program address (refer to *Table 6* and *Table 7*)
3. the data is then loaded into the data registers
4. one bus cycle is required to issue the Page Program Confirm command to start the P/E/R controller. The P/E/R will only start if the data has been loaded in step 3
5. the P/E/R controller then programs the data into the array.

6.3.2 Random data input in a page

During a sequential input operation, the next sequential address to be programmed can be replaced by a random address, by issuing a Random Data Input command. The following two steps are required to issue the command:

1. one bus cycle is required to setup the Random Data Input command (see *Table 10*)
2. two bus cycles are then required to input the new column address (refer to *Table 6*).

Random Data Input can be repeated as often as required in any given page.

Once the program operation has started the status register can be read using the Read Status Register command. During program operations the status register will only flag errors for bits set to '1' that have not been successfully programmed to '0'.

During the program operation, only the Read Status Register and Reset commands will be accepted, all other commands will be ignored.

Once the program operation has completed the P/E/R controller bit SR6 is set to '1' and the Ready/Busy signal goes High.

The device remains in read status register mode until another valid command is written to the command interface.

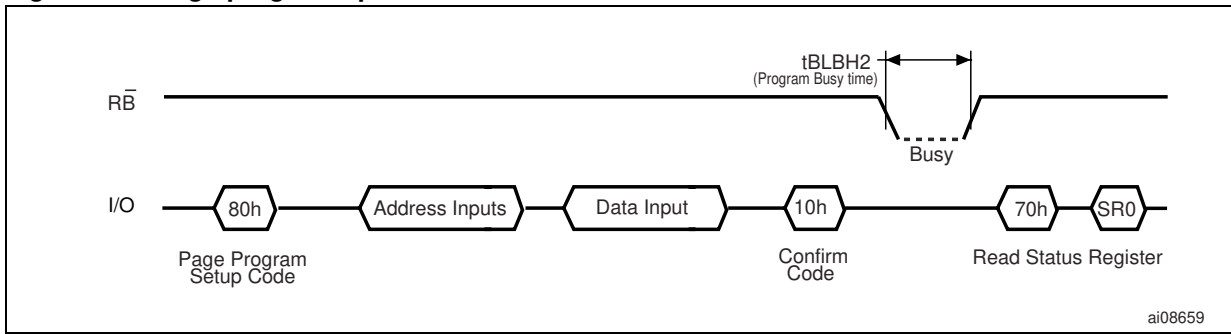**Figure 9.   Page program operation**

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Figure 10.   Random data input during sequential data input

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