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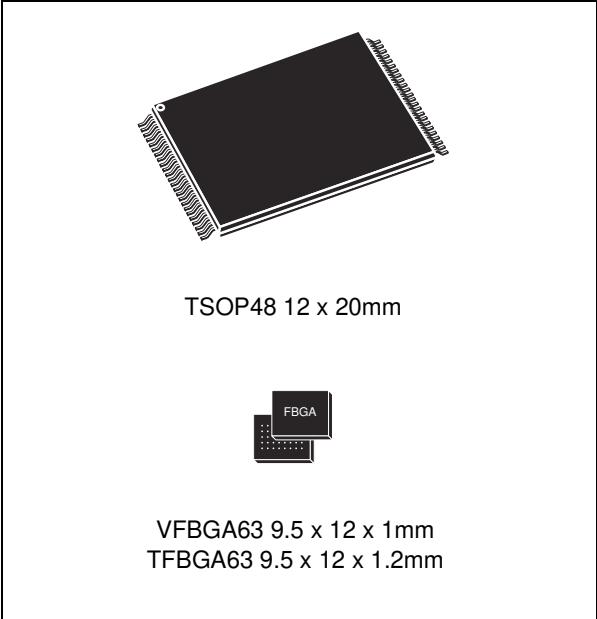
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NAND01G-B
NAND02G-B

1 Gbit, 2 Gbit, 2112 Byte/1056 Word Page, 1.8V/3V, NAND Flash Memory

Feature summary

- High Density NAND Flash memories
  - Up to 2 Gbit memory array
  - Up to 64Mbit spare area
  - Cost effective solutions for mass storage applications
- NAND interface
  - x8 or x16 bus width
  - Multiplexed Address/ Data
  - Pinout compatibility for all densities
- Supply voltage
  - 1.8V device: V_{DD} = 1.7 to 1.95V
  - 3.0V device: V_{DD} = 2.7 to 3.6V
- Page size
  - x8 device: (2048 + 64 spare) Bytes
  - x16 device: (1024 + 32 spare) Words
- Block size
  - x8 device: (128K + 4K spare) Bytes
  - x16 device: (64K + 2K spare) Words
- Page Read/Program
  - Random access: 25µs (max)
  - Sequential access: 50ns (min)
  - Page program time: 300µs (typ)
- Copy Back Program mode
  - Fast page copy without external buffering
- Cache Program and Cache Read modes
  - Internal Cache Register to improve the program and read throughputs
- Fast Block Erase
  - Block erase time: 2ms (typ)
- Status Register
- Electronic Signature
- Chip Enable 'don't care'
  - for simple interface with microcontroller

TSOP48 12 x 20mm

VFBGA63 9.5 x 12 x 1mm
TFBGA63 9.5 x 12 x 1.2mm

- Serial Number option
- Data protection
  - Hardware and Software Block Locking
  - Hardware Program/Erase locked during Power transitions
- Data integrity
  - 100,000 Program/Erase cycles
  - 10 years Data Retention
- ECOPACK® packages
- Development tools
  - Error Correction Code software and hardware models
  - Bad Blocks Management and Wear Leveling algorithms
  - File System OS Native reference software
  - Hardware simulation models

Table 1.   Product List[1]

Reference	Part Number
NAND01G-B	NAND01GR3B
	NAND01GW3B
	NAND01GR4B
	NAND01GW4B
NAND02G-B	NAND02GR3B
	NAND02GW3B
	NAND02GR4B
	NAND02GW4B

1. x16 organization only available for MCP Products.

Contents

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1 Summary description

The NAND Flash 2112 Byte/ 1056 Word Page is a family of non-volatile Flash memories that uses NAND cell technology. The devices range from 1 Gbit to 2 Gbits and operate with either a 1.8V or 3V voltage supply. The size of a Page is either 2112 Bytes (2048 + 64 spare) or 1056 Words (1024 + 32 spare) depending on whether the device has a x8 or x16 bus width.

The address lines are multiplexed with the Data Input/Output signals on a multiplexed x8 or x16 Input/Output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased over 100,000 cycles. To extend the lifetime of NAND Flash devices it is strongly recommended to implement an Error Correction Code (ECC).

The devices have hardware and software security features:

● A Write Protect pin is available to give a hardware protection against program and erase operations.

● A Block Locking scheme is available to provide user code and/or data protection.

The devices feature an open-drain Ready/Busy output that can be used to identify if the Program/Erase/Read (P/E/R) Controller is currently active. The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor.

A Copy Back Program command is available to optimize the management of defective blocks. When a Page Program operation fails, the data can be programmed in another page without having to resend the data to be programmed.

Each device has Cache Program and Cache Read features which improve the program and read throughputs for large files. During Cache Programming, the device loads the data in a Cache Register while the previous data is transferred to the Page Buffer and programmed into the memory array. During Cache Reading, the device loads the data in a Cache Register while the previous data is transferred to the I/O Buffers to be read.

All devices have the Chip Enable Don't Care feature, which allows code to be directly downloaded by a microcontroller, as Chip Enable transitions during the latency time do not stop the read operation.

All devices have the option of a Unique Identifier (serial number), which allows each device to be uniquely identified.

The Unique Identifier options is subject to an NDA (Non Disclosure Agreement) and so not described in the datasheet. For more details of this option contact your nearest ST Sales office.

The devices are available in the following packages:

● TSOP48 (12 x 20mm) for all products

● VFBGA63 (9.5 x 12 x 1mm, 0.8mm pitch) for 1Gb products

● TFBGA63 (9.5 x 12 x 1.2mm, 0.8mm pitch) for 2Gb Dual Die products

In order to meet environmental requirements, ST offers the NAND01G-B and NAND02G-B in ECOPACK® packages. ECOPACK packages are Lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with

JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

For information on how to order these options refer to *Table 29: Ordering Information Scheme*. Devices are shipped from the factory with Block 0 always valid and the memory content bits, in valid blocks, erased to '1'.

See *Table 2: Product Description*, for all the devices available in the family.

Table 2.   Product Description[1]

Reference	Part Number	Density	Bus Width	Page Size	Block Size	Memory Array	Operating Voltage	Timings			Block Erase (typ)	Packages
								Random access time (max)	Sequential access time (min)	Page Program time (typ)		
NAND01G-B	NAND01GR3B	1Gbit	x8	2048+64 Bytes	128K+4K Bytes	64 Pages x 1024 Blocks	1.7 to 1.95V	25µs	60ns	300µs	2ms	TSOP48 VFBGA63
	NAND01GW3B						2.7 to 3.6V	25µs	50ns	300µs		
	NAND01GR4B		x16[2]	1024+32 Words	64K+2K Words		1.7 to 1.95V	25µs	60ns	300µs		
	NAND01GW4B						2.7 to 3.6V	25µs	50ns	300µs		
NAND02G-B	NAND02GR3B	2Gbit	x8	2048+64 Bytes	128K+4K Bytes	64 Pages x 2048 Blocks	1.7 to 1.95V	25µs	60ns	300µs	2ms	TSOP48 TFBGA63 [2]
	NAND02GW3B						2.7 to 3.6V	25µs	50ns	300µs		
	NAND02GR4B		x16[2]	1024+32 Words	64K+2K Words		1.7 to 1.95V	25µs	60ns	300µs		
	NAND02GW4B						2.7 to 3.6V	25µs	50ns	300µs		

1. x16 organization only available for MCP

2. Dual Die devices only

Figure 1.   Logic Block Diagram
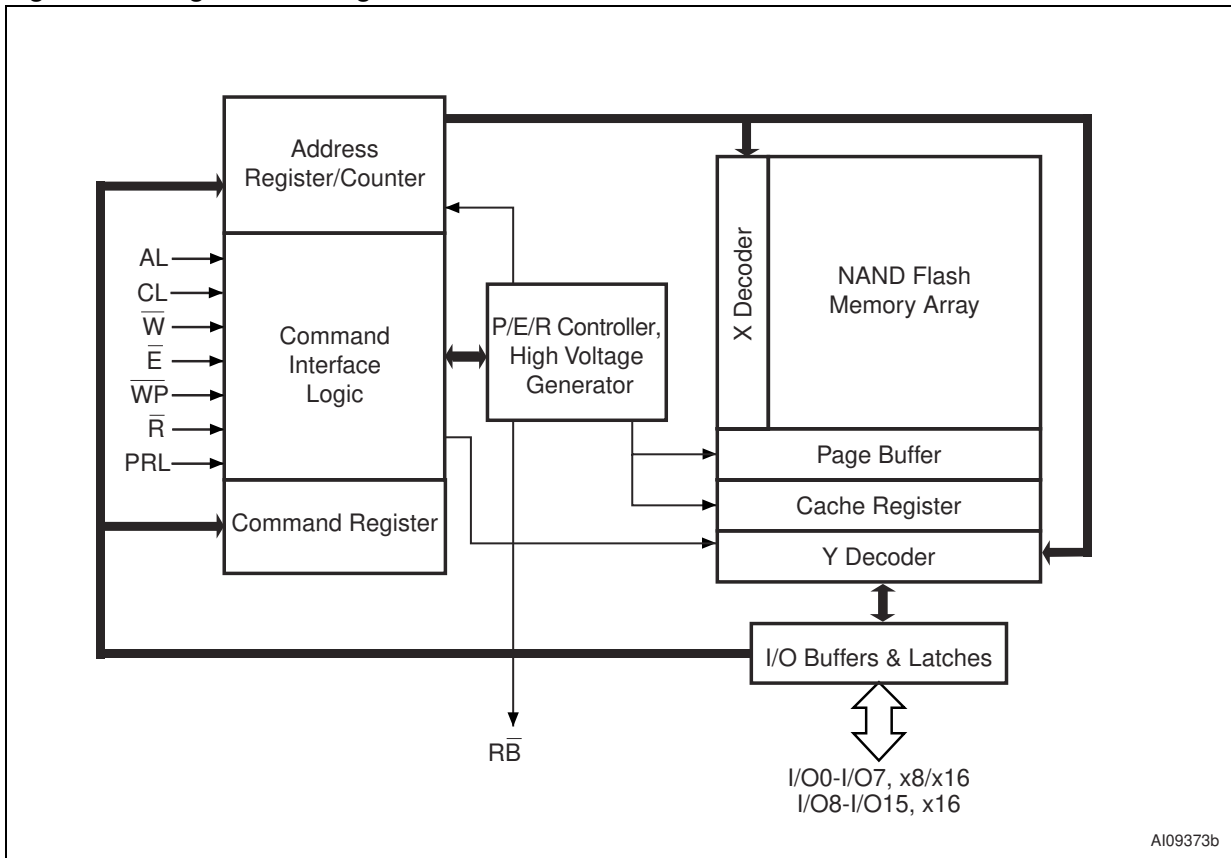
Figure 2.   Logic Diagram
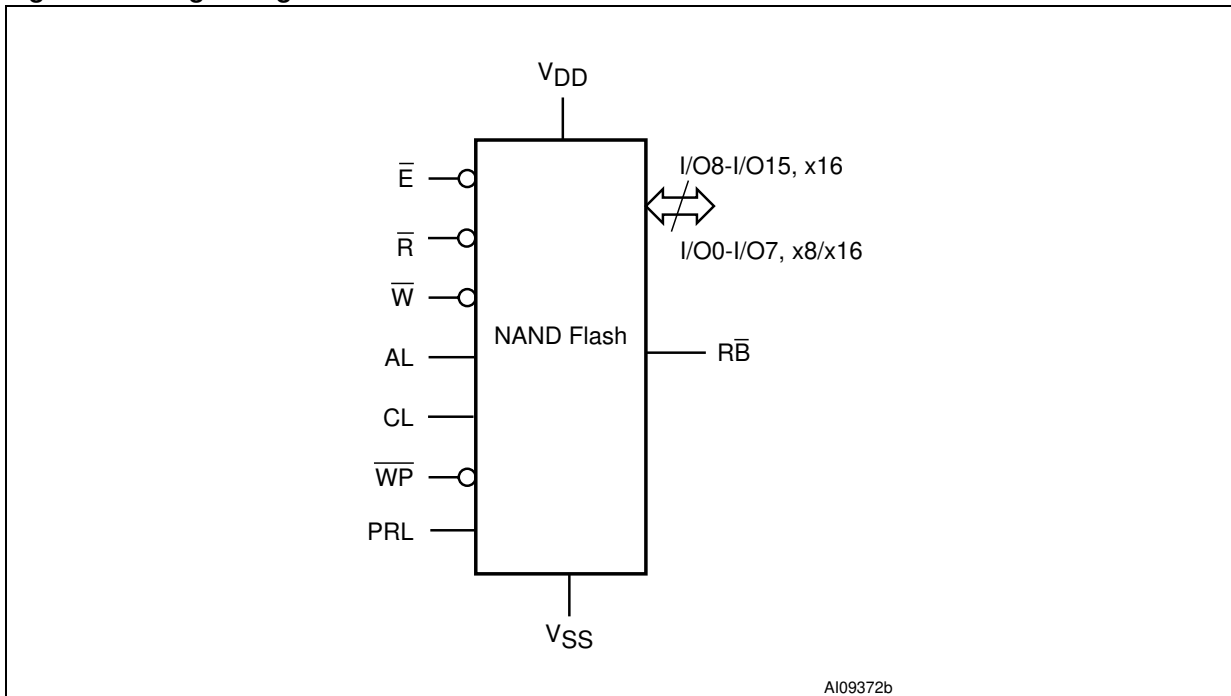
1.   x16 organization only available for MCP

Table 3.   Signal Names

I/O8-15	Data Input/Outputs for x16 devices
I/O0-7	Data Input/Outputs, Address Inputs, or Command Inputs for x8 and x16 devices
AL	Address Latch Enable
CL	Command Latch Enable
$\overline{E}$	Chip Enable
$\overline{R}$	Read Enable
$R\overline{B}$	Ready/Busy (open-drain output)
$\overline{W}$	Write Enable
$\overline{WP}$	Write Protect
PRL	Power-Up Read Enable, Lock/Unlock Enable
V_{DD}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally
DU	Do Not Use

Figure 3.   TSOP48 Connections, x8 devices

AI11750
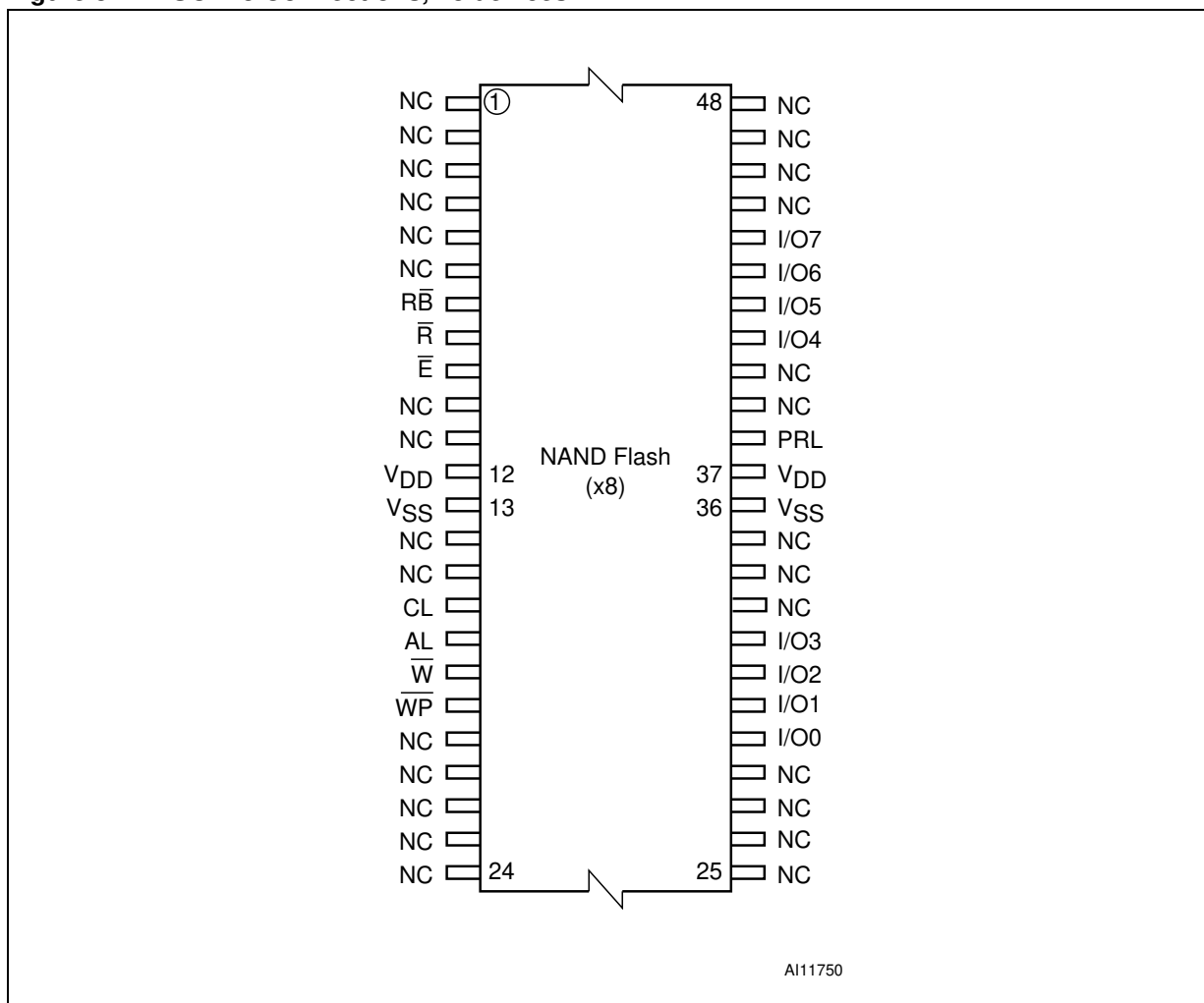
Figure 4.   FBGA63 Connections, x8 devices (Top view through package)
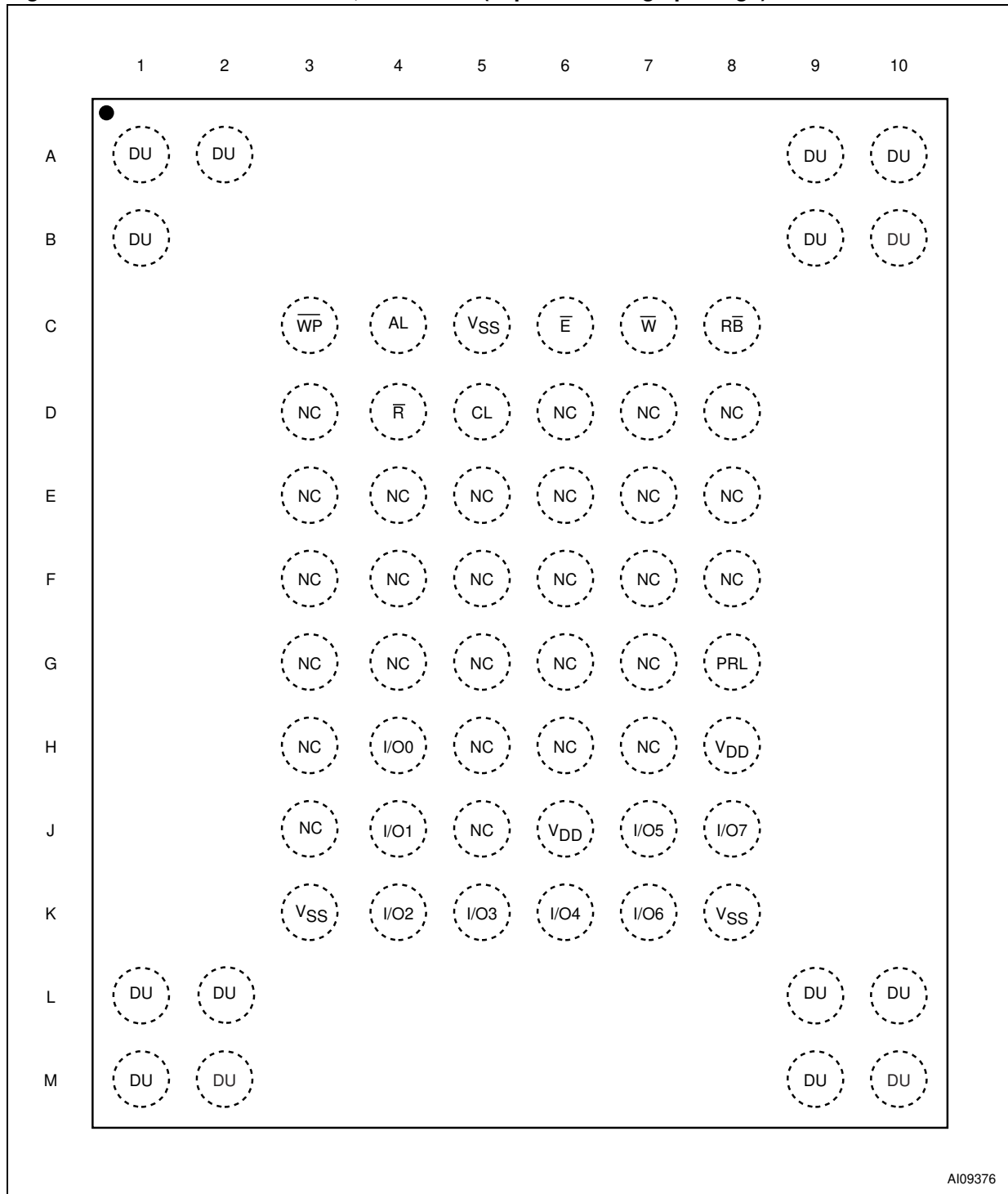
AI09376

Figure 5.   FBGA63 Connections, x16 devices (Top view through package)

AI09377
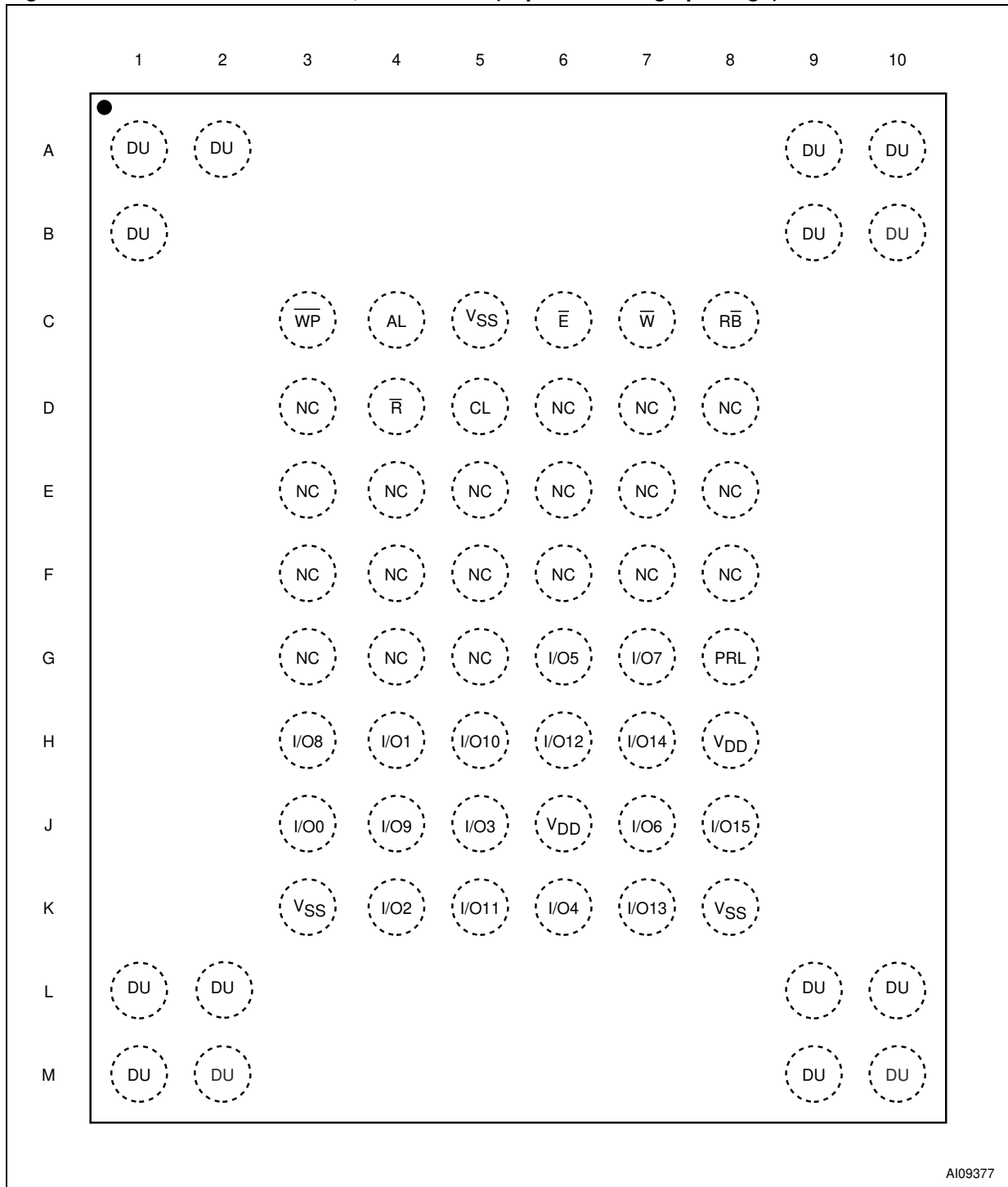
2   Memory array organization

The memory array is made up of NAND structures where 32 cells are connected in series.

The memory array is organized in blocks where each block contains 64 pages. The array is split into two areas, the main area and the spare area. The main area of the array is used to store data whereas the spare area is typically used to store Error correction Codes, software flags or Bad Block identification.

In x8 devices the pages are split into a 2048 Byte main area and a spare area of 64 Bytes. In the x16 devices the pages are split into a 1,024 Word main area and a 32 Word spare area. Refer to *Figure 6: Memory Array Organization*.

2.1   Bad blocks

The NAND Flash 2112 Byte/ 1056 Word Page devices may contain Bad Blocks, that is blocks that contain one or more invalid bits whose reliability is not guaranteed. Additional Bad Blocks may develop during the lifetime of the device.

The Bad Block Information is written prior to shipping (refer to *Section 8.1: Bad Block Management* for more details).

Table 4: Valid Blocks shows the minimum number of valid blocks in each device. The values shown include both the Bad Blocks that are present when the device is shipped and the Bad Blocks that could develop later on.

These blocks need to be managed using Bad Blocks Management, Block Replacement or Error Correction Codes (refer to *Section 8: Software algorithms*).

Table 4.   Valid Blocks

Density of Device	Min	Max
2 Gbits	2008	2048
1 Gbit	1004	1024

Figure 6.   Memory Array Organization
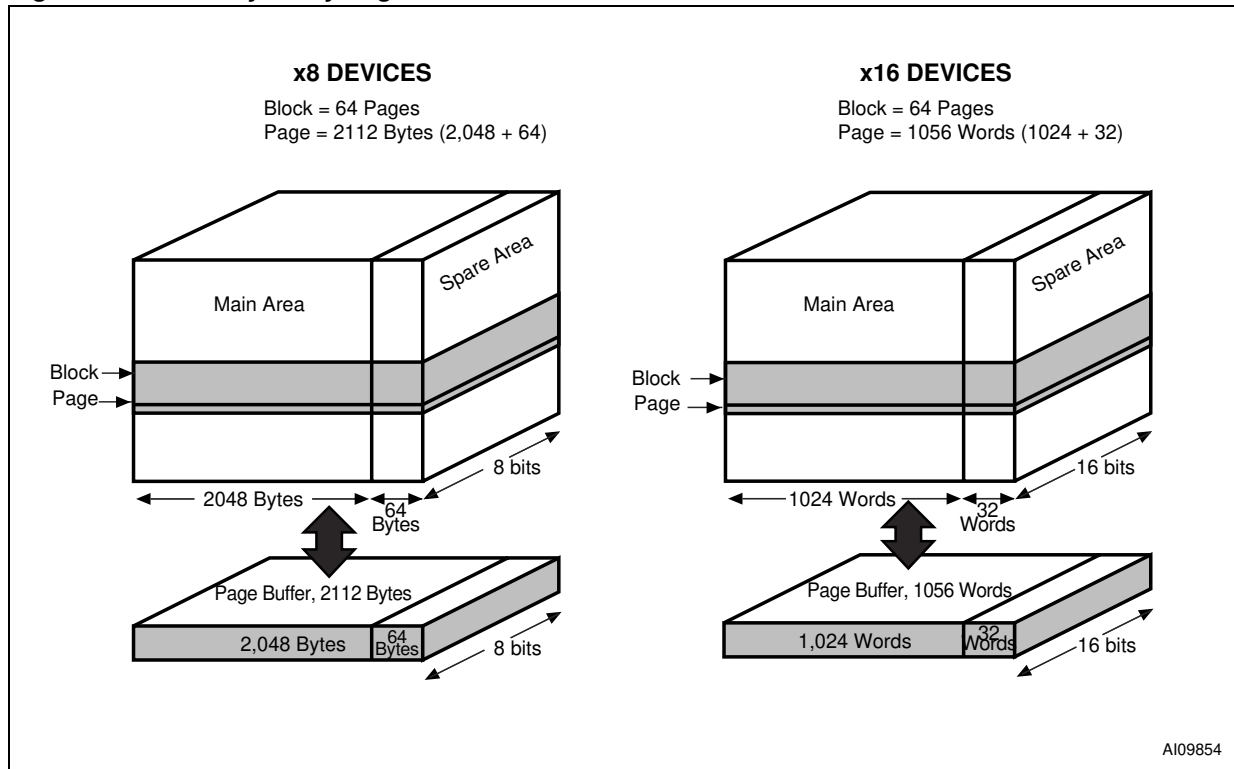
3 Signal descriptions

See *Figure 2: Logic Diagram*, and *Table 3: Signal Names*, for a brief overview of the signals connected to this device.

3.1 Inputs/Outputs (I/O0-I/O7)

Input/Outputs 0 to 7 are used to input the selected address, output the data during a Read operation or input a command or data during a Write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

3.2 Inputs/Outputs (I/O8-I/O15)

Input/Outputs 8 to 15 are only available in x16 devices. They are used to output the data during a Read operation or input data during a Write operation. Command and Address Inputs only require I/O0 to I/O7.

The inputs are latched on the rising edge of Write Enable. I/O8-I/O15 are left floating when the device is deselected or the outputs are disabled.

3.3 Address Latch Enable (AL)

The Address Latch Enable activates the latching of the Address inputs in the Command Interface. When AL is high, the inputs are latched on the rising edge of Write Enable.

3.4 Command Latch Enable (CL)

The Command Latch Enable activates the latching of the Command inputs in the Command Interface. When CL is high, the inputs are latched on the rising edge of Write Enable.

3.5 Chip Enable ($\overline{E}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is low, V_{IL}, the device is selected. If Chip Enable goes high, v_{IH}, while the device is busy, the device remains selected and does not go into standby mode.

3.6 Read Enable ($\overline{R}$)

The Read Enable pin, $\overline{R}$, controls the sequential data output during Read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

3.7 Power-Up Read Enable, Lock/Unlock Enable (PRL)

The Power-Up Read Enable, Lock/Unlock Enable input, PRL, is used to enable and disable the lock mechanism. When PRL is High, V_{IH}, the device is in Block Lock mode.

If the Power-Up Read Enable, Lock/Unlock Enable input is not required, the PRL pin should be left unconnected (Not Connected) or connected to V_{SS}.

3.8 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 10µs (min) is required before the Command Interface is ready to accept a command. It is recommended to keep Write Enable high during the recovery time.

3.9 Write Protect ($\overline{WP}$)

The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

3.10 Ready/Busy ($R\overline{B}$)

The Ready/Busy output, $R\overline{B}$, is an open-drain output that can be used to identify if the P/E/R Controller is currently active. When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

Refer to the *Section 11.1: Ready/Busy Signal electrical characteristics* for details on how to calculate the value of the pull-up resistor.

3.11 V_{DD} Supply Voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

An internal voltage detector disables all functions whenever V_{DD} is below V_{LKO} (see *Table 22* and *Table 23*) or 1.5V (for 1.8V devices) to protect the device from any involuntary program/erase during power-transitions.

Each device in a system should have V_{DD} decoupled with a 0.1µF capacitor. The PCB track widths should be sufficient to carry the required program and erase currents.

3.12 V~SS~ Ground

3.12 V_{SS} Ground

Ground, $V_{SS,}$ is the reference for the power supply. It must be connected to the system ground.

4 Bus operations

There are six standard bus operations that control the memory. Each of these is described in this section, see *Table 5: Bus Operations*, for a summary.

Typically, glitches of less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

4.1 Command Input

Command Input bus operations are used to give commands to the memory. Commands are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O0 to I/O7 are used to input commands.

See *Figure 23* and *Table 24* for details of the timings requirements.

4.2 Address Input

Address Input bus operations are used to input the memory addresses. Four bus cycles are required to input the addresses for 1Gb devices whereas five bus cycles are required for the 2Gb device (refer to *Table 6* and *Table 7*, Address Insertion).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal. Only I/O0 to I/O7 are used to input addresses.

See *Figure 24* and *Table 24* for details of the timings requirements.

4.3 Data Input

Data Input bus operations are used to input the data to be programmed.

Data is accepted only when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low and Read Enable is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

See *Figure 25* and *Table 24* and *Table 25* for details of the timings requirements.

4.4 Data Output

Data Output bus operations are used to read: the data in the memory array, the Status Register, the lock status, the Electronic Signature and the Unique Identifier.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low. The data is output sequentially using the Read Enable signal.

See *Figure 26* and *Table 25* for details of the timings requirements.

4.5 Write Protect

Write Protect bus operations are used to protect the memory against program or erase operations. When the Write Protect signal is Low the device will not accept program or erase operations and so the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection even during power-up.

4.6 Standby

When Chip Enable is High the memory enters Standby mode, the device is deselected, outputs are disabled and power consumption is reduced.

Table 5. Bus Operations

Bus Operation	$\overline{E}$	AL	CL	$\overline{R}$	$\overline{W}$	$\overline{WP}$	I/O0 - I/O7	I/O8 - I/O15[1]
Command Input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X[2]	Command	X
Address Input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address	X
Data Input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	V_{IH}	Data Input	Data Input
Data Output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data Output	Data Output
Write Protect	X	X	X	X	X	V_{IL}	X	X
Standby	V_{IH}	X	X	X	X	V_{IL}/V_{DD}	X	X

1. Only for x16 devices.

2. $\overline{WP}$ must be V_{IH} when issuing a program or erase command.

Table 6. Address Insertion, x8 Devices

Bus Cycle[1]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A11	A10	A9	A8
3rd	A19	A18	A17	A16	A15	A14	A13	A12
4th	A27	A26	A25	A24	A23	A22	A21	A20
5th[2]	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A28

1. Any additional address input cycles will be ignored.

2. The fifth cycle is valid for 2Gb devices. A28 is for 2Gb devices only.

Table 7.   Address Insertion, x16 Devices

Bus Cycle[1]	I/O8-I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	X	A7	A6	A5	A4	A3	A2	A1	A0
2nd	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A10	A9	A8
3rd	X	A18	A17	A16	A15	A14	A13	A12	A11
4th	X	A26	A25	A24	A23	A22	A21	A20	A19
5th[2]	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A27

1. Any additional address input cycles will be ignored.

2. The fifth cycle is valid for 2Gb devices. A27 is for 2Gb devices only.

Table 8.   Address Definitions, x8

Address	Definition	
A0 - A11	Column Address	
A12 - A17	Page Address	
A18 - A27	Block Address	1Gb device
A18 - A28	Block Address	2Gb device

Table 9.   Address Definitions, x16

Address	Definition	
A0 - A10	Column Address	
A11 - A16	Page Address	
A17 - A26	Block Address	1Gb device
A17 - A27	Block Address	2Gb device

5   Command Set

All bus write operations to the device are interpreted by the Command Interface. The Commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is high. Device operations are selected by writing specific commands to the Command Register. The two-step command sequences for program and erase operations are imposed to maximize data security.

The Commands are summarized in *Table 10: Commands*.

Table 10.   Commands

Command	Bus Write Operations[1][2]				Commands accepted during busy
	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	
Read	00h[2]	30h	–	–	
Random Data Output	05h	E0h	–	–	
Cache Read	00h	31h	–	–	
Exit Cache Read	34h	–	–	–	Yes[3]
Page Program (Sequential Input default)	80h	10h	–	–	
Random Data Input	85h	–	–	–	
Copy Back Program	00h	35h	85h	10h	
Cache Program	80h	15h	–	–	
Block Erase	60h	D0h	–	–	
Reset	FFh	–	–	–	Yes
Read Electronic Signature	90h	–	–	–	
Read Status Register	70h	–	–	–	Yes
Read Block Lock Status	7Ah	–	–	–	
Blocks Unlock	23h	24h	–	–	
Blocks Lock	2Ah	–	–	–	
Blocks Lock-Down	2Ch	–	–	–	

1. The bus cycles are only shown for issuing the codes. The cycles required to input the addresses or input/output data are not shown.

2. For consecutive Read operations the 00h command does not need to be repeated.

3. Only during Cache Read busy.

6   Device operations

The following section gives the details of the device operations.

6.1   Read Memory Array

At Power-Up the device defaults to Read mode. To enter Read mode from another mode the Read command must be issued, see *Table 10: Commands*. Once a Read command is issued, subsequent consecutive Read commands only require the confirm command code (30h).

Once a Read command is issued two types of operations are available: Random Read and Page Read.

6.1.1   Random Read

Each time the Read command is issued the first read is Random Read.

6.1.2   Page Read

After the first Random Read access, the page data (2112 Bytes or 1056 Words) is transferred to the Page Buffer in a time of t_{WHBH} (refer to *Table 25* for value). Once the transfer is complete the Ready/Busy signal goes High. The data can then be read out sequentially (from selected column address to last column address) by pulsing the Read Enable signal.

The device can output random data in a page, instead of the consecutive sequential data, by issuing a **Random Data Output command**.

The Random Data Output command can be used to skip some data during a sequential data output.

The sequential operation can be resumed by changing the column address of the next data to be output, to the address which follows the Random Data Output command.

The Random Data Output command can be issued as many times as required within a page.

The Random Data Output command is not accepted during Cache Read operations.

Figure 7.   Read Operations
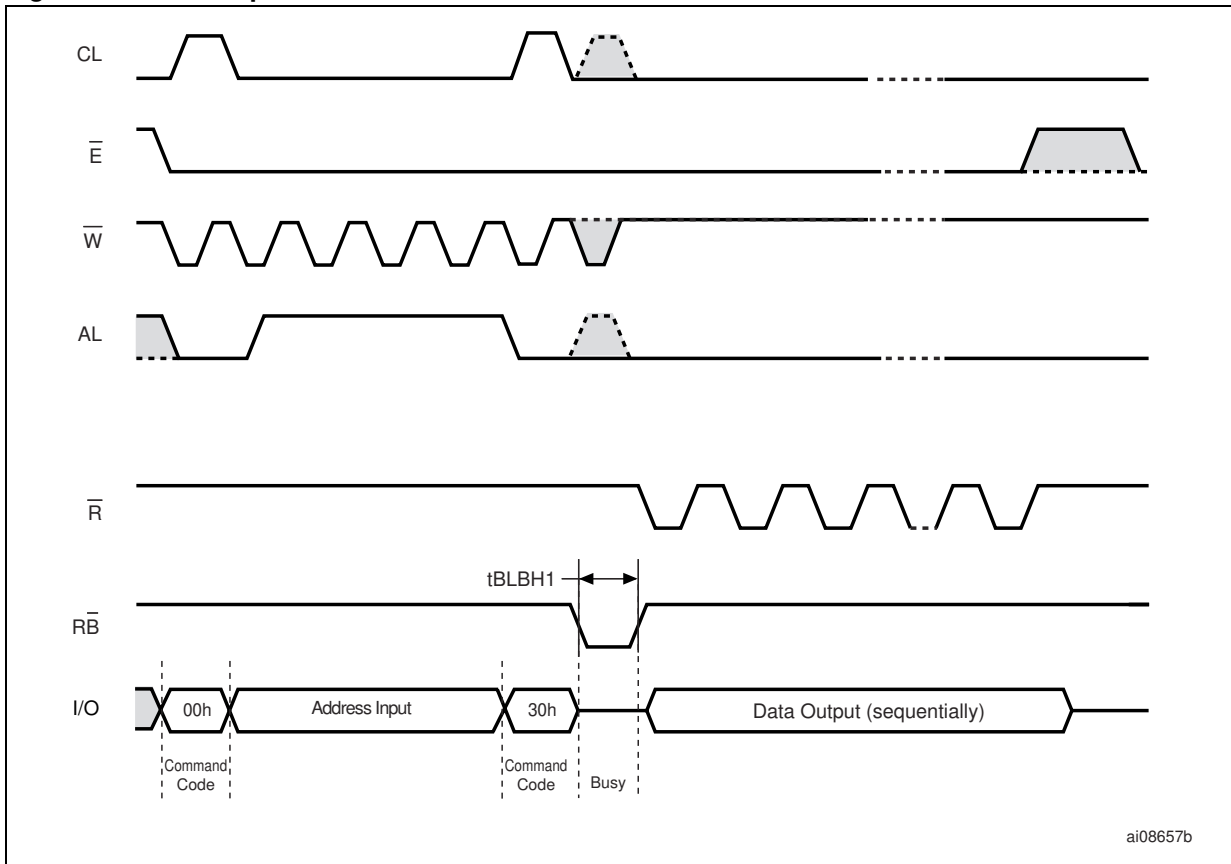
1.   Highest address depends on device density.

Figure 8.   **Random Data Output During Sequential Data Output**