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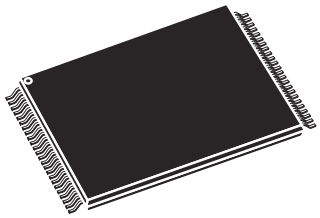
NAND04G-B2D
NAND08G-BxC

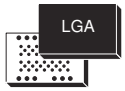
4-Gbit, 8-Gbit, 2112-byte/1056-word page multiplane architecture, 1.8 V or 3 V, SLC NAND flash memories

Features

- High density NAND flash memory
  - Up to 8 Gbits of memory array
  - Cost-effective solution for mass storage applications
- NAND interface
  - x8 or x16 bus width
  - Multiplexed address/data
- Supply voltage: 1.8 V or 3 V device
- Page size
  - x8 device: (2048 + 64 spare) bytes
  - x16 device: (1024 + 32 spare) words
- Block size
  - x8 device: (128K + 4 K spare) bytes
  - x16 device: (64K + 2K spare) words
- Multiplane architecture
  - Array split into two independent planes
  - Program/erase operations can be performed on both planes at the same time
- Page read/program
  - Random access: 25 µs (max)
  - Sequential access: 25 ns (min)
  - Page program time: 200 µs (typ)
  - Multiplane page program time (2 pages): 200 µs (typ)
- Copy back program with automatic error detection code (EDC)
- Cache read mode
- Fast block erase
  - Block erase time: 1.5 ms (typ)
  - Multiblock erase time (2 blocks): 1.5 ms (typ)
- Status register
- Electronic signature
- Chip enable ‘don’t care’
- ONFI 1.0 compliant command set



TSOP48 12 x 20 mm (N)



ULGA52 12 x 17 x 0.65 mm (ZL)

- Security features
  - OTP area
  - Serial number (unique ID)
  - Non-volatile protection option
- Data protection: hardware program/erase disabled during power transitions
- Data integrity
  - 100,000 program/erase cycles (with ECC)
  - 10 years data retention
- RoHS compliant packages

Table 1. Device summary

Reference	Part number
NAND04G-B2D	NAND04GR3B2D
	NAND04GW3B2D
	NAND04GR4B2D(1)
	NAND04GW4B2D(1)
NAND08G-BxC	NAND08GR3B2C,
	NAND08GW3B2C
	NAND08GR4B2C(1)
	NAND08GW4B2C(1)
	NAND08GR3B4C
	NAND08GW3B4C

1. x16 organization only available for MCP products.

Contents

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1 Description

The NAND04G-B2D and NAND08G-BxC are part of the NAND flash 2112-byte/1056-word page family of non-volatile flash memories. They use NAND cell technology have a density of 4 Gbits and 8 Gbits, respectively.

The NAND04G-B2D memory array is split into 2 planes of 2048 blocks each. This multiplane architecture makes it possible to program 2 pages at a time (one in each plane), or to erase 2 blocks at a time (one in each plane). This feature reduces the average program and erase times by 50%.

The NAND08G-BxC is a stacked device that combines two NAND04G-B2D dice, both of which feature a multiplane architecture.

In the NAND08G-B2C devices, only one of the memory components can be enabled at a time, therefore, operations can only be performed on one of the memory components at any one time.

The devices operate from a 1.8 V or 3 V voltage supply. Depending on whether the device has a x8 or x16 bus width, the page size is 2112 bytes (2048 + 64 spare) or 1056 words (1024 + 32 spare), respectively.

The address lines are multiplexed with the data input/output signals on a multiplexed x8 input/output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased up to 100,000 cycles with ECC (error correction code) on. To extend the lifetime of NAND flash devices, the implementation of an ECC is mandatory.

A write protect pin is available to provide hardware protection against program and erase operations.

The devices feature an open-drain ready/busy output that identifies if the P/E/R (program/erase/read) controller is currently active. The use of an open-drain output allows the ready/busy pins from several memories to connect to a single pull-up resistor.

A Copy Back Program command is available to optimize the management of defective blocks. When a page program operation fails, the data can be programmed in another page without having to resend the data to be programmed. An embedded error detection code (EDC) is automatically executed after each copy back operation: 1 error bit can be detected for every 528 bytes. With this feature it is no longer necessary to use an external ECC to detect copy back operation errors.

The devices have a cache read feature that improves the read throughput for large files. During cache reading, the device loads the data in a cache register while the previous data is transferred to the I/O buffers to be read.

The devices have the chip enable ‘don’t care’ feature, which allows code to be directly downloaded by a microcontroller. This is possible because chip enable transitions during the latency time do not stop the read operation.

Both the NAND04G-B2D and NAND08G-BxC support the ONFI 1.0 specification.

The devices are available in the following packages:

- TSOP48 (12 x 20 mm)
- ULGA52 (12 x 17 x 0.65 mm)

and come with three security features:

- OTP (one time programmable) area, which is a restricted access area where sensitive data/code can be stored permanently
- Serial number (unique identifier), which allows the device to be uniquely identified
- Non-volatile protection to lock sensible data permanently.

These security features are subject to an NDA (non-disclosure agreement) and are, therefore, not described in the datasheet. For more details about them, contact your nearest Numonyx sales office.

For information on how to order these options, refer to *Table 34: Ordering information scheme*. Devices are shipped from the factory with block 0 always valid and the memory content bits, in valid blocks, erased to '1'.

Table 2: Product description lists the part numbers and other information for all the devices available in the family.

Table 2. Product description

Part number	Density	Bus width	Page size	Block size	Memory array	Operating voltage	Timings				Package
							Sequential access time (min)	Random access time (max)	Page Program (typ)	Block Erase (typ)	
NAND04GR3B2D	4-Gbit	x8	2048+64 bytes	128K+ 4K bytes	64 pages x 4096 blocks	1.7 to 1.95 V	45 ns	25 µs	200 µs	1.5 ms	ULGA52
NAND04GW3B2D						2.7 to 3.6 V	25 ns				TSOP48 ULGA52
NAND04GR4B2D		x16	1024+ 32 words	64K + 2K words		1.7 to 1.95 V	45 ns				(1)
NAND04GW4B2D						2.7 to 3.6 V	25 ns				
NAND08GR3B2C	8-Gbit	x8	2048+64 bytes	128K + 4K bytes	64 pages x 8192 blocks	1.7 to 1.95 V	45 ns	25 µs	200 µs	1.5 ms	ULGA52(2)
NAND08GW3B2C						2.7 to 3.6 V	25 ns				TSOP48 ULGA52(2)
NAND08GR4B2C		x16	1024+ 32 words	64K + 2K words		1.7 to 1.95 V	45 ns				(1)(2)
NAND08GW4B2C						2.7 to 3.6 V	25 ns				
NAND08GR3B4C		x8	2048+64 bytes	128K + 4K bytes		1.7 to 1.95 V	45 ns				ULGA52(2)
NAND08GW3B4C		x8				2.7 to 3.6 V	25 ns				

1. x16 organization is only available for MCP products.
2. The NAND08G-BxC is composed of two 4-Gbit dice.

Figure 1. Logic block diagram

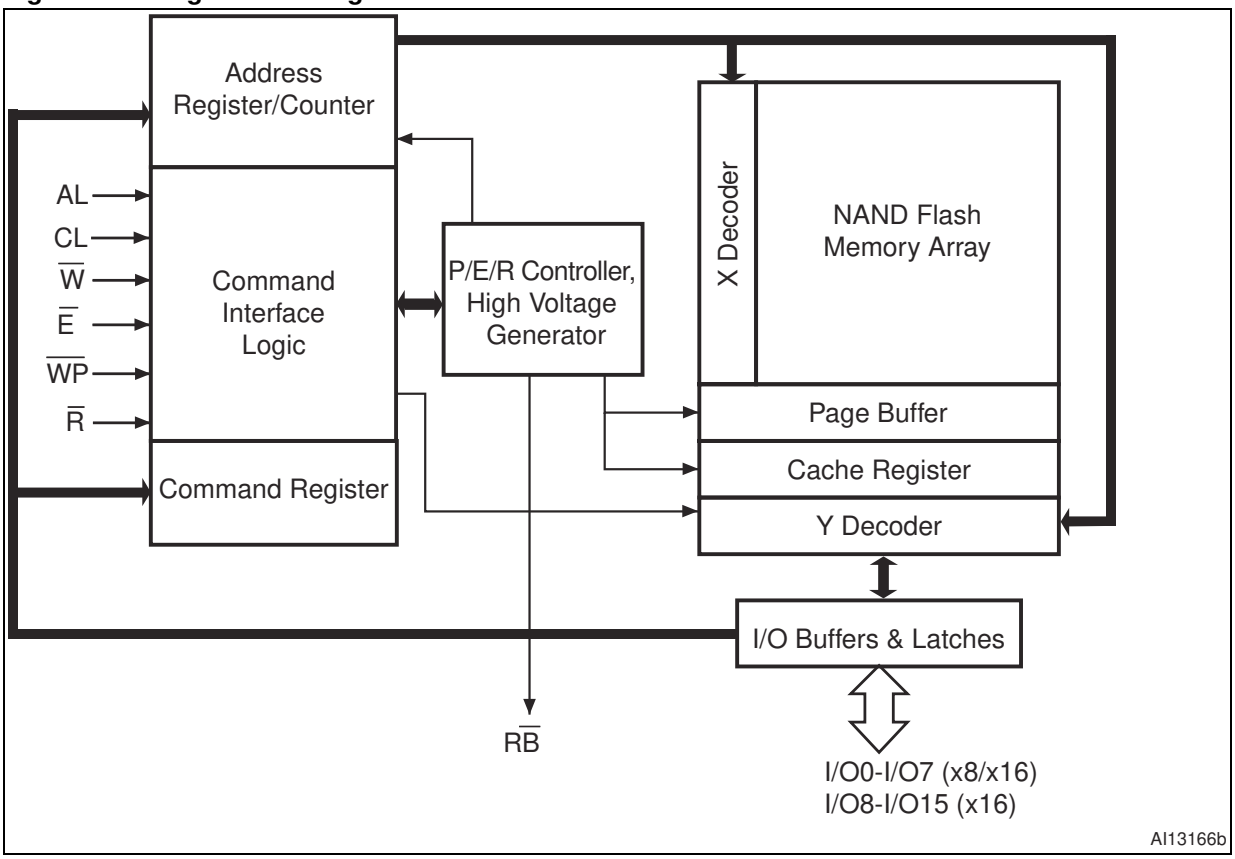


Figure 2. Logic diagram

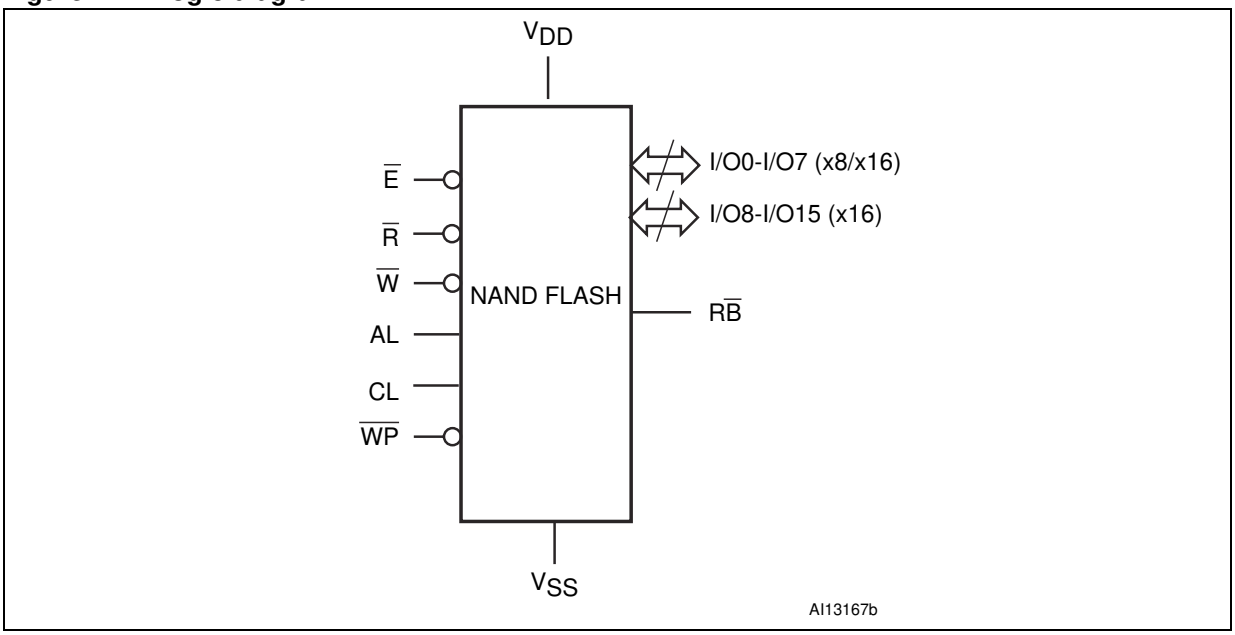


Table 3. Signals names

Signal	Function	Direction
I/O0-7	Data input/outputs, address inputs, or command inputs (x8/x16 devices)	Input/output
I/O8-15	Data input/outputs (x16 devices)	Input/output
AL	Address Latch Enable	Input
CL	Command Latch Enable	Input
$\overline{E}$	Chip Enable	Input
$\overline{R}$	Read Enable	Input
$R\overline{B}$	Ready/Busy (open-drain output)	Output
$\overline{W}$	Write Enable	Input
$\overline{WP}$	Write Protect	Input
V_{DD}	Supply voltage	Power supply
V_{SS}	Ground	Ground
NC	Not connected internally	–
DU	Do not use	–

Figure 3. TSOP48 connections for NAND04G-B2D and NAND08G-BxC

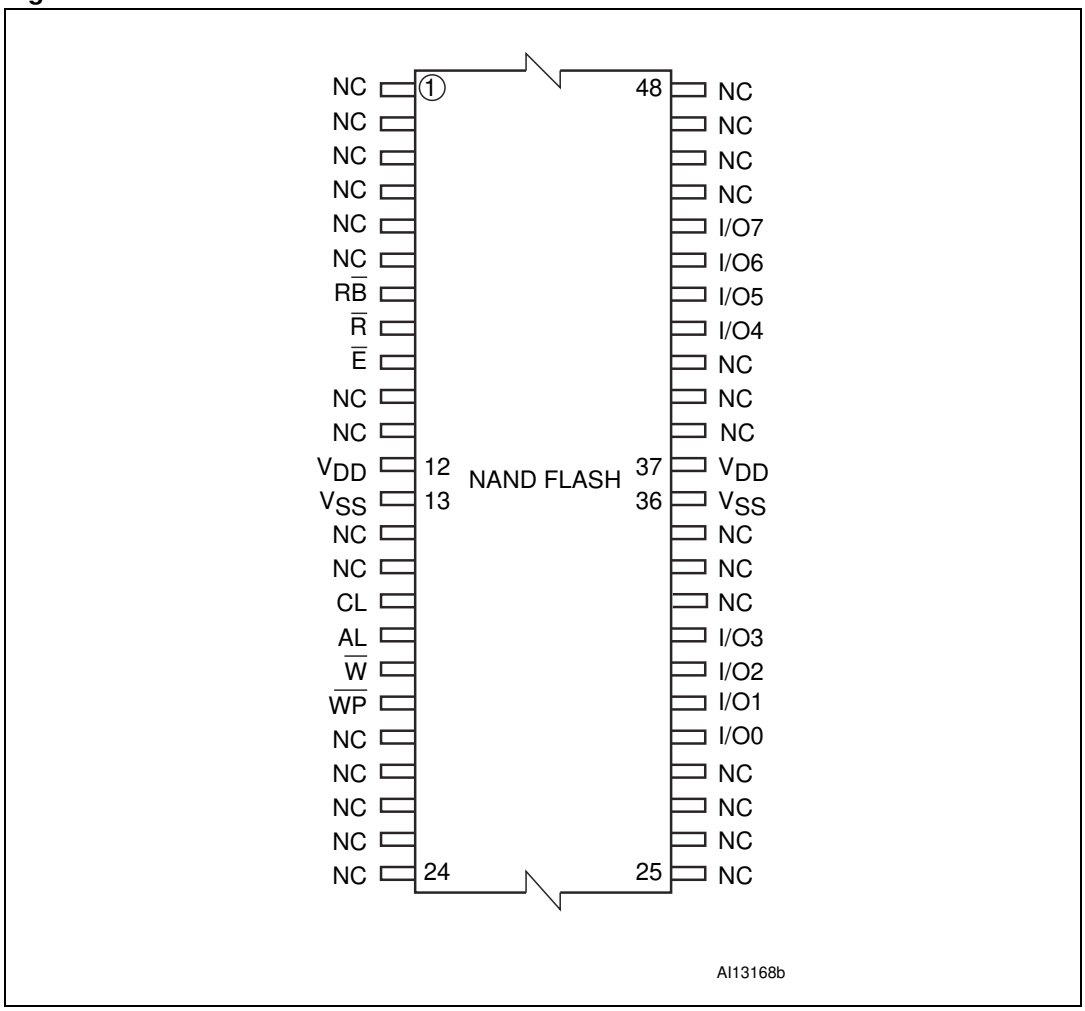


Figure 4. ULGA52 connections for NAND04G-B2D and NAND08G-B2C devices

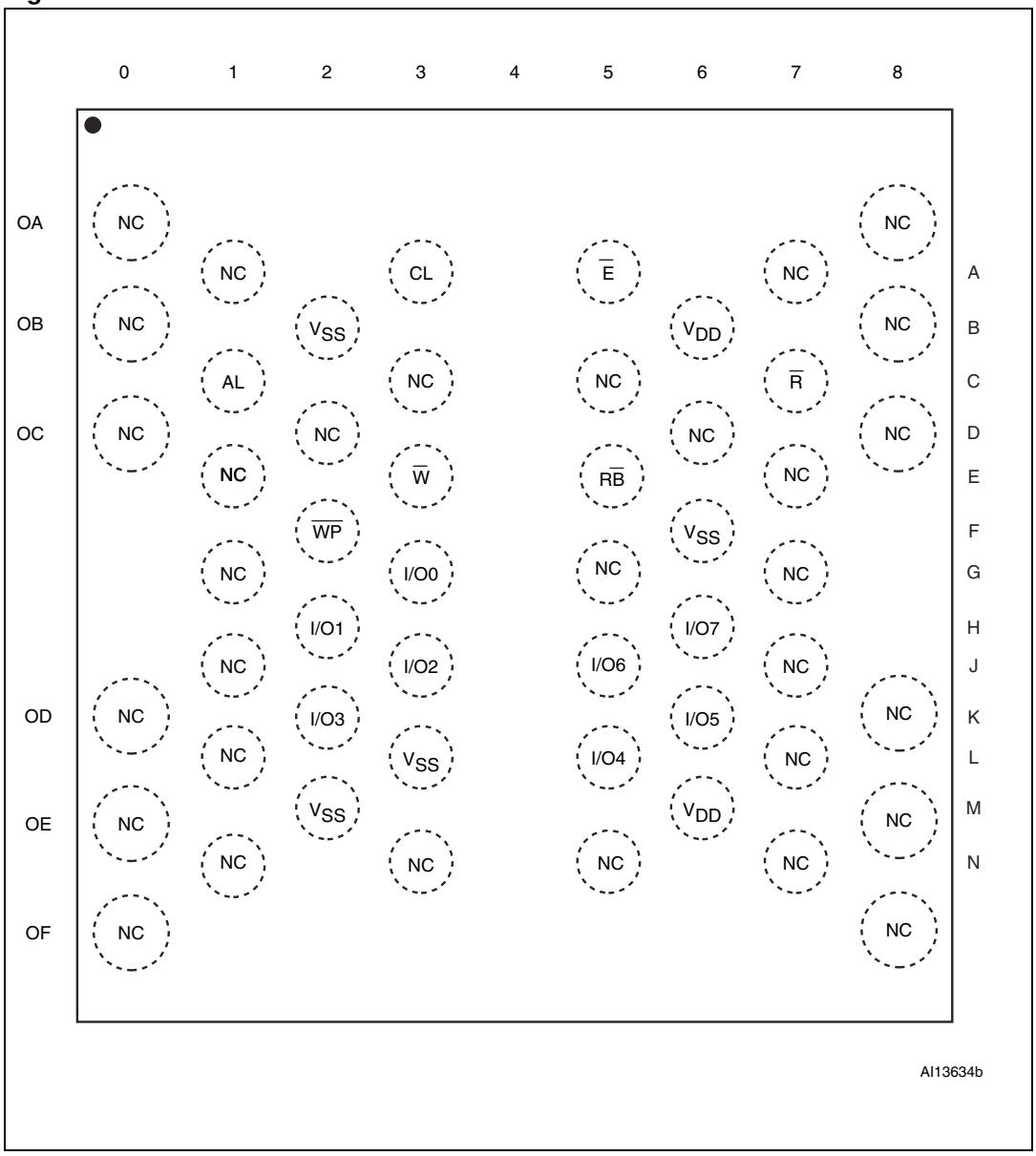
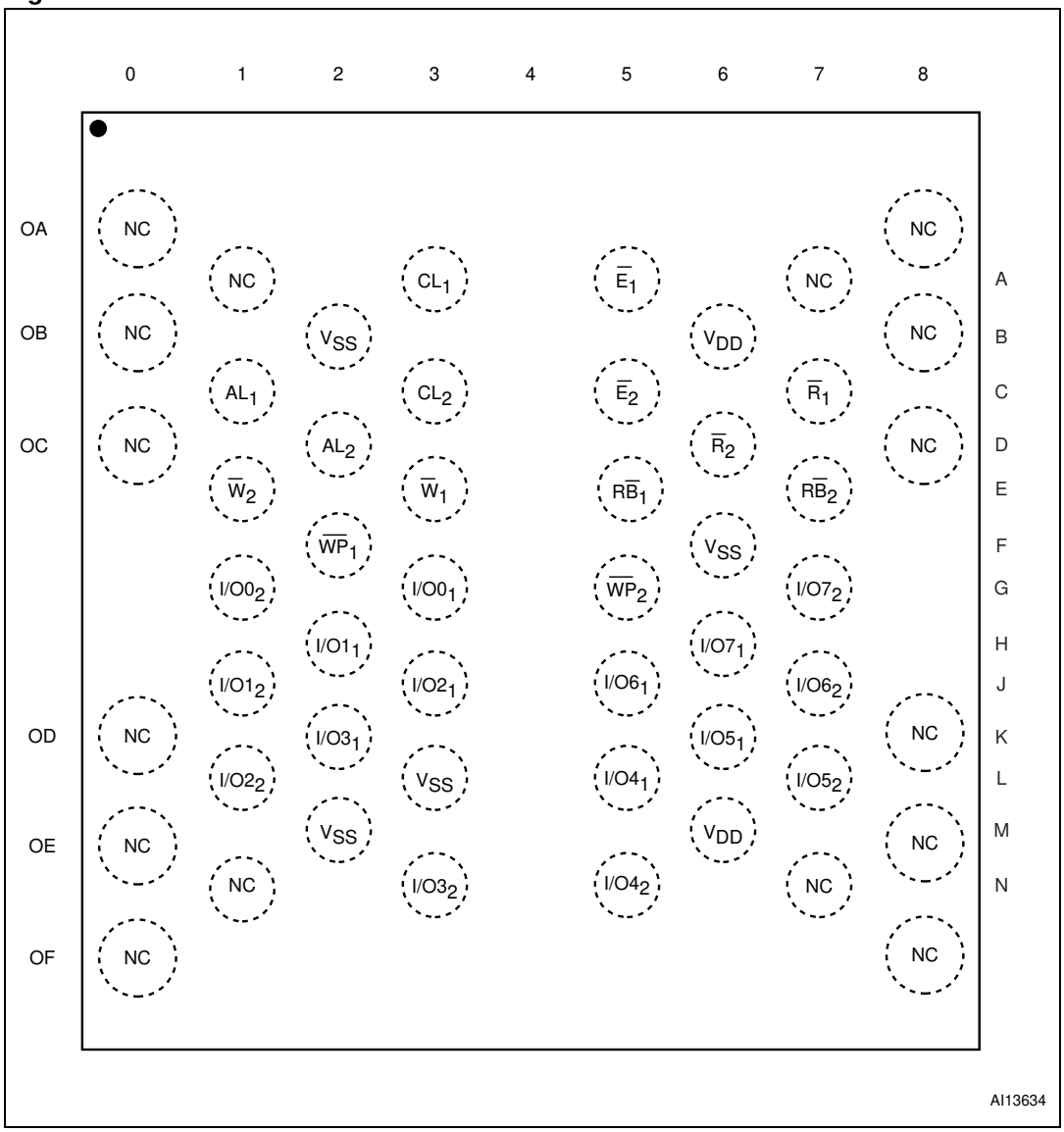


Figure 5. ULGA52 connections for the NAND08G-B4C devices



2 Memory array organization

The memory array of the devices is made up of NAND structures where 32 cells are connected in series. It is organized into blocks where each block contains 64 pages. The array is split into two areas, the main area, and the spare area. The main area of the array is used to store data, and the spare area typically stores error correction codes, software flags, or bad block identification.

In x8 devices, the pages are split into a 2048-byte main area and a spare area of 64 bytes. In x16 devices, the pages are split into a 1024-word main area and a spare area of 32 words. Refer to *Figure 6: Memory array organization*.

Bad blocks

In x8 devices, the NAND flash 2112-byte/1056-word page devices may contain bad blocks, which are blocks that contain one or more invalid bits whose reliability is not guaranteed. Additional bad blocks may develop during the lifetime of the device.

The bad block information is written prior to shipping (refer to *Section 9.1: Bad block management* for more details).

Table 4 shows the minimum number of valid blocks. The values shown include both the bad blocks that are present when the device is shipped and the bad blocks that could develop later on.

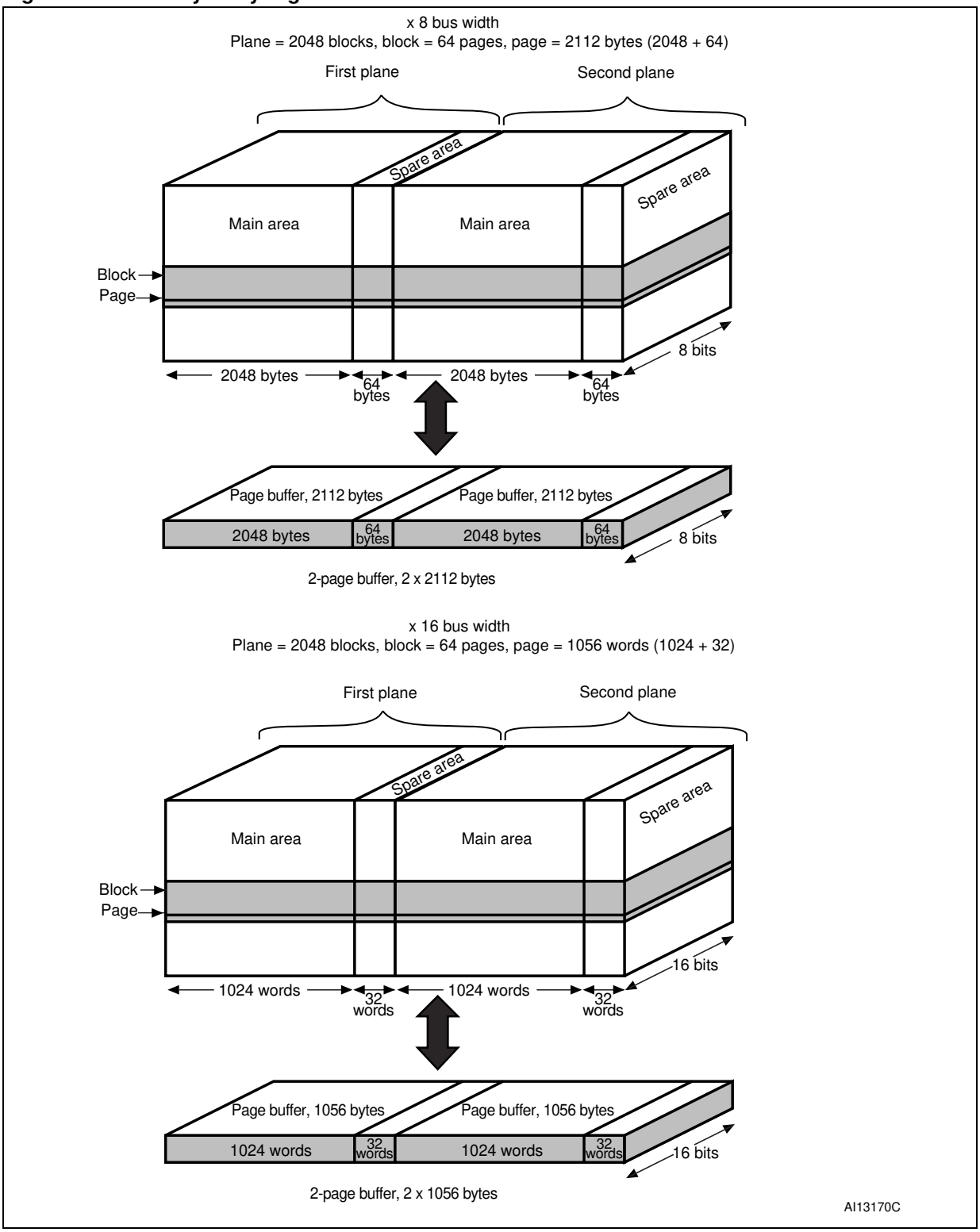
These blocks need to be managed using bad blocks management, block replacement, or error correction codes (refer to *Section 9: Software algorithms*).

Table 4. Valid blocks

Density of device	Min	Max
4 Gbits	4016	4096
8 Gbits(1)	8032	8192

1. The NAND08G-BxC devices are composed of two 4-Gbit dice. The minimum number of valid blocks is 4016 for each die.

Figure 6. Memory array organization



3 Signals description

See *Figure 2: Logic diagram* and *Table 3: Signals names* for a brief overview of the signals connected to this device.

3.1 Inputs/outputs (I/O0-I/O7)

Input/outputs 0 to 7 input the selected address, output the data during a read operation, or input a command or data during a write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

3.2 Inputs/outputs (I/O8-I/O15)

Input/outputs 8 to 15 are only available in x16 devices. They output the data during a read operation or input data during a write operation. Command and address inputs only require I/O0 to I/O7.

The inputs are latched on the rising edge of Write Enable. I/O8-I/O15 are left floating when the device is deselected or the outputs are disabled.

3.3 Address latch enable (AL)

The address latch enable activates the latching of the address inputs in the command interface. When AL is High, the inputs are latched on the rising edge of Write Enable.

3.4 Command latch enable (CL)

The command latch enable activates the latching of the command inputs in the command interface. When CL is High, the inputs are latched on the rising edge of Write Enable.

3.5 Chip enable ($\overline{E}$)

The Chip Enable input, $\overline{E}$, activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is Low, V_{IL}, the device is selected. If Chip Enable goes High, V_{IH}, while the device is busy, the device remains selected and does not go into standby mode.

3.6 Read enable ($\overline{R}$)

The Read Enable pin, $\overline{R}$, controls the sequential data output during read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

3.7 Write enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing to the command interface, input address and data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 10 µs (min) is required before the command interface is ready to accept a command. It is recommended to keep Write Enable High during the recovery time.

3.8 Write protect ($\overline{WP}$)

The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

3.9 Ready/Busy ($R\overline{B}$)

The Ready/Busy output, $R\overline{B}$, is an open-drain output that identifies if the P/E/R controller is currently active.

When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes, Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the ready/busy pins from several memories to be connected to a single pull-up resistor. A Low then indicates that one or more of the memories is busy.

During power-up and power-down a minimum recovery time of 10 µs is required before the command interface is ready to accept a command. During this period the $R\overline{B}$ signal is Low, V_{OL}.

Refer to *Section 12.1: Ready/busy signal electrical characteristics* for details on how to calculate the value of the pull-up resistor.

3.10 V_{DD} supply voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

An internal voltage detector disables all functions whenever V_{DD} is below V_{LKO} (see *Table 29*) to protect the device from any involuntary program/erase during power-transitions.

Each device in a system should have V_{DD} decoupled with a 0.1 µF capacitor. The PCB track widths should be sufficient to carry the required program and erase currents.

3.11 V_{SS} ground

Ground, V_{SS}, is the reference for the power supply. It must be connected to the system ground.

4 Bus operations

There are six standard bus operations that control the memory, as described in this section. See *Table 5: Bus operations* for a summary of these operations.

Typically, glitches of less than 5 ns on Chip Enable, Write Enable, and Read Enable are ignored by the memory and do not affect bus operations.

4.1 Command input

Command input bus operations give commands to the memory.

Commands are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low, and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O0 to I/O7 are used to input commands.

See *Figure 24* and *Table 30* for details of the timings requirements.

4.2 Address input

Address input bus operations input the memory addresses. Five bus cycles are required to input the addresses (refer to *Table 6: Address insertion (x8 devices)* and *Table 7: Address insertion (x16 devices)*).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low, and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O0 to I/O7 are used to input addresses.

See *Figure 25* and *Table 30* for details of the timings requirements.

4.3 Data input

Data input bus operations input the data to be programmed.

Data is accepted only when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low, and Read Enable is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

See *Figure 26* and *Table 30* and *Table 31* for details of the timings requirements.

4.4 Data output

Data output bus operations read the data in the memory array, the status register, the electronic signature, and the unique identifier.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low.

The data is output sequentially using the Read Enable signal.

If the Read Enable pulse frequency is lower then 33 MHz (t_{RLRL} higher than 30 ns), the output data is latched on the rising edge of Read Enable signal (see *Figure 27*).

For higher frequencies (t_{RLRL} lower than 30 ns), the EDO (extended data out) mode must be used. In this mode, data output bus operations are valid on the input/output bus for a time of t_{RLQX} after the falling edge of Read Enable signal (see *Figure 28*).

See *Table 31* for details on the timings requirements.

4.5 Write protect

Write protect bus operations protect the memory against program or erase operations. When the Write Protect signal is Low the device does not accept program or erase operations, and, therefore, the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection, even during power-up.

4.6 Standby

When Chip Enable is High the memory enters standby mode, the device is deselected, outputs are disabled, and power consumption is reduced.

Table 5. Bus operations

Bus operation	$\overline{E}$	AL	CL	$\overline{R}$	$\overline{W}$	$\overline{WP}$	I/O0 - I/O7	I/O8 - I/O15(1)
Command input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X(2)	Command	X
Address input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address	X
Data input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	V_{IH}	Data input	Data input
Data output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data output	Data output
Write protect	X	X	X	X	X	V_{IL}	X	X
Standby	V_{IH}	X	X	X	X	V_{IL}/V_{DD}	X	X

1. Only for x16 devices.
2. $\overline{WP}$ must be V_{IH} when issuing a Program or Erase command.

Table 6. Address insertion (x8 devices)

Bus cycle(1)	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A11	A10	A9	A8
3rd	A19	A18	A17	A16	A15	A14	A13	A12
4th	A27	A26	A25	A24	A23	A22	A21	A20
5th	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A30(2)	A29	A28

1. Any additional address input cycles are ignored.
2. A30 is only valid for the NAND08G-BxC devices.

Table 7. Address insertion (x16 devices)

Bus cycle(1)	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A10	A9	A8
3rd	A18	A17	A16	A15	A14	A13	A12	A11
4th	A26	A25	A24	A23	A22	A21	A20	A19
5th	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A29(2)	A28	A27

1. Any additional address input cycles are ignored.
2. A29 is only valid for the NAND08G-BxC devices.

Table 8. Address definition (x8 devices)

Address	Definition
A0 - A11	Column address
A12 - A17	Page address
A18 - A29	Block address(NAND04G-B2D)
A18 - A30	Block address (NAND08G-BxC)
A18 = 0	First plane
A18 = 1	Second plane

Table 9. Address definition (x16 devices)

Address	Definition
A0 - A10	Column address
A11 - A16	Page address
A17 - A28	Block address (NAND04G-B2D)
A17 - A29	Block address (NAND08G-BxC)
A17 = 0	First plane
A17 = 1	Second plane

5 Command set

All bus write operations to the device are interpreted by the command interface. The commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the command Latch Enable signal is High. Device operations are selected by writing specific commands to the command register. The two-step command sequences for program and erase operations are imposed to maximize data security.

Table 10 summarizes the commands.

Table 10. Commands

Command[1]	Bus write operations				Commands accepted during busy
	1st cycle	2nd cycle	3rd cycle	4th cycle	
Read	00h	30h	–	–	
Random Data Output	05h	E0h	–	–	
Cache Read (sequential)	31h	–	–	–	
Enhanced Cache Read (random)	00h	31h	–	–	
Exit Cache Read	3Fh	–	–	–	Yes[2]
Page Program (sequential input default)	80h	10h	–	–	
Random Data Input	85h	–	–	–	
Multiplane Page Program[3]	80h	11h	81h	10h	
Multiplane Page Program	80h	11h	80h	10h	
Copy Back Read	00h	35h	–	–	
Copy Back Program	85h	10h	–	–	
Multiplane Copy Back Program[3]	85h	11h	81h	10h	
Multiplane Copy Back Program	85h	11h	85h	10h	
Block Erase	60h	D0h	–	–	
Multiplane Block Erase[3]	60h	60h	D0h	–	
Multiplane Block Erase	60h	D1h	60h	D0h	
Reset	FFh	–	–	–	Yes
Read Electronic Signature	90h	–	–	–	
Read Status Register	70h	–	–	–	Yes
Read Status Enhanced	78h	–	–	–	Yes
Read Parameter Page	ECh	–	–	–	
Read EDC Status Register	7Bh	–	–	–	

1. Commands in bold are referring to ONFI 1.0 specifications.
2. Only during cache read busy.
3. Command maintained for backward compatibility.

6 Device operations

This section provides details of the device operations.

6.1 Read memory array

At power-up the device defaults to read mode. To enter read mode from another mode, the Read command must be issued (see *Table 10: Commands*).

6.1.1 Random read

Each time the Read command is issued, the first read is random read.

6.1.2 Page read

After the first random read access, the page data (2112 bytes or 1056 words) are transferred to the page buffer in a time of t_{WHBH} (see *Table 31*). Once the transfer is complete, the Ready/Busy signal goes High. The data can then be read sequentially (from selected column address to last column address) by pulsing the Read Enable signal.

The device can output random data in a page, instead of consecutive sequential data, by issuing a Random Data Output command. The Random Data Output command can be used to skip some data during a sequential data output.

The sequential operation can be resumed by changing the column address of the next data to be output, to the address which follows the Random Data Output command. The Random Data Output command can be issued as many times as required within a page.

The Random Data Output command is not accepted during cache read operations.

Figure 7. Read operations

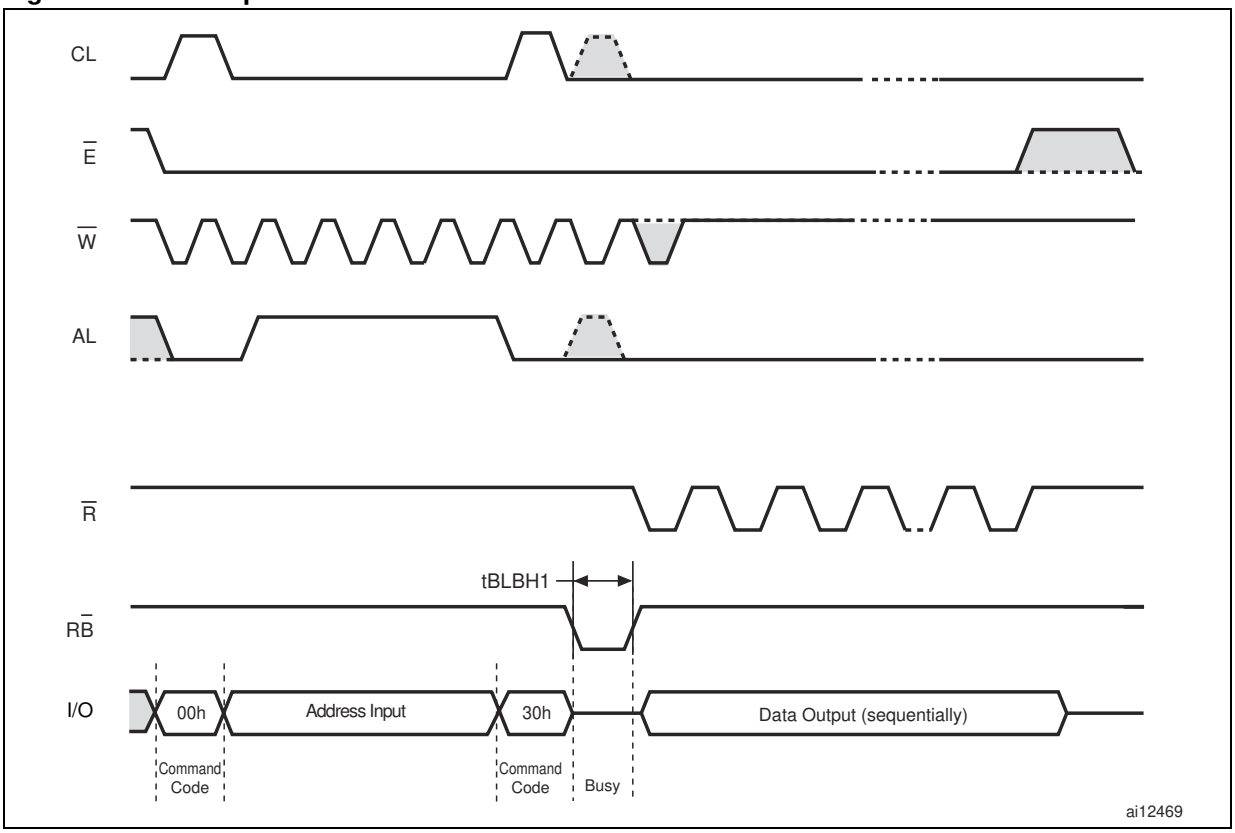
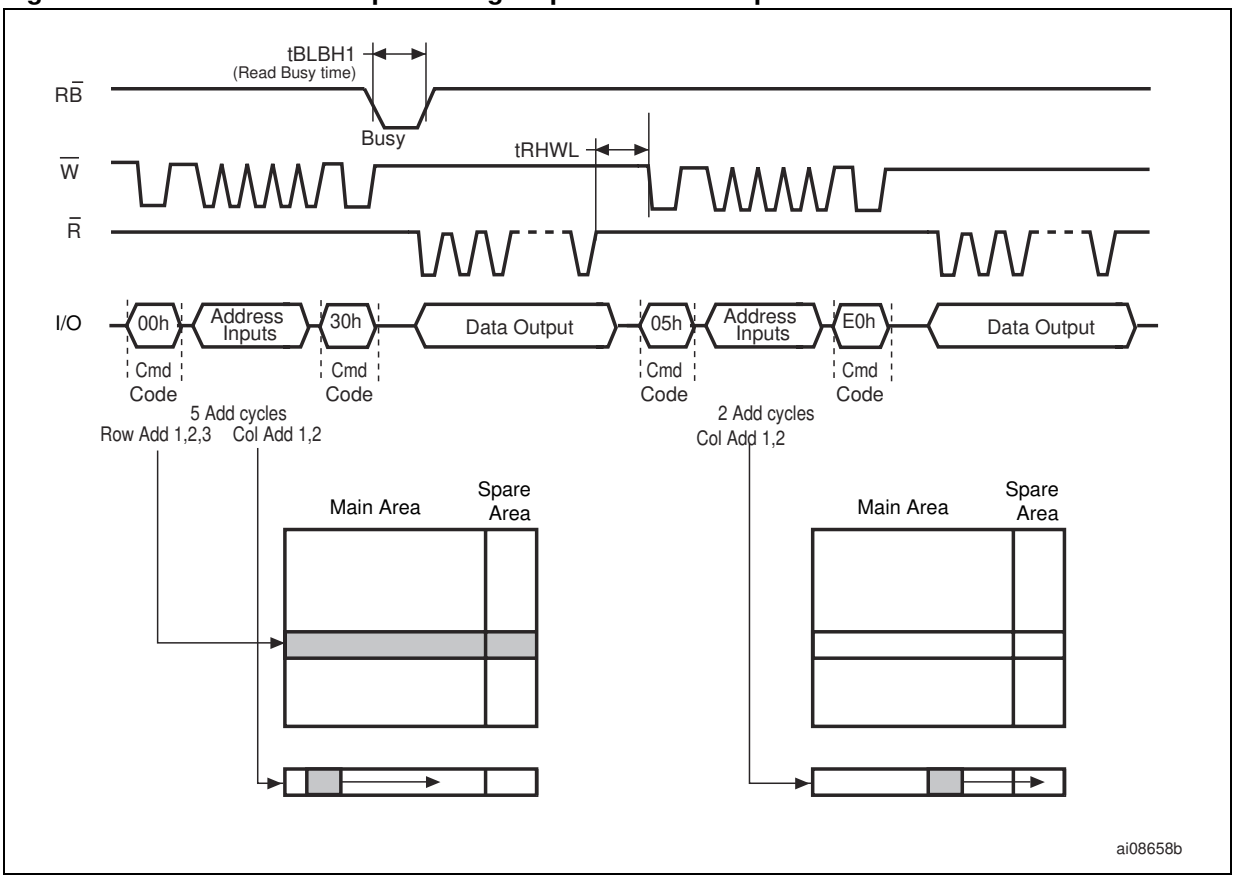


Figure 8. Random data output during sequential data output



6.2 Cache read

The cache read operation improves the read throughput by reading data using the cache register. As soon as the user starts to read one page, the device automatically loads the next page into the cache register.

A Read Page command, as defined in *Section 6.1.1: Random read*, is issued prior to the first Read Cache command in a read cache sequence. Once the Read Page command execution is terminated, the Cache Read command can be issued as follows:

1. Issue a Sequential Cache Read command to copy the next page in sequential order to the cache register
2. Issue a Random Cache Read command to copy the page addressed in this command to the cache register.

The two commands can be used interchangeably, in any order. When there are no more pages are to be read, the final page is copied into the cache register by issuing the Exit Cache Read command. A Read Cache command must not be issued after the last page of the device is read. Data output only starts after issuing the 31h command for the first time.

See *Figure 9: Cache read (sequential) operation* and *Figure 10: Cache read (random) operation* for examples of the two sequences.

After the Sequential Cache Read or Random Cache Read command has been issued, the Ready/Busy signal goes Low and the status register bits are set to SR5 =' 0' and SR6 ='0' for a period of cache read busy time, t_{RCBSY}, while the device copies the next page into the cache register.

After the cache read busy time has passed, the Ready/Busy signal goes High and the status register bits are set to SR5 = '0' and SR6 = '1', signifying that the cache register is ready to download new data. Data of the previously read page can be output from the page buffer by toggling the Read Enable signal. Data output always begins at column address 00h, but the Random Data Output command is also supported.

Figure 9. Cache read (sequential) operation

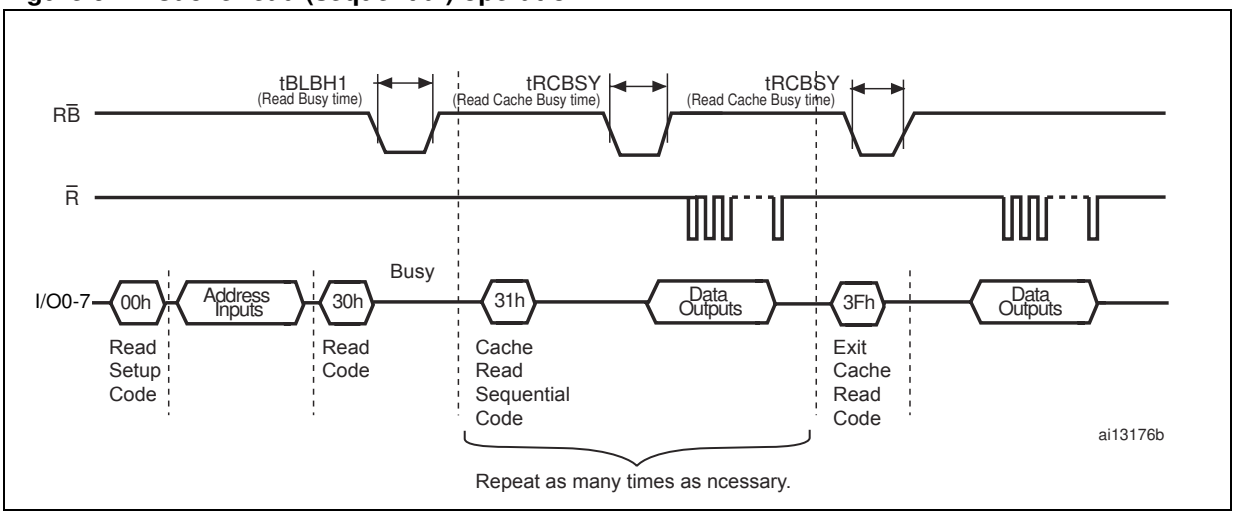


Figure 10. Cache read (random) operation