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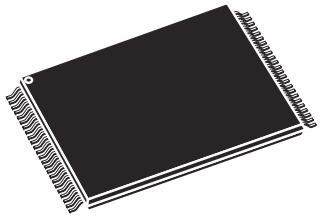
NAND08GW3F2A
NAND16GW3F2A

8-Gbit, 16-Gbit, 4224-byte page, 3 V supply, multiplane architecture, SLC NAND flash memories

Preliminary Data

Features

- High density SLC NAND flash memory
  - 8, 16 Gbits of memory array
  - Cost-effective solutions for mass storage applications
- NAND interface
  - x8 bus width
  - Multiplexed address/data
- Supply voltage: V_{DD} = 2.7 to 3.6 V
- Page size: (4096 + 128 spare) bytes
- Block size: (256K + 8K spare) bytes
- Multiplane architecture
  - Array split into two independent planes
  - All operations can be performed on both planes simultaneously
- Page read/program
  - Random access: 25 µs (max)
  - Sequential access: 25 ns (min)
  - Page program operation time: 500 µs (typ)
- Multiplane program time (2 pages): 500 µs (typ)
- Copy-back program
  - Automatic block download without latency time
- Fast block erase
  - Block erase time: 1.5 ms (typ)
  - Multiplane block erase time (2 blocks): 1.5 ms (typ)
- Status register
- Electronic signature
- Chip enable ‘don’t care’



TSOP48 12 x 20 mm (N)

- Data protection
  - Hardware program/erase locked during power transitions
- Security features
  - OTP area
  - Serial number (unique ID)
- Development tools
  - Error correction code models
  - Bad block management and wear leveling algorithm
  - HW simulation models
- Data integrity
  - 100,000 program/erase cycles (with ECC)
  - 10 years data retention
- RoHS compliant packages

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1 Description

The NANDxxGW3F2A device belongs to the 4224-byte page family of non-volatile NAND flash memories. The NANDxxGW3F2A has a density of 8 or 16 Gbits (2 x 8 Gbits). The device operates from a 3 V power supply.

The address lines are multiplexed with the data input/output signals on a multiplexed x8 input/output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased up to 100,000 cycles (with error correction code (ECC) on). A write protect pin is available to provide hardware protection against program and erase operations.

The devices feature an open-drain, ready/busy output that identifies if the program/erase/read (P/E/R) controller is currently active. The use of an open-drain output allows the ready/busy pins of several memories to be connected to a single pull-up resistor.

For each die, the memory array is split into 2 planes of 2048 blocks each. This multiplane architecture makes it possible to program 2 pages at a time (one in each plane), to erase 2 blocks at a time (one in each plane), or to read 2 pages at a time (one in each plane) dividing by two the average program, erase, and read times.

The device has the Chip Enable ’don’t care’ feature, which allows the bus to be shared between more than one memory at the same time, as Chip Enable transition during the latency time do not stop the read operation. Program and erase operations can never be interrupted by Chip Enable transition.

The device comes with two security features:

- OTP (one time programmable) area, which is a restricted access area where sensitive data/code can be stored permanently. The access sequence and further details about this feature are subject to an NDA (non disclosure agreement)
- Serial number (unique identifier), which allows the NANDxxGW3F2A to be uniquely identified. It is subject to an NDA (non-disclosure agreement) and is, therefore, not described in the datasheet.

For more details about these security features, contact your nearest Numonyx sales office.

The device is available in TSOP48 (12 × 20 mm) package. and is shipped from the factory with block 0 always valid and the memory content bits, in valid blocks, erased to ‘1’.

Refer to the list of available part numbers and to *Table 23: Ordering information scheme* for information on how to order these options.

Table 1. Device summary

Part number	Density	Bus width	Page size	Block size	Memory array	Operating voltage (V_{DD})	Timings				Package
							Random access time (max)	Sequential access time (min)	Page program (typ)	Block erase (typ)	
NAND08GW3F2A	8 Gbits	x8	4096+128 bytes	256K + 8K bytes	64 pages x 4096 blocks	2.7 to 3.6 V	25 µs	25 ns	500 µs	1.5 ms	TSOP48
NAND16GW3F2A	16 Gbits				64 pages x 8192 blocks						

Figure 1. Logic block diagram

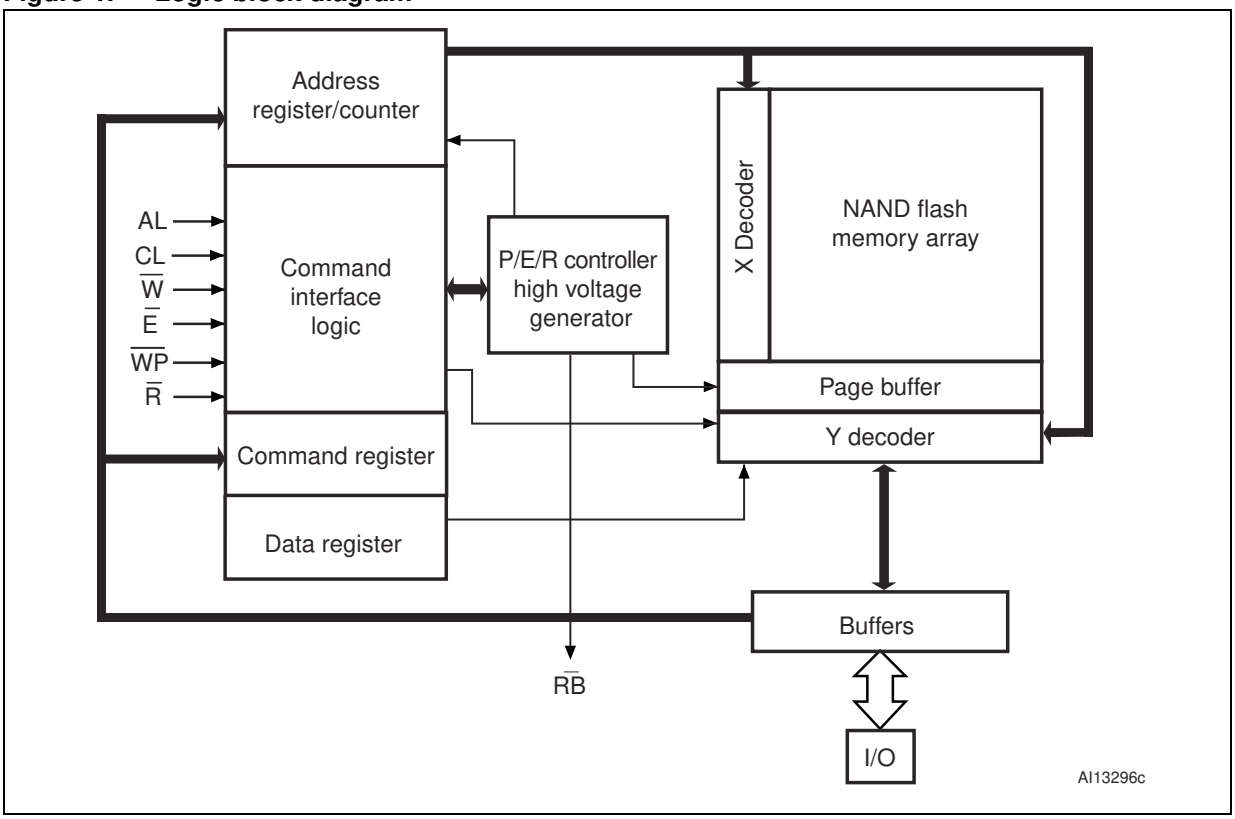


Figure 2. Logic diagram

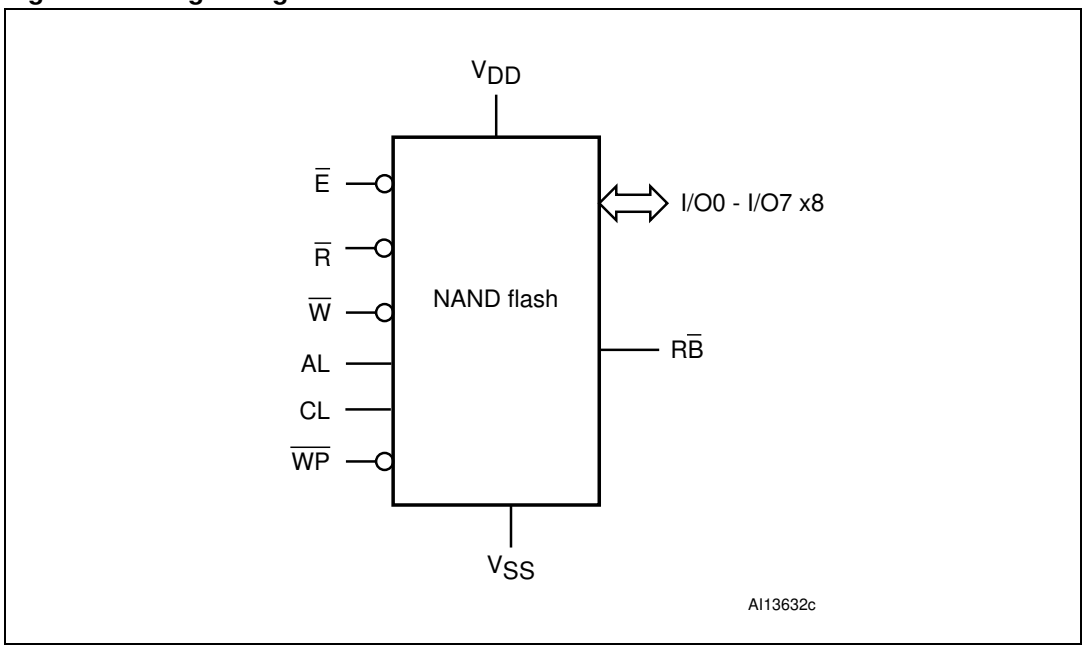
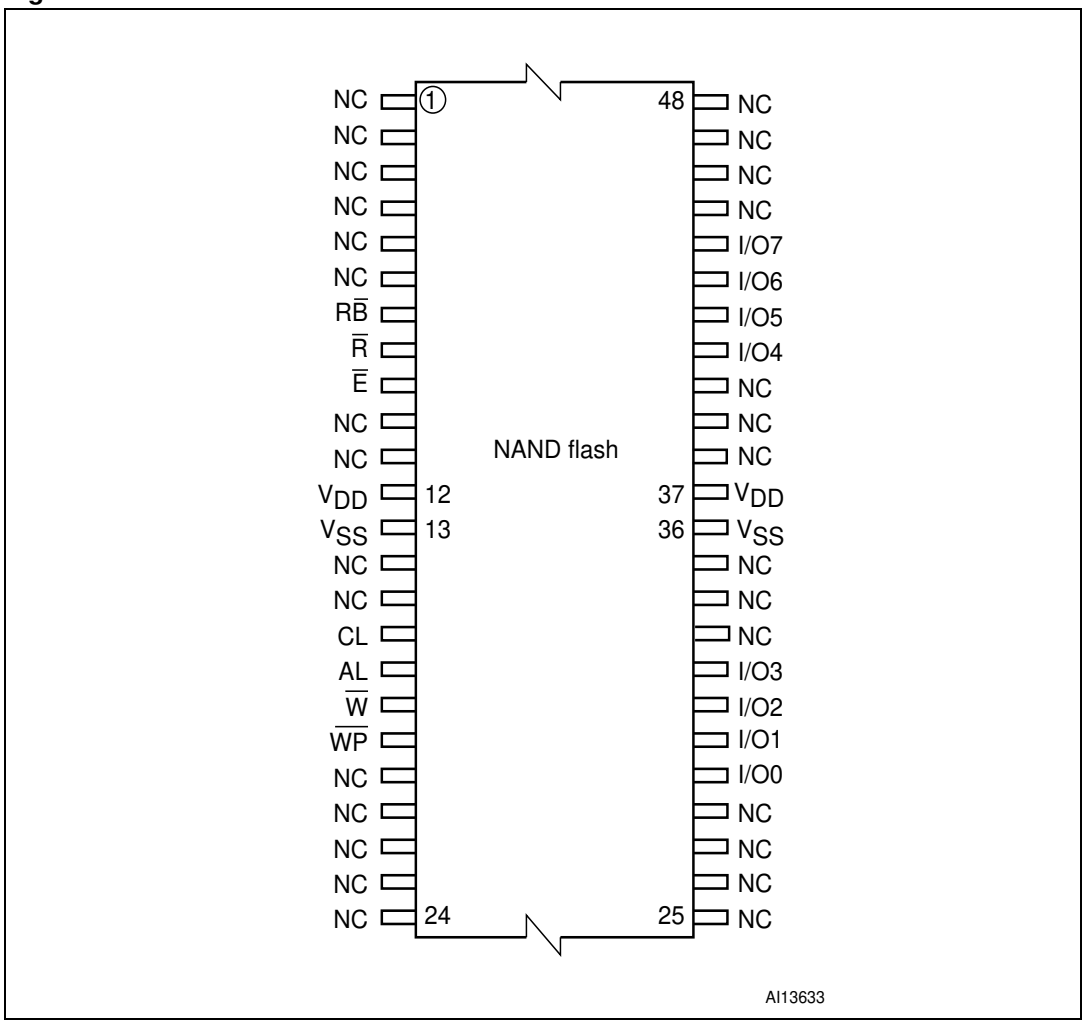


Table 2. Signal names

Signal	Function	Direction
I/O0 - I/O7	Data input/outputs	Input/output
CL	Command Latch Enable	Input
AL	Address Latch Enable	Input
$\overline{E}$	Chip Enable	Input
$\overline{R}$	Read Enable	Input
$\overline{W}$	Write Enable	Input
$\overline{WP}$	Write Protect	Input
$R\overline{B}$	Ready/Busy (open drain output)	Output
V_{DD}	Power supply	Power supply
V_{SS}	Ground	Ground
NC	No connection	–
DU	Do not use	–

Figure 3. TSOP48 connections



2 Memory array organization

The memory array is comprised of NAND structures where 32 cells are connected in series.

It is organized into blocks where each block contains 64 pages. The array is split into two areas, the main area and the spare area. The main area of the array stores data, whereas the spare area typically stores software flags or bad block identification.

The pages are split into a 4096-byte main area and a spare area of 128 bytes. Refer to *Figure 4: Memory array organization*.

2.1 Bad blocks

The NANDxxGW3F2A devices may contain bad blocks, where the reliability of blocks that contain one or more invalid bits is not guaranteed. Additional bad blocks may develop during the lifetime of the device.

The bad block information is written prior to shipping (refer to *Section 9.1: Bad block management* for more details).

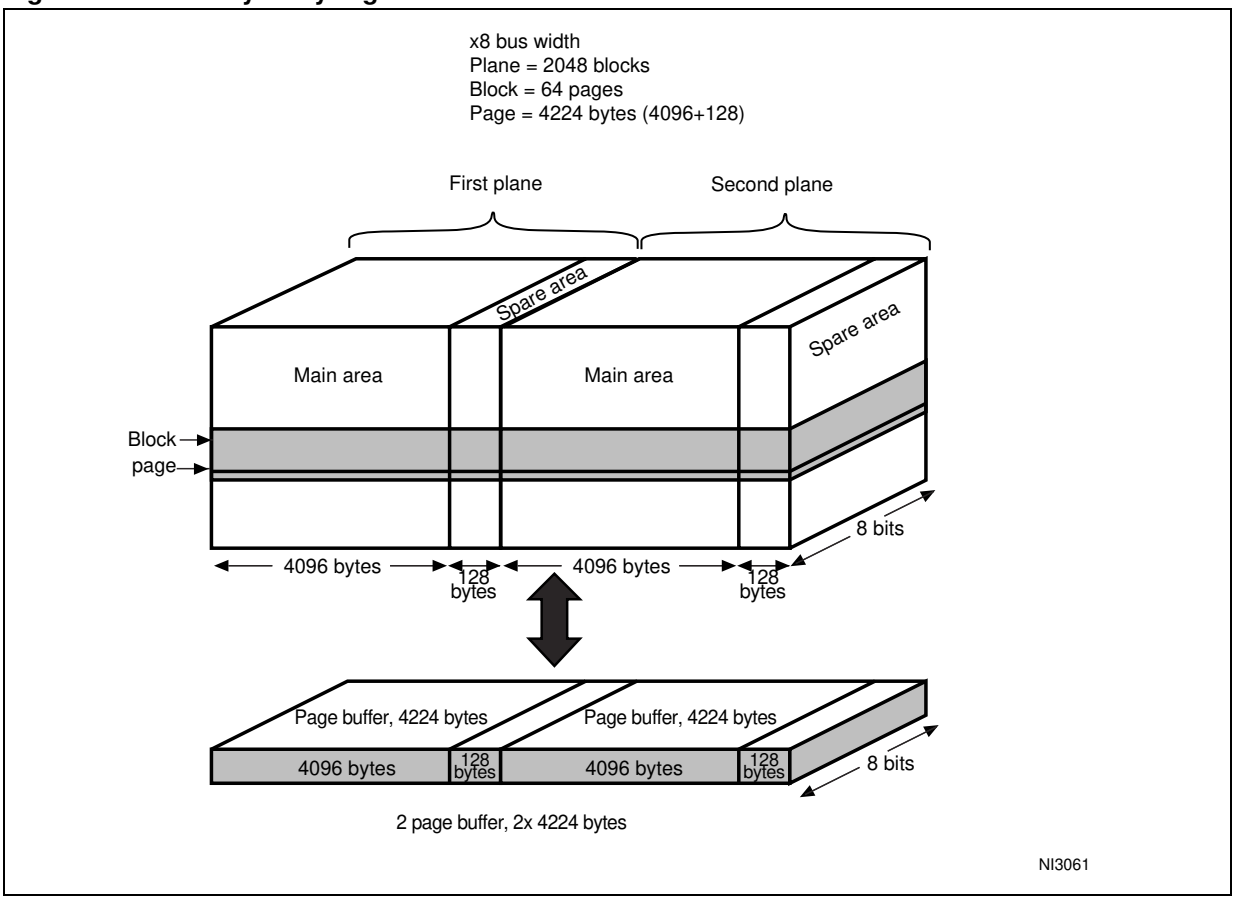
Table 3: Valid blocks shows the minimum number of valid blocks. The values shown include both the bad blocks that are present when the device is shipped and the bad blocks that could develop later on.

These blocks need to be managed using bad blocks management and block replacement (refer to *Section 9: Software algorithms*).

Table 3. Valid blocks

Density of device	Minimum	Maximum
8 Gbits	4016	4096
16 Gbits	8032	8192

Figure 4. Memory array organization



3 Signal descriptions

See *Figure 1: Logic block diagram*, and *Table 2: Signal names* for a brief overview of the signals connected to this device.

3.1 Inputs/outputs (I/O0-I/O7)

Input/outputs 0 to 7 are used to input the selected address, output the data during a read operation, or input a command or data during a write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

3.2 Address Latch Enable (AL)

The Address Latch Enable activates the latching of the address inputs in the command interface. When AL is High, the inputs are latched on the rising edge of Write Enable.

3.3 Command Latch Enable (CL)

The Command Latch Enable activates the latching of the command inputs in the command interface. When CL is High, the inputs are latched on the rising edge of Write Enable.

3.4 Chip Enable ($\overline{E}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is Low, V_{IL}, the device is selected. If Chip Enable goes High, V_{IH}, while the device is busy, the device remains selected and does not go into standby mode.

3.5 Read Enable ($\overline{R}$)

The Read Enable pin, $\overline{R}$, controls the sequential data output during read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

3.6 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing to the command interface, input address, and data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 10 µs (min) is required before the command interface is ready to accept a command. It is recommended to keep Write Enable High during the recovery time.

3.7 Write Protect ($\overline{WP}$)

The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

3.8 Ready/Busy ($R\overline{B}$)

The Ready/Busy output, $R\overline{B}$, is an open-drain output that can identify if the P/E/R controller is currently active.

When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes, Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low indicates that one, or more, of the memories is busy.

During power-up and power-down a minimum recovery time of 10 µs is required before the command interface is ready to accept a command. During this period the Ready/Busy signal is Low, V_{OL}.

Refer to *Section 12.1: Ready/Busy signal electrical characteristics* for details on how to calculate the value of the pull-up resistor.

3.9 V_{DD} supply voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

An internal voltage detector disables all functions whenever V_{DD} is below V_{LKO} (see *Table 19: DC characteristics*) to protect the device from any involuntary program/erase during power transitions.

Each device in a system should have V_{DD} decoupled with a 0.1 µF capacitor. The PCB track widths should be sufficient to carry the required program and erase currents.

3.10 V_{SS} ground

Ground, $V_{SS,}$ is the reference for the power supply. It must be connected to the system ground.

4 Bus operations

There are six standard bus operations that control the memory. Each of these is described in this section. See the summary in *Table 4: Bus operations*.

Typically, glitches of less than 3 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

4.1 Command input

Command input bus operations give commands to the memory. Commands are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O0 to I/O7 are used to input commands.

See *Figure 33* and *Table 20* for details of the timings requirements.

4.2 Address input

Address input bus operations input the memory addresses. Five bus cycles are required to input the addresses (refer to *Table 5: Address insertion*).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal. Only I/O0 to I/O7 are used to input addresses.

See *Figure 34* and *Table 20* for details of the timings requirements.

4.3 Data input

Data input bus operations input the data to be programmed. Data is only accepted when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low and Read Enable is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

See *Figure 35* and *Table 20* for details of the timing requirements.

4.4 Data output

Data output bus operations read the data in the memory array, the status register, the electronic signature, and the unique identifier.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low.

The data is output sequentially using the Read Enable signal.

If the Read Enable pulse frequency is lower then 33 MHz (t_{RLRL} higher than 30 ns), the output data is latched on the rising edge of Read Enable signal (see *Figure 36: Sequential data output after read AC waveforms*).

For higher frequencies (t_{RLRL} lower than 30 ns), the extended data out (EDO) mode must be considered. In this mode, data output is valid on the input/output bus for a time of t_{RLQX} after the falling edge of Read Enable signal (see *Figure 36: Sequential data output after read AC waveforms*).

See *Table 21: AC characteristics for operations,* for details on the timings requirements.

4.5 Write protect

Write protect bus operations protect the memory against program or erase operations. When the Write Protect signal is Low the device does not accept program or erase operations, therefore, the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection, even during power-up.

4.6 Standby

The memory enters standby mode by holding Chip Enable, $\overline{E}$, High for at least 10 µs. In standby mode, the device is deselected, outputs are disabled and power consumption is reduced.

Table 4. Bus operations

Bus operation	$\overline{E}$	AL	CL	$\overline{R}$	$\overline{W}$	$\overline{WP}$	I/O0 - I/O7
Command input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X(1)	Command
Address input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address
Data input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	V_{IH}	Data input
Data output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data output
Write protect	X	X	X	X	X	V_{IL}	X
Standby	V_{IH}	X	X	X	X	V_{IL}/V_{DD}	X

1. $\overline{WP}$ must be V_{IH} when issuing a program or erase command.

Table 5. Address insertion(1)

Bus cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	V_{IL}	V_{IL}	V_{IL}	A12	A11	A10	A9	A8
3rd	A20	A19	A18	A17	A16	A15	A14	A13
4th	A28	A27	A26	A25	A24	A23	A22	A21
5th	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A31(2)	A30	A29

1. Any additional address input cycles are ignored.
2. A31 is required only for 16-Gbit devices.

Table 6. Address definitions

Address	Definition
A0 - A12	Column address
A13 - A18	Page address
A19 - A31	Block address

5 Command set

All bus write operations to the device are interpreted by the command interface. The commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is High. Device operations are selected by writing specific commands to the command register. The two-step command sequences for program and erase operations are imposed to maximize data security.

The commands are summarized in *Table 7: Command set*.

Table 7. Command set

Function	1st cycle	2nd cycle	3rd cycle	4th cycle	Acceptable during command busy
Page Read	00h	30h			
Read for Copy Back	00h	35h			
Read ID	90h				
Reset	FFh				Yes
Page Program	80h	10h			
Multiplane Page Program	80h	11h	81h	10h	
Multiplane Read	60h	60h	30h		
Copy Back Program	85h	10h			
Multiplane Copy Back Program	85h	11h	81h	10h	
Multiplane Copy Back Read	60h	60h	35h		
Block Erase	60h	D0h			
Multiplane Block Erase	60h	60h	D0h		
Read Status Register	70h				Yes
Random Data Input	85h				
Random Data Output	05h	E0h			
Multiplane Random Data Output	00h	05h	E0h		
Cache Read	31h				
End Cache Read	3Fh				
Page Program with 2-Kbyte compatibility	80h	11h	80h	10h	
Copy Back Program with 2-Kbyte compatibility	85h	11h	85h	10h	

6 Device operations

6.1 Single plane operations

This section gives the details of the single plane device operations.

6.1.1 Page read

At power-up the device defaults to read mode. To enter read mode from another mode the Read command must be issued, see *Table 7: Command set*. Once a Read command is issued, subsequent consecutive read commands only require the confirm command code (30h).

After a first page read operation, the device stays in read mode and a second page read can be started by inputting 5 address cycles and a read confirm command.

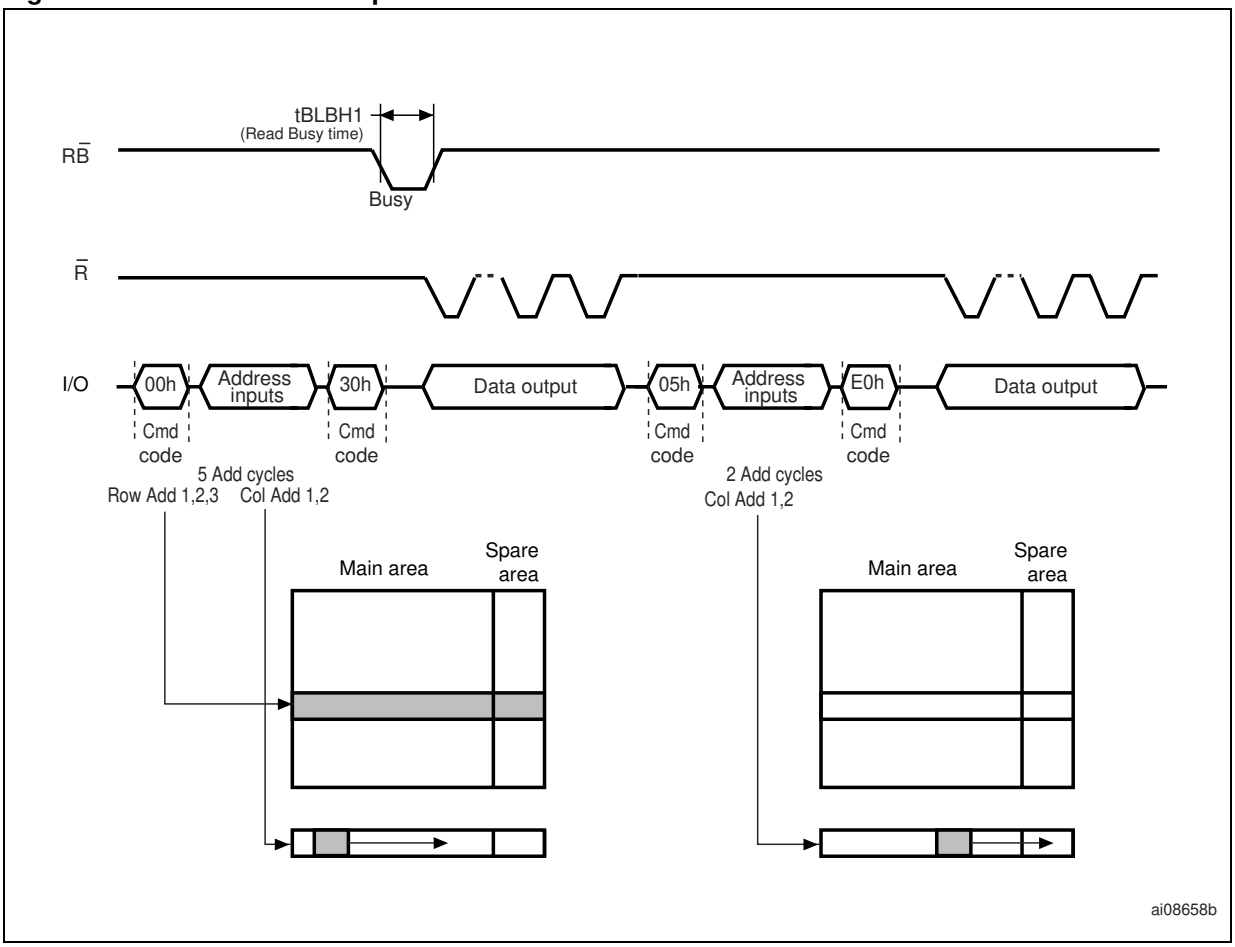
Once a read command is issued, two types of operations are available: random read and sequential page read. The random read mode is enabled when the page address is changed.

After the first random read access, the page data (4224 bytes) is transferred to the page buffer in a time of t_{WHBH} (refer to *Table 21: AC characteristics for operations* for value). Once the transfer is complete, the Ready/Busy signal goes High. The data can then be read out sequentially (from the selected column address to last column address) by pulsing the Read Enable signal (see *Figure 39: Page read operation AC waveforms*).

The device can output random data in a page, instead of the consecutive sequential data, by issuing a Random Data Output command. The Random Data Output command can be used to skip some data during a sequential data output.

The sequential operation can be resumed by changing the column address of the next data to be output, to the address which follows the Random Data Output command. The Random Data Output command can be issued as many times as required within a page.

Figure 5. Random data output



6.1.2 Cache read

The cache read operation improves the read throughput by reading data using the cache register. As soon as the user starts to read one page, the device automatically loads the next page into the cache register.

A Read Page command is issued prior to the first Cache Read command in a cache read sequence. Once the Read Page command execution is terminated, the Cache Read command can be issued as follows:

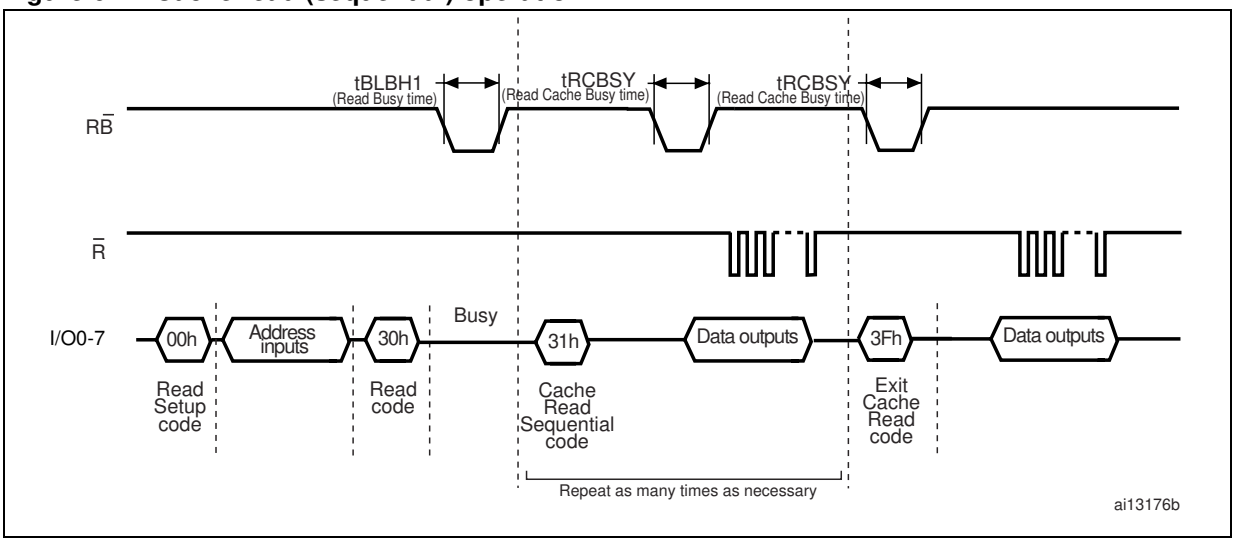
1. Issue a Sequential Cache Read command to copy the next page in sequential order to the cache register
2. Issue a Random Cache Read command to copy the page addressed in this command to the cache register.

The two commands can be used interchangeably, in any order. When there are no more pages to be read, the final page is copied into the cache register by issuing the Exit Cache Read command. A Cache Read command must not be issued after the last page of the device is read. Data output only starts after issuing the 31st command for the first time. See *Figure 6: Cache read (sequential) operation* and *Figure 6.1.3: Page program* for examples of the two sequences.

After the Sequential Cache Read or Random Cache Read command has been issued, the Ready/Busy signal goes Low and the status register bits are set to SR5='0' and SR6='0' for a period of cache read busy time, t_{RCBSY}, while the device copies the next page into the cache register.

After the cache read busy time has passed, the Ready/Busy signal goes High and the status register bits are set to SR5='0' and SR6='1', signifying that the cache register is ready to download new data. data of the previously read page can be output from the page buffer by toggling the Read Enable signal. Data output always begins at column address 00h, but the Random Data Output command is also supported.

Figure 6. Cache read (sequential) operation



6.1.3 Page program

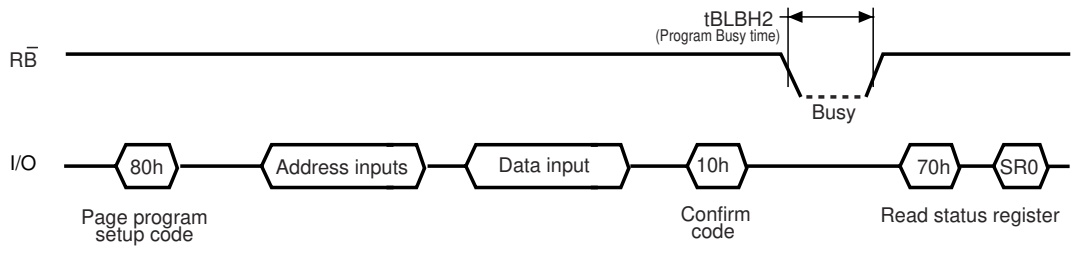
The page program operation is the standard operation to program data to the memory array. Generally, data is programmed sequentially, however, the device does support random input within a page.

The memory array is programmed by page, however, partial page programming is allowed where any number of bytes (1 to 4224) can be programmed.

The maximum number of consecutive partial page program operations on the same page is 8 (see *Table 15: Program and erase times and program erase endurance cycles*). After exceeding this a Block Erase command must be issued before any further program operations can take place in that page (see *Figure 7: Page program operation*).

Within a given block, the pages must be programmed sequentially and random page address programming is not allowed.

Figure 7. Page program operation



Once the program operation has started the status register can be read using the Read Status Register command. During program operations the status register only flags errors for bits set to '1' that have not been successfully programmed to '0'.

During the program operation, only the Read Status Register and Reset commands are accepted; all other commands are ignored. Once the program operation has completed, the P/E/R controller bit SR6 is set to '1' and the Ready/Busy signal goes High.

The device remains in read status register mode until another valid command is written to the command interface.

Sequential input

To input data sequentially the addresses must be sequential and remain in one block.

For sequential input, each page program operation comprises five steps:

1. One bus cycle is required to set up the Page Program (sequential input) command (see *Table 7: Command set*)
2. Five bus cycles are then required to input the program address (refer to *Table 5: Address insertion*)
3. The data is loaded into the data registers
4. One bus cycle is required to issue the Page Program Confirm command to start the P/E/R controller. The P/E/R controller only starts if the data has been loaded in step 3
5. The P/E/R controller then programs the data into the array.

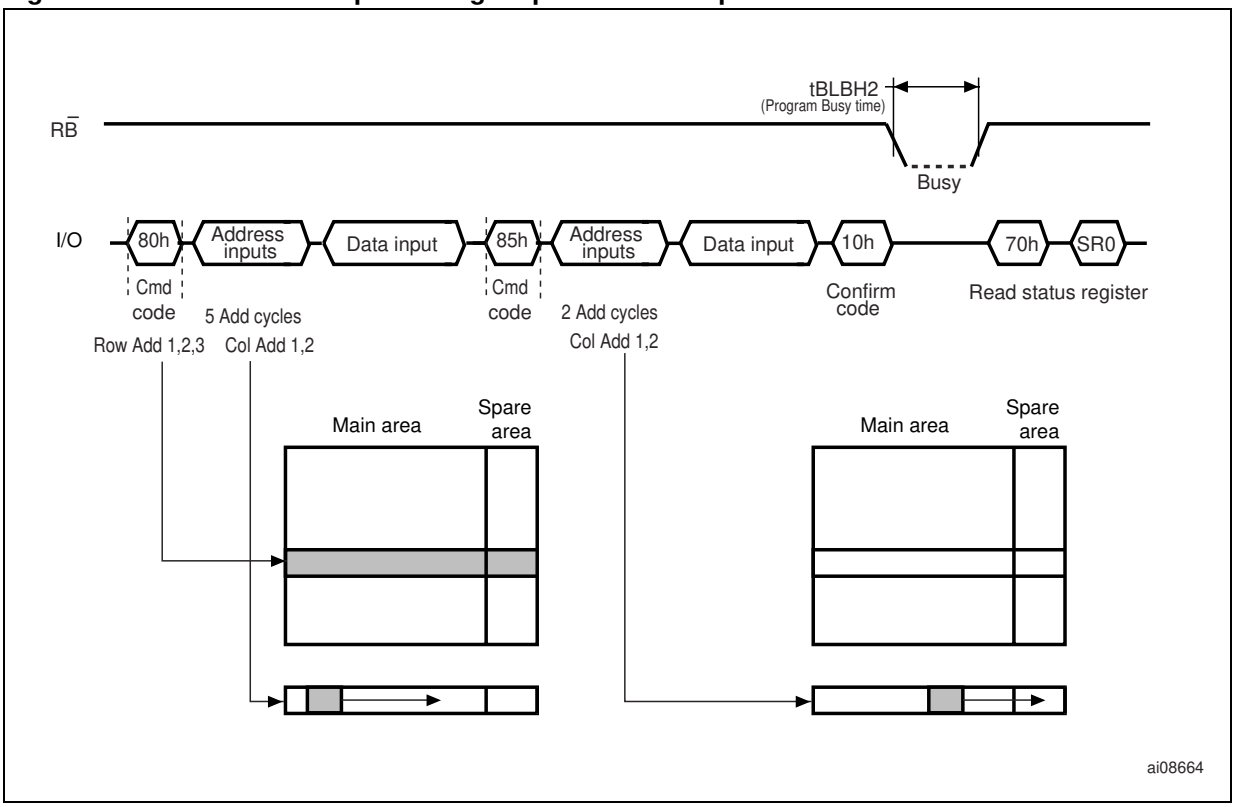
Random data input

During a sequential input operation, the next sequential address to be programmed can be replaced by a random address issuing a Random Data Input command. The following two steps are required to issue the command:

1. One bus cycle is required to setup the Random Data Input command (see *Table 7*).
2. Two bus cycles are then required to input the new column address (refer to *Table 5*).

Random data input operations can be repeated as often as required in any given page.

Figure 8. Random data input during sequential data input



6.1.4 Block erase

Erase operations are done one block at a time. An erase operation sets all the bits in the addressed block to ‘1’. All previous data in the block is lost.

An erase operation consists of three steps (refer to *Figure 9: Block erase operation*):

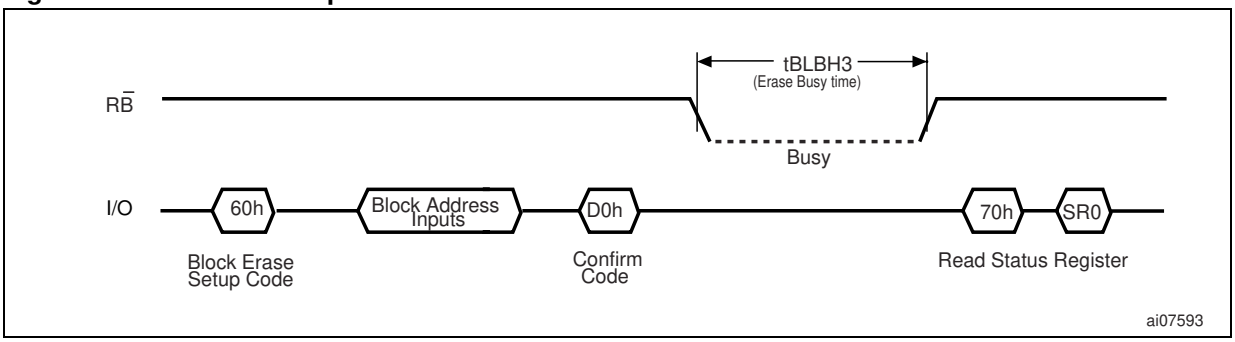
1. One bus cycle is required to setup the Block Erase command. Only addresses A19 to A30 are valid while the addresses A13 to A18 are ignored
2. Three bus cycles are then required to load the address of the block to be erased. Refer to *Table 6: Address definitions* for the block addresses of each device
3. One bus cycle is required to issue the Block Erase Confirm command to start the P/E/R controller.

The erase operation is initiated on the rising edge of Write Enable, $\overline{W}$, after the Confirm command is issued. The P/E/R controller handles block erase and implements the verify process.

During the block erase operation, only the Read Status Register and Reset commands are accepted; all other commands are ignored.

Once the program operation has completed, the P/E/R controller bit SR6 is set to ‘1’ and the Ready/Busy signal goes High. If the operation completes successfully, the write status bit SR0 is ‘0’, otherwise it is set to ‘1’ (refer to *Section 6.5: Read status register*).

Figure 9. Block erase operation



6.1.5 Copy-back program

The copy-back program with read for copy-back operation is configured to quickly and efficiently rewrite data stored in one page without data reloading when the bit error is not in data stored.

Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly-assigned free block. The copy-back operation is a sequential execution of read for copy-back and copy back program with the destination page address. A read operation with a 35h command in the address of the source page moves the entire 4224 bytes into the internal data buffer. When the device returns to the ready state ($R\overline{B}$ High), optional readout of data is allowed by pulsing $\overline{R}$ to check ECC (see *Figure 11: Copy back program operation (with readout of data)*). The next bus write cycle of the command is given to input the target page address.

The actual programming operation begins after the Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the $R\overline{B}$ output, or the status bit (I/O6) of the status register. When the copy back program is complete, the write status bit (I/O0) can be checked. The command register remains in read status command mode until another valid command is written to the command register. During the copy back program, data modification is possible using Random Data Input command (85h) as shown in *Figure 12: Copy back program operation with random data input*.

The copy back program operation is only allowed within the same memory plane (A19 and A31 fixed for source and target address).

Figure 10. Copy back program operation (without readout of data)

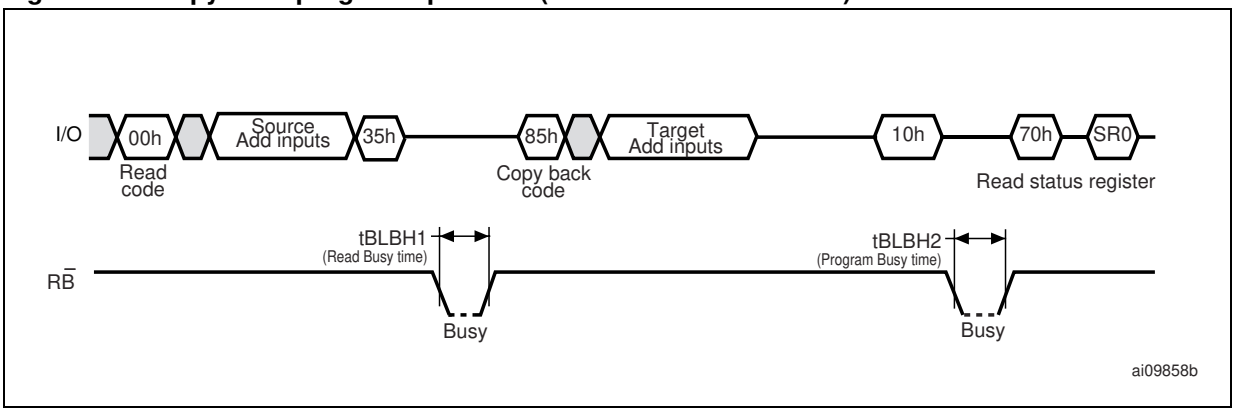


Figure 11. Copy back program operation (with readout of data)

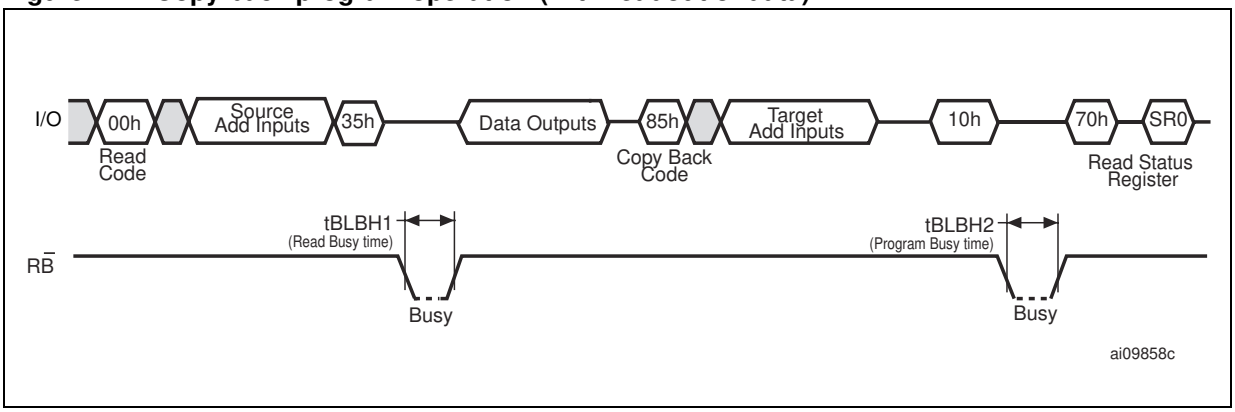


Figure 12. Copy back program operation with random data input