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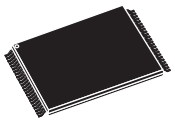
NAND128-A NAND256-A

128-Mbit or 256-Mbit, 528-byte/264-word page, 3 V, SLC NAND flash memories

Features

- High density NAND flash memories
  - Up to 256-Mbit memory array
  - Up to 32-Mbit spare area
  - Cost effective solutions for mass storage applications
- NAND interface
  - x8 or x16 bus width
  - Multiplexed address/ data
  - Pinout compatibility for all densities
- Supply voltage
  - V_{DD} = 2.7 to 3.6 V
- Page size
  - x8 device: (512 + 16 spare) bytes
  - x16 device: (256 + 8 spare) words
- Block size
  - x8 device: (16 K + 512 spare) bytes
  - x16 device: (8 K + 256 spare) words
- Page read/program
  - Random access: 12 µs (3V)/15 us (1.8V) (max)
  - Sequential access: 50 ns (min)
  - Page program time: 200 µs (typ)
- Copy back program mode
  - Fast page copy without external buffering
- Fast block erase
  - Block erase time: 2 ms (typical)
- Status register
- Electronic signature
- Chip enable 'don't care'
  - Simple interface with microcontroller
- Security features
  - OTP area
  - Serial number (unique ID)



TSOP48 12 x 20mm

VFBGA55 8 x 10 x 1.05mm

- Hardware data protection
  - Program/erase locked during power transitions
- Data integrity
  - 100,000 program/erase cycles
  - 10 years data retention
- RoHS compliance
  - Lead-free components are compliant with the RoHS directive
- Development tools
  - Error correction code software and hardware models
  - Bad blocks management and wear leveling algorithms
  - File system OS native reference software
  - Hardware simulation models

Contents

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1 Description

The NAND flash 528 byte/ 264 word page is a family of non-volatile flash memories that uses the single level cell (SLC) NAND cell technology, referred to as the SLC small page family. The devices are either 128 Mbits or 256 Mbits and operate with a 3 V voltage supply. The size of a page is either 528 bytes (512 + 16 spare) or 264 words (256 + 8 spare) depending on whether the device has a x8 or x16 bus width.

The address lines are multiplexed with the data input/output signals on a multiplexed x8 or x16 input/output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased up to 100,000 cycles. To extend the lifetime of NAND flash devices it is strongly recommended to implement an error correction code (ECC). A Write Protect pin is available to provide hardware protection against program and erase operations.

The devices feature an open-drain ready/busy output that identifies if the program/erase/read (P/E/R) controller is currently active. The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor.

A Copy Back command is available to optimize the management of defective blocks. When a page program operation fails, the data can be programmed in another page without having to resend the data to be programmed.

Table 1 lists the individual part numbers of the device.

Table 1. NAND128-A and NAND256-A device summary

Reference	Part Number
NAND128-A	NAND128W3A
NAND256-A(1)	NAND256W3A
	NAND256W4A

1. x16 organization only available for MCP.

The NAND128-A devices are only available in the TSOP48 (12 x 20 mm), while the NAND256-A devices are available in both the TSOP48 and the VFBGA55 (8 x 10 x 1.05 mm) packages.

The devices are available in two different versions:

- No option (Chip Enable ‘care’, sequential row read enabled): the sequential row read feature allows to download up to all the pages in a block with one read command and addressing only the first page to read
- With Chip Enable ‘don’t care’ feature. This enables the sharing of the bus between more active memories that are simultaneously active as Chip Enable transitions during latency do not stop read operations. Program and erase operations are not interrupted by Chip Enable transitions.

The devices come with the following security features:

- OTP (one time programmable) area, which is a restricted access area where sensitive data/code can be stored permanently. The access sequence and further details about this feature are subject to an NDA (non disclosure agreement)
- Serial number (unique identifier), which enables each device to be uniquely identified. It is subject to an NDA and is, therefore, not described in the datasheet.

For more details about these security features, contact your nearest Micron sales office.

For information on how to order these devices, refer to *Table 24: Ordering information scheme*. Devices are shipped from the factory with Block 0 always valid and the memory content bits in valid blocks erased to '1'.

See *Table 2* for all the devices available in the family.

Table 2. Product description

Reference	Part Number	Density	Bus Width	Page Size	Block Size	Memory Array	Operating Voltage	Timings				Package
								Rand Access Max	Seq Access Min	Page Program Typical	Block Erase Typical	
NAND128-A	NAND128W3A	128 Mbit	x8	512+16 Bytes	16K+512 Bytes	32 pages x 1024 Blocks	2.7 to 3.6V	12µs	50ns	200µs	2ms	TSOP48
NAND256-A(1)	NAND256W3A	256 Mbit	x8	512+16 Bytes	16K+512 Bytes	32 pages x 2048 Blocks						TSOP48 VFBGA55
	NAND256W4A		x16	256+8 Words	8K+256 Words							

1. x16 organization only available for MCP.

Figure 1. Logic diagram

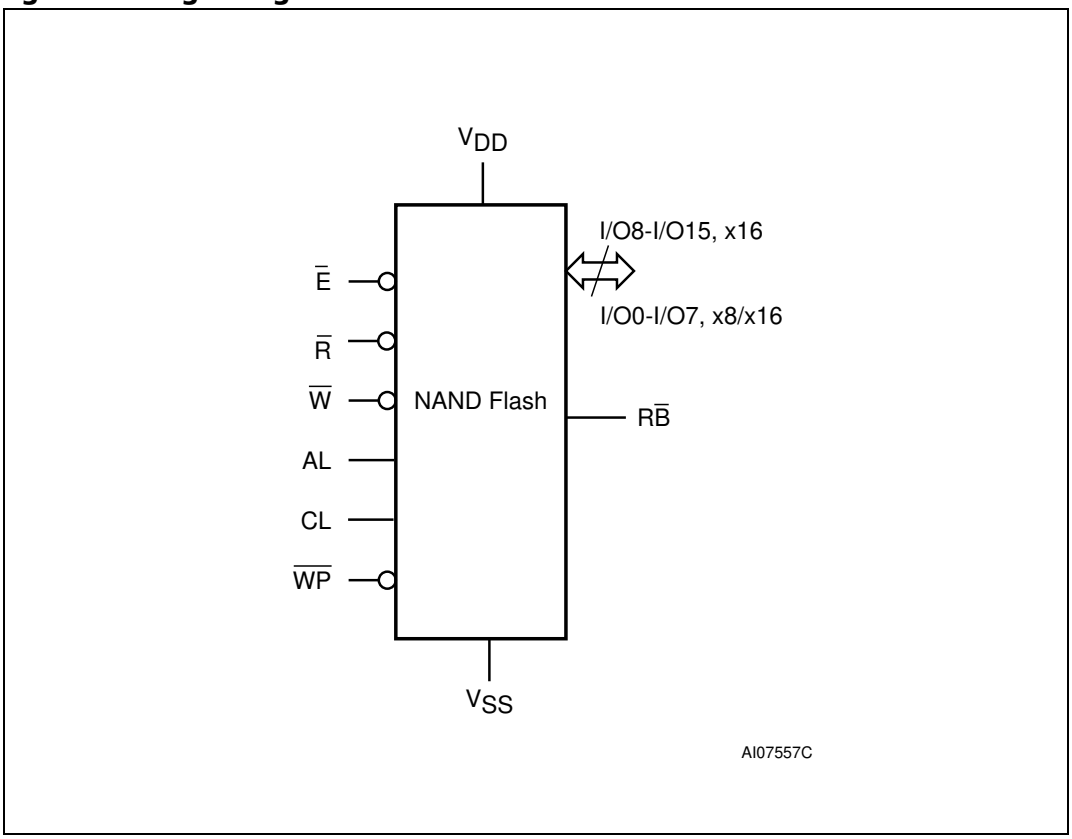


Table 3. Signal names

Symbol	Function
I/O8-15	Data input/outputs for x16 devices
I/O0-7	Data input/outputs, address inputs, or command inputs for x8 and x16 devices
AL	Address Latch Enable
CL	Command Latch Enable
E	Chip Enable
R	Read Enable
RB	Ready/Busy (open-drain output)
W	Write Enable
WP	Write Protect
V_{DD}	Supply voltage
V_{SS}	Ground
NC	Not connected internally
DU	Do not use

Figure 2. Logic block diagram

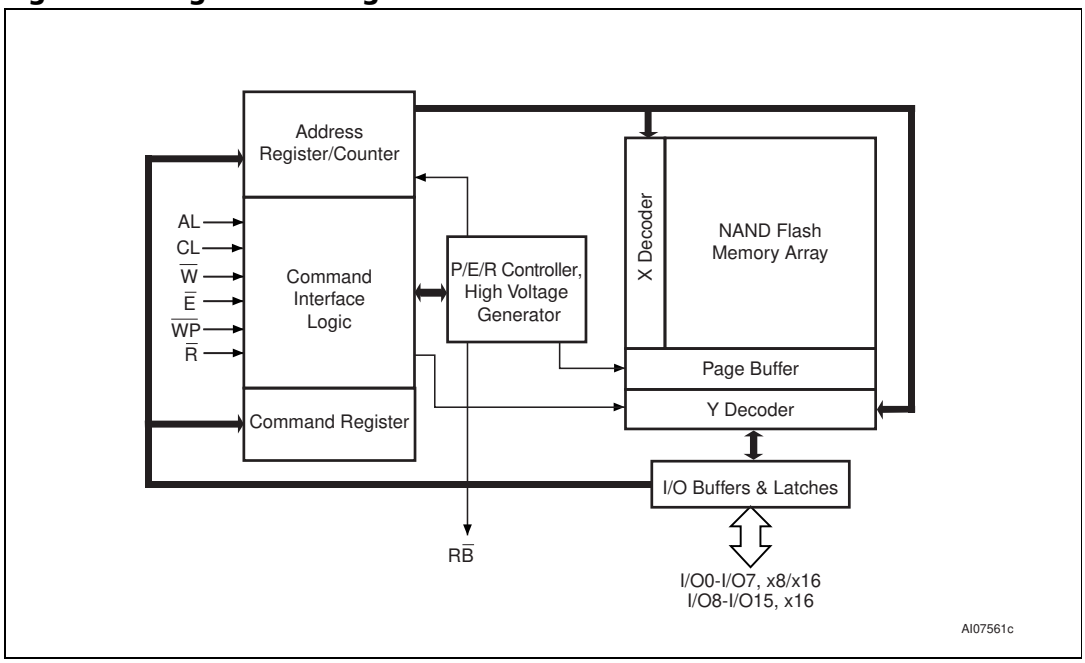
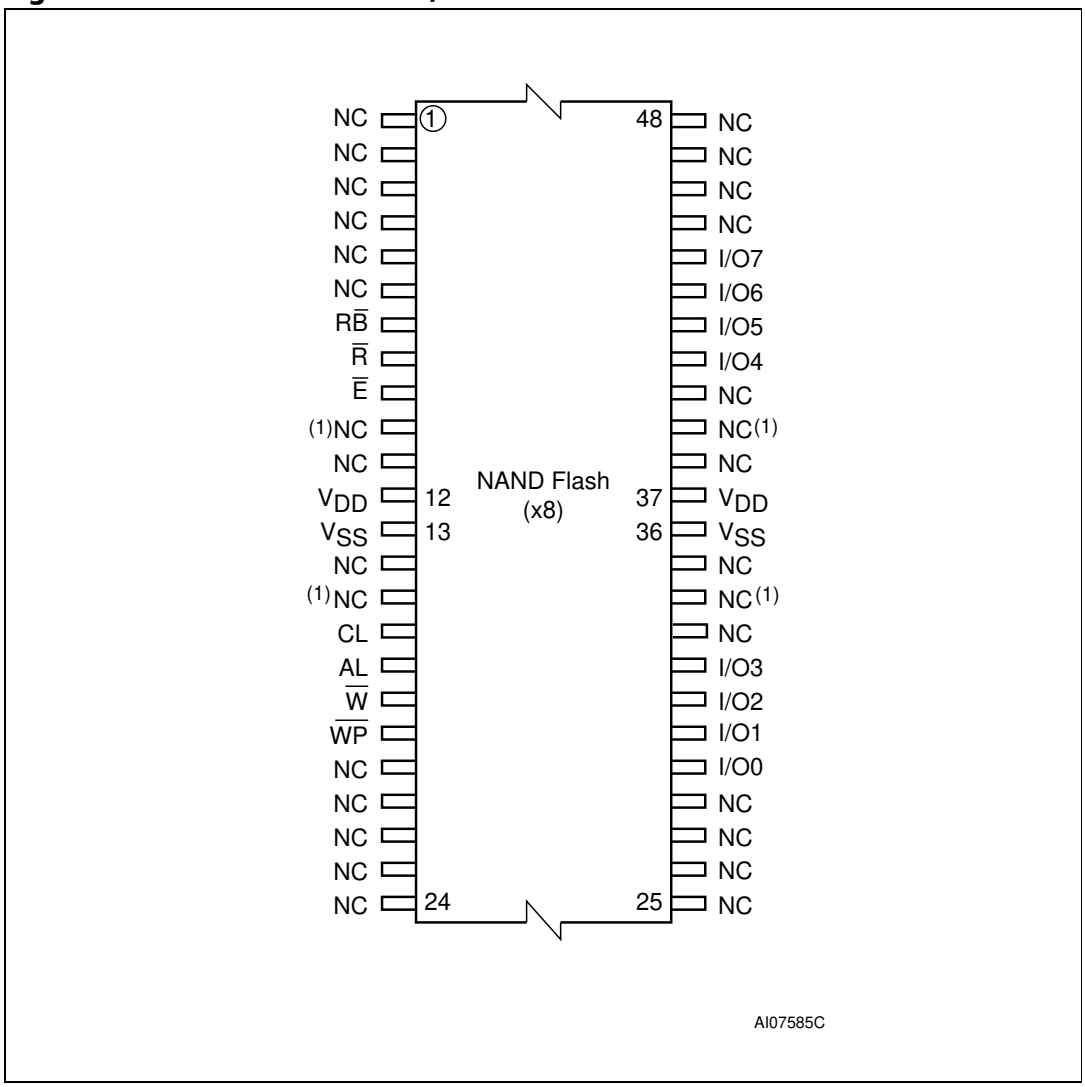
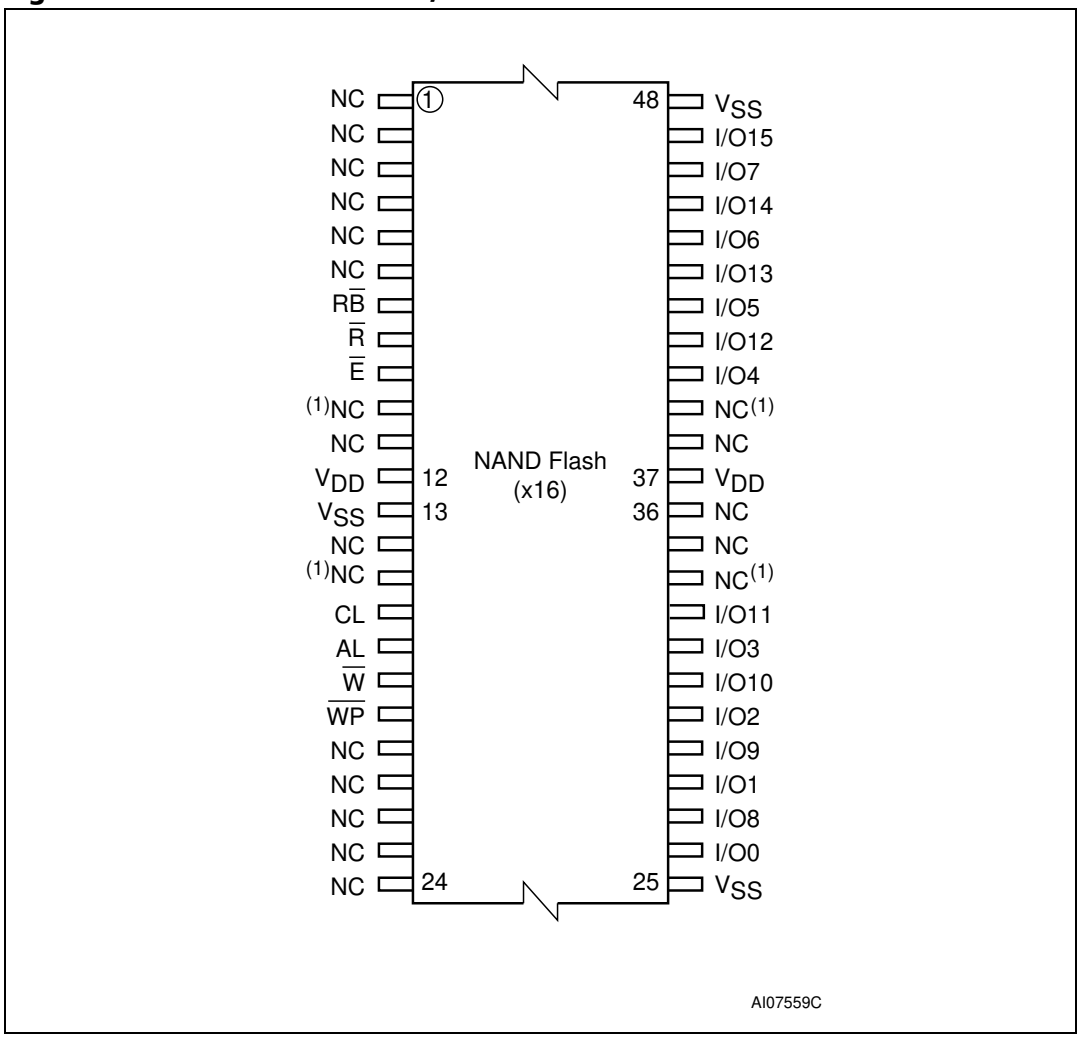


Figure 3. TSOP48 connections, x8 devices



1. This pin is DU in the USOP48 package

Figure 4. TSOP48 connections, x16 devices



1. This pin is DU in the USOP48 package.

Figure 5. VFBGA55 connections, x8 devices (top view through package)

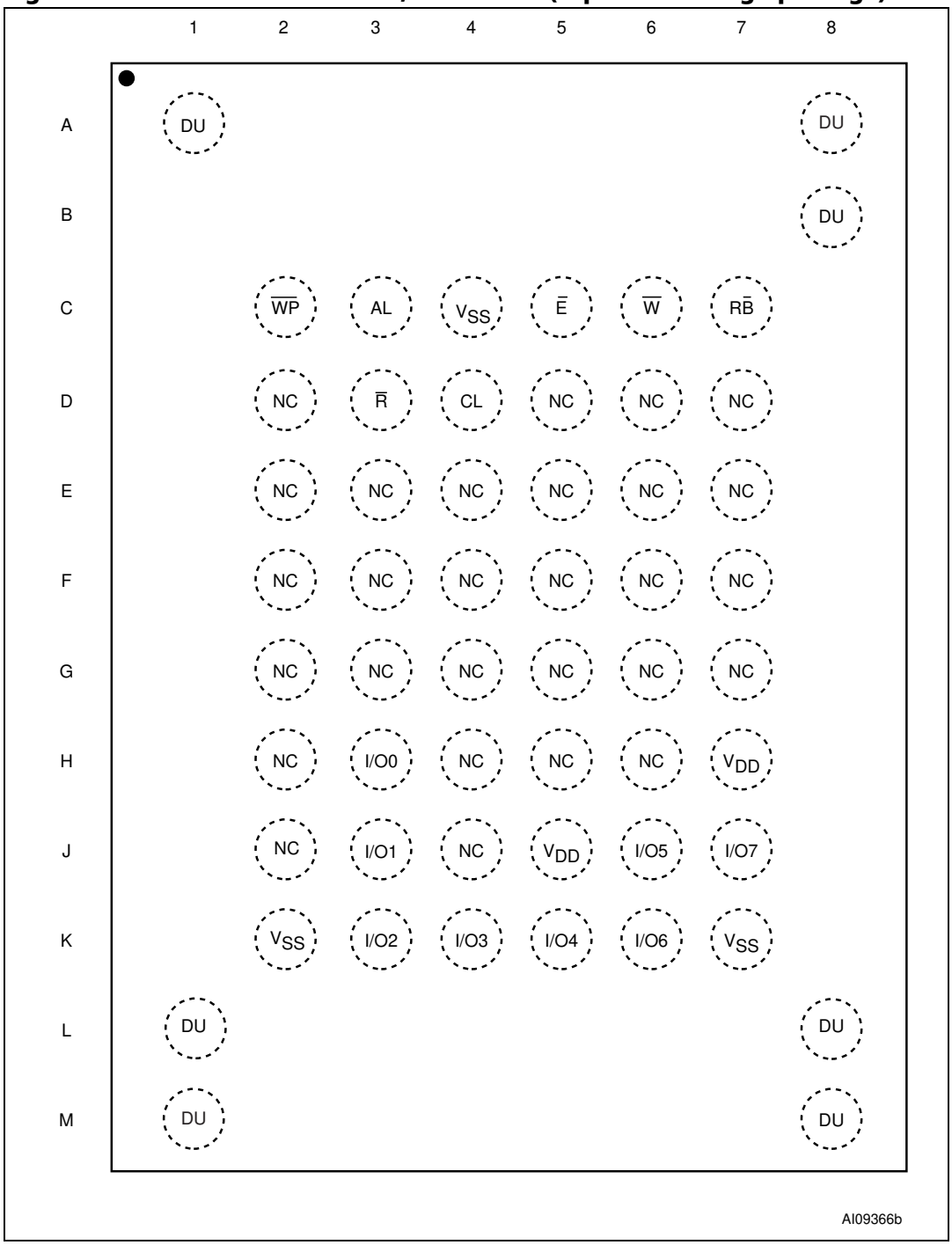
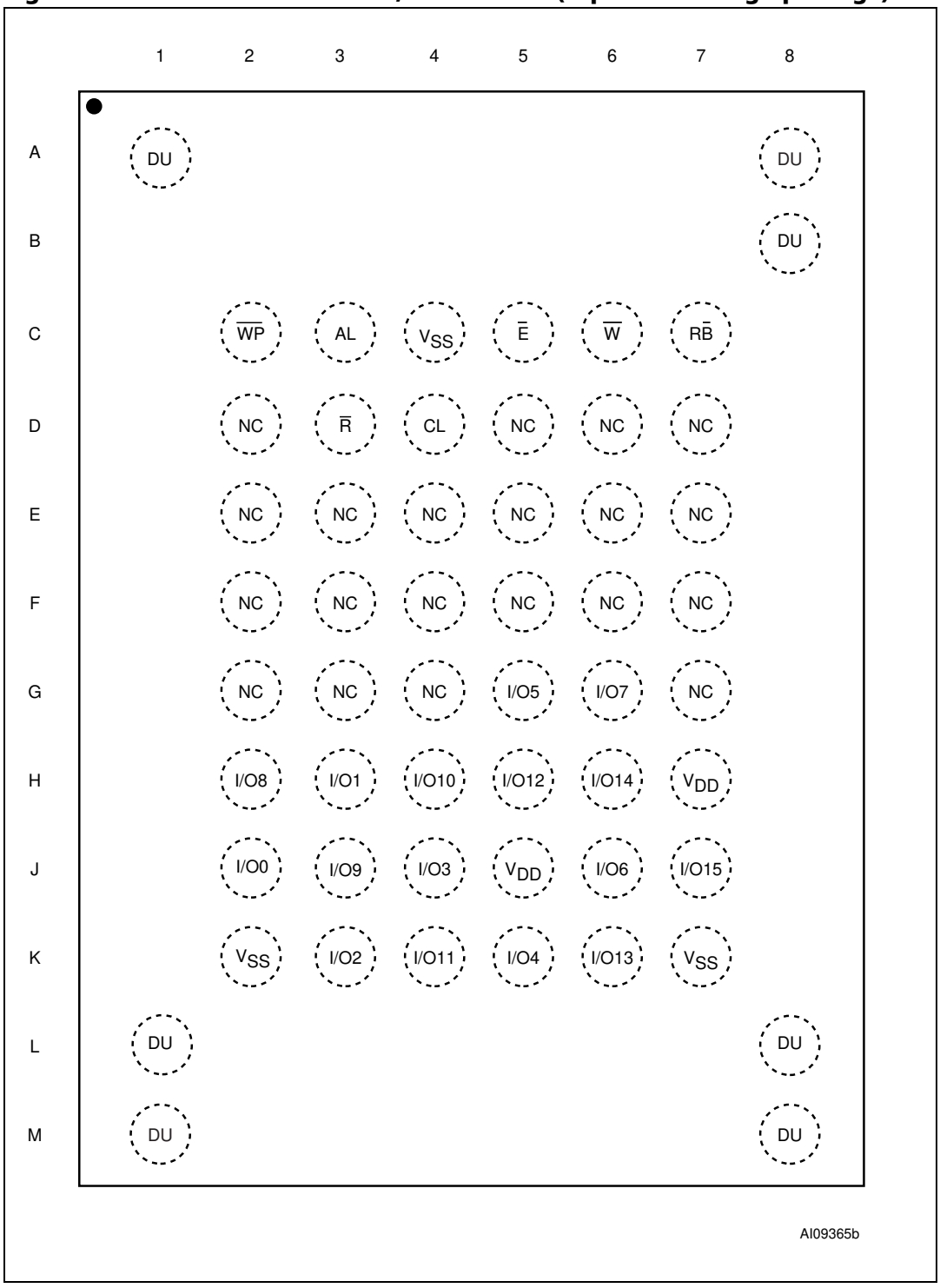


Figure 6. VFBGA55 connections, x16 devices (top view through package)



2 Memory array organization

The memory array comprises NAND structures where 16 cells are connected in series.

The memory array is organized in blocks where each block contains 32 pages. The array is split into two areas, the main area and the spare area. The main area of the array stores data, whereas the spare area is typically used to store error correction codes, software flags or bad block identification.

In x8 devices the pages are split into a main area with two half pages of 256 bytes each and a spare area of 16 bytes. In the x16 devices the pages are split into a 256-word main area and an 8-word spare area. Refer to *Figure 7: Memory array organization*.

2.1 Bad Blocks

The NAND flash 528 byte/ 264 word page devices may contain bad blocks, that is blocks that contain one or more invalid bits whose reliability is not guaranteed. Additional bad blocks may develop during the lifetime of the device.

The bad block information is written prior to shipping (refer to *Section 2.1: Bad Blocks* for more details).

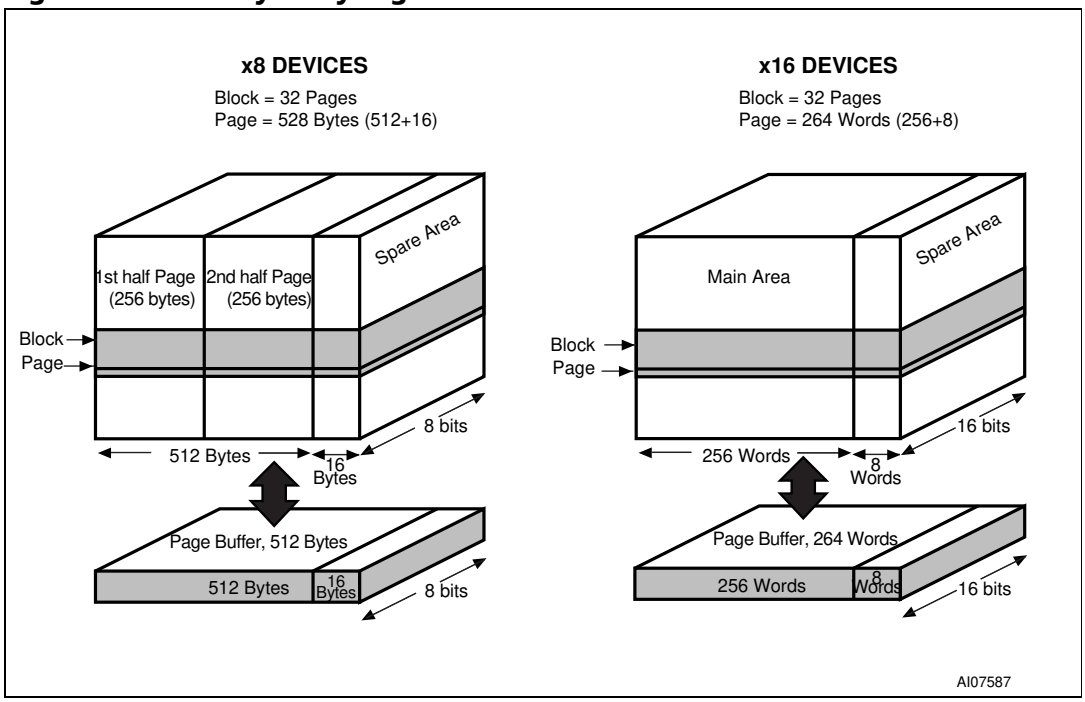
Table 4 shows the minimum number of valid blocks in each device. The values shown include both the bad blocks that are present when the device is shipped and the bad blocks that could develop later on.

These blocks need to be managed using bad blocks management, block replacement or error correction codes (refer to *Section 7: Software algorithms*).

Table 4. Valid blocks

Density of device	Minimum	Maximum
256 Mbits	2008	2048
128 Mbits	1004	1024

Figure 7. Memory array organization



3 Signal descriptions

See *Figure 1: Logic diagram* and *Table 3: Signal names* for a brief overview of the signals connected to this device.

3.1 Inputs/outputs (I/O0-I/O7)

Input/Outputs 0 to 7 input the selected address, output the data during a read operation or input a command or data during a write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

3.2 Inputs/outputs (I/O8-I/O15)

Input/outputs 8 to 15 are only available in x16 devices. They output the data during a read operation or input data during a write operation. Command and address inputs only require I/O0 to I/O7.

The inputs are latched on the rising edge of Write Enable. I/O8-I/O15 are left floating when the device is deselected or the outputs are disabled.

3.3 Address Latch Enable (AL)

Address Latch Enable activates the latching of the address inputs in the command interface. When AL is high, the inputs are latched on the rising edge of Write Enable.

3.4 Command Latch Enable (CL)

The Command Latch Enable activates the latching of the command inputs in the command interface. When CL is high, the inputs are latched on the rising edge of Write Enable.

3.5 Chip Enable ($\overline{E}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and read circuitry. When Chip Enable is low, V_{IL}, the device is selected. If Chip Enable goes High (V_{IH}) while the device is busy, the device remains selected and does not go into standby mode.

3.6 Read Enable ($\overline{R}$)

Read Enable, $\overline{R}$, controls the sequential data output during read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

3.7 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 10µs (min) is required before the Command Interface is ready to accept a command. It is recommended to keep Write Enable high during the recovery time.

3.8 Write Protect ($\overline{WP}$)

The Write Protect pin is an input that provides hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

3.9 Ready/Busy ($R\overline{B}$)

The Ready/Busy output, $R\overline{B}$, is an open-drain output that can be used to identify if the P/E/R controller is currently active.

When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low then indicates that one or more of the memories is busy.

Refer to the *Section 10.1: Ready/busy signal electrical characteristics* for details on how to calculate the value of the pull-up resistor.

3.10 V_{DD} supply voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

An internal voltage detector disables all functions whenever V_{DD} is below the V_{LKO} threshold (see paragraph *Figure 35: Data protection*) to protect the device from any involuntary program/erase operations durings power-transitions.

Each device in a system should have V_{DD} decoupled with a 0.1 µF capacitor. The PCB track widths should be sufficient to carry the required program and erase currents

3.11 V_{SS} ground

Ground, V_{SS}, is the reference for the power supply. It must be connected to the system ground.

4 Bus operations

There are six standard bus operations that control the memory. Each of these is described in this section, see *Table 5: Bus operations* for a summary.

4.1 Command input

Command input bus operations give commands to the memory. Commands are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low, and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O0 to I/O7 input commands.

See *Figure 21: Command latch AC waveforms* and *Table 14: Program, erase times and program erase endurance cycles* for details of the timings requirements.

4.2 Address input

Address input bus operations input the memory address. Three bus cycles are required to input the addresses (refer to Tables *Table 6: Address insertion, x8 devices* and *Table 7: Address insertion, x16 device*).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low, and Read Enable is High. They are latched on the rising edge of the Write Enable signal. Only I/O0 to I/O7 input addresses.

See *Figure 22: Address latch AC waveforms* and *Table 14: Program, erase times and program erase endurance cycles* for details of the timings requirements.

4.3 Data input

Data input bus operations input the data to be programmed.

Data is accepted only when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low, and Read Enable is High. The data is latched on the rising edge of the Write Enable signal and is input sequentially using the Write Enable signal.

See *Figure 23: Data input latch AC waveforms* and *Table 14: Program, erase times and program erase endurance cycles* and *Table 21: AC characteristics for operations* for details of the timings requirements.

4.4 Data output

Data output bus operations read the data in the memory array, the status register, the electronic signature, and the serial number.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low.

The data is output sequentially using the Read Enable signal.

See *Figure 24: Sequential data output after read AC waveforms* and *Table 21: AC characteristics for operations* for details of the timings requirements.

4.5 Write protect

Write protect bus operations protect the memory against program or erase operations. When the Write Protect signal is Low the device does not accept program or erase operations, therefore, the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection, even during power-up.

4.6 Standby

When Chip Enable is High the memory enters standby mode: the device is deselected, outputs are disabled and power consumption is reduced.

Table 5. Bus operations

Bus operation	E	AL	CL	R	W	WP	I/O0 - I/O7	I/O8 - I/O15(1)
Command input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X(2)	Command	X
Address input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address	X
Data input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	X	Data input	Data input
Data output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data output	Data output
Write protect	X	X	X	X	X	V_{IL}	X	X
Standby	V_{IH}	X	X	X	X	X	X	X

1. Only for x16 devices.
2. $\overline{WP}$ must be V_{IH} when issuing a program or erase command.

Table 6. Address insertion, x8 devices(1) (2)

Bus Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	A16	A15	A14	A13	A12	A11	A10	A9
3rd	A24	A23	A22	A21	A20	A19	A18	A17

1. A8 is set Low or High by the 00h or 01h command (see *Section 6.1: Pointer operations*)
2. Any additional address input cycles are ignored.

Table 7. Address insertion, x16 device(1) (2) (3)

Bus Cycle	I/O8-I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	X	A7	A6	A5	A4	A3	A2	A1	A0
2nd	X	A16	A15	A14	A13	A12	A11	A10	A9
3rd	X	A24	A23	A22	A21	A20	A19	A18	A17

1. A8 is 'don't care' in x16 devices.
2. Any additional address input cycles are ignored.
3. The 01h command is not used in x16 devices

Table 8. Address definitions

Address	Definition
A0 - A7	Column address
A9 - A26	Page address
A9 - A13	Address in block
A14 - A26	Block address
A8	A8 is set Low or High by the 00h or 01h command, and is 'don't care' in x16 devices

5 Command set

All bus write operations to the device are interpreted by the command interface. The commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is high. Device operations are selected by writing specific commands to the command register. The two-step command sequences for program and erase operations are imposed to maximize data security.

The commands are summarized in *Table 9*.

Table 9. Commands

Command	Bus write operations(1) (2)			Command accepted during busy
	1st cycle	2nd cycle	3rd cycle	
Read A	00h	-	-	
Read B	01h(2)	-	-	
Read C	50h	-	-	
Read Electronic Signature	90h	-	-	
Read Status Register	70h	-	-	Yes
Page Program	80h	10h	-	
Copy Back Program	00h	8Ah	10h	
Block Erase	60h	D0h	-	
Reset	FFh	-	-	Yes

1. The bus cycles are only shown for issuing the codes. The cycles required to input the addresses or input/output data are not shown.
2. Any undefined command sequence is ignored by the device.

6 Device operations

6.1 Pointer operations

As the NAND flash memories contain two different areas for x16 devices and three different areas for x8 devices (see *Figure 8*) the read command codes (00h, 01h, 50h) act as pointers to the different areas of the memory array (they select the most significant column address).

The Read A and Read B commands act as pointers to the main memory area. Their use depends on the bus width of the device.

- In x16 devices the Read A command (00h) sets the pointer to Area A (the whole of the main area), that is words 0 to 255.
- In x8 devices the Read A command (00h) sets the pointer to Area A (the first half of the main area), that is bytes 0 to 255, and the Read B command (01h) sets the pointer to Area B (the second half of the main area), that is bytes 256 to 511.

In both the x8 and x16 devices the Read C command (50h) acts as a pointer to Area C (the spare memory area), that is bytes 512 to 527 or words 256 to 263.

Once the Read A and Read C commands have been issued the pointer remains in the respective areas until another pointer code is issued. However, the Read B command is effective for only one operation, once an operation has been executed in Area B the pointer returns automatically to Area A.

The pointer operations can also be used before a program operation, that is the appropriate code (00h, 01h or 50h) can be issued before the program command 80h is issued (see *Figure 9: Pointer operations for programming*).

Figure 8. Pointer operations

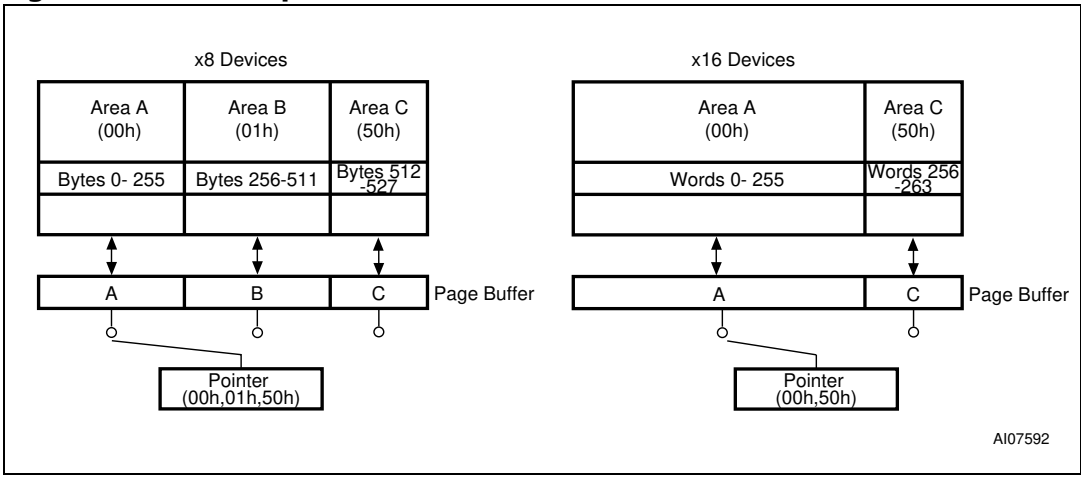
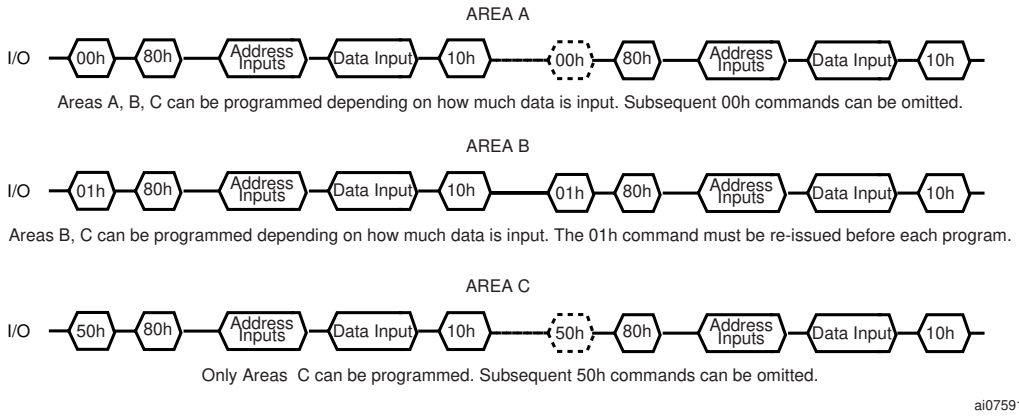


Figure 9. Pointer operations for programming



6.2 Read memory array

Each operation to read the memory area starts with a pointer operation as shown in the *Section 6.1: Pointer operations*. Once the area (main or spare) has been selected using the Read A, Read B or Read C commands three bus cycles are required to input the address of the data to be read.

The device defaults to Read A mode after power-up or a reset operation.

When reading the following spare area addresses:

- A0 to A3 (x8 devices)
- A0 to A2 (x16 devices)

set the start address of the spare area, while the following addresses are ignored:

- A4 to A7 (x8 devices)
- A3 to A7 (x16 devices)

Once the Read A or Read C commands have been issued they do not need to be reissued for subsequent read operations as the pointer remains in the respective area. However, the Read B command is effective for only one operation; once an operation has been executed in Area B the pointer returns automatically to Area A. Another Read B command is required to start another read operation in Area B.

Once a read command is issued two types of operations are available: random read and page read.

- Random read

  Each time the command is issued the first read is random read.
- Page read

  After the random read access the page data is transferred to the page buffer in a time of t_{WHBH} (refer to *Table 21: AC characteristics for operations* for the value). Once the transfer is complete the Ready/Busy signal goes High. The data can then be read out sequentially (from the selected column address to the last column address) by pulsing the Read Enable signal.
- Sequential row read
  After the data in last column of the page is output, if the Read Enable signal is pulsed

and Chip Enable remains Low, then the next page is automatically loaded into the page buffer and the read operation continues. A sequential row read operation can only be used to read within a block. If the block changes a new read command must be issued. Refer to *Figure 12: Sequential row read operations* and *Figure 13: Sequential row read block diagrams* for details about sequential row read operations. To terminate a sequential row read operation, set to High the Chip Enable signal for more than t_{EHEL}. Sequential row read is not available when the Chip Enable don't care option is enabled.

Figure 10. Read (A, B, C) operations

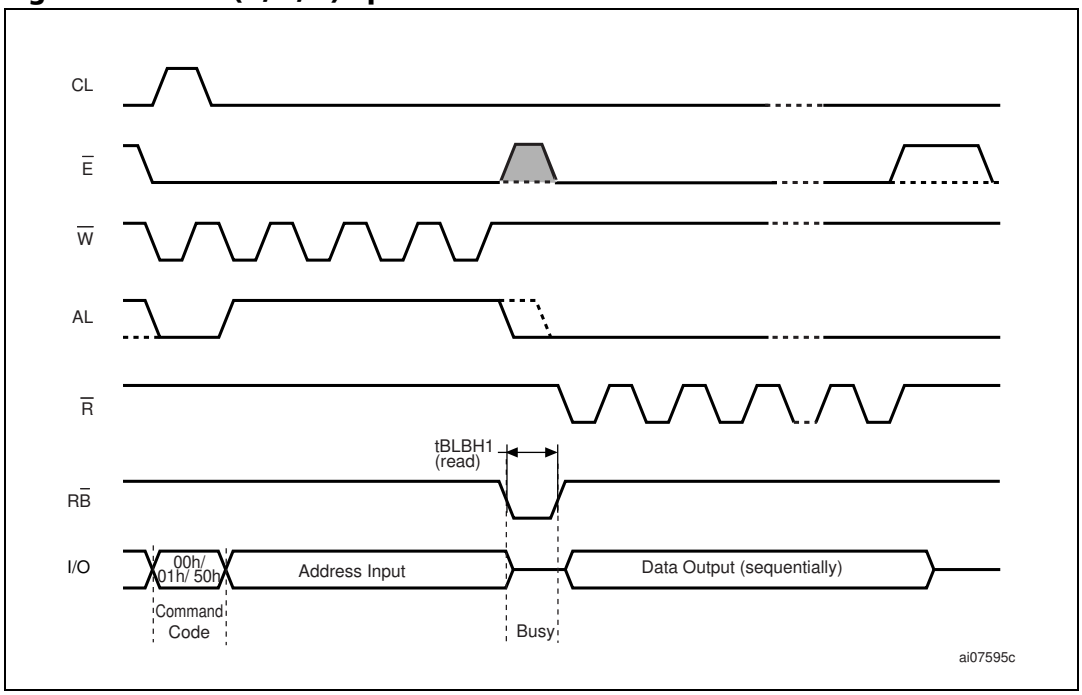
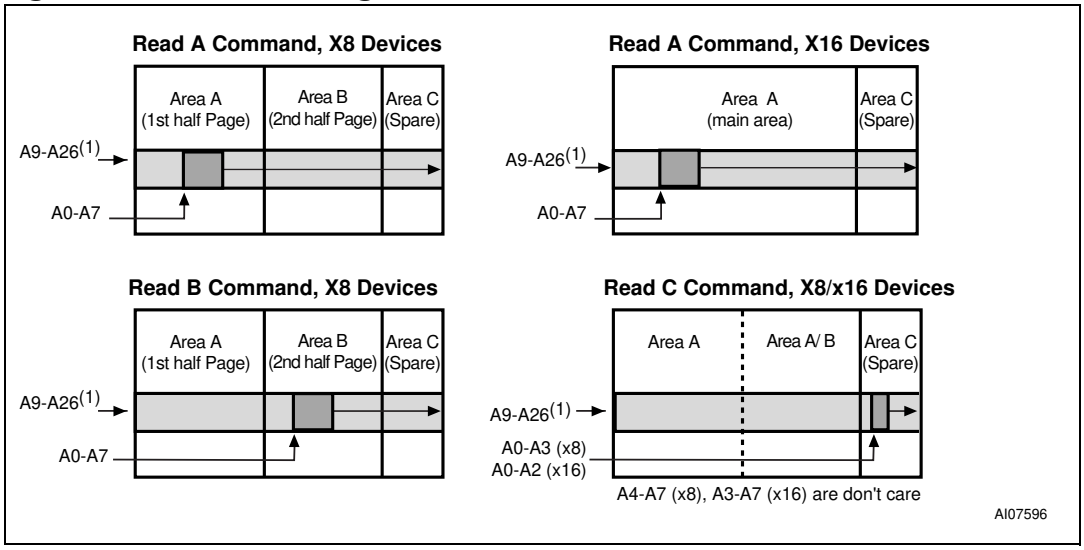


Figure 11. Read block diagrams



1. The highest address depends on the device density.

Figure 12. Sequential row read operations

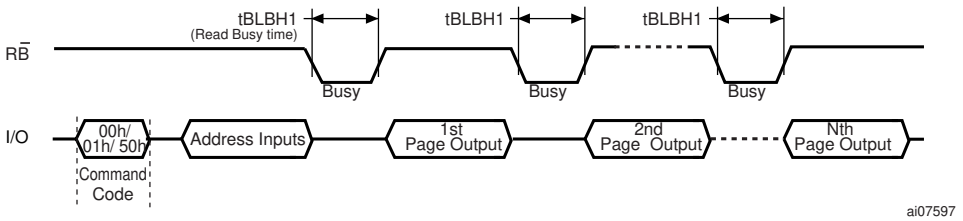


Figure 13. Sequential row read block diagrams