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NAND128-A, NAND256-A
NAND512-A, NAND01G-A

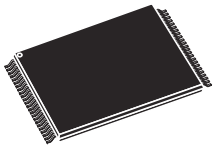
128 Mbit, 256 Mbit, 512 Mbit, 1 Gbit (x8/x16)
528 Byte/264 Word Page, 1.8V/3V, NAND Flash Memories

PRELIMINARY DATA

FEATURES SUMMARY

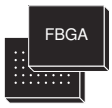
- HIGH DENSITY NAND FLASH MEMORIES
  - Up to 1 Gbit memory array
  - Up to 32 Mbit spare area
  - Cost effective solutions for mass storage applications
- NAND INTERFACE
  - x8 or x16 bus width
  - Multiplexed Address/ Data
  - Pinout compatibility for all densities
- SUPPLY VOLTAGE
  - 1.8V device: V_{DD} = 1.7 to 1.95V
  - 3.0V device: V_{DD} = 2.7 to 3.6V
- PAGE SIZE
  - x8 device: (512 + 16 spare) Bytes
  - x16 device: (256 + 8 spare) Words
- BLOCK SIZE
  - x8 device: (16K + 512 spare) Bytes
  - x16 device: (8K + 256 spare) Words
- PAGE READ / PROGRAM
  - Random access: 12µs (max)
  - Sequential access: 50ns (min)
  - Page program time: 200µs (typ)
- COPY BACK PROGRAM MODE
  - Fast page copy without external buffering
- FAST BLOCK ERASE
  - Block erase time: 2ms (Typ)
- STATUS REGISTER
- ELECTRONIC SIGNATURE
- CHIP ENABLE 'DON'T CARE' OPTION
  - Simple interface with microcontroller
- AUTOMATIC PAGE 0 READ AT POWER-UP OPTION
  - Boot from NAND support
  - Automatic Memory Download
- SERIAL NUMBER OPTION

Figure 1. Packages



TSOP48 12 x 20mm

WSOP48 12 x 17 x 0.65mm



VFBGA55 8 x 10 x 1mm
TFBGA55 8 x 10 x 1.2mm
VFBGA63 8.5 x 15 x 1mm
TFBGA63 8.5 x 15 x 1.2mm

- HARDWARE DATA PROTECTION
  - Program/Erase locked during Power transitions
- DATA INTEGRITY
  - 100,000 Program/Erase cycles
  - 10 years Data Retention
- DEVELOPMENT TOOLS
  - Error Correction Code software and hardware models
  - Bad Blocks Management and Wear Leveling algorithms
  - PC Demo board with simulation software
  - File System OS Native reference software
  - Hardware simulation models

Table 1. Product List

Reference	Part Number
NAND128-A	NAND128R3A
	NAND128W3A
	NAND1282R4A
	NAND128W4A
NAND256-A	NAND256R3A
	NAND256W3A
	NAND256R4A
	NAND256W4A
NAND512-A	NAND512R3A
	NAND512W3A
	NAND512R4A
	NAND512W4A
NAND01G-A	NAND01GR3A
	NAND01GW3A
	NAND01GR4A
	NAND01GW4A

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SUMMARY DESCRIPTION

The NAND Flash 528 Byte/ 264 Word Page is a family of non-volatile Flash memories that uses NAND cell technology. The devices range from 128Mbits to 1Gbit and operate with either a 1.8V or 3V voltage supply. The size of a Page is either 528 Bytes (512 + 16 spare) or 264 Words (256 + 8 spare) depending on whether the device has a x8 or x16 bus width.

The address lines are multiplexed with the Data Input/Output signals on a multiplexed x8 or x16 Input/Output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased over 100,000 cycles. To extend the lifetime of NAND Flash devices it is strongly recommended to implement an Error Correction Code (ECC). A Write Protect pin is available to give a hardware protection against program and erase operations.

The devices feature an open-drain Ready/Busy output that can be used to identify if the Program/ Erase/Read (P/E/R) Controller is currently active. The use of an open-drain output allows the Ready/ Busy pins from several memories to be connected to a single pull-up resistor.

A Copy Back command is available to optimize the management of defective blocks. When a Page Program operation fails, the data can be programmed in another page without having to resend the data to be programmed.

The devices are available in the following packages:

- TSOP48 12 x 20mm for all products
- WSOP48 12 x 17 x 0.65mm for 128Mb, 256Mb and 512Mb products
- VFBGA55 (8 x 10 x 1mm, 6 x 8 ball array, 0.8mm pitch) for 128Mb and 256Mb products
- TFBGA55 (8 x 10 x 1.2mm, 6 x 8 ball array, 0.8mm pitch) for 512Mb Dual Die product
- VFBGA63 (8.5 x 15 x 1mm, 6 x 8 ball array, 0.8mm pitch) for the 512Mb product
- TFBGA63 (8.5 x 15 x 1.2mm, 6 x 8 ball array, 0.8mm pitch) for the 1Gb Dual Die product

Three options are available for the NAND Flash family:

- Automatic Page 0 Read after Power-up, which allows the microcontroller to directly download the boot code from page 0.
- Chip Enable Don't Care, which allows code to be directly downloaded by a microcontroller, as Chip Enable transitions during the latency time do not stop the read operation.
- A Serial Number, which allows each device to be uniquely identified. The Serial Number options is subject to an NDA (Non Disclosure Agreement) and so not described in the datasheet. For more details of this option contact your nearest ST Sales office.

For information on how to order these options refer to Table 28., Ordering Information Scheme. Devices are shipped from the factory with Block 0 always valid and the memory content bits, in valid blocks, erased to '1'.

See Table 2., Product Description, for all the devices available in the family.

Table 2. Product Description

Reference	Part Number	Density	Bus Width	Page Size	Block Size	Memory Array	Operating Voltage	Timings				Package
								Random Access Max	Sequential Access Min	Page Program Typical	Block Erase Typical	
NAND128-A	NAND128R3A	128Mbit	x8	512+16 Bytes	16K+512 Bytes	32 Pages x 1024 Blocks	1.7 to 1.95V	10µs	60ns	200µs	2ms	TSOP48 WSOP48 VFBGA55
	NAND128W3A						2.7 to 3.6V	10µs	50ns	200µs		
	NAND128R4A		x16	256+8 Words	8K+256 Words		1.7 to 1.95V	10µs	60ns	200µs		
	NAND128W4A						2.7 to 3.6V	10µs	50ns	200µs		
NAND256-A	NAND256R3A	256Mbit	x8	512+16 Bytes	16K+512 Bytes	32 Pages x 2048 Blocks	1.7 to 1.95V	10µs	60ns	200µs	2ms	TSOP48 WSOP48 VFBGA55
	NAND256W3A						2.7 to 3.6V	10µs	50ns	200µs		
	NAND256R4A		x16	256+8 Words	8K+256 Words		1.7to 1.95V	10µs	60ns	200µs		
	NAND256W4A						2.7 to 3.6V	10µs	50ns	200µs		
NAND512-A	NAND512R3A	512Mbit	x8	512+16 Bytes	16K+512 Bytes	32 Pages x 4096 Blocks	1.7to 1.95V	10µs	60ns	200µs	2ms	TFBGA55
	NAND512W3A						2.7 to 3.6V	10µs	50ns	200µs		
	NAND512R4A		x16	256+8 Words	8K+256 Words		1.7 to 1.95V	10µs	60ns	200µs		
	NAND512W4A						2.7 to 3.6V	10µs	50ns	200µs		
NAND512-A	NAND512R3A	512Mbit	x8	512+16 Bytes	16K+512 Bytes	32 Pages x 4096 Blocks	1.7to 1.95V	15µs	60ns	200µs	2ms	TSOP48 WSOP48 VFBGA63
	NAND512W3A						2.7 to 3.6V	12µs	50ns	200µs		
	NAND512R4A		x16	256+8 Words	8K+256 Words		1.7 to 1.95V	15µs	60ns	200µs		
	NAND512W4A						2.7 to 3.6V	12µs	50ns	200µs		
NAND01G-A	NAND01GR3A	1Gbit	x8	512+16 Bytes	16K+512 Bytes	32 Pages x 8192 Blocks	1.7 to 1.95V	15µs	60ns	200µs	2ms	TSOP48 TFBGA63
	NAND01GW3A						2.7 to 3.6V	12µs	50ns	200µs		
	NAND01GR4A		x16	256+8 Words	8K+256 Words		1.7 to 1.95V	15µs	60ns	200µs		
	NAND01GW4A						2.7 to 3.6V	12µs	50ns	200µs		

Figure 2. Logic Diagram

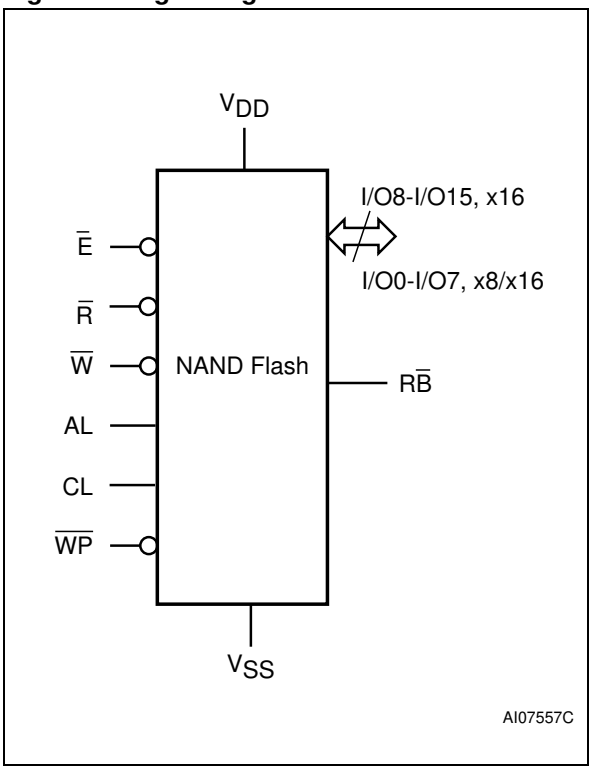


Table 3. Signal Names

I/O8-15	Data Input/Outputs for x16 devices
I/O0-7	Data Input/Outputs, Address Inputs, or Command Inputs for x8 and x16 devices
AL	Address Latch Enable
CL	Command Latch Enable
$\overline{E}$	Chip Enable
$\overline{R}$	Read Enable
$R\overline{B}$	Ready/Busy (open-drain output)
$\overline{W}$	Write Enable
$\overline{WP}$	Write Protect
V_{DD}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally
DU	Do Not Use

Figure 3. Logic Block Diagram

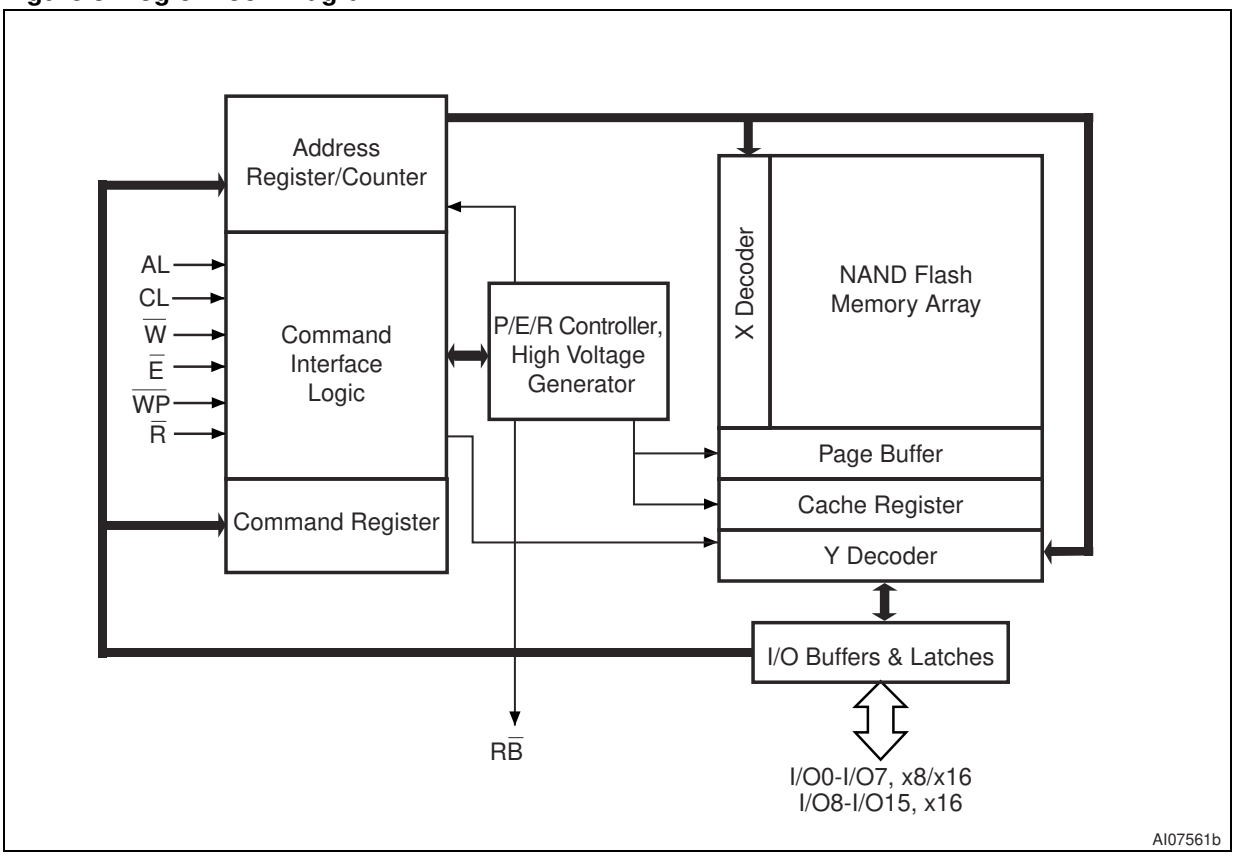


Figure 4. TSOP48 and WSOP48 Connections, x8 devices

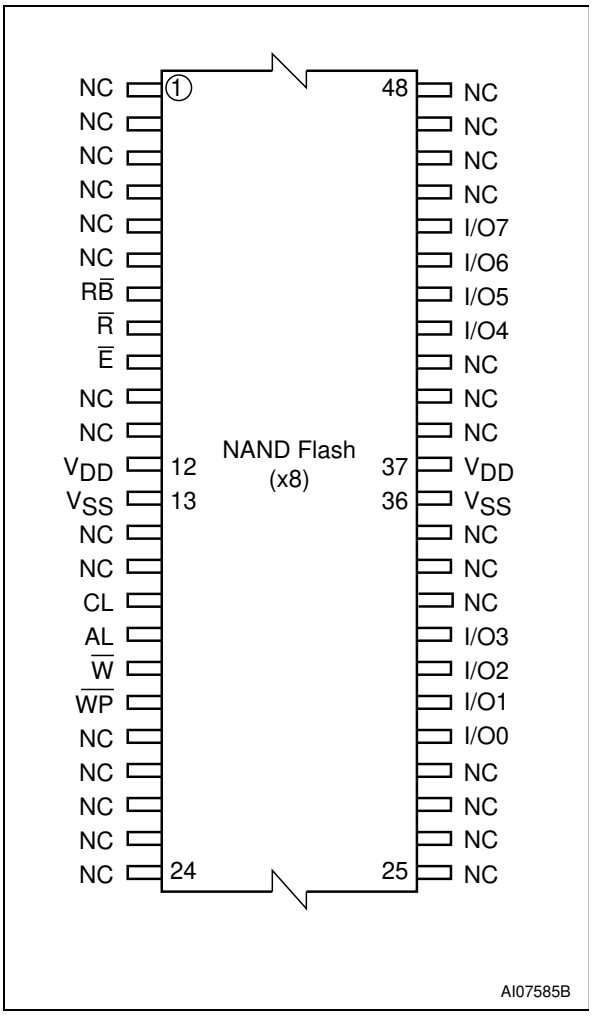


Figure 5. TSOP48 and WSOP48 Connections, x16 devices

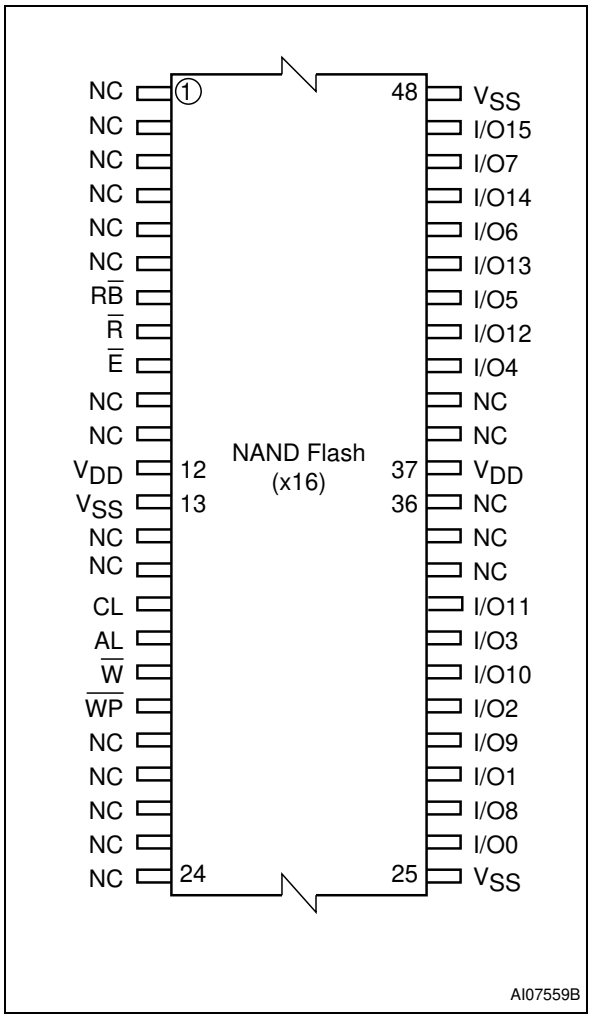


Figure 6. FBGA55 Connections, x8 devices (Top view through package)

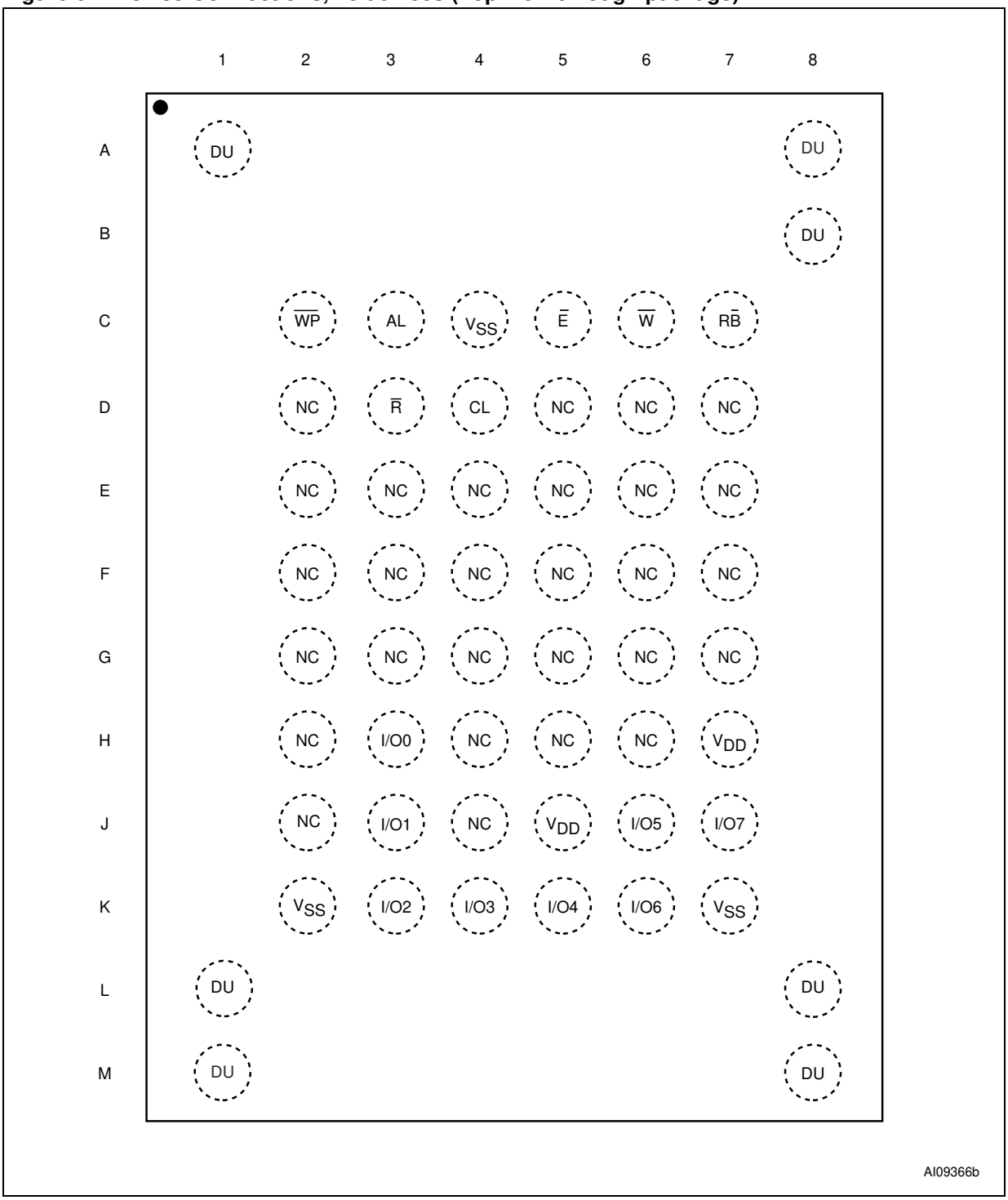


Figure 7. FBGA55 Connections, x16 devices (Top view through package)

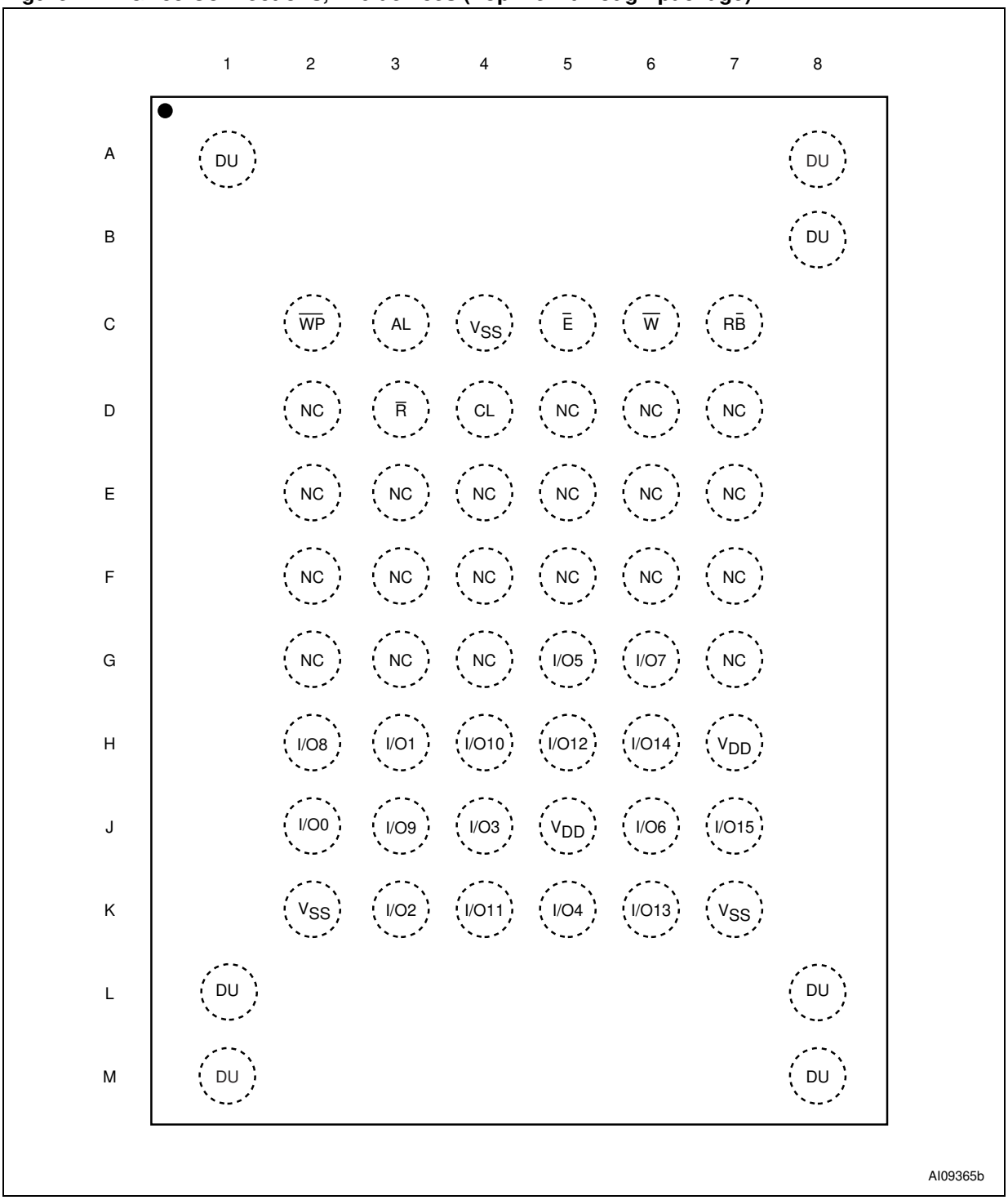


Figure 8. FBGA63 Connections, x8 devices (Top view through package)

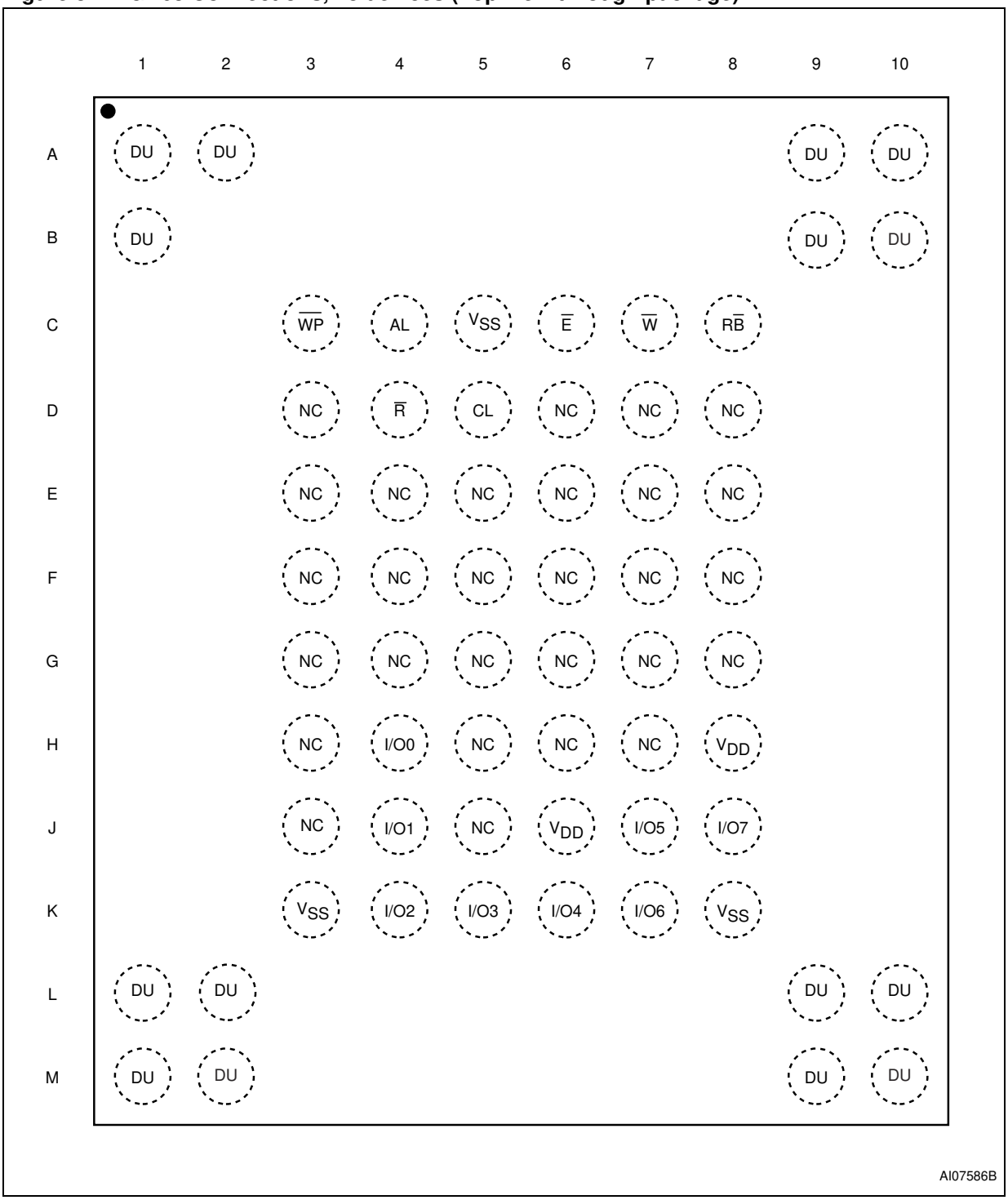
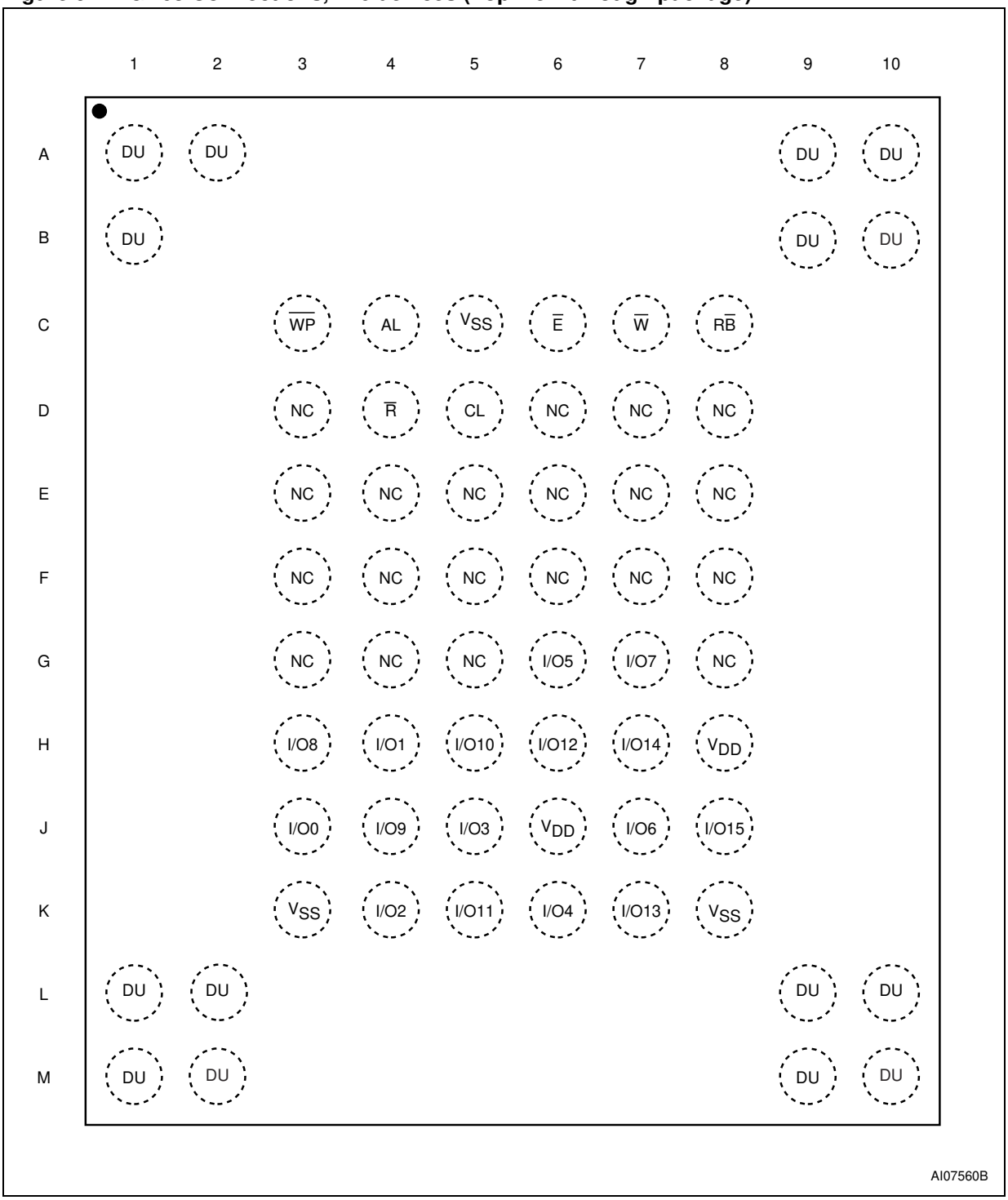


Figure 9. FBGA63 Connections, x16 devices (Top view through package)



MEMORY ARRAY ORGANIZATION

The memory array is made up of NAND structures where 16 cells are connected in series.

The memory array is organized in blocks where each block contains 32 pages. The array is split into two areas, the main area and the spare area. The main area of the array is used to store data whereas the spare area is typically used to store Error correction Codes, software flags or Bad Block identification.

In x8 devices the pages are split into a main area with two half pages of 256 Bytes each and a spare area of 16 Bytes. In the x16 devices the pages are split into a 256 Word main area and an 8 Word spare area. Refer to Figure 10., Memory Array Organization.

Bad Blocks

The NAND Flash 528 Byte/ 264 Word Page devices may contain Bad Blocks, that is blocks that contain one or more invalid bits whose reliability is not guaranteed. Additional Bad Blocks may develop during the lifetime of the device.

The Bad Block Information is written prior to shipping (refer to Bad Block Management section for more details).

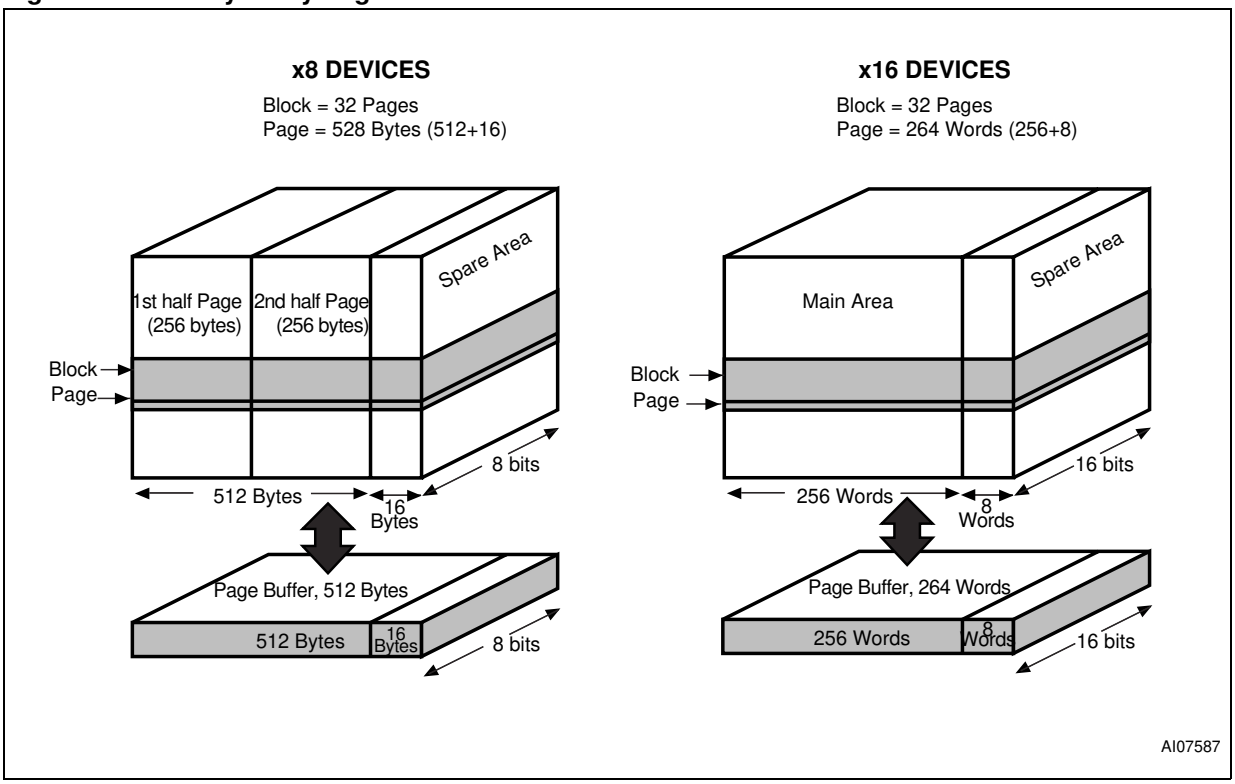
Table 4. shows the minimum number of valid blocks in each device. The values shown include both the Bad Blocks that are present when the device is shipped and the Bad Blocks that could develop later on.

These blocks need to be managed using Bad Blocks Management, Block Replacement or Error Correction Codes (refer to SOFTWARE ALGORITHMS section).

Table 4. Valid Blocks

Density of Device	Min	Max
1Gbit	8032	8192
512Mbits	4016	4096
256Mbits	2008	2048
128Mbits	1004	1024

Figure 10. Memory Array Organization



SIGNAL DESCRIPTIONS

See Figure 2., Logic Diagram, and Table 3., Signal Names, for a brief overview of the signals connected to this device.

Inputs/Outputs (I/O0-I/O7). Input/Outputs 0 to 7 are used to input the selected address, output the data during a Read operation or input a command or data during a Write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

Inputs/Outputs (I/O8-I/O15). Input/Outputs 8 to 15 are only available in x16 devices. They are used to output the data during a Read operation or input data during a Write operation. Command and Address Inputs only require I/O0 to I/O7.

The inputs are latched on the rising edge of Write Enable. I/O8-I/O15 are left floating when the device is deselected or the outputs are disabled.

Address Latch Enable (AL). The Address Latch Enable activates the latching of the Address inputs in the Command Interface. When AL is high, the inputs are latched on the rising edge of Write Enable.

Command Latch Enable (CL). The Command Latch Enable activates the latching of the Command inputs in the Command Interface. When CL is high, the inputs are latched on the rising edge of Write Enable.

Chip Enable ($\overline{E}$). The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is low, V_{IL}, the device is selected. If Chip Enable goes high, v_{IH}, while the device is busy, the device remains selected and does not go into standby mode.

When the device is executing a Sequential Row Read operation, Chip Enable must be held low (from the second page read onwards) during the time that the device is busy (t_{BLBH1}). If Chip Enable goes high during t_{BLBH1} the operation is aborted.

Read Enable ($\overline{R}$). The Read Enable, $\overline{R}$, controls the sequential data output during Read operations. Data is valid t_{RLQV} after the falling edge of R. The falling edge of R also increments the internal column address counter by one.

Write Enable ($\overline{W}$). The Write Enable input, $\overline{W}$, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 1µs (min) is required before the Command Interface is ready to accept a command. It is recommended to keep Write Enable high during the recovery time.

Write Protect ($\overline{WP}$). The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

Ready/Busy ($\overline{RB}$). The Ready/Busy output, $\overline{RB}$, is an open-drain output that can be used to identify if the P/E/R Controller is currently active.

When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

Refer to the Ready/Busy Signal Electrical Characteristics section for details on how to calculate the value of the pull-up resistor.

V_{DD} Supply Voltage. V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

An internal voltage detector disables all functions whenever V_{DD} is below 2.5V (for 3V devices) or 1.5V (for 1.8V devices) to protect the device from any involuntary program/erase during power-transitions.

Each device in a system should have V_{DD} decoupled with a 0.1µF capacitor. The PCB track widths should be sufficient to carry the required program and erase currents

V_{SS} Ground. Ground, V_{SS}, is the reference for the power supply. It must be connected to the system ground.

BUS OPERATIONS

There are six standard bus operations that control the memory. Each of these is described in this section, see Table 5., Bus Operations, for a summary.

Command Input

Command Input bus operations are used to give commands to the memory. Command are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O0 to I/O7 are used to input commands.

See Figure 25. and Table 20. for details of the timings requirements.

Address Input

Address Input bus operations are used to input the memory address. Three bus cycles are required to input the addresses for the 128Mb and 256Mb devices and four bus cycles are required to input the addresses for the 512Mb and 1Gb devices (refer to Tables 6 and 7, Address Insertion).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal. Only I/O0 to I/O7 are used to input addresses.

See Figure 26. and Table 20. for details of the timings requirements.

Data Input

Data Input bus operations are used to input the data to be programmed.

Data is accepted only when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low and Read Enable is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

See Figure 27. and Table 20. and Table 21. for details of the timings requirements.

Data Output

Data Output bus operations are used to read: the data in the memory array, the Status Register, the Electronic Signature and the Serial Number.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low.

The data is output sequentially using the Read Enable signal.

See Figure 28. and Table 21. for details of the timings requirements.

Write Protect

Write Protect bus operations are used to protect the memory against program or erase operations. When the Write Protect signal is Low the device will not accept program or erase operations and so the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection even during power-up.

Standby

When Chip Enable is High the memory enters Standby mode, the device is deselected, outputs are disabled and power consumption is reduced.

Table 5. Bus Operations

Bus Operation	$\overline{E}$	AL	CL	$\overline{R}$	$\overline{W}$	$\overline{WP}$	I/O0 - I/O7	I/O8 - I/O15(1)
Command Input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X(2)	Command	X
Address Input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address	X
Data Input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	X	Data Input	Data Input
Data Output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data Output	Data Output
Write Protect	X	X	X	X	X	V_{IL}	X	X
Standby	V_{IH}	X	X	X	X	X	X	X

Note: 1. Only for x16 devices.
2. $\overline{WP}$ must be V_{IH} when issuing a program or erase command.

Table 6. Address Insertion, x8 Devices

Bus Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	A16	A15	A14	A13	A12	A11	A10	A9
3rd	A24	A23	A22	A21	A20	A19	A18	A17
4th(4)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A26	A25

Note: 1. A8 is set Low or High by the 00h or 01h Command, see Pointer Operations section.
2. Any additional address input cycles will be ignored.
3. The 4th cycle is only required for 512Mb and 1Gb devices.

Table 7. Address Insertion, x16 Devices

Bus Cycle	I/O8-I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	X	A7	A6	A5	A4	A3	A2	A1	A0
2nd	X	A16	A15	A14	A13	A12	A11	A10	A9
3rd	X	A24	A23	A22	A21	A20	A19	A18	A17
4th(4)	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A26	A25

Note: 1. A8 is Don't Care in x16 devices.
2. Any additional address input cycles will be ignored.
3. The 01h Command is not used in x16 devices.
4. The 4th cycle is only required for 512Mb and 1Gb devices.

Table 8. Address Definitions

Address	Definition
A0 - A7	Column Address
A9 - A26	Page Address
A9 - A13	Address in Block
A14 - A26	Block Address
A8	A8 is set Low or High by the 00h or 01h Command, and is Don't Care in x16 devices

COMMAND SET

All bus write operations to the device are interpreted by the Command Interface. The Commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is high. Device operations are selected by writing specific commands to the Command Register. The two-step command sequences for program and erase operations are imposed to maximize data security.

The Commands are summarized in Table 9., Commands.

Table 9. Commands

Command	Bus Write Operations(1)			Command accepted during busy
	1st CYCLE	2nd CYCLE	3rd CYCLE	
Read A	00h	-	-	
Read B	01h(2)	-	-	
Read C	50h	-	-	
Read Electronic Signature	90h	-	-	
Read Status Register	70h	-	-	Yes
Page Program	80h	10h	-	
Copy Back Program	00h	8Ah	10h	
Block Erase	60h	D0h	-	
Reset	FFh	-	-	Yes

Note: 1. The bus cycles are only shown for issuing the codes. The cycles required to input the addresses or input/output data are not shown.
2. Any undefined command sequence will be ignored by the device.

DEVICE OPERATIONS

Pointer Operations

As the NAND Flash memories contain two different areas for x16 devices and three different areas for x8 devices (see Figure 11.) the read command codes (00h, 01h, 50h) are used to act as pointers to the different areas of the memory array (they select the most significant column address).

The Read A and Read B commands act as pointers to the main memory area. Their use depends on the bus width of the device.

- In x16 devices the Read A command (00h) sets the pointer to Area A (the whole of the main area) that is Words 0 to 255.
- In x8 devices the Read A command (00h) sets the pointer to Area A (the first half of the main area) that is Bytes 0 to 255, and the Read B command (01h) sets the pointer to Area B (the second half of the main area) that is Bytes 256 to 511.

In both the x8 and x16 devices the Read C command (50h), acts as a pointer to Area C (the spare memory area) that is Bytes 512 to 527 or Words 256 to 263.

Once the Read A and Read C commands have been issued the pointer remains in the respective areas until another pointer code is issued. However, the Read B command is effective for only one operation, once an operation has been executed in Area B the pointer returns automatically to Area A.

The pointer operations can also be used before a program operation, that is the appropriate code (00h, 01h or 50h) can be issued before the program command 80h is issued (see Figure 12.).

Figure 11. Pointer Operations

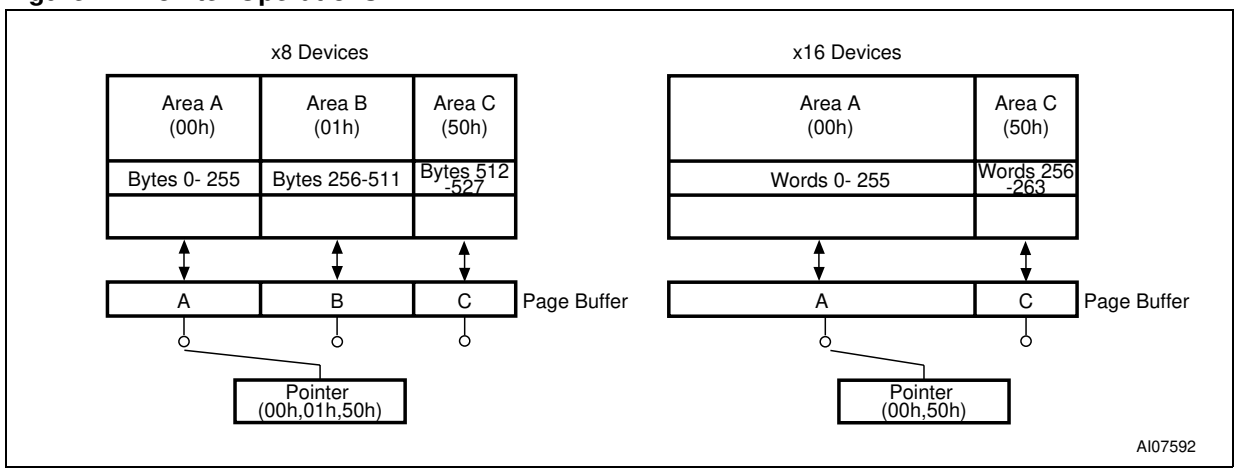
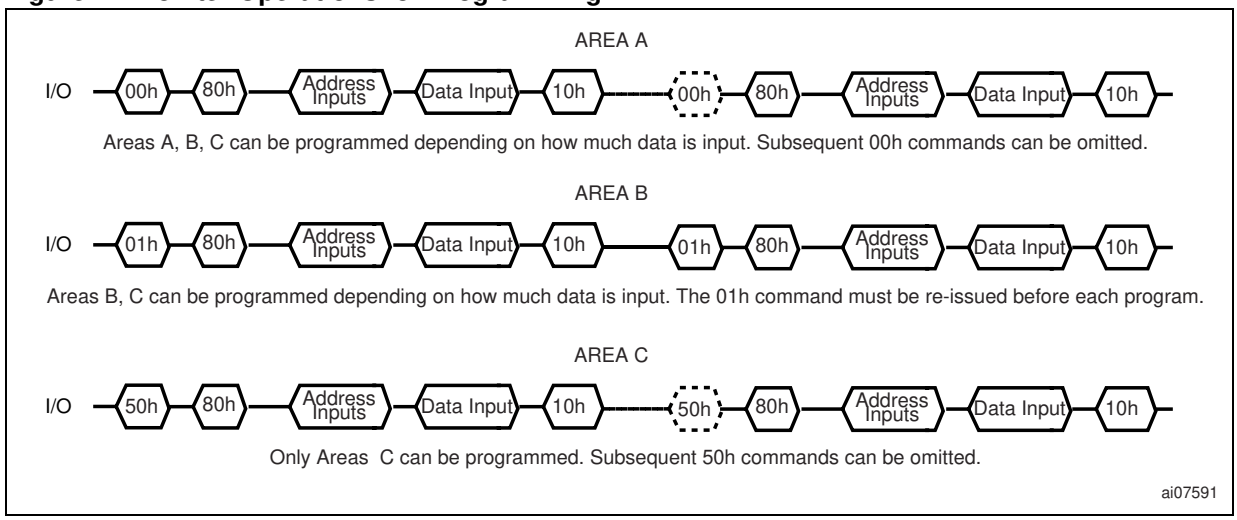


Figure 12. Pointer Operations for Programming



Read Memory Array

Each operation to read the memory area starts with a pointer operation as shown in the Pointer Operations section. Once the area (main or spare) has been selected using the Read A, Read B or Read C commands four bus cycles (for 512Mb and 1Gb devices) or three bus cycles (for 128Mb and 256Mb devices) are required to input the address (refer to Table 6.) of the data to be read.

The device defaults to Read A mode after power-up or a Reset operation. Devices, where page0 is read automatically at power-up, are available on request.

When reading the spare area addresses:

- A0 to A3 (x8 devices)
- A0 to A2 (x16 devices)

are used to set the start address of the spare area while addresses:

- A4 to A7 (x8 devices)
- A3 to A7 (x16 devices)

are ignored.

Once the Read A or Read C commands have been issued they do not need to be reissued for subsequent read operations as the pointer remains in the respective area. However, the Read B command is effective for only one operation, once an operation has been executed in Area B the pointer returns automatically to Area A and so another Read B command is required to start another read operation in Area B.

Once a read command is issued three types of operations are available: Random Read, Page Read and Sequential Row Read.

Random Read. Each time the command is issued the first read is Random Read.

Page Read. After the Random Read access the page data is transferred to the Page Buffer in a time of t_{WHBH} (refer to Table 21. for value). Once the transfer is complete the Ready/Busy signal goes High. The data can then be read out sequentially (from selected column address to last column address) by pulsing the Read Enable signal.

Sequential Row Read. After the data in last column of the page is output, if the Read Enable signal is pulsed and Chip Enable remains Low then the next page is automatically loaded into the Page Buffer and the read operation continues. A Sequential Row Read operation can only be used to read within a block. If the block changes a new read command must be issued.

Refer to Figure 15. and Figure 16. for details of Sequential Row Read operations.

To terminate a Sequential Row Read operation set the Chip Enable signal to High for more than t_{EHEL}.

Sequential Row Read is not available when the Chip Enable Don't Care option is enabled.

Figure 13. Read (A,B,C) Operations

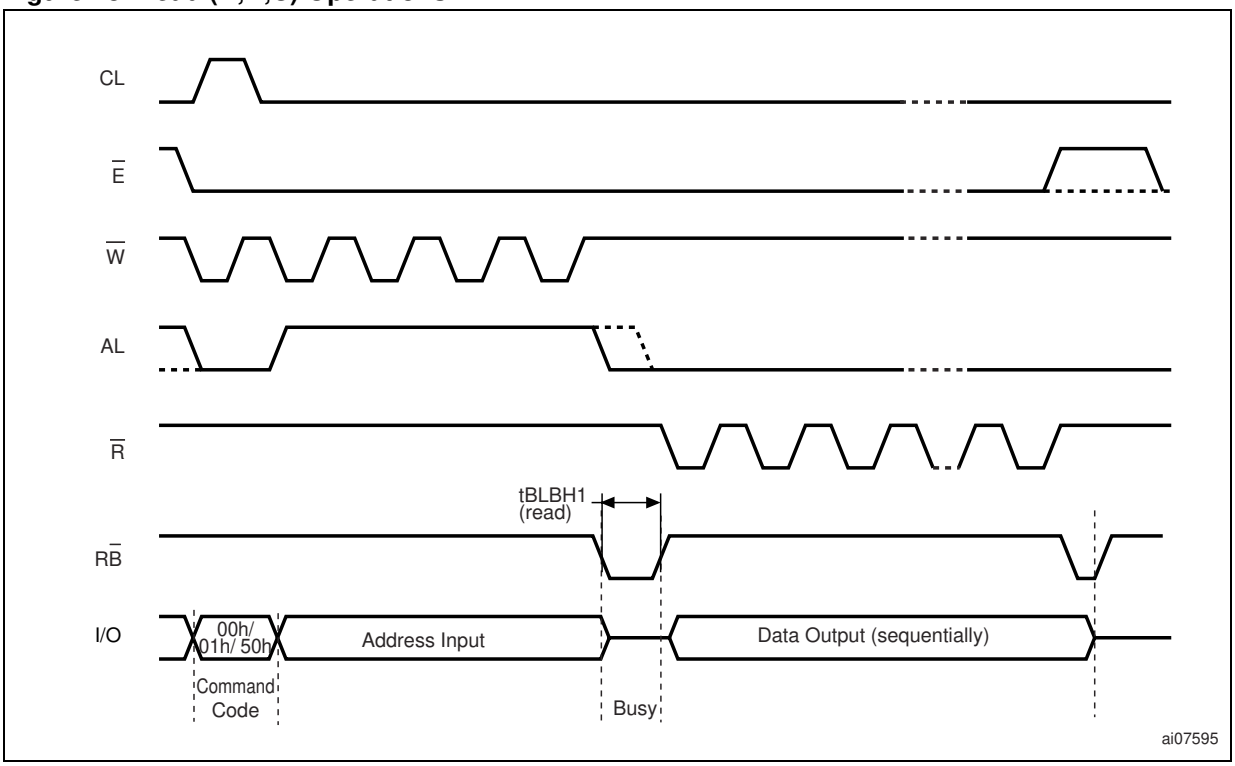
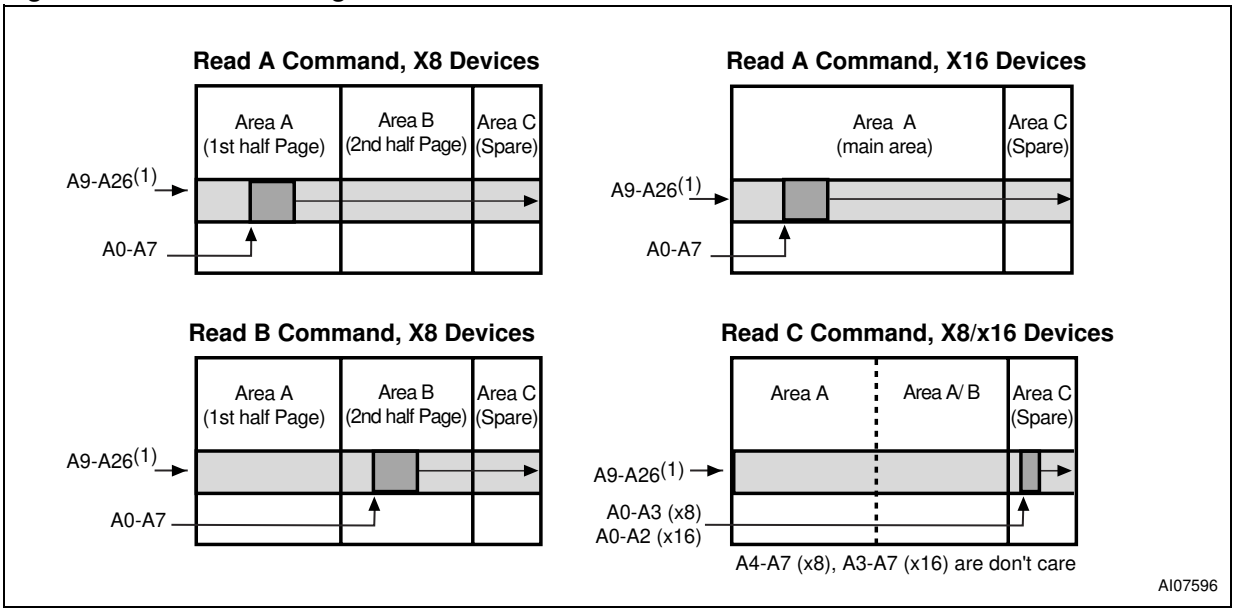


Figure 14. Read Block Diagrams



Note: 1. Highest address depends on device density.

Figure 15. Sequential Row Read Operations

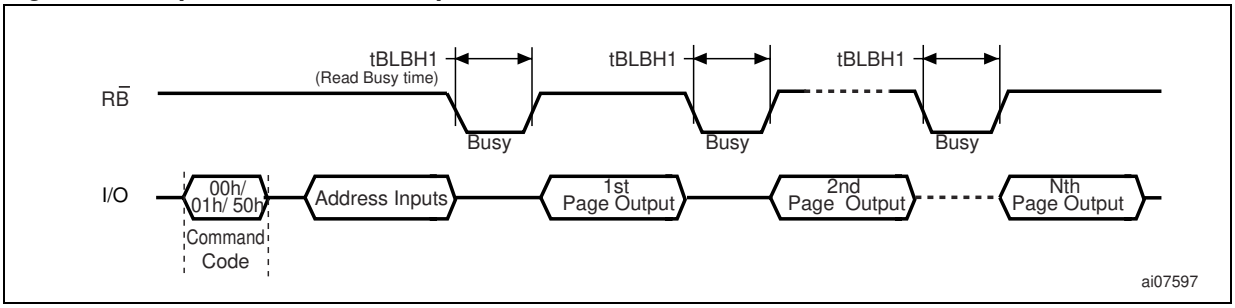
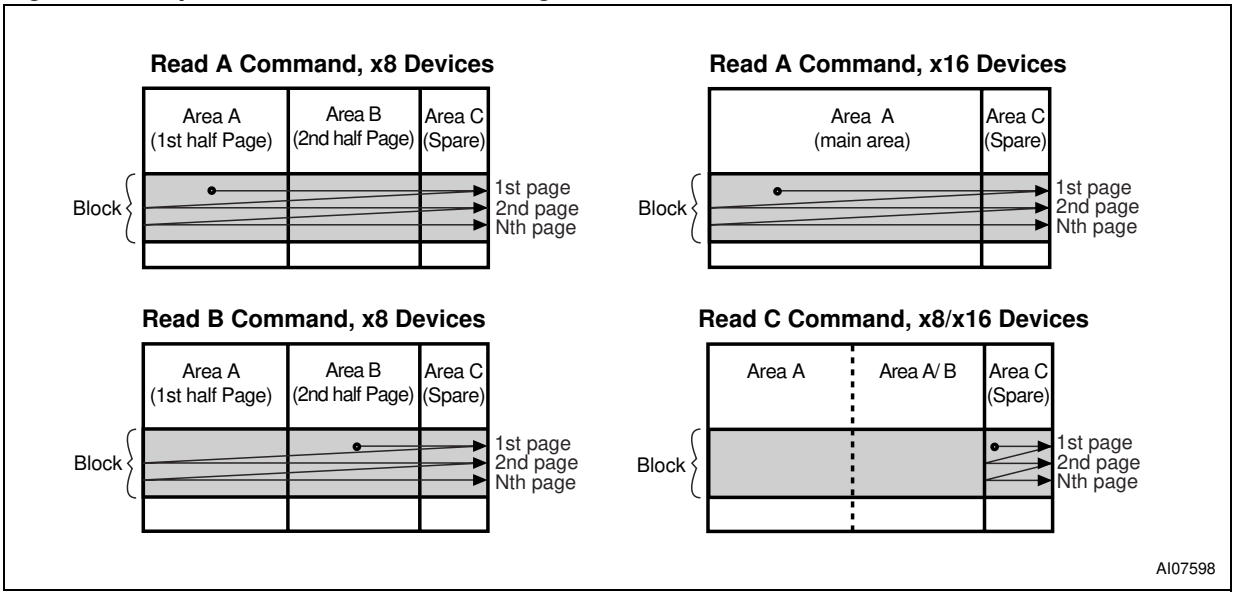


Figure 16. Sequential Row Read Block Diagrams



Page Program

The Page Program operation is the standard operation to program data to the memory array.

The main area of the memory array is programmed by page, however partial page programming is allowed where any number of bytes (1 to 528) or words (1 to 264) can be programmed.

The maximum number of consecutive partial page program operations allowed in the same page is three. After exceeding this a Block Erase command must be issued before any further program operations can take place in that page.

Before starting a Page Program operation a Pointer operation can be performed to point to the area to be programmed. Refer to the Pointer Operations section and Figure 12. for details.

Each Page Program operation consists of five steps (see Figure 17.):

1. one bus cycle is required to setup the Page Program command
2. four bus cycles are then required to input the program address (refer to Table 6.)
3. the data is then input (up to 528 Bytes/ 264 Words) and loaded into the Page Buffer
4. one bus cycle is required to issue the confirm command to start the P/E/R Controller.
5. The P/E/R Controller then programs the data into the array.

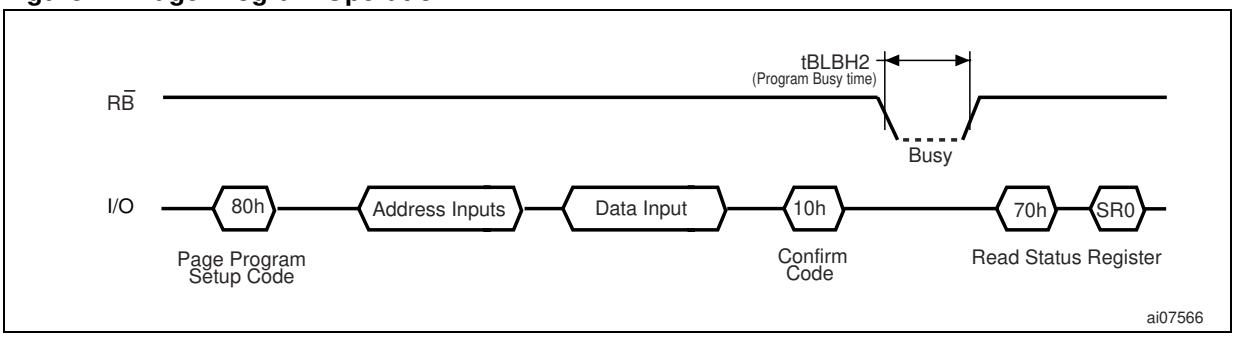
Once the program operation has started the Status Register can be read using the Read Status Register command. During program operations the Status Register will only flag errors for bits set to '1' that have not been successfully programmed to '0'.

During the program operation, only the Read Status Register and Reset commands will be accepted, all other commands will be ignored.

Once the program operation has completed the P/E/R Controller bit SR6 is set to ‘1’ and the Ready/Busy signal goes High.

The device remains in Read Status Register mode until another valid command is written to the Command Interface.

Figure 17. Page Program Operation



Note: Before starting a Page Program operation a Pointer operation can be performed. Refer to Pointer Operations section for details.

Copy Back Program

The Copy Back Program operation is used to copy the data stored in one page and reprogram it in another page.

The Copy Back Program operation does not require external memory and so the operation is faster and more efficient because the reading and loading cycles are not required. The operation is particularly useful when a portion of a block is updated and the rest of the block needs to be copied to the newly assigned block.

If the Copy Back Program operation fails an error is signalled in the Status Register. However as the standard external ECC cannot be used with the Copy Back operation bit error due to charge loss cannot be detected. For this reason it is recommended to limit the number of Copy Back operations on the same data and or to improve the performance of the ECC.

The Copy Back Program operation requires three steps:

1. The source page must be read using the Read A command (one bus write cycle to setup the command and then 4 bus write cycles to input the source page address). This operation copies all 264 Words/ 528 Bytes from the page into the Page Buffer.
2. When the device returns to the ready state (Ready/Busy High), the second bus write cycle of the command is given with the 4 bus cycles to input the target page address. Refer to Table 10. for the addresses that must be the same for the Source and Target pages.
3. Then the confirm command is issued to start the P/E/R Controller.

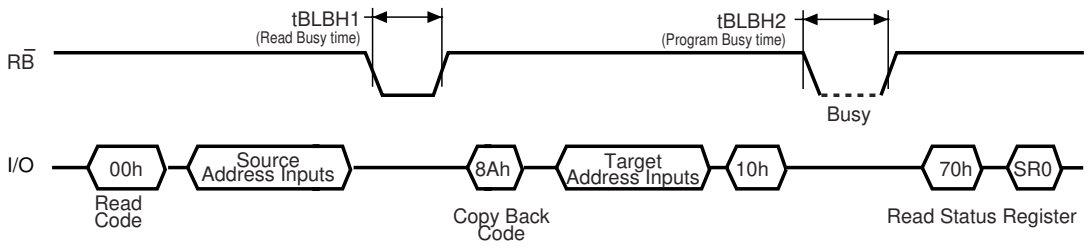
After a Copy Back Program operation, a partial-page program is not allowed in the target page until the block has been erased.

See Figure 18. for an example of the Copy Back operation.

Table 10. Copy Back Program Addresses

Density	Same Address for Source and Target Pages
128Mbit	A23
256Mbit	A24
512Mbit	A25
1Gbit	A25,A26

Figure 18. Copy Back Operation



Block Erase

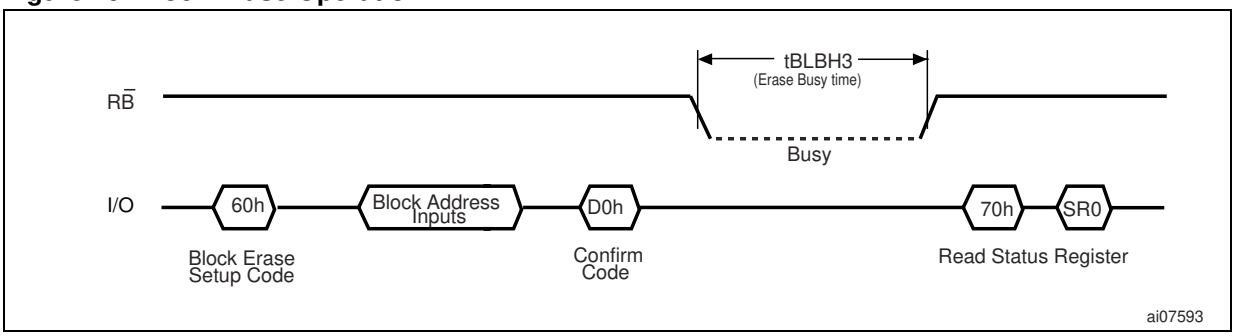
Erase operations are done one block at a time. An erase operation sets all of the bits in the addressed block to '1'. All previous data in the block is lost.

An erase operation consists of three steps (refer to Figure 19.):

1. One bus cycle is required to setup the Block Erase command.
2. Only three bus cycles for 512Mb and 1Gb devices, or two for 128Mb and 256Mb devices are required to input the block address. The first cycle (A0 to A7) is not required as only addresses A14 to A26 (highest address depends on device density) are valid, A9 to A13 are ignored. In the last address cycle I/O0 to I/O7 must be set to V_{IL}.
3. One bus cycle is required to issue the confirm command to start the P/E/R Controller.

Once the erase operation has completed the Status Register can be checked for errors.

Figure 19. Block Erase Operation



Reset

The Reset command is used to reset the Command Interface and Status Register. If the Reset command is issued during any operation, the operation will be aborted. If it was a program or erase operation that was aborted, the contents of the memory locations being modified will no longer be valid as the data will be partially programmed or erased.

If the device has already been reset then the new Reset command will not be accepted.

The Ready/Busy signal goes Low for t_{BLBH4} after the Reset command is issued. The value of t_{BLBH4} depends on the operation that the device was performing when the command was issued, refer to Table 21. for the values.