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NuMicro™ Family Nano100 Series Datasheet

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1 GENERAL DESCRIPTION

The Nano100 series ultra-low power 32-bit microcontroller is embedded with ARM® Cortex™-M0 core operated at a wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded Flash and 8K/16K-byte embedded SRAM. Integrating LCD 4x40 or 6x38 (COM/Segment), USB 2.0 full-speed function, RTC, 12-bit SAR ADC, 12-bit DAC and provides high performance connectivity peripheral interfaces such as UART, SPI, I²C, I²S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and ISO-7816-3 for Smart card, the Nano100 series supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano100 series provides low power voltage, low power consumption, low standby current, high integration peripherals, high-efficiency operation, fast wake-up function and the lowest cost 32-bit microcontrollers. The Nano100 series is suitable for a wide range of battery device applications such as:

- Portable Data Collector
- Portable Medical Monitor
- Portable RFID Reader
- Portable Barcode Scanner
- Security Alarm System
- System Supervisors
- Power Metering
- USB Accessories
- Smart Card Reader
- Wireless Game Control Device
- IPTV Remote Smart Keyboard
- Wireless Sensors Node Device (WSN)
- Wireless RF4CE Remote Control
- Wireless Audio
- Wireless Automatic Meter Reader (AMR)
- Electronic Toll Collection (ETC)

The Nano100 Base line, an ultra-low power 32-bit microcontroller with the embedded ARM® Cortex™-M0 core, operates at wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded flash and 8K/16K bytes embedded SRAM. It integrates RTC, 12- channels 12-bit SAR ADC, 2-channels 12-bit DAC and provides high performance connectivity peripheral interfaces such as 2xUART, 3xSPI, 2xI²C, I²S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and 3xISO-7816-3 for Smart card. The Nano100 Base line supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano110 LCD line, an ultra-low power 32-bit microcontroller with the embedded ARM® Cortex™-M0 core, operates at wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded flash and 8K/16K bytes embedded SRAM. It integrates LCD 4x40 or 6x38 (COM/Segment). RTC, 12-channels 12-bit SAR ADC, 2-channels 12-bit DAC and provides high performance connectivity peripheral interfaces such as 2xUART, 2xSPI, 2xI²C, I²S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and 3xISO-7816-3 for Smart card. The Nano110 LCD line supports Brown-out Detector,

Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano120 USB Connectivity line, an ultra-low power 32-bit microcontroller with the embedded ARM® Cortex™-M0 core, operates at wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded flash and 8K/16K bytes embedded SRAM. It integrates USB 2.0 full-speed device function, RTC, 12-channels 12-bit SAR ADC, 2-channels 12-bit DAC and provides high performance connectivity peripheral interfaces such as 2xUART, 3xSPI, 2xI2C, I2S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and 3xISO-7816-3 for Smart card. The Nano120 USB Connectivity line supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano130 Advanced line, an ultra-low power 32-bit microcontroller with the embedded ARM® Cortex™-M0 core, operates at wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded flash and 8K/16K bytes embedded SRAM. It integrated LCD 4x40 or 6x38 (COM/Segment), USB 2.0 full-speed device function, RTC, 8-channels 12-bit SAR ADC, 2-channels 12-bit DAC and provides high performance connectivity peripheral interfaces such as 2xUART, 2xSPI, 2xI²C, I²S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and 3xISO-7816-3 for Smart card. The Nano130 Advanced line supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

Product Line	UART	SPI	I ² C	I ² S	USB	LCD	ADC	DAC	RTC	EBI	SC	Timer
Nano100	●	●	●	●			●	●	●	●	●	●
Nano110	●	●	●	●		●	●	●	●	●	●	●
Nano120	●	●	●	●	●		●	●	●	●	●	●
Nano130	●	●	●	●	●	●	●	●	●	●	●	●

Table 1-1 Connectivity Support Table

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 Nano100 Features – Base Line

- Core
 - ◆ ARM® Cortex™-M0 core running up to 42 MHz
 - ◆ One 24-bit system timer
 - ◆ Supports Low Power Sleep mode
 - ◆ Single-cycle 32-bit hardware multiplier
 - ◆ NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - ◆ Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
 - ◆ Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
 - ◆ Runs up to 42 MHz with zero wait state for discontinuous address read access
 - ◆ 64K/32K/123K bytes application program memory (APROM)
 - ◆ 4 KB in system programming (ISP) loader program memory (LDRROM)
 - ◆ Programmable data flash start address and memory size with 512 bytes page erase unit
 - ◆ In System Program (ISP)/In Application Program (IAP) to update on-chip Flash EPROM
- SRAM Memory
 - ◆ 16K/8K bytes embedded SRAM
 - ◆ Supports DMA mode
- DMA: Supports 8 channels: one VDMA channel, 6 PDMA channels and one CRC channel
 - ◆ VDMA
 - Memory-to-memory transfer
 - Supports block transfer with stride
 - Supports word/half-word/byte boundary address
 - Supports address direction: increment and decrement
 - ◆ PDMA
 - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
 - Supports word boundary address
 - Supports word alignment transfer length in memory-to-memory mode
 - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode

- Supports word/half-word/byte transfer data width from/to peripheral
 - Supports address direction: increment, fixed, and wrap around
- ◆ CRC
 - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
 - ◆ CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
 - ◆ CRC-8: $X^8 + X^2 + X + 1$
 - ◆ CRC-16: $X^{16} + X^{15} + X^2 + 1$
 - ◆ CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Clock Control
 - ◆ Flexible selection for different applications
 - ◆ Built-in 12 MHz OSC, can be trimmed to 0.25% deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12 MHz OSC has 2 % deviation within all temperature range.
 - ◆ Low power 10 kHz OSC for watchdog and low power system operation
 - ◆ Supports one PLL, up to 120 MHz, for high performance system operation and USB application (48 MHz).
 - ◆ External 4~24 MHz crystal input for precise timing operation
 - ◆ External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
 - ◆ Three I/O modes:
 - Push-Pull output
 - Open-Drain output
 - Input only with high impedance
 - ◆ All inputs with Schmitt trigger
 - ◆ I/O pin configured as interrupt source with edge/level setting
 - ◆ Supports High Driver and High Sink I/O mode
 - ◆ Supports input 5V tolerance, except PA.0 ~ PA.7, PD.0 ~ PD.1 and PC.6 ~ PC.7
- Timer
 - ◆ Supports 4 sets of 32-bit timers, each with 24-bit up-counting timer and one 8-bit pre-scale counter
 - ◆ Independent Clock Source for each timer
 - ◆ Provides one-shot, periodic, output toggle and continuous operation modes
 - ◆ Internal trigger event to ADC, DAC and PDMA
 - ◆ Supports PDMA mode
 - ◆ Wake system up from Power-down mode

- Watchdog Timer
 - ◆ Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)
 - ◆ Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
 - ◆ Interrupt or reset selectable when watchdog time-out
 - ◆ Wake system up from Power-down mode
- Window Watchdog Timer(WWDT)
 - ◆ 6-bit down counter and 6-bit compare value to make the window period flexible
 - ◆ Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.
- RTC
 - ◆ Supports software compensation by setting frequency compensate register (FCR)
 - ◆ Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
 - ◆ Supports Alarm registers (second, minute, hour, day, month, year)
 - ◆ Selectable 12-hour or 24-hour mode
 - ◆ Automatic leap year recognition
 - ◆ Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
 - ◆ Wake system up from Power-down mode
 - ◆ Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers
- PWM/Capture
 - ◆ Supports 2 PWM modules, each has two 16-bit PWM generators
 - ◆ Provides eight PWM outputs or four complementary paired PWM outputs
 - ◆ Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-zone generator for complementary paired PWM
 - ◆ (Shared with PWM timers) with eight 16-bit digital capture timers provides eight rising/ falling/both capture inputs.
 - ◆ Supports One-shot and Continuous mode
 - ◆ Supports Capture interrupt
- UART
 - ◆ Up to two 16-byte FIFO UART controllers
 - ◆ UART ports with flow control (TX, RX, CTSn and RTSn)
 - ◆ Supports IrDA (SIR) function
 - ◆ Supports LIN function
 - ◆ Supports RS-485 9 bit mode and direction control.
 - ◆ Programmable baud rate generator
 - ◆ Supports PDMA mode

- ◆ Wake system up from Power-down mode
- SPI
 - ◆ Up to three sets of SPI controller
 - ◆ Master up to 32 MHz, and Slave up to 16 MHz
 - ◆ Supports SPI/MICROWIRE Master/Slave mode
 - ◆ Full duplex synchronous serial data transfer
 - ◆ Variable length of transfer data from 4 to 32 bits
 - ◆ MSB or LSB first data transfer
 - ◆ RX and TX on both rising or falling edge of serial clock independently
 - ◆ Two slave/device select lines when SPI controller is used as the master, and 1 slave/device select line when SPI controller is used as the slave
 - ◆ Supports byte suspend mode in 32-bit transmission
 - ◆ Supports two channel PDMA requests, one for transmit and another for receive
 - ◆ Supports three wire mode, no slave select signal, bi-direction interface
 - ◆ Wake system up from Power-down mode
- I²C
 - ◆ Up to two sets of I²C device
 - ◆ Master/Slave up to 1 Mbit/s
 - ◆ Bi-directional data transfer between masters and slaves
 - ◆ Multi-master bus (no central master)
 - ◆ Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - ◆ Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
 - ◆ Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
 - ◆ Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
 - ◆ Programmable clocks allowing for versatile rate control
 - ◆ Supports 7-bit addressing mode
 - ◆ Supports multiple address recognition (four slave addresses with mask option)
- I²S
 - ◆ Interface with external audio CODEC
 - ◆ Operated as either Master or Slave mode
 - ◆ Capable of handling 8, 16, 24 and 32 bit word sizes
 - ◆ Supports Mono and stereo audio data
 - ◆ Supports I²S and MSB justified data format
 - ◆ Provides two 8 word FIFO data buffers: one for transmitting and the other for

- receiving
- ◆ Generates interrupt requests when buffer levels cross a programmable boundary
- ◆ Supports two PDMA requests: one for transmitting and the other for receiving
- ADC
 - ◆ 12-bit SAR ADC up to 2Msps conversion rate
 - ◆ Up to 12-ch single-ended input from external pin (PA.0 ~ PA.7 and PD.0 ~ PD.3)
 - ◆ Six internal channels from DAC0, DAC1, internal reference voltage (Int_VREF), Temperature sensor, AVDD, and AVSS.
 - ◆ Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
 - ◆ Supports Single Scan, Single Cycle Scan, and Continuous Scan mode
 - ◆ Each channel with individual result register
 - ◆ Only scan on enabled channels
 - ◆ Threshold voltage detection (comparator function)
 - ◆ Conversion started by software programming or external input
 - ◆ Supports PDMA mode
 - ◆ Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3) to enable ADC
- DAC
 - ◆ 12-bit monotonic output with 400K conversion rate
 - ◆ Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
 - ◆ Synchronized update capability for two DACs (group function)
 - ◆ Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3), software or PDMA to trigger DAC to conversion
- SmartCard (SC)
 - ◆ Compliant to ISO-7816-3 T=0, T=1
 - ◆ Supports up to three ISO-7816-3 ports
 - ◆ Separates receive/transmit 4 bytes entry FIFO for data payloads
 - ◆ Programmable transmission clock frequency
 - ◆ Programmable receiver buffer trigger level
 - ◆ Programmable guard time selection (11 ETU ~ 266 ETU)
 - ◆ A 24-bit and two 8-bit time-out counters for Answer to Reset (ATR) and waiting times processing
 - ◆ Supports auto inverse convention function
 - ◆ Supports stop clock level and clock stop (clock keep) function
 - ◆ Supports transmitter and receiver error retry and error limit function
 - ◆ Supports hardware activation sequence process

- ◆ Supports hardware warm reset sequence process
- ◆ Supports hardware deactivation sequence process
- ◆ Supports hardware auto deactivation sequence when detect the card is removal
- ◆ Supports UART mode (Half Duplex)
- EBI (External bus interface) support
 - ◆ Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
 - ◆ Supports 8bit/16bit data width
 - ◆ Supports byte write in 16-bit Data Width mode
- One built-in temperature sensor with 1°C resolution
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40°C~85°C
- Packages:
 - ◆ All Green package (RoHS)
 - ◆ LQFP 128-pin(14x14) / 64-pin(7x7) / 48-pin(7x7) / QFN 48-pin(7x7)

2.2 Nano110 Features – LCD Line

- Core
 - ◆ ARM® Cortex™-M0 core running up to 42 MHz
 - ◆ One 24-bit system timer
 - ◆ Supports Low Power Sleep mode
 - ◆ Single-cycle 32-bit hardware multiplier
 - ◆ NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - ◆ Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
 - ◆ Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
 - ◆ Runs up to 42 MHz with zero wait state for discontinuous address read access.
 - ◆ 64K/32K/123K bytes application program memory (APROM)
 - ◆ 4 KB In System Programming (ISP) loader program memory (LDROM)
 - ◆ Programmable data flash start address and memory size with 512 bytes page erase unit
 - ◆ In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
 - ◆ 16K/8K bytes embedded SRAM
 - ◆ Supports DMA mode
- DMA : Supports 8 channels: one VDMA channel, 6 PDMA channels, and one CRC channel
 - ◆ VDMA
 - Memory-to-memory transfer
 - Supports block transfer with stride
 - Supports word/half-word/byte boundary address
 - Supports address direction: increment and decrement
 - ◆ PDMA
 - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
 - Supports word boundary address
 - Supports word alignment transfer length in memory-to-memory mode
 - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
 - Supports word/half-word/byte transfer data width from/to peripheral
 - Supports address direction: increment, fixed, and wrap around
 - ◆ CRC

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
 - ◆ CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
 - ◆ CRC-8: $X^8 + X^2 + X + 1$
 - ◆ CRC-16: $X^{16} + X^{15} + X^2 + 1$
 - ◆ CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Clock Control
 - ◆ Flexible selection for different applications
 - ◆ Built-in 12 MHz OSC, can be trimmed to 0.25% deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12 MHz OSC has 2 % deviation within all temperature range.
 - ◆ Low power 10 kHz OSC for watchdog and low power system operation
 - ◆ Supports one PLL, up to 120 MHz, for high performance system operation and USB application (48 MHz).
 - ◆ External 4~24 MHz crystal input for precise timing operation
 - ◆ External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
 - ◆ Three I/O modes:
 - Push-Pull output
 - Open-Drain output
 - Input only with high impedance
 - ◆ All inputs with Schmitt trigger
 - ◆ I/O pin configured as interrupt source with edge/level setting
 - ◆ Supports High Driver and High Sink I/O mode
 - ◆ Supports input 5V tolerance, except PA.0 ~ PA.7, PD.0 ~ PD.1 and PC.6 ~ PC.7)
- Timer
 - ◆ Supports 4 sets of 32-bit timers, each with 24-bit up-timer and one 8-bit pre-scale counter
 - ◆ Independent Clock Source for each timer
 - ◆ Provides one-shot, periodic, output toggle and continuous operation modes
 - ◆ Internal trigger event to ADC, DAC and PDMA module
 - ◆ Supports PDMA mode
 - ◆ Wake system up from Power-down mode
- Watchdog Timer
 - ◆ Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)

- ◆ Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
- ◆ Interrupt or reset selectable when watchdog time-out
- ◆ Wake system up from Power-down mode
- Window Watchdog Timer(WWDT)
 - ◆ 6-bit down counter and 6-bit compare value to make the window period flexible
 - ◆ Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.
- RTC
 - ◆ Supports software compensation by setting frequency compensate register (FCR)
 - ◆ Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
 - ◆ Supports Alarm registers (second, minute, hour, day, month, year)
 - ◆ Selectable 12-hour or 24-hour mode
 - ◆ Automatic leap year recognition
 - ◆ Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
 - ◆ Wake system up from Power-down mode
 - ◆ Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers
- PWM/Capture
 - ◆ Supports 2 PWM modules, each has two 16-bit PWM generators
 - ◆ Provides eight PWM outputs or four complementary paired PWM outputs
 - ◆ Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-zone generator for complementary paired PWM
 - ◆ (Shared with PWM timers) with eight 16-bit digital capture timers provides eight rising/ falling/both capture inputs.
 - ◆ Supports Capture interrupt
- UART
 - ◆ Up to two 16-byte FIFO UART controllers
 - ◆ UART ports with flow control (TX, RX, CTSn and RTSn)
 - ◆ Supports IrDA (SIR) function
 - ◆ Supports LIN function
 - ◆ Supports RS-485 9 bit mode and direction control (Low Density Only)
 - ◆ Programmable baud rate generator
 - ◆ Supports PDMA mode
 - ◆ Wake system up from Power-down mode
- SPI
 - ◆ Up to three sets of SPI controller

- ◆ Master up to 32 MHz, and Slave up to 16 MHz
- ◆ Supports SPI/MICROWIRE Master/Slave mode
- ◆ Full duplex synchronous serial data transfer
- ◆ Variable length of transfer data from 4 to 32 bits
- ◆ MSB or LSB first data transfer
- ◆ RX and TX on both rising or falling edge of serial clock independently
- ◆ Two slave/device select lines when SPI controller is as the master, and 1 slave/device select line when SPI controller is as the slave
- ◆ Supports byte suspend mode in 32-bit transmission
- ◆ Supports two channel PDMA requests, one for transmit and another for receive
- ◆ Supports three wire mode, no slave select signal, bi-direction interface
- ◆ Wake system up from Power-down mode
- I²C
 - ◆ Up to two sets of I²C device
 - ◆ Master/Slave up to 1Mbit/s
 - ◆ Bidirectional data transfer between masters and slaves
 - ◆ Multi-master bus (no central master)
 - ◆ Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - ◆ Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
 - ◆ Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
 - ◆ Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
 - ◆ Programmable clocks allow versatile rate control
 - ◆ Supports 7-bit addressing mode
 - ◆ Supports multiple address recognition (four slave address with mask option)
- I²S
 - ◆ Interface with external audio CODEC
 - ◆ Operated as either Master or Slave mode
 - ◆ Capable of handling 8, 16, 24 and 32 bit word sizes
 - ◆ Supports Mono and stereo audio data
 - ◆ Supports I²S and MSB justified data format
 - ◆ Provides two 8 word FIFO data buffers: one for transmitting and the other for receiving
 - ◆ Generates interrupt requests when buffer levels cross a programmable boundary
 - ◆ Supports two PDMA requests: one for transmitting and the other for receiving

- ADC
 - ◆ 12-bit SAR ADC up to 2Msps conversion rate
 - ◆ Up to 12-ch single-ended input from external pin (PA.0 ~ PA.7 and PD.0 ~ PD.3)
 - ◆ Six internal channels from DAC0, DAC1, internal reference voltage (Int_VREF), Temperature sensor, AVDD, and AVSS
 - ◆ Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
 - ◆ Single scan/single cycle scan/continuous scan
 - ◆ Each channel with individual result register
 - ◆ Only scan on enabled channels
 - ◆ Threshold voltage detection (comparator function)
 - ◆ Conversion start by software programming or external input
 - ◆ Supports PDMA mode
 - ◆ Supports up to four timer time-out events (TMR0, TMR1, TMR2, and TMR3) to enable ADC
- DAC
 - ◆ 12-bit monotonic output with 400K conversion rate
 - ◆ Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
 - ◆ Synchronized update capability for two DACs (group function)
 - ◆ Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3), software or PDMA to trigger DAC to conversion
- SmartCard (SC)
 - ◆ Compliant to ISO-7816-3 T=0, T=1
 - ◆ Supports up to three ISO-7816-3 ports
 - ◆ Separates receive / transmit 4 bytes entry FIFO for data payloads
 - ◆ Programmable transmission clock frequency
 - ◆ Programmable receiver buffer trigger level
 - ◆ Programmable guard time selection (11 ETU ~ 266 ETU)
 - ◆ A 24-bit and two 8-bit time-out counter for Answer to Reset (ATR) and waiting times processing
 - ◆ Supports auto inverse convention function
 - ◆ Supports stop clock level and clock stop (clock keep) function
 - ◆ Supports transmitter and receiver error retry and error limit function
 - ◆ Supports hardware activation sequence process
 - ◆ Supports hardware warm reset sequence process
 - ◆ Supports hardware deactivation sequence process
 - ◆ Supports hardware auto deactivation sequence when detect the card is removal

- ◆ Supports UART mode (Half Duplex)
- LCD
 - ◆ LCD driver for up to 4 COM x 40 SEG or 6 COM x 38 SEG
 - ◆ Supports Static, 1/2 bias and 1/3 bias voltage
 - ◆ Four display modes; Static, 1/2 duty, 1/3 duty, 1/4 duty, 1/5 duty and 1/6 duty.
 - ◆ Selectable LCD frequency by frequency divider
 - ◆ Configurable frame frequency
 - ◆ Internal Charge pump, adjustable contrast adjustment
 - ◆ Configurable Charge pump frequency
 - ◆ Blinking capability
 - ◆ Supports R-type/C-type method
 - ◆ LCD frame interrupt
- One built-in temperature sensor with 1°C resolution
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40°C~85°C
- Packages:
 - ◆ All Green package (RoHS)
 - ◆ LQFP 128-pin(14x14) / 64-pin(10x10) / 64-pin(7x7)

2.3 Nano120 Features – USB Connectivity Line

- Core
 - ◆ ARM® Cortex™-M0 core running up to 42 MHz
 - ◆ One 24-bit system timer
 - ◆ Supports Low Power Sleep mode
 - ◆ Single-cycle 32-bit hardware multiplier
 - ◆ NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - ◆ Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
 - ◆ Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
 - ◆ Runs up to 42 MHz with zero wait state for discontinuous address read access.
 - ◆ 64K/32K/123K bytes application program memory (APROM)
 - ◆ 4KB in system programming (ISP) loader program memory (LDROM)
 - ◆ Programmable data flash start address and memory size with 512 bytes page erase unit
 - ◆ In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
 - ◆ 16K/8K bytes embedded SRAM
 - ◆ Supports PDMA mode
- DMA: Support 8 channels: one VDMA channel, 6 PDMA channels, and one CRC channel
 - ◆ VDMA
 - Memory-to-memory transfer
 - Supports block transfer with stride
 - Supports word/half-word/byte boundary address
 - Supports address direction: increment and decrement
 - ◆ PDMA
 - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
 - Supports word boundary address
 - Supports word alignment transfer length in memory-to-memory mode
 - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
 - Supports word/half-word/byte transfer data width from/to peripheral
 - Supports address: increment, fixed, and wrap around
 - ◆ CRC

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
 - ◆ CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
 - ◆ CRC-8: $X^8 + X^2 + X + 1$
 - ◆ CRC-16: $X^{16} + X^{15} + X^2 + 1$
 - ◆ CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Clock Control
 - ◆ Flexible selection for different applications
 - ◆ Built-in 12MHz OSC, can be trimmed to 0.25% deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12 MHz OSC has 2 % deviation within all temperature range
 - ◆ Low power 10 kHz OSC for watchdog and low power system operation
 - ◆ Supports one PLL, up to 120 MHz, for high performance system operation and USB application (48 MHz).
 - ◆ External 4~24 MHz crystal input for precise timing operation
 - ◆ External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
 - ◆ Three I/O modes:
 - Push-Pull output
 - Open-Drain output
 - Input only with high impedance
 - ◆ All inputs with Schmitt trigger
 - ◆ I/O pin can be configured as interrupt source with edge/level setting
 - ◆ High driver and high sink IO mode support
 - ◆ Supports input 5V tolerance (except ADC and DAC shared pins)
- Timer
 - ◆ Supports 4 sets of 32-bit timers, each with 24-bit up-timer and one 8-bit pre-scale counter
 - ◆ Independent Clock Source for each timer
 - ◆ Provides one-shot, periodic, output toggle and continuous operation modes
 - ◆ Internal trigger event to ADC, DAC and PDMA module
 - ◆ Supports PDMA mode
 - ◆ Wake system up from Power-down mode
- Watchdog Timer
 - ◆ Clock Source from LIRC. (Internal 10 kHz Low Speed Oscillator Clock)
 - ◆ Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)

- ◆ Interrupt or reset selectable on watchdog time-out
- ◆ Wake system up from Power-down mode
- Window Watchdog Timer(WWDT)
 - ◆ 6-bit down counter and 6-bit compare value to make the window period flexible
 - ◆ Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.
- RTC
 - ◆ Supports software compensation by setting frequency compensate register (FCR)
 - ◆ Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
 - ◆ Supports Alarm registers (second, minute, hour, day, month, year)
 - ◆ Selectable 12-hour or 24-hour mode
 - ◆ Automatic leap year recognition
 - ◆ Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
 - ◆ Wake system up from Power-down or Idle mode
 - ◆ Support 80 bytes spare registers and a snoop pin to clear the content of these spare registers
- PWM/Capture
 - ◆ Supports 2 PWM module, each has two 16-bit PWM generators
 - ◆ Provide eight PWM outputs or four complementary paired PWM outputs
 - ◆ Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-Zone generator for complementary paired PWM
 - ◆ (Shared with PWM timers) with eight 16-bit digital capture timers provides eight rising/ falling/both capture inputs.
 - ◆ Supports one shot and continuous mode
 - ◆ Supports Capture interrupt
- UART
 - ◆ Up to two 16-byte FIFO UART controllers
 - ◆ UART ports with flow control (TX, RX, CTSn and RTSn)
 - ◆ Supports IrDA (SIR) function
 - ◆ Supports LIN function
 - ◆ Supports RS-485 9 bit mode and direction control. (Low Density Only)
 - ◆ Programmable baud rate generator
 - ◆ Supports PDMA mode
 - ◆ Wake system up from Power-down mode
- SPI
 - ◆ Up to three sets of SPI controller

- ◆ Master up to 32 MHz, and Slave up to 16 MHz
- ◆ Supports SPI/MICROWIRE Master/Slave mode
- ◆ Full duplex synchronous serial data transfer
- ◆ Variable length of transfer data from 4 to 32 bits
- ◆ MSB or LSB first data transfer
- ◆ RX and TX on both rising or falling edge of serial clock independently
- ◆ Two slave/device select lines when SPI controller is as the master, and 1 slave/device select line when SPI controller is as the slave
- ◆ Supports byte suspend mode in 32-bit transmission
- ◆ Supports two channel PDMA requests, one for transmit and another for receive
- ◆ Supports three wire, no slave select signal, bi-direction interface
- ◆ Wake system up from Power-down mode
- I²C
 - ◆ Up to two sets of I²C device
 - ◆ Master/Slave up to 1Mbit/s
 - ◆ Bi-directional data transfer between masters and slaves
 - ◆ Multi-master bus (no central master)
 - ◆ Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - ◆ Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
 - ◆ Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
 - ◆ Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
 - ◆ Programmable clocks allow versatile rate control
 - ◆ Supports 7-bit addressing mode
 - ◆ Supports multiple address recognition (four slave addresses with mask option)
- I²S
 - ◆ Interface with external audio CODEC
 - ◆ Operated as either Master or Slave mode
 - ◆ Capable of handling 8, 16, 24 and 32 bit word sizes
 - ◆ Supports Mono and stereo audio data
 - ◆ Supports I²S and MSB justified data format
 - ◆ Provides two 8 word FIFO data buffers: one for transmitting and the other for receiving
 - ◆ Generates interrupt requests when buffer levels cross a programmable boundary
 - ◆ Supports two PDMA requests: one for transmitting and the other for receiving