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ARM® Cortex®-M

32-bit Microcontroller

NuMicro® Family
Nano103 Series
Datasheet

For additional information or questions, please contact:Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The Nano103 series ultra-low-power 32-bit microcontroller embeded with ARM® Cortex®-M0 core operates at low voltage ranged from 1.8V to 3.6V and runs up to 36 MHz frequency with 64 Kbytes embedded Flash(APROM) and 16 Kbytes embedded SRAM and 4 Kbytes Flash loader memory(LDROM) for In-System Programming (ISP). In additon, Nano103 include special 512 bytes security protection memory (SPROM) and 1 Kbytes key protection memory (KPROM) to enhance the security and protection of customer application.

The Nano103 series integrates RTC with independent V_{BAT} pin, 12-bit SAR ADC, comparator and provides high performance connectivity peripheral interfaces such as UART, SPI, I^2C, GPIOs, and ISO-7816-3 for Smart card.

The Nano103 series supports main power off with only V_{BAT} and RTC on less than 1.0 uA and Deep Power-down mode with RAM retention is less than 1.6 uA and fast wake-up via many peripheral interfaces.

The Nano103 series provides low voltage, low operating power consumption, low standby current, high integration peripherals, high-efficiency operation, fast wake-up function and the lowest cost 32-bit microcontrollers. The Nano103 series is suitable for a wide range of battery device applications such as:

- Hand-Held Medical Device
- Wearable Device & Smart Watch
- Wireless Gaming Control, Thermostats, Sensors Node Device (WSND)
- Wireless Auto Meter Reading (AMR)
- RFID Reader
- Portable Wireless Data Collector
- Mobile Payment Smart Card Reader
- Security Alarm System
- Smart Home Appliance
- Smart Water, Gas, Heat Meters

Product Line	SPROM	KPROM	UART	SPI	I^2C	ADC	ACMP	RTC/V_{bat}	SC	Timer
Nano103	●	●	●	●	●	●	●	●	●	●

Table 4.1-1 Connectivity Support Table

2 FEATURES

- Low Supply Voltage Range: 1.8V to 3.6V
- Operating Temperature: -40℃~105℃
- Four power modes
  - Normal mode
  - Idle mode
  - Power-down mode with RTC on and RAM retention
  - RTC domain only
- Wake-up sources
  - RTC, WDT, I²C, Timer, UART, SPI, BOD, GPIO
- Fast wake-up from power-down mode: less than 3.5 μs when using HIRC0
- Brown-out
  - Built-in 1.7~3.1V BOD for wide operating voltage range operation
  - Built-in low power 2.0/2.5V BOD
- Core
  - ARM® Cortex®-M0 core running up to 36 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Flash EPROM Memory
  - 64 Kbytes application program memory (APROM)
  - 4 Kbytes in system programming (ISP) loader program memory (LDROM)
  - 512 bytes security protection memory (SPROM)
  - 1 Kbytes key protection memory (KPROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on-chip Flash EPROM
- SRAM Memory
  - 16 Kbytes embedded SRAM
  - Supports DMA mode
- DMA: Supports Five channels includingfour PDMA channels and one CRC channel
  - PDMA
    - Three modes: peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Source address and destination address must be word alignment in all modes.

- Memory-to-memory mode: transfer length must be word alignment.
- Peripheral-to-memory and memory-to-peripheral mode: transfer length could be word/half-word/byte alignment.
- Peripheral-to-memory and memory-to-peripheral mode: transfer data width could be word/half-word/byte alignment
- Supports source and destination address direction: increment, fixed, and wrap around

◆ CRC

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - ◆ CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - ◆ CRC-8: $X^8 + X^2 + X + 1$
  - ◆ CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - ◆ CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Clock Control
  - ◆ Built-in 12/16MHz OSC (HIRC0) has 2 % deviation within all temperarure range. Deviation could be reduced to 1% if turning on auto-trim function.
  - ◆ Built-in 36MHz OSC(HIRC1)
  - ◆ Built-in 4MHz OSC(MIRC)
  - ◆ Supports one PLL, up to 36 MHz, for high performance system operation
  - ◆ External 4~24 MHz(HXT) crystal input for precise timing operation
  - ◆ Low power 10 kHz OSC(LIRC) for watchdog and low power system operation
  - ◆ External 32.768 kHz(LXT) crystal input for RTC and low power system operation
- GPIO
  - ◆ Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - ◆ All inputs with Schmitt trigger
  - ◆ I/O pin configured as interrupt source with edge/level setting
  - ◆ Supports input 5V tolerance, except
    - PA.0 ~ PA.7 (sharing pin with ADC),
    - PA.12~ PA.13 (sharing pin with comparator),
    - PF.0~ PF.1 and PF.6 ~ PF.7(sharing pin with HXT and LXT)
    - PA.8, PB.4 and PB.5
- Timer
  - ◆ Supports 4 sets of 32-bit timers, each timer with 24-bit up-counting timer and one 8-bit pre-scale counter
  - ◆ Each timer could have independent clock source selection

- Supports one-shot,periodic, output toggle and continuous operation modes
- Internal trigger event to ADC and PDMA
- Supports PDMA mode
- Wake system up from Power-down mode

- Watchdog Timer
  - Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)
  - Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
  - Interrupt or reset selectable when watchdog time-out
  - Wakes system up from Power-down mode
- Window Watchdog Timer(WWDT)
  - 6-bit down counter and 6-bit compare value to make the window period flexible
  - Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.
- RTC
  - Supports software compensation by setting frequency compensate register (FREQADJ)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Wake system up from Power-down mode
  - Supports 20 bytes spare registers and a tamper pin to clear the content of these spare registers
  - Supports 1 Hz clock output
  - Support independent V_{BAT} power domain to provide for PF.6~PF.7 (sharing pin with LXT) and tamper pins (LQFP64: PB.13/LQFP48: PA.9/QFN32: PB.8)
- PWM/Capture
  - Supports one PWM module to provides 6 output channels
  - Supports independent mode for PWM output/Capture input channe
  - Supports complementary mode for 3 complementary paired PWM output channel
  - Supports 16-bit resolution PWM counter, each module provides 3 PWM counters
  - Supports PWM triggerADC function
  - Supports up to 12 capture input channels with 16-bit resolution
- UART
  - Supports up to two sets of UART
  - Up to 1 Mbit/s baud rate

- Support 9600 baud rate at 32.768 kHz
- Up to two 16-byte FIFO UART controllers
- UART ports with flow control (TX, RX, nCTS and nRTS)
- Supports IrDA (SIR) function
- Supports LIN function
- Supports RS-485 9 bit mode and direction control.
- Programmable baud rate generator
- Supports PDMA mode
- Supports wake-up function (nCTS, incoming RX data, RS-485 AAD mode address matched or received FIFO is equal to the RFITL)

- SPI
  - Up to two sets of SPI controllers
  - Supports Master (max. 32 MHz) or Slave (max. 16 MHz) mode operation
  - Supports 1 bit and 2 bit transfer mode
  - Support Dual IO transfer mode
  - Configurable bit length of a transaction from 8 to 32-bit
  - Supports MSB first or LSB first transfer sequence
  - Two slave select lines supported in Master mode
  - Configurable byte or word suspend mode
  - Supports byte re-ordering function
  - Supports variable serial clock in Master mode
  - Provide separate 8-level depth transmit and receive FIFO buffer
  - Supports wake-up function(SPI clock toggle in Power-down mode)
  - Supports PDMA transfer
  - Supports 3-wires, no slave select signal, bi-direction interface
- I^2C
  - Up to two sets of I^2C device
  - Master/Slave up to 1 Mbit/s
  - Bi-directional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Built-in 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows
  - Programmable clocks allowing for versatile rate control

- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave addresses with mask option)
- Wake system up(address match) from Power-down mode

- ADC
  - 12-bit SAR ADC
  - Up to 12 channels: 8 external channel(PA.0 ~ PA.6 and PC.7) and 4 internal channels.
  - Four internal channels: internal reference voltage (Int_V_{REF}), Temperature sensor, AV_{DD}, and AV_{SS}.
  - Supports three reference voltage sources: V_{REF} pin, internal reference voltage (Int_V_{REF}: 2.5V/1.8V/1.5V), and AV_{DD}.
  - Supports Single Scan, Single Cycle Scan, and Continuous Scan mode
  - Each channel with individual result register
  - Threshold voltage detection (comparator function)
  - Conversion started by software programming or external input
  - Supports PDMA mode
  - Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3) to enable ADC
- SmartCard (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to two ISO-7816-3 ports
  - Separates receive/transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 267 ETU)
  - A 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detect the card is removal
  - Supports UART mode (full–duplex)
- ACMP
  - Supports one comparator
  - Analog input voltage range: 0~AV_{DD}
  - Supports Hysteresis function
- 96-bit unique ID

- 128-bit unique customer ID
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin(7x7) / 48-pin(7x7) / QFN33-pin(5x5)

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12/16 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NTC	Negative Temperature Coefficient
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PTC	Positive Temperature Coefficient
PT1000	Thermal Resistance
PWM	Pulse Width Modulation

QEI	Quadrature Encoder Interface
SDIO	Secure Digital Input/Output
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 4.1-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® Nano103 Series Selection Code

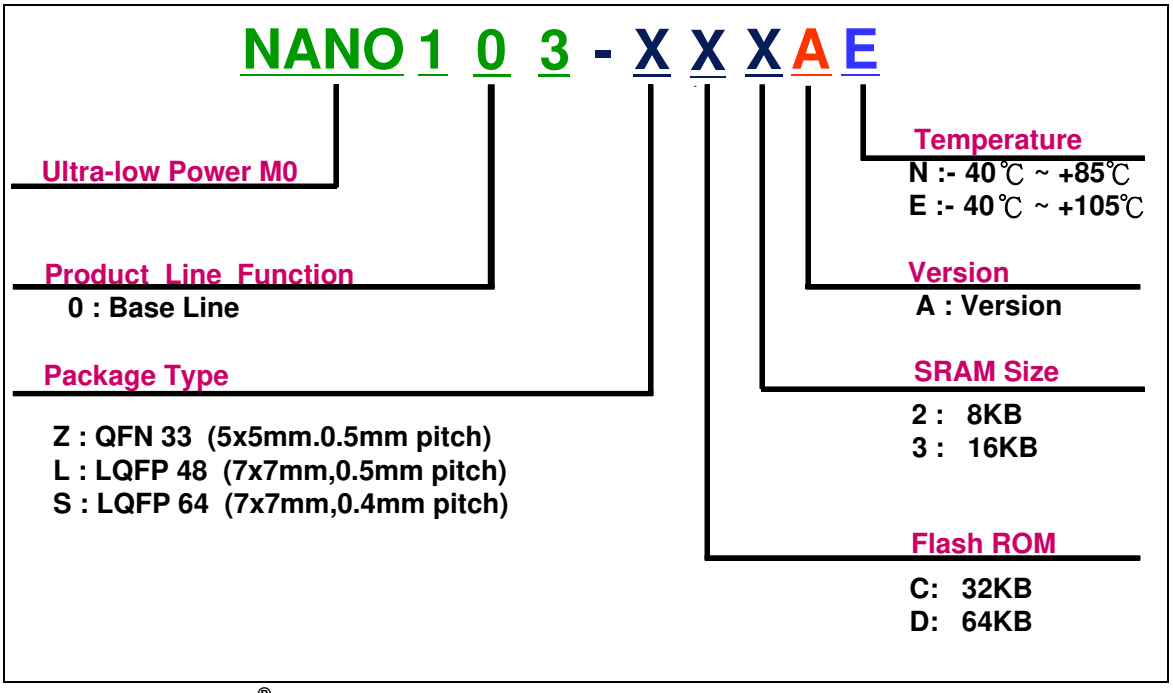

Figure 4.1-1 NuMicro® Nano103 Series Selection Code

4.2 NuMicro® Nano103 Products Selection Guide

Part No.	Flash	SRAM	Data Flash Shared AP ROM	SPROM (Security Protection)	KPROM (Key Protection)	LDROM (ISP Loader)	I/O	Timer	Connectivity			I²S	PWM	12-Bit ADC	ACMP	RTC	IRC 10KHz 4MHz 12/16MHz 36MHz	PDMA	Smart Card	ISP/ICP	Package
									UART	SPI	I²C										
NANO103ZD3AE	64K	16K	Config urable	0.5K	1K	4K	26	4x32-bit	2	4	2	-	2	6	1	V	V	4	2	V	QFN33
NANO103LD3AE	64K	16K	Config urable	0.5K	1K	4K	39	4x32-bit	2	4	2	-	6	8	1	V	V	4	2	V	LQFP48
NANO103SD3AE	64K	16K	Config urable	0.5K	1K	4K	53	4x32-bit	2	4	2	-	6	8	1	V	V	4	2	V	LQFP64

4.3 Pin Configuration

4.3.1 NuMicro® Nano103 Pin Diagrams

4.3.1.1 NuMicro® Nano103 LQFP 64-pin

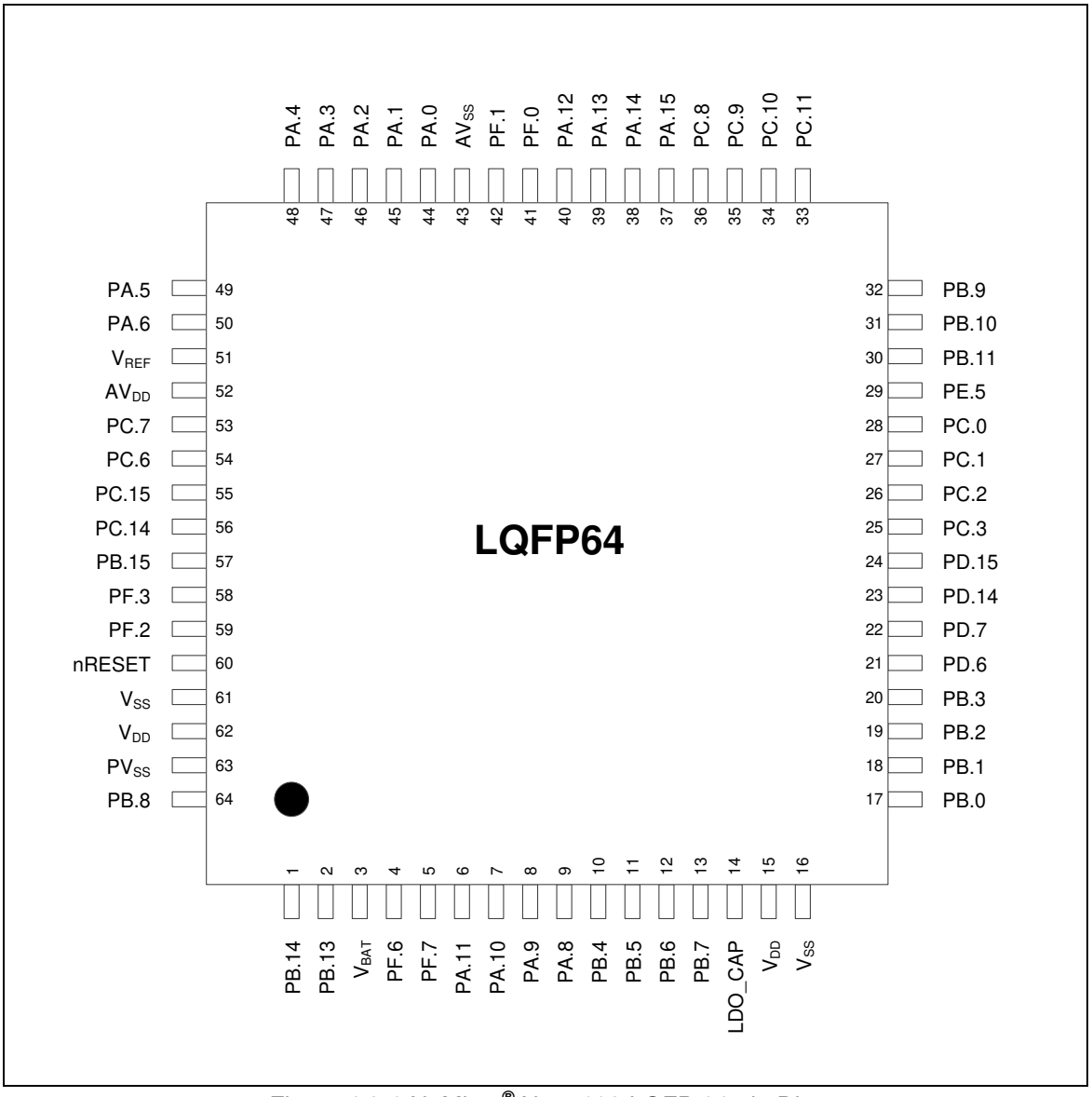

Figure 4.3-1 NuMicro® Nano103 LQFP 64-pin Diagram

4.3.1.2 NuMicro® Nano103 LQFP 48-pin

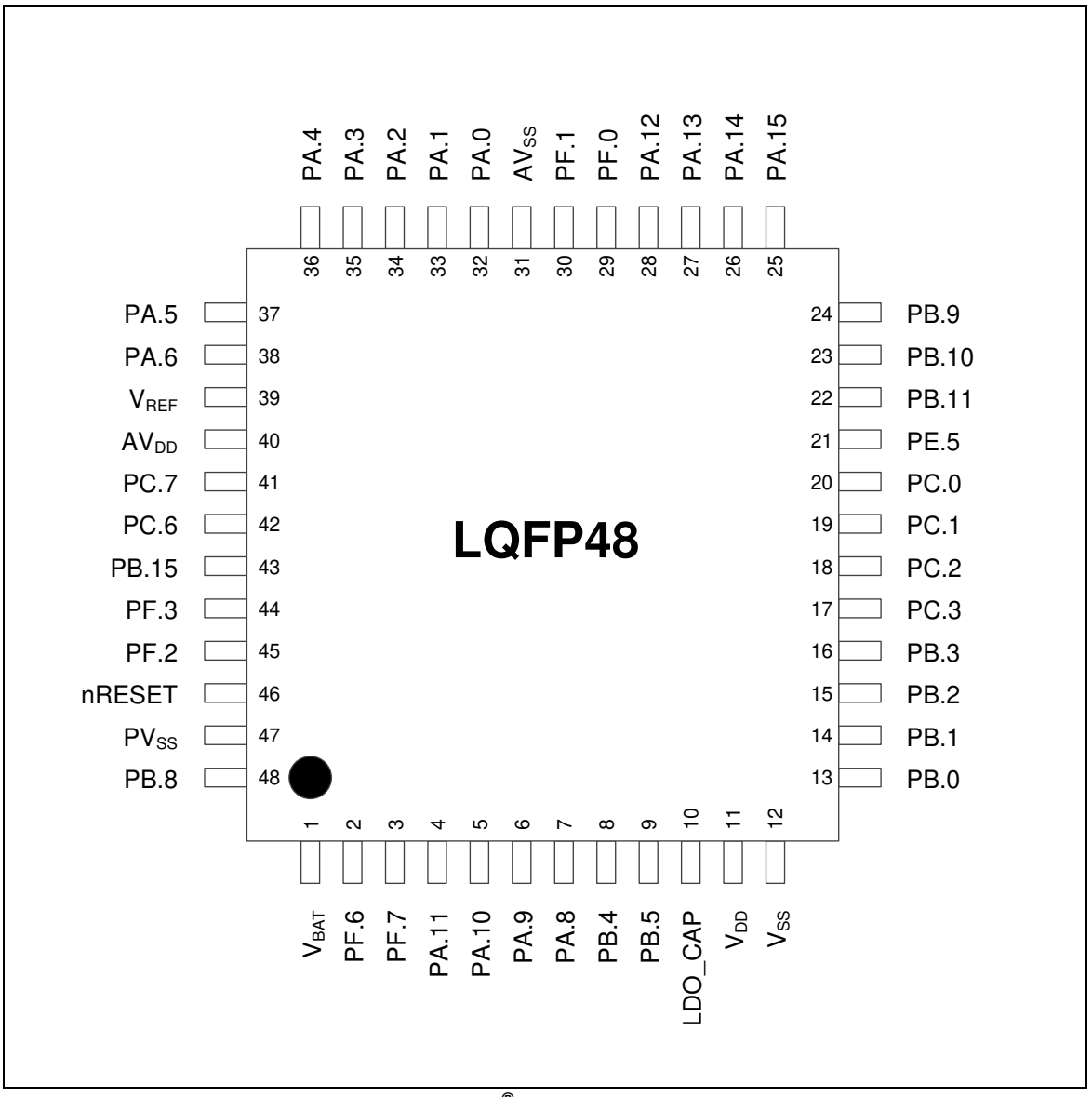

Figure 4.3-2 NuMicro® Nano103 LQFP 48-pin Diagram

4.3.1.3 NuMicro® Nano103 QFN33-pin

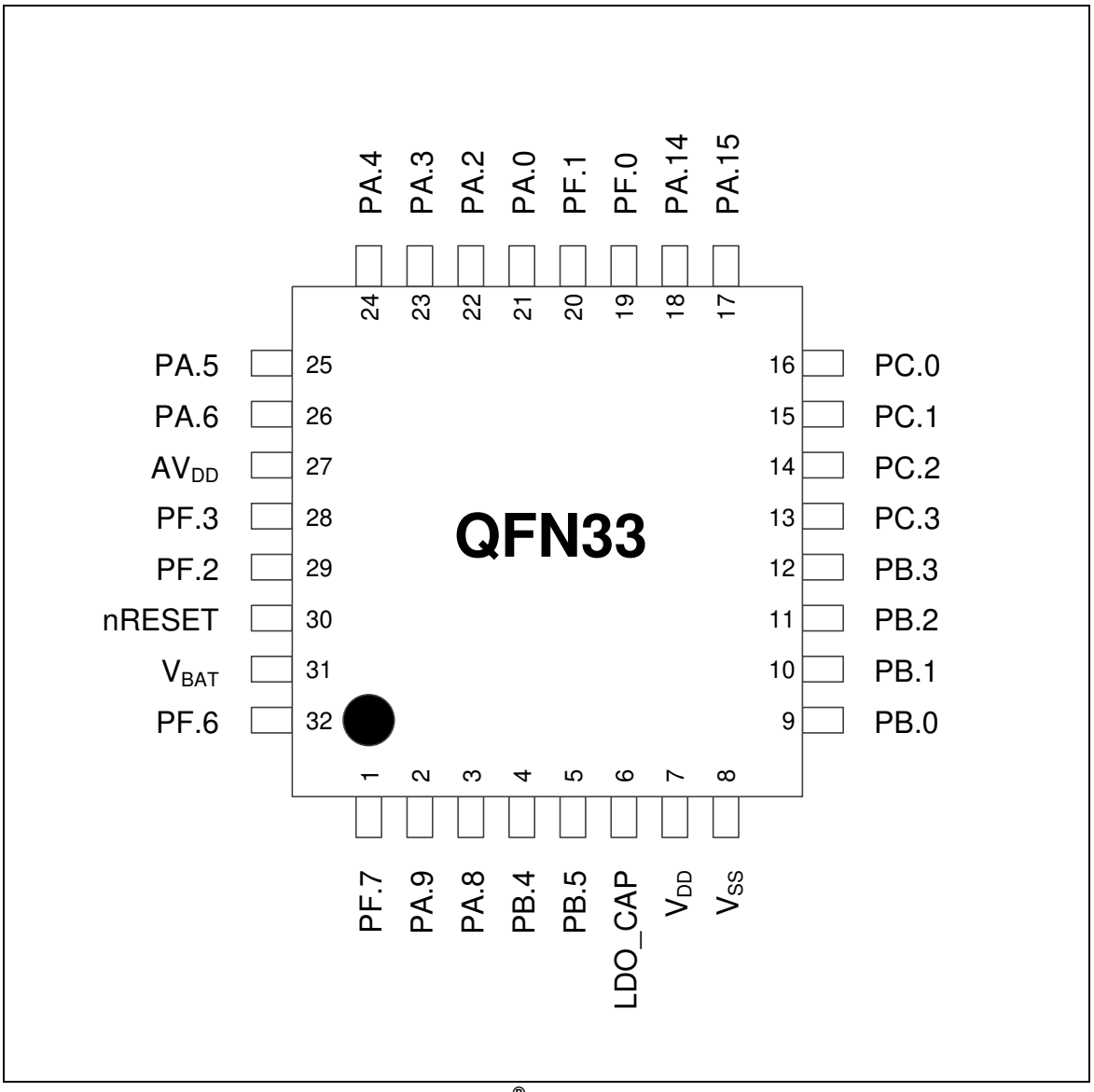

Figure 4.3-3 NuMicro® Nano103 QFN33-pin Diagram

4.4 Pin Description

4.4.1 NuMicro® Nano103 Pin Description

Pin No.			Pin Name	Pin Type	MFP*	Description
64-pin	48-pin	32-pin				
1	-	-	PB.14	I/O	MFP0	General purpose digital I/O pin.
			INT0	I	MFP1	External interrupt0 input pin.
			SPI2_MOSI1	I/O	MFP3	SPI2 2nd MOSI (Master Out, Slave In) pin.
			SPI2_SS1	I/O	MFP4	SPI2 2nd slave select pin.
2	-	-	PB.13	I/O	MFP0	General purpose digital I/O pin.
			SPI2_MISO1	I/O	MFP3	SPI2 2nd MISO (Master In, Slave Out) pin.
			TAMPER	I	MFP7	Tamper pin.
3	1	31	V_{BAT}	P	MFP0	Power supply for tamper pin (LQFP64: PB.13/LQFP48: PA.9/QFN32: PB.8) and RTC.
4	2	32	PF.6	I/O	MFP0	General purpose digital I/O pin.
			I2C1_SDA	I/O	MFP1	I^2C1 data input/output pin.
			X32_OUT	O	MFP7	External 32.768 kHz crystal output pin(default).
5	3	1	PF.7	I/O	MFP0	General purpose digital I/O pin.
			I2C1_SCL	I/O	MFP1	I^2C1 clock pin.
			SC0_CD	I	MFP3	SmartCard0 card detect pin.
			X32_IN	I	MFP7	External 32.768 kHz crystal input pin(default).
-	-	2	PA.9	I/O	MFP0	General purpose digital I/O pin.
			I2C0_SCL	I/O	MFP1	I^2C0 clock pin.
			TM1_CNT	I	MFP2	Timer1 event counter input.
			SC0_DAT	I/O	MFP3	SmartCard0 data pin.
			SPI2_CLK	I/O	MFP4	SPI2 serial clock pin.
			TM1_OUT	O	MFP5	Timer1 toggle output.
			UART1_nRTS	O	MFP6	UART1 Request to Send output pin.
			TAMPER	I	MFP7	Tamper pin.
6	4	-	PA.11	I/O	MFP0	General purpose digital I/O pin.
			I2C1_SCL	I/O	MFP1	I^2C1 clock pin.
			TM3_CNT	I	MFP2	Timer3 event counter input.
			SC0_RST	O	MFP3	SmartCard0 reset pin.
			SPI2_MOSI0	I/O	MFP4	SPI2 1st MOSI (Master Out, Slave In) pin.
			TM3_OUT	O	MFP5	Timer3 toggle output.

Pin No.			Pin Name	Pin Type	MFP*	Description
64-pin	48-pin	32-pin				
7	5	-	PA.10	I/O	MFP0	General purpose digital I/O pin.
			I2C1_SDA	I/O	MFP1	I^2C1 data input/output pin.
			TM2_CNT	I	MFP2	Timer2 event counter input.
			SC0_PWR	O	MFP3	SmartCard0 power pin.
			SPI2_MISO0	I/O	MFP4	SPI2 1st MISO (Master In, Slave Out) pin.
			TM2_OUT	O	MFP5	Timer2 toggle output.
8	6	-	PA.9	I/O	MFP0	General purpose digital I/O pin.
			I2C0_SCL	I/O	MFP1	I^2C0 clock pin.
			TM1_CNT	I	MFP2	Timer1 event counter input.
			SC0_DAT	I/O	MFP3	SmartCard0 data pin.
			SPI2_CLK	I/O	MFP4	SPI2 serial clock pin.
			TM1_OUT	O	MFP5	Timer1 toggle output.
			UART1_nRTS	O	MFP6	UART1 Request to Send output pin.
			TAMPER	I	MFP7	Tamper pin.
9	7	3	PA.8	I/O	MFP0	General purpose digital I/O pin.
			I2C0_SDA	I/O	MFP1	I^2C0 data input/output pin.
			TM0_CNT	I	MFP2	Timer0 event counter input.
			SC0_CLK	O	MFP3	SmartCard0 clock pin.
			SPI2_SS0	I/O	MFP4	SPI2 1st slave select pin.
			TM0_OUT	O	MFP5	Timer0 toggle output.
			UART1_nCTS	I	MFP6	UART1 Clear to Send input pin.
10	8	4	PB.4	I/O	MFP0	General purpose digital I/O pin.
			UART1_RXD	I	MFP1	Data receiver input pin for UART1.
			SC0_CD	I	MFP3	SmartCard0 card detect pin.
			SPI2_SS0	I/O	MFP4	SPI2 1st slave select pin.
			RTC_HZ	O	MFP6	RTC 1Hz output.
11	9	5	PB.5	I/O	MFP0	General purpose digital I/O pin.
			UART1_TXD	O	MFP1	Data transmitter output pin for UART1.
			SC0_RST	O	MFP3	SmartCard0 reset pin.
			SPI2_CLK	I/O	MFP4	SPI2 serial clock pin.
12	-	-	PB.6	I/O	MFP0	General purpose digital I/O pin.
			UART1_RSTn	O	MFP1	UART1 Request to Send output pin.
			SPI2_MISO0	I/O	MFP4	SPI2 1st MISO (Master In, Slave Out) pin.

Pin No.			Pin Name	Pin Type	MFP*	Description
64-pin	48-pin	32-pin				
13	-	-	PB.7	I/O	MFP0	General purpose digital I/O pin.
			UART1_nCTS	I	MFP1	UART1 Clear to Send input pin.
			SPI2_MOSI0	I/O	MFP4	SPI21st MOSI (Master Out, Slave In) pin.
14	10	6	LDO_CAP	AO	MFP0	LDO output pin.
15	11	7	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital function.
16	12	8	V_{SS}	G	MFP0	Ground pin for digital circuit.
17	13	9	PB.0	I/O	MFP0	General purpose digital I/O pin.
			UART0_RXD	I	MFP1	Data receiver input pin for UART0.
			SPI1_MOSI0	I/O	MFP3	SPI11st MOSI (Master Out, Slave In) pin.
18	14	10	PB.1	I/O	MFP0	General purpose digital I/O pin.
			UART0_TXD	O	MFP1	Data transmitter output pin for UART0.
			SPI1_MISO0	I/O	MFP3	SPI11st MISO (Master In, Slave Out) pin.
19	15	11	PB.2	I/O	MFP0	General purpose digital I/O pin.
			UART0_nRTS	O	MFP1	UART0 Request to Send output pin.
			SPI1_CLK	I/O	MFP3	SPI1 serial clock pin.
			CLKO	O	MFP4	Frequency Divider output pin.
20	16	12	PB.3	I/O	MFP0	General purpose digital I/O pin.
			UART0_nCTS	I	MFP1	UART0 Clear to Send input pin.
			SPI1_SS0	I/O	MFP3	SPI1 1st slave select pin.
			SC1_CD	I	MFP4	SmartCard1 card detect pin.
21	-	-	PD.6	I/O	MFP0	General purpose digital I/O pin.
			SPI1_MOSI1	I/O	MFP3	SPI1 2nd MOSI (Master Out, Slave In) pin.
			SC1_RST	O	MFP4	SmartCard1 reset pin.
22	-	-	PD.7	I/O	MFP0	General purpose digital I/O pin.
			SPI1_MISO1	I/O	MFP3	SPI1 2nd MISO (Master In, Slave Out) pin.
			SC1_PWR	O	MFP4	SmartCard1 power pin.
23	-	-	PD.14	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MOSI1	I/O	MFP1	SPI0 2nd MOSI (Master Out, Slave In) pin.
			SC1_DAT	I/O	MFP4	SmartCard1 data pin.
24	-	-	PD.15	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MISO1	I/O	MFP1	SPI0 2nd MISO (Master In, Slave Out) pin.
			SC1_CLK	O	MFP4	SmartCard1 clock pin.
25	17	13	PC.3	I/O	MFP0	General purpose digital I/O pin.

Pin No.			Pin Name	Pin Type	MFP*	Description
64-pin	48-pin	32-pin				
			SPI0_MOSI0	I/O	MFP1	SPI0 1st MOSI (Master Out, Slave In) pin.
			SC1_RST	O	MFP4	SmartCard1 reset pin.
			PWM0_BRAKE0	I	MFP5	PWM0 Brake0 input pin .
26	18	14	PC.2	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MISO0	I/O	MFP1	SPI0 1st MISO (Master In, Slave Out) pin.
			SC1_PWR	O	MFP4	SmartCard1 power pin.
			PWM0_BRAKE1	I	MFP5	PWM0 Brake1 input pin.
27	19	15	PC.1	I/O	MFP0	General purpose digital I/O pin.
			SPI0_CLK	I/O	MFP1	SPI0 serial clock pin.
			SC1_DAT	I/O	MFP4	SmartCard1 data pin.
			PWM0_BRAKE0	I	MFP5	PWM0 Brake0 input pin.
28	20	16	PC.0	I/O	MFP0	General purpose digital I/O pin.
			SPI0_SS0	I/O	MFP1	SPI0 1st slave select pin.
			SC1_CLK	O	MFP4	SmartCard1 clock pin.
			PWM0_BRAKE1	I	MFP5	PWM0 Brake1 input pin..
29	21	-	PE.5	I/O	MFP0	General purpose digital I/O pin.
			PWM0_CH5	I/O	MFP1	PWM0 channel5 output/capture input.
			RTC_HZ	O	MFP6	RTC 1Hz output.
30	22	-	PB.11	I/O	MFP0	General purpose digital I/O pin.
			PWM0_CH4	I/O	MFP1	PWM0 channel4 output/capture input.
			TM3_CNT	I	MFP2	Timer3 event counter input.
			TM3_OUT	O	MFP4	Timer3 toggle output.
			SPI0_MISO0	I/O	MFP5	SPI0 1st MISO (Master In, Slave Out) pin.
31	23	-	PB.10	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MOSI0	I/O	MFP1	SPI0 1st MOSI (Master Out, Slave In) pin.
			TM2_CNT	I	MFP2	Timer2 event counter input.
			TM2_OUT	O	MFP4	Timer2 toggle output.
			SPI0_SS1	I/O	MFP5	SPI0 2nd slave select pin.
32	24	-	PB.9	I/O	MFP0	General purpose digital I/O pin.
			SPI1_SS1	I/O	MFP1	SPI1 1st slave select pin.
			TM1_CNT	I	MFP2	Timer1 event counter input.
			TM1_OUT	O	MFP4	Timer1 toggle output.
			INT0	I	MFP5	External interrupt0 input pin.

Pin No.			Pin Name	Pin Type	MFP*	Description
64-pin	48-pin	32-pin				
33	-	-	PC.11	I/O	MFP0	General purpose digital I/O pin.
			SPI1_MOSI0	I/O	MFP1	SPI1 1st MOSI (Master Out, Slave In) pin.
			UART1_TXD	O	MFP5	Data transmitter output pin for UART1.
34	-	-	PC.10	I/O	MFP0	General purpose digital I/O pin.
			SPI1_MISO0	I/O	MFP1	SPI1 1st MISO (Master In, Slave Out) pin.
			UART1_RXD	I	MFP5	Data receiver input pin for UART1.
35	-	-	PC.9	I/O	MFP0	General purpose digital I/O pin.
			SPI1_CLK	I/O	MFP1	SPI1 serial clock pin.
			I2C1_SCL	I/O	MFP5	I^2C1 clock pin.
36	-	-	PC.8	I/O	MFP0	General purpose digital I/O pin.
			SPI1_SS0	I/O	MFP1	SPI1 1st slave select pin.
			I2C1_SDA	I/O	MFP5	I^2C1 data input/output pin.
37	25	17	PA.15	I/O	MFP0	General purpose digital I/O pin.
			PWM0_CH3	I/O	MFP1	PWM0 channel3 output/capture input.
			I2C1_SCL	I/O	MFP2	I^2C1 clock pin.
			TM3_EXT	I	MFP3	Timer3 external capture input.
			SC0_PWR	O	MFP4	SmartCard0 power pin.
			TM3_CNT	I	MFP5	Timer3 event counter input.
			UART0_TXD	O	MFP6	Data transmitter output pin for UART0.
			TM3_OUT	O	MFP7	Timer3 toggle output.
38	26	18	PA.14	I/O	MFP0	General purpose digital I/O pin.
			PWM0_CH2	I/O	MFP1	PWM0 channel2 output/capture input.
			I2C1_SDA	I/O	MFP2	I^2C1 data input/output pin.
			TM2_EXT	I	MFP3	Timer2 external capture input.
			TM2_CNT	I	MFP5	Timer2 event counter input.
			UART0_RXD	I	MFP6	Data receiver input pin for UART0.
			TM2_OUT	O	MFP7	Timer2 toggle output.
39	27	-	PA.13	I/O	MFP0	General purpose digital I/O pin.
			PWM0_CH1	I/O	MFP1	PWM0 channel1 output/capture input.
			TM1_EXT	I	MFP3	Timer1 external capture input.
			I2C0_SCL	I/O	MFP5	I^2C0 clock pin.
40	28	-	PA.12	I/O	MFP0	General purpose digital I/O pin.
			PWM0_CH0	I/O	MFP1	PWM0 channel0 output/capture input.

Pin No.			Pin Name	Pin Type	MFP*	Description
64-pin	48-pin	32-pin				
			TM0_EXT	I	MFP3	Timer0 external capture input.
			I2C0_SDA	I/O	MFP5	I^2C0 data input/output pin.
41	29	19	PF.0	I/O	MFP0	General purpose digital I/O pin.
			INT0	I	MFP5	External interrupt0 input pin.
			ICE_DAT	I/O	MFP7	Serial wired debugger data pin
42	30	20	PF.1	I/O	MFP0	General purpose digital I/O pin.
			CLKO	O	MFP4	Frequency Divider output pin.
			INT1	I	MFP5	External interrupt1 input pin.
			ICE_CLK	I	MFP7	Serial wired debugger clock pin.
43	31	-	AV_{SS}	G	MFP0	Ground pin for analog circuit.
44	32	21	PA.0	I/O	MFP0	General purpose digital I/O pin.
			ADC_CH0	AI	MFP1	ADC analog input0.
			ACMP0_P	AI	MFP2	Comparator0 P-end input.
			TM2_EXT	I	MFP3	Timer2 external capture input.
			PWM0_CH2	I/O	MFP5	PWM0 channel2 output/capture input.
			SPI3_MOSI1	I/O	MFP6	SPI3 2^{nd}MOSI (Master Out, Slave In) pin.
45	33	-	PA.1	I/O	MFP0	General purpose digital I/O pin.
			ADC_CH1	AI	MFP1	ADC analog input1.
			ACMP0_N	AI	MFP2	Comparator0 N-end input.
			SPI3_MISO1	I/O	MFP6	SPI3 2^{nd} MISO (Master In, Slave Out) pin.
46	34	22	PA.2	I/O	MFP0	General purpose digital I/O pin.
			ADC_CH2	AI	MFP1	ADC analog input2.
			UART1_RXD	I	MFP5	Data receiver input pin for UART1.
47	35	23	PA.3	I/O	MFP0	General purpose digital I/O pin.
			ADC_CH3	AI	MFP1	ADC analog input3.
			UART1_TXD	O	MFP5	Data transmitter output pin for UART1.
			SPI3_MOSI0	I/O	MFP6	SPI3 1^{st} MOSI (Master Out, Slave In) pin.
48	36	24	PA.4	I/O	MFP0	General purpose digital I/O pin.
			ADC_CH4	AI	MFP1	ADC analog input4.
			I2C0_SDA	I/O	MFP5	I^2C0 data input/output pin.
			SPI3_MISO0	I/O	MFP6	SPI3 1^{st} MISO (Master In, Slave Out) pin.
49	37	25	PA.5	I/O	MFP0	General purpose digital I/O pin.
			ADC_CH5	AI	MFP1	ADC analog input5.