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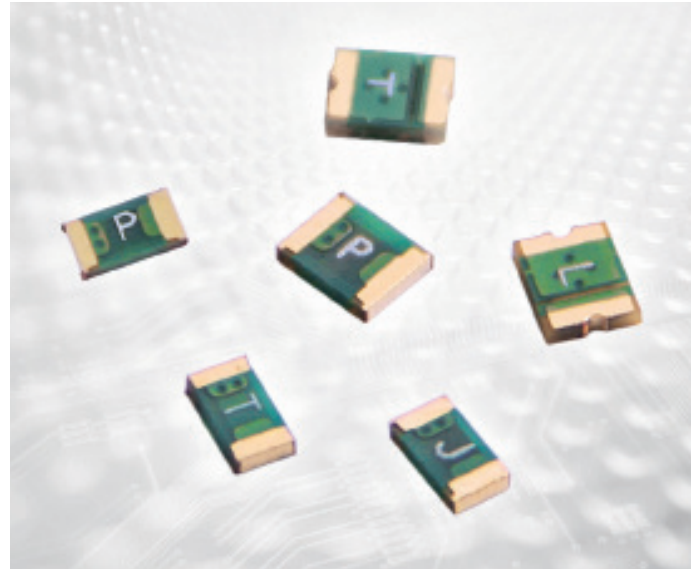


POLYSWITCH RESETTABLE DEVICES

Low Resistivity SMD Devices

The low resistivity SMD (surface-mount device) series is well suited to space-constrained mobile applications. The devices can help provide both overcurrent and overtemperature protection for battery pack PCMs (protection circuit modules) used in compact consumer devices such as smartphones and MP3/MP4 media players. In particular, the low resistivity SMD series helps battery pack suppliers achieve their design goals and simplify their installation methods.

The low resistivity SMD series comprises eleven devices. In the model number descriptions, the “micro” prefix refers to the 1210 form factor and the “nano” prefix refers to the 1206 form factor.



BENEFITS

- Helps save board space and power consumption, and therefore costs, in space-constrained mobile electronics
- Are more compact in comparison with similar offerings and are available in an industry-standard form factor
- Can be assembled with a reflowable soldering technique, as opposed to the spot welding process required by many other components
- Maximum electrical rating: Voltage $6V_{DC}$ and short circuit current 50A
- Industry-standard form factor of 1210 (3.0mmx2.54mm; or 0.12inx0.10in), or 1206 (3.0mmx1.52mm; or 0.12inx0.060in)
- Useful for an operating current of 2A and above
- Useful for and packaged for surface mounting on the PCB

FEATURES

- RoHS compliant
- Halogen free (refers to: Br \geq 900ppm, Cl \geq 900ppm, Br+Cl \geq 1500ppm)
- Current ratings from 1.75 to 5.0A

APPLICATIONS

- Mobile and smart phones
- Media players (MP3/MP4)
- Digital still and video cameras
- Mini notebooks
- Tablets

- Agency recognition: UL, CSA, TÜV
- Small footprint
- Fast time-to-trip

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Table LR1 – Thermal Derating [Hold Current (A) at Ambient Temperature (°C)]

Part Number	Maximum Ambient Temperature										
	-40°C	-20°C	0°C	20°C	25°C	40°C	50°C	60°C	70°C	80°C	85°C
nanoSMDLR Series Size 3216mm/1206mils											
nanoSMD175LR	3.00	2.60	2.20	1.75	1.70	1.40	1.20	1.00	0.80	0.60	0.50
nanoSMD200LR	3.60	3.20	2.80	2.00	1.90	1.80	1.60	1.40	1.20	1.00	0.80
nanoSMD270LR	4.00	3.50	3.00	2.70	2.60	2.20	2.00	1.60	1.40	1.20	1.10
nanoSMD350LR	5.50	4.80	4.00	3.50	3.30	2.70	2.30	1.90	1.60	1.40	1.30
nanoSMD500LR	7.40	6.60	6.00	5.00	4.90	4.60	4.20	3.70	3.30	3.00	2.80
microSMDLR Series Size 3225mm/1210mils											
microSMD190LR	3.40	2.90	2.40	1.90	1.80	1.40	1.15	0.90	0.65	0.40	0.28
microSMD200LR	3.50	3.00	2.50	2.00	1.90	1.50	1.25	1.00	0.75	0.50	0.38
microSMD250LR	4.40	3.80	3.20	2.50	2.40	1.90	1.60	1.30	1.00	0.65	0.50
microSMD350LR	5.40	4.75	4.00	3.50	3.20	2.70	2.40	2.00	1.70	1.35	1.20
microSMD450LR	7.00	6.20	5.50	4.50	4.40	3.80	3.50	3.20	2.75	2.35	2.16

Figure LR1 – Thermal Derating Curve

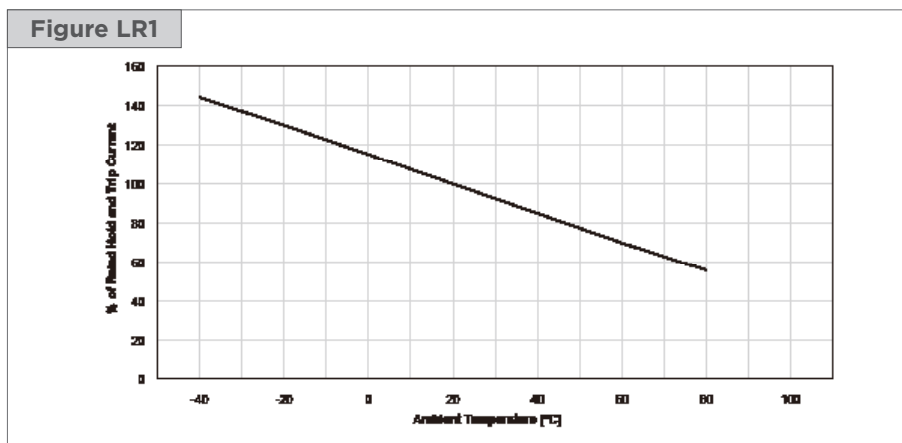


Table LR2 – Electrical Characteristics for low resistivity SMD Devices at Room Temperature

Part Number	I_H	I_T	V_{MAX}	I_{MAX}	$P_{D MAX}$	Max Time-to-Trip		R_{MIN}	R_{1MAX}	Figure for Dimensions
	(A)	(A)	(V _{DC})	(A)	(W)	(A)	(S)	(Ω)	(Ω)	
nanoSMDLR Series Size 3216mm/1206mils										
nanoSMD175LR	1.75	5.00	6	50	1.00	9.50	1.00	0.008	0.034	LR2
nanoSMD200LR	2.00	6.00	6	50	1.00	9.50	3.00	0.006	0.024	LR2
nanoSMD270LR	2.70	6.30	6	50	1.00	8.00	5.00	0.005	0.018	LR2
nanoSMD350LR	3.50	6.30	6	50	1.00	8.00	5.00	0.004	0.018	LR2
nanoSMD500LR	5.00	10.00	6	50	1.00	25.00	2.00	0.002	0.008	LR2
microSMDLR Series Size 3225mm/1210mils										
microSMD190LR	1.90	4.90	6	50	1.00	9.50	4.00	0.006	0.021	LR3
microSMD200LR	2.00	5.00	6	50	1.00	9.50	4.00	0.006	0.021	LR3
microSMD250LR	2.50	5.20	6	50	1.00	9.50	5.00	0.005	0.018	LR3
microSMD350LR	3.50	9.00	6	50	1.00	9.50	10.00	0.0025	0.011	LR2
microSMD450LR	4.50	9.00	5	50	1.00	25.00	2.00	0.002	0.008	LR3

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Figures LR2-LR3 – Dimensions Figures

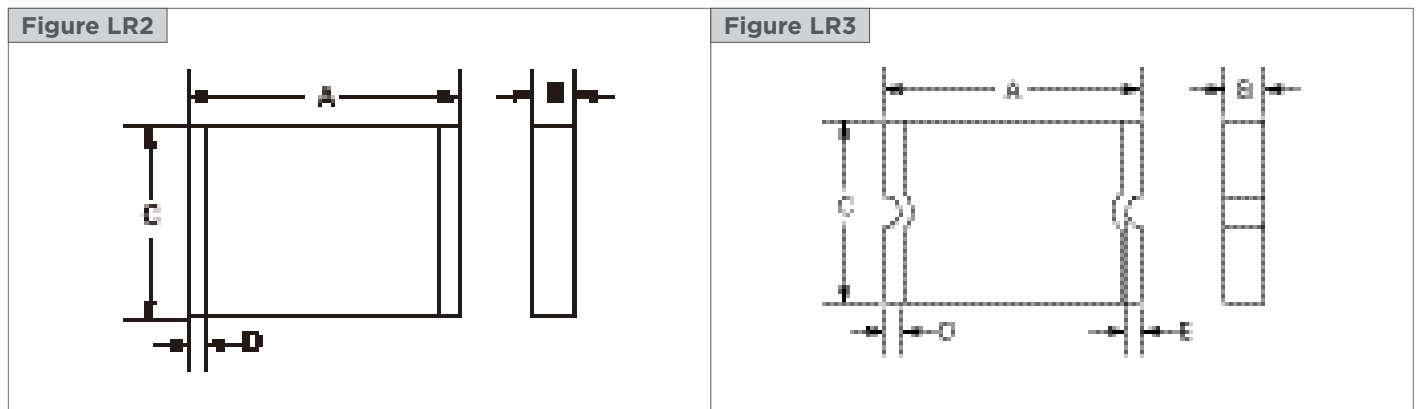


Table LR3 – Dimensions in Millimeters (Inches)

Part Number	A		B		C		D		E	Figure
	Min	Max	Min	Max	Min	Max	Min	Max	Min	
nanoSMDLR Series										
Size 3216mm/1206mils										
nanoSMD175LR	3.00 (0.118)	3.43 (0.135)	0.50 (0.019)	1.00 (0.039)	1.37 (0.054)	1.85 (0.073)	0.25 (0.010)	0.75 (0.030)	—	LR2
nanoSMD200LR	3.00 (0.118)	3.43 (0.135)	0.50 (0.019)	1.00 (0.039)	1.37 (0.054)	1.85 (0.073)	0.25 (0.010)	0.75 (0.030)	—	LR2
nanoSMD270LR	3.00 (0.118)	3.43 (0.135)	0.50 (0.019)	1.00 (0.039)	1.37 (0.054)	1.85 (0.073)	0.25 (0.010)	0.75 (0.030)	—	LR2
nanoSMD350LR	3.00 (0.118)	3.43 (0.135)	0.50 (0.019)	1.00 (0.039)	1.37 (0.054)	1.85 (0.073)	0.25 (0.010)	0.75 (0.030)	—	LR2
nanoSMD500LR	3.00 (0.118)	3.43 (0.135)	0.50 (0.019)	0.80 (0.031)	1.37 (0.054)	1.85 (0.073)	0.25 (0.010)	0.75 (0.030)	—	LR2
microSMDLR Series										
Size 3225mm/1210mils										
microSMD190LR	3.00 (0.118)	3.43 (0.135)	0.50 (0.019)	1.00 (0.039)	2.35 (0.092)	2.80 (0.110)	0.25 (0.010)	0.75 (0.030)	0.076 (0.003)	LR3
microSMD200LR	3.00 (0.118)	3.43 (0.135)	0.50 (0.019)	1.00 (0.039)	2.35 (0.092)	2.80 (0.110)	0.25 (0.010)	0.75 (0.030)	0.076 (0.003)	LR3
microSMD250LR	3.00 (0.118)	3.43 (0.135)	0.50 (0.019)	1.00 (0.039)	2.35 (0.092)	2.80 (0.110)	0.25 (0.010)	0.75 (0.030)	0.076 (0.003)	LR3
microSMD350LR	3.00 (0.118)	3.43 (0.135)	0.50 (0.019)	1.00 (0.039)	2.35 (0.092)	2.80 (0.110)	0.25 (0.010)	0.75 (0.030)	—	LR2
microSMD450LR	3.00 (0.118)	3.43 (0.135)	0.50 (0.019)	1.00 (0.039)	2.35 (0.092)	2.80 (0.110)	0.25 (0.010)	0.75 (0.030)	0.076 (0.003)	LR3

Table LR4 – Physical Characteristics Operating Temperature Range -40°C to 85°C

Physical Characteristics	
Terminal Pad Material	Gold with Nickel Underplate
Soldering Characteristics	ANSI/J-STD-002 Category 3
Solder Heat Withstand	per IEC-STD 68-2-20, Test Tb, Section 5, Method 1A
Flammability Resistance	per IEC 695-2-2 Needle Flame Test for 20 sec.
Recommended Storage Conditions	40°C max, 70% R.H. max; Devices May Not Meet Specified Ratings if Storage Conditions Are Exceeded.

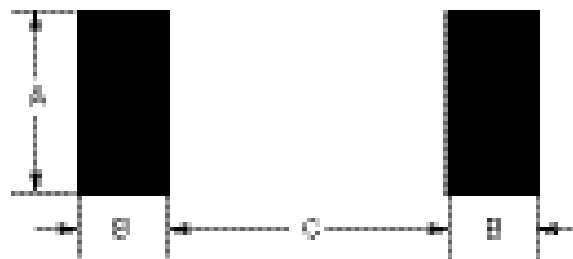
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Table LR5 – Packaging and Marking Information

Part Number	Tape & Reel Quantity	Standard Package	Part Marking	Recommended Pad Layout Figures [mm (in)]			Agency Recognition
				Dimension A (Nom)	Dimension B (Nom)	Dimension C (Nom)	
nanoSMDLR Series Size 3216mm/1206mils							
nanoSMD175LR	3,000	15,000	J	1.75 (0.069)	1.10 (0.043)	2.00 (0.079)	UL, CSA, TÜV
nanoSMD200LR	3,000	15,000	T	1.75 (0.069)	1.10 (0.043)	2.00 (0.079)	UL, CSA
nanoSMD270LR	3,000	15,000	L	1.75 (0.069)	1.10 (0.043)	2.00 (0.079)	UL, CSA, TÜV
nanoSMD350LR	3,000	15,000	P	1.75 (0.069)	1.10 (0.043)	2.00 (0.079)	UL, CSA, TÜV
nanoSMD500LR	3,000	15,000	H	1.75 (0.069)	1.10 (0.043)	2.00 (0.079)	UL, CSA, TÜV
microSMDLR Series Size 3225mm/1210mils							
microSMD190LR	3,000	15,000	None	2.65 (0.104)	1.00 (0.039)	2.00 (0.079)	UL, CSA
microSMD200LR	3,000	15,000	T	2.65 (0.104)	1.00 (0.039)	2.00 (0.079)	UL, CSA
microSMD250LR	3,000	15,000	L	2.65 (0.104)	1.00 (0.039)	2.00 (0.079)	UL, CSA
microSMD350LR	3,000	15,000	P	2.65 (0.104)	1.10 (0.043)	2.00 (0.079)	UL, CSA
microSMD450LR	3,000	15,000	H	2.65 (0.104)	1.00 (0.039)	2.00 (0.079)	UL

Figure LR4 – Recommended Pad Layout



Agency Recognition

UL	File # E74889 for all low resistivity SMD Devices
CSA	File # CA78165 for all low resistivity SMD Devices
TÜV	Certificate Number Available Upon Request (Certified to IEC 60730-1)

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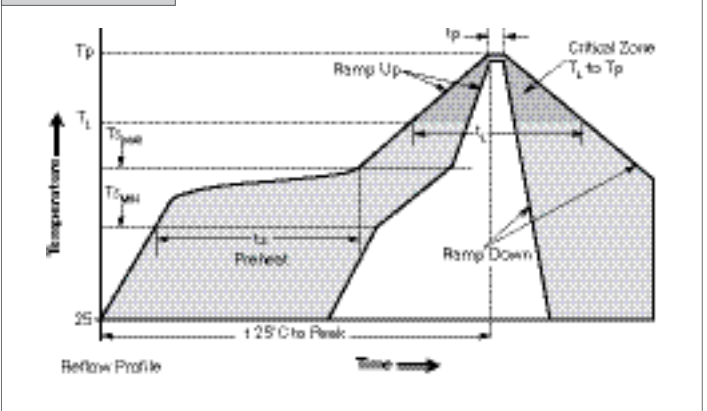
Solder Reflow Recommendation

Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Average Ramp-up Rate (Ts_{MAX} to Tp)	3°C/s max
Preheat	
• Temperature min (Ts _{MIN})	150°C
• Temperature max (Ts _{MAX})	200°C
• Time (ts _{MIN} to ts _{MAX})	60-120s
Time Maintained Above:	
• Temperature (T _L)	217°C
• Time (t _L)	60-150s
Peak/Classification Temperature (Tp)	260°C
Time within 5°C of Actual Peak Temperature	
Time (tp)	30s max
Ramp-down Rate	2°C/s max
Time 25°C to Peak Temperature	8 mins max

Note: All temperatures refer to topside of the package measured on the package body surface.

Figure LR5



Solder Reflow

- Recommended reflow methods:
 - IR
 - Hot air
 - Nitrogen
- Recommended maximum paste thickness: 0.25mm (0.010 inch)
- Devices can be cleaned using standard methods and aqueous solvents.
- Experience has shown the optimum conditions for forming acceptable solder fillets occur when a reasonable amount of solder paste is placed underneath each device's termination. As such, we request that customers comply with our recommended solder pad layouts.
- Customer should validate that the solder paste amount and reflow recommendations meet its application.
- We request that customer board layouts refrain from placing raised features (e.g. vias, nomenclature, traces, etc.) underneath PolySwitch devices. It is possible that raised features could negatively impact solderability performance of our devices.

Table LR6 – Tape and Reel Specifications in Millimeters

Description	nanoSMDLR Series EIA 481-1	microSMDLR Series EIA 481-1
W	8.0 ± 0.30	8.0 ± 0.30
P ₀	4.0 ± 0.10	4.0 ± 0.10
P ₁	4.0 ± 0.10	4.0 ± 0.10
P ₂	2.0 ± 0.05	2.0 ± 0.05
A ₀	1.95 ± 0.10	2.9 ± 0.10
B ₀	3.50 +0.1/-0.08	3.55 ± 0.10
B ₁ MAX	4.35	4.35
D ₀	1.55 ± 0.05	1.55 ± 0.05
F	3.50 ± 0.05	3.50 ± 0.05
E ₁	1.75 ± 0.10	1.75 ± 0.10
E ₂ MIN	6.25	6.25
T MAX	0.3	0.3
T ₁ MAX	0.1	0.1
K ₀	0.89 ± 0.10	1.27 ± 0.10
A MAX	185	185
N MIN	50	50
W ₁	12.4 + 2.0/-0.0	12.4 + 2.0/-0.0
W ₂ MAX	14.4	14.4

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Figure LR6 – EIA Referenced Taped Component Dimensions

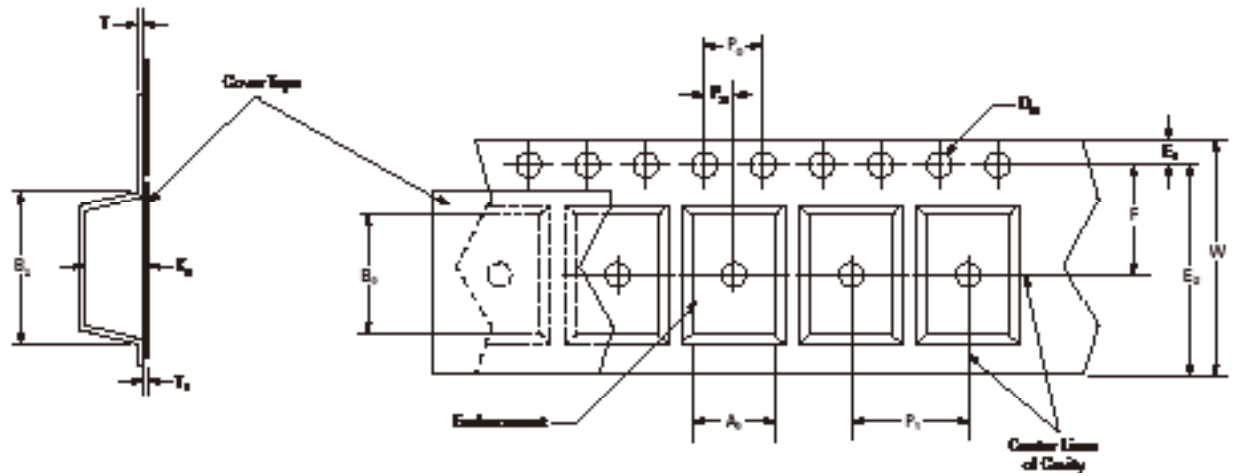
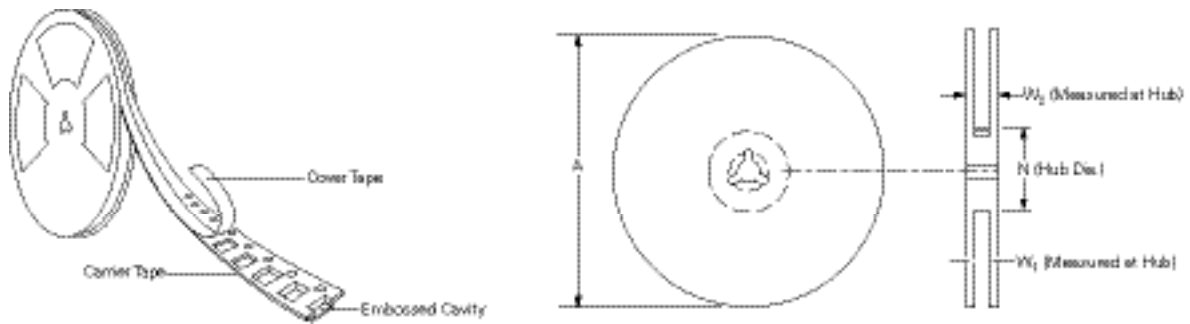


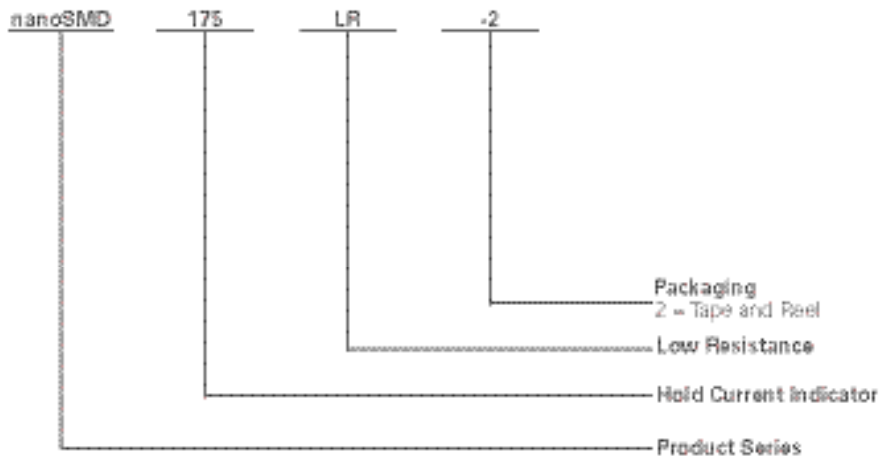
Figure LR7 – EIA Referenced Reel Dimensions



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Part Numbering System



Warning :

- Users should independently evaluate the suitability of and test each product selected for their own application.
- Operation beyond the maximum ratings or improper use may result in device damage and possible electrical arcing and flame.
- These devices are intended for protection against damage caused by occasional overcurrent or overtemperature fault conditions and should not be used when repeated fault conditions or prolonged trip events are anticipated.
- Contamination of the PPTC material with certain silicone-based oils or some aggressive solvents can adversely impact the performance of the devices.
- Device performance can be impacted negatively if devices are handled in a manner inconsistent with recommended electronic, thermal, and mechanical procedures for electronic components.
- PPTC devices are not recommended for installation in applications where the device is constrained such that its PTC properties are inhibited, for example in rigid potting materials or in rigid housings, which lack adequate clearance to accommodate device expansion.
- Operation in circuits with a large inductance can generate a circuit voltage (Ldi/dt) above the rated voltage of the device.

Notice:

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