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NAU7802

24-Bit Dual-Channel ADC

For Bridge Sensors

Date: January, 2012

Revision 1.7

Table of Contents

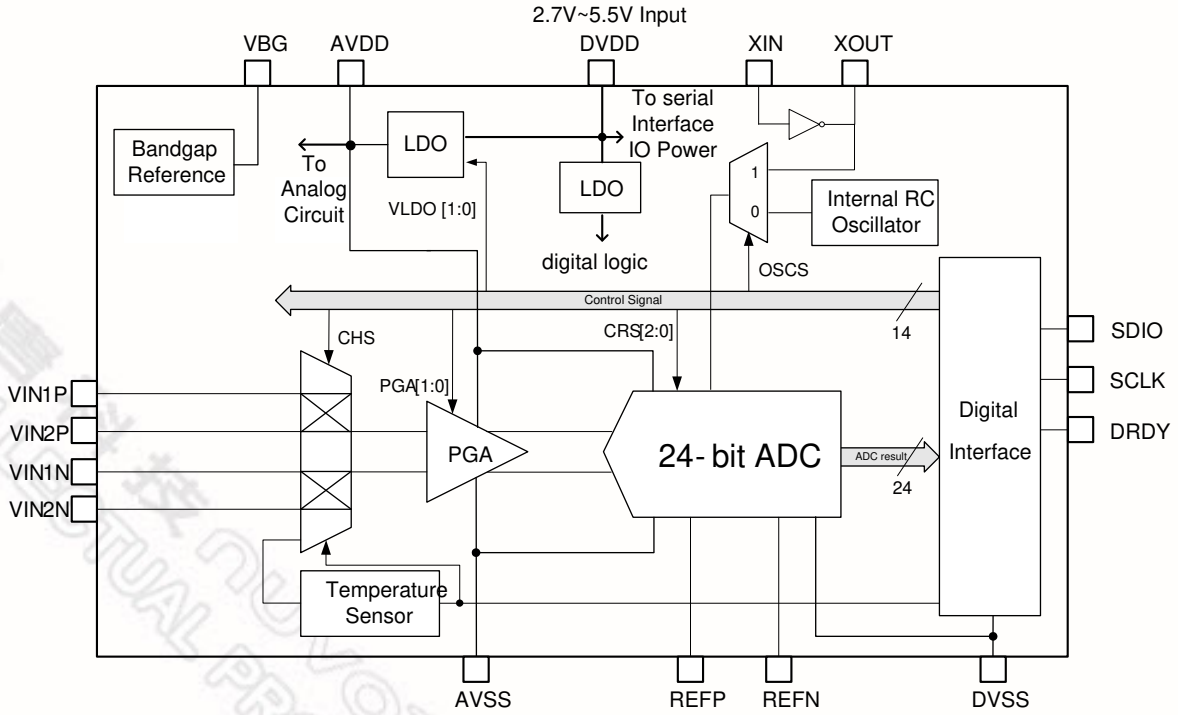
1 GENERAL DESCRIPTION

The Nuvoton NAU7802 is a precision low-power 24-bit analog-to-digital converter (ADC), with an onboard low-noise programmable gain amplifier (PGA), onboard RC or Crystal oscillator, and a precision 24-bit sigma-delta (Σ-Δ) analog to digital converter (ADC). The NAU7802 device is capable of up to 23-bit ENOB (Effective Number Of Bits) performance. This device provides a complete front-end solution for bridge/sensor measurement such as in weigh scales, strain gauges, and many other high resolution, low sample rate applications.

The many built-in features enable high performance applications with very low external parts count. Additionally, both operating current and standby current are very low, and many power management features are included. These enable powering only those elements of the chip that are needed, and also, to operate at greatly reduced power if the full 23-bit ENOB performance is not required.

The Programmable Gain Amplifier (PGA) provides selectable gains from 1 to 128. The A/D conversion is performed with a Sigma-Delta modulator and programmable FIR filter that provides a simultaneous 50Hz and 60Hz notch filter to effectively improve interference immunity. Also, this device provides a standard 2-wire interface compatible with I2C protocol for simple and straightforward connection to and interoperation with a wide range of possible host processors.

2 SYSTEM BLOCK DIAGRAM



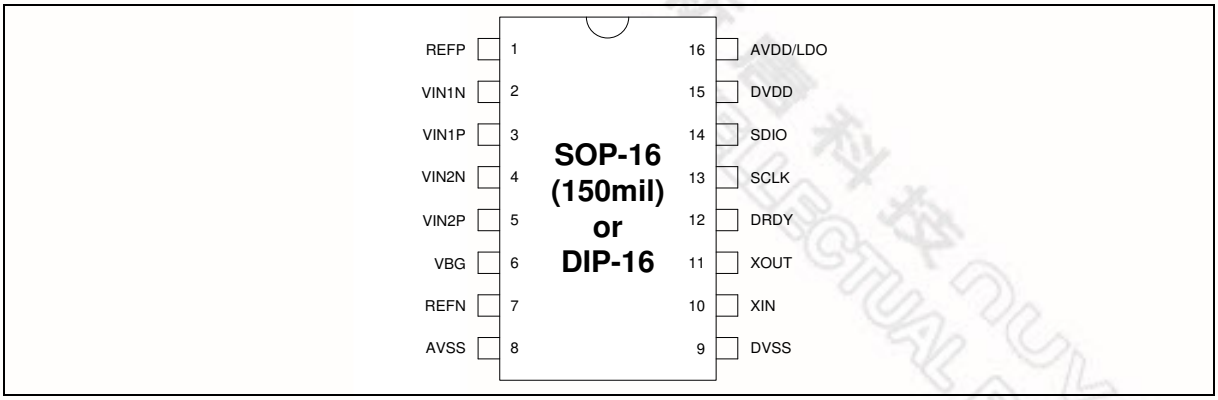
3 FEATURES

- Supply power: 2.7V~5.5V
- On-chip VDDA regulator for internal analog circuit or external load cell
  - Programmable VDDA: Off, 2.4V to 4.5V with eight options
    Minimum 10mA output drive capability at 3.0V output voltage
    Note: DVDD must be 0.3Vdc greater than desired VDDA output voltage
- 23 bits effective precision analog-to-digital converter
- Simultaneous 50Hz and 60Hz rejection (reaching －90dB）
- RMS Noise:
  - 50nV in 10 SPS data output rate and PGA gain = 128
  - 150nV in 80 SPS data output rate and PGA gain = 128
- Programmable PGA gains from 1 to 128
- Programmable ADC data output rates
- External differential reference voltage range from 0.1V to 5V
- System clock: External crystal oscillator or on-chip RC oscillator (4.9152Mhz)
- On-chip calibration
- On-chip power-on reset circuit
- On-chip temperature sensor
- Low Power Consumption and Programmable Power Management Options
  - < 1uA standby current
- External 4.9152MHz Crystal oscillator
- System clock:
  - Internal 4.9152MHz RC oscillator (power-on default system clock)
  - External 4.9152MHz Crystal oscillator
- MCU control interface: 2-wire interface compatible with I2C protocol
- Operating Temperature: -40~85C
- Packages:
  - SOP-16 (150mil) / PDIP-16

4 APPLICATIONS

- Weigh scales
- Strain Gauge
- Industrial process control
- Liquid/gas flow control
- Pressure sensors
- Voltage monitors

5 PIN CONFIGURATION



6 PIN DESCRIPTION

Pin No.	Pin Name	Type	DESCRIPTIONS
1	REFP	AI	Positive reference input
2	VIN1N	AI	Inverting Input #1
3	VIN1P	AI	Non-Inverting Input #1
4	VIN2N	AI	Inverting Input #2
5	VIN2P	AI	Non-Inverting Input #2
6	VBG	A	High impedance Reference Voltage Output and Bypass
7	REFN	AI	Negative Reference Input
8	AVSS	P	Analog Ground
9	DVSS	P	Digital ground
10	XIN	I	External crystal oscillator input. Typically 4.9152 MHz
11	XOUT	O	External crystal oscillator output.
12	DRDY	O	Data Ready Output indicating a conversion is complete and new data are available for readout. (CMOS Driver high / low)
13	SCLK	I	Serial Data Clock Input (CMOS open drain output)
14	SDIO	I/O	Data Input / Output for serial communication with host (CMOS open drain output)
15	DVDD	P	Digital power supply: 2.7V ~ 5.5V
16	AVDD/LDO	P	Analog power supply: 1. From programmable LDO output, low ESR 1 ohm or less capacitor recommended 2. LDO off: external power supply: 2.7V ~ 5.5V

- Note : **TYPE P**: Power, **AI**: Analog input, **AO**: Analog output, **I**: input, **O**: output, **I/O**: bi-directional

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
DC Power Supply	DVDD	DVDD–DVSS	-0.3	+6.0	V
	AVDD*	AVDD–AVSS	-0.3	+6.0	V
	AVSS–DVSS	-	-0.3	+0.3	V
Analog Input Voltage	AV_{IN}	AV_{IN} – AVSS	-0.3	AVDD + 0.3	V
Digital input Voltage	DV_{IN}	DV_{IN} – DVSS	-0.3	DVDD + 0.3	V
Operating Temperature	TA		-40	+85	°C
Storage Temperature	Tst		-55	+150	°C

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life time and reliability

* AVDD should not exceed DVDD supply voltage

7.2 DC ELECTRICAL CHARACTERISTICS

(Unless otherwise specified; Typical value is tested at TA=25°C, DVDD = 5V, AVDD = 5V)

PARAMETER	SPECIFICATION				TEST CONDITIONS
	MIN.	TYP.	MAX.	UNIT	
POWER SUPPLY					
Operating Voltage	2.7		5.5	V	DVDD
	2.7		DVDD	V	AVDD
Operating Current		2.1		mA	Internal OSC & LDO
		2		mA	Internal OSC, no LDO
Power Down Current		0.2	1	μA	All analog part include internal RC oscillator or external crystal oscillator. PUA =PUD=0

ANALOG INPUT					
Full-scale input range (VINxP – VINxN)	± 0.5/(VREF/PGA)			V	VREF = REFP – REFN
Common mode range with PGA gain 64, 128	AVSS + 1.5		AVDD – 1.5	V	
Common mode range with PGA bypass enabled	AVSS - 0.1		AVDD + 0.1	V	
Differential input impedance		5		GΩ	PGA bypass=off, DC
Bandwidth (-3dB)		2.27		Hz	Data output rate = 10 SPS
		18.17		Hz	Data output rate = 80 SPS
PGA	1		128		User-selectable gain range
Input capacitance channel 1		14		pF	
Input capacitance channel 2		5		pF	
Differential Input leakage current		20		pA	PGA bypass=off
Burnout current sources		2.5		µA	
SYSTEM PERFORMANCE					
Resolution		24			No missing codes
Integral nonlinearity NAU7802		± 0.0015		% of FS	With calibration
Offset error		+/-0.3		ppm of FS	With calibration, 1024 samples
Offset error drift		0.02		ppm of FS/°C	With calibration
Gain error		0.01		%	With calibration
Gain error drift		1		ppm/°C	With calibration
Common-mode rejection	96	100		dB	at DC 2.5 V ± 0.5 V
		130		dB	f_{CM} = 60 Hz, 500 mVpp ADC data rate = 10 SPS
		120		dB	f_{CM} = 50 Hz, 500 mVpp ADC data rate = 10 SPS
Notch rejection		100		dB	f_{CM} = 60 Hz, 500 mVpp ADC data rate = 10 SPS
		100		dB	f_{CM} = 50 Hz, 500 mVpp ADC data rate = 10 SPS
Power supply rejection	96	100		dB	at DC 5 V ± 0.25 V, with LDO
VOLTAGE REFERENCE INPUT					
VREF = REFP – REFN	1.5	AVDD	AVDD+. 0.1	V	
REFN input range	-0.1		VREFP-1.5	V	
REFP input range	VREFN+ 1.5		AVDD+ 0.1		

DIGITAL SERIAL INTERFACE					
Input Leakage Current SCK, SI	-1	-	+1	µA	DVDD = 5.5V, 0<V_{IN}<DVDD
Input High Voltage VIH	0.7 VDD		5.5	V	
Input low Voltage VIL	DVSS		0.3 VDD	V	
VOH (DRDY)	0.9 DVDD			V	IOH = 1 mA
VOH (SCLK, SDIO)	0.9 DVDD			V	Defined by pull up resistor. (Internal weak, internal strong, external.)
VOL (SCLK, SDIO, DRDY)			0.2 DVDD	V	IOL = 1 mA
SDIO pull-up resistor Input High Voltage P1, P2, P3 (TTL input)		DVDD		V	V_{DD} = 5.5V
SDIO, SCLK; pull up resistor value	1.6 k	50 k	none	Ohm	Selectable; strong, weak, none
Power On Reset Voltage		1.6		V	

7.3 RC OSC AND AC CHARACTERISTICS

Parameter	Specification (reference)				Test Conditions
	Min.	Typ.	Max.	Unit	
4.9152 MHz On-chip RC oscillator		+/-3		%	DVDD = 5V, T=25C; NAU7802 only
T_{RDY}: Analog part wakeup stable plus Data Ready after exiting power-down mode		600		ms	DVDD = 5V; at 10 S/sec (5 sample times plus 100 ms)

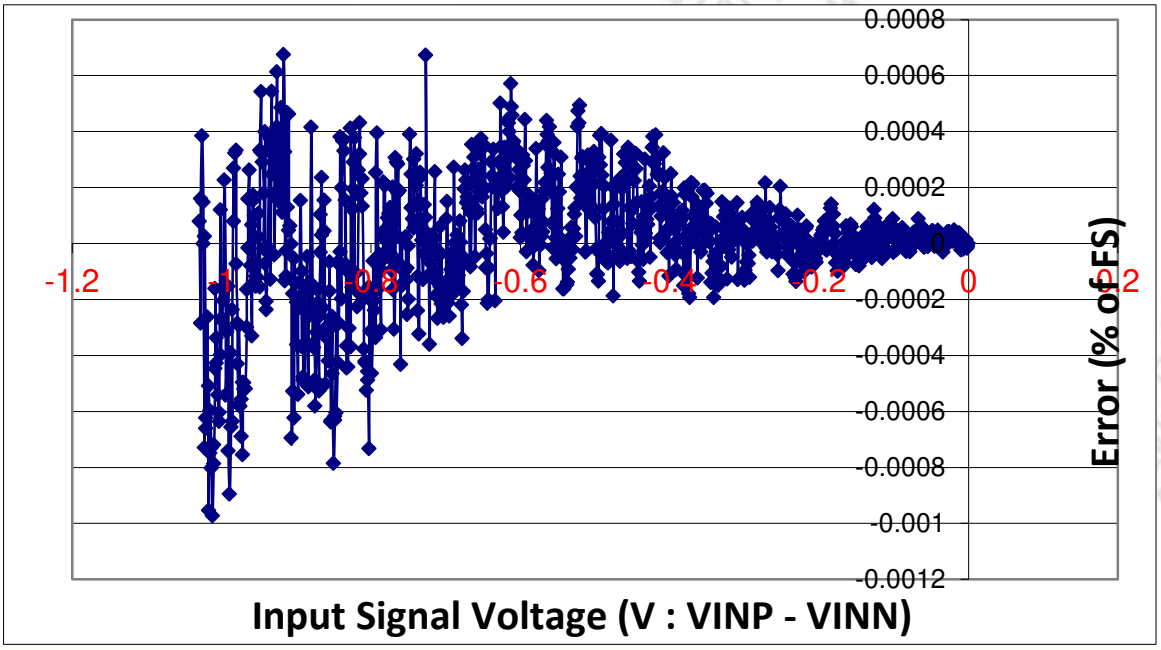
7.4 TEMPERATURE SENSOR

Parameter	Specification (reference)				Test Conditions
	Min.	Typ.	Max.	Unit	
Temperature sensor output		109		mV	at 25°C
Temperature sensor delta coefficient		360		uV / °C	relative to 25°C

7.5 Typical Characteristic

7.5.1 NAU7802 Linearity – (Error % vs. Input Voltage)

AVDD = 4.5V / PGA gain = 1x



- NAU7802 Linearity Performance is symmetric, from the differential input voltage -1.2V to 0V and from 0V to 1.2V. One-sided linearity performance result is shown.

7.5.2 Noise Performance – NAU7802

NAU7802 with LDO and Cfilter=330pF on VIN2P & VIN2N at 10 S/sec

AVDD/ REFP (V)	PGA Gain	ENOB	ENOB2	NOISE_FREE_BITS
4.5	1	22.29	22.31	20.09
4.5	2	22.15	22.16	19.75
4.5	4	22.01	22.02	19.61
4.5	8	21.88	21.91	19.36
4.5	16	21.39	21.42	18.71
4.5	32	21.09	21.11	18.42
4.5	64	20.42	20.43	17.89
4.5	128	19.73	19.74	17.11
3.3	1	21.14	21.15	19.09
3.3	2	21.11	21.13	18.96
3.3	4	21.1	21.1	19
3.3	8	21.03	21.04	18.64
3.3	16	20.8	20.81	18.19
3.3	32	20.41	20.42	17.85
3.3	64	19.84	19.85	17.23
3.3	128	19.16	19.17	16.54

7.5.3 ESD Performance – NAU7802

Zapping Method	PD	PS	ND	NS	Remark
HBM	4kV	4kV	-4kV	-4kV	Pass
MM	400V	400V	-400V	-400V	Pass

7.6 DIGITAL SERIAL INTERFACE TIMING

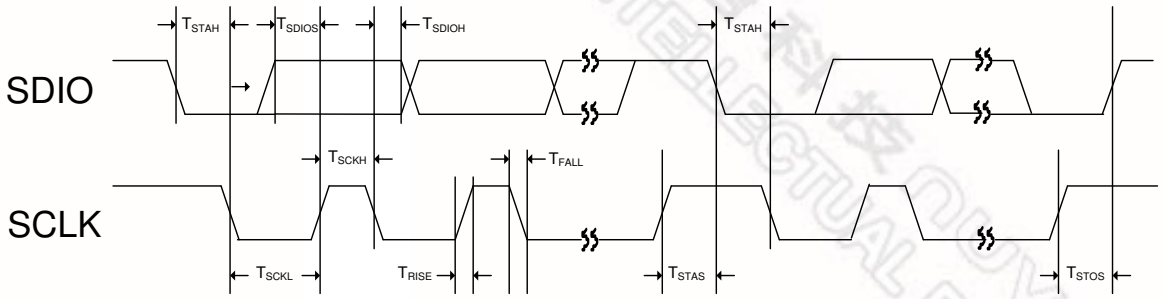


Figure 7: Two-wire Control Mode Timing

Symbol	Description	min	typ	max	unit
T_{STAH}	SDIO falling edge to SCLK falling edge hold timing in START / Repeat START condition	600	-	-	ns
T_{STAS}	SCLK rising edge to SDIO falling edge setup timing in Repeat START condition	600	-	-	ns
T_{STOS}	SCLK rising edge to SDIO rising edge setup timing in STOP condition	600	-	-	ns
T_{SCKH}	SCLK High Pulse Width	600	-	-	ns
T_{SCKL}	SCLK Low Pulse Width	1,300	-	-	ns
T_{RISE}	Rise Time for all 2-wire Mode Signals	-	-	300	ns
T_{FALL}	Fall Time for all 2-wire Mode Signals	-	-	300	ns
T_{SDIOS}	SDIO to SCLK Rising Edge DATA Setup Time	100	-	-	ns
T_{SDIOH}	SCLK falling Edge to SDIO DATA Hold Time	0	-	600	ns

8 FUNCTIONAL DESCRIPTION

8.1 Analog input (VIN1P, VIN1N, VIN2N, VIN2P)

The input signal to be measured is applied to one of two differential input signal pairs. The desired signal pair is selected using an analog input multiplexer, which is controlled by settings in the device command and control registers. The 8-pin version of the device supports only one input signal pair.

This device is optimized to accept differential input signals, but can also measure single-ended signals. When measuring single-ended signals with respect to ground, connect the negative input (VIN1N or VIN2N) to ground and connect the input signal to the positive input (VIN1P or VIN2P). Note that when this device is configured this way, only half of the converter full-scale range is used, since only positive digital output codes are produced.

8.2 Power supply

The digital power supply DVDD should use the same power source as used for the host processor supporting the digital interface communication. The analog power supply AVDD can be provided by external regulator output (power-on default setting) or provided by a built-in voltage regulator. The eight programmable output voltage levels of the built-in regulator are: off (high-Z output, default power-on setting), 2.4V, 2.7V, 3.0V 3.3V, 3.6V, 4.2V, and 4.5V. This output is intended to provide the driving current for external sensors such as load cells for weight measurement applications.

8.3 2-Wire-Serial Control and Data Bus (I^2C Style Interface)

The serial interface provides a 2-wire bidirectional read/write data interface similar to and typically compatible with standard I2C protocol. This protocol defines any device that sends CLK onto the bus as a master, and the receiving device as slave. The NAU7802 can function only as a slave device.

An external clock drives the device, and in accordance with the protocol, data is sent to or from the device accordingly. All functions are controlled by means of a register control interface in the device. Additionally, a "data ready" output pin is provided to indicate to the host that a new conversion has been completed and that data are ready to be read from the device. The host may either use this signal or poll device register R0x00 Bit 5 to determine when new data are available.

8.3.1 2-Wire Protocol Convention

All 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDIO while SCLK is HIGH. All 2-Wire interface operations are terminated by a STOP condition, which is a LOW to HIGH transition of SDIO while SCLK is HIGH. A STOP condition at the end of a read or write operation places the serial interface in standby mode.

An acknowledge (ACK), is a software convention is used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDIO bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDIO line LOW to acknowledge the reception of the eight bits of data.

Following a START condition, the master must output a device address byte. This consists of a 7-bit device address, and the LSB of the device address byte is the R/W (Read/Write) control bit. When R/W=1, this indicates the master is initiating a read operation from the slave device, and when R/W=0, the master is initiating a write operation to the slave device. If the device address matches the address of the slave device, the slave will output an ACK during the period when the master allows for the ACK signal.

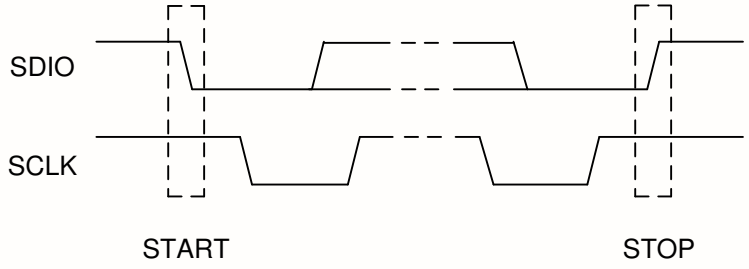


Figure 1: START and STOP

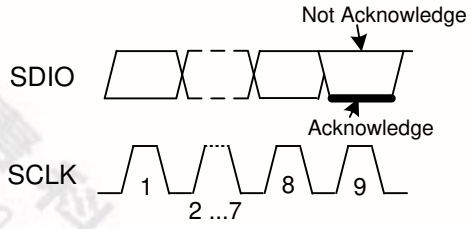


Figure 2: Acknowledge and NOT Acknowledge

0	1	0	1	0	1	0	R/W	Device Address Byte
A7	A6	A5	A4	A3	A2	A1	A0	Control Address Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte

Figure 3: Slave Address Byte, Control Address Byte, and Data Byte

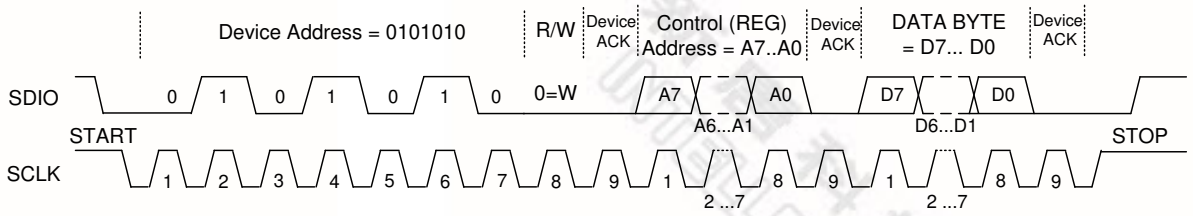


Figure 4: A complete 2 wire write 1 control register sequence

8.3.2 2-Wire Write Operation

A Write operation consists of a two-byte instruction followed by one or more Data Bytes. A Write operation requires a START condition, followed by a valid device address byte with R/W=0, a valid control address byte, data byte(s), and a STOP condition.

When more than one Data Byte is written, this is known as a "burst write" operation. In this operation, the host may write sequential bytes of information simply by transmitting a new data byte after each ACK from the NAU7802. The NAU7802 automatically increments the register address by one for each subsequent byte-write operation. This will continue until the STOP condition is met.

The NAU87802 is permanently programmed with "010 1010" (0x2A) as the Device Address. If the Device Address matches this value, the NAU7802 will respond with the expected ACK signaling as it accepts the data being transmitted into it.

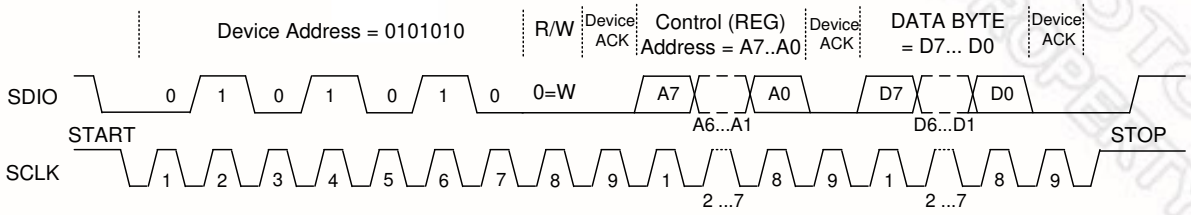


Figure 5: Single Write Sequence

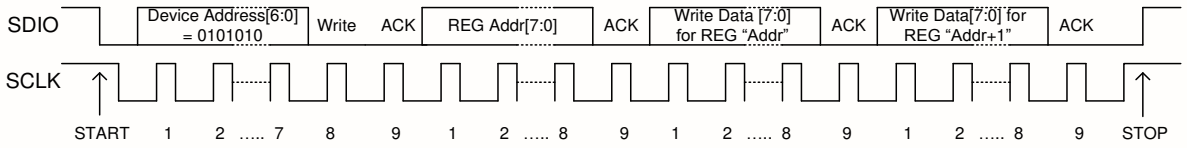


Figure 6: Burst Write Sequence

8.3.3 2-Wire Single Read Operation

A Read operation consists of a three-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, device address byte with the R/W bit set to "0", and a Control Register Address byte. This indicates to the slave device which of its control registers is to be accessed.

The NAU7802 is permanently programmed with "010 1010" (0x2A) as its device address. If the device address matches this value, the NAU7802 will respond with the expected ACK signaling as it accepts the Control Register Address being transmitted into it. After this, the master transmits a second START condition, and a second instantiation of the same device address, but now with R/W=1.

After again recognizing its device address, the NAU7802 transmits an ACK, followed by a one byte value containing the data from the selected control register inside the NAU7802. During this phase, the master generates the ACK signaling with each byte transferred from the NAU7802. If there is no STOP signal from the master, the NAU7802 will internally auto-increment the target Control Register Address and then output the data bytes for this next register in the sequence.

This process will continue while the Master continues to issue ACK signaling. If the Control Register Address being indexed inside the NAU7802 reaches the value 0x7F (hexadecimal) and the value for this register is output, the index will roll over to 0x00. The data bytes will continue to be output until the master terminates the read operation by issuing a STOP condition.

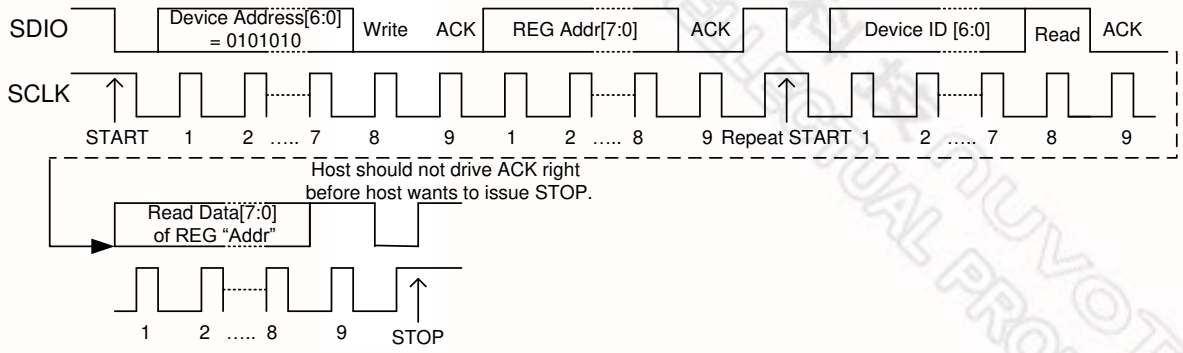


Figure 7: Single Read Sequence

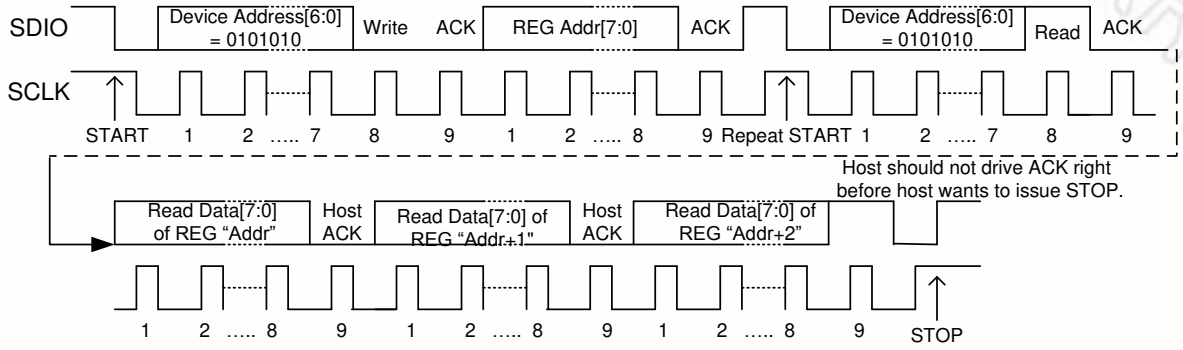


Figure 8: Burst Read Sequence

8.4 2-Wire Timing

Please see electrical specifications

The NAU7802 is compatible with serial clock speeds defined as "standard mode" with SCLK 0 - 100 kHz, and "fast mode" with SCLK 0 - 400 kHz. At these speeds the total bus line capacitance load is required to be 400 pF or less.

Open collector drivers are required for the serial interface. Therefore, the bus line rise time is determined by the total serial bus capacitance and the DVDD pull-up resistors. The NAU7802 defaults to a weak pull up (typical 50 k ohm) for applications with no external pull up resistor. Register 0x11 bits 5:4 provide other options including a strong internal pull-up (typical 1.6 k ohm) or no internal pull-up resistor.

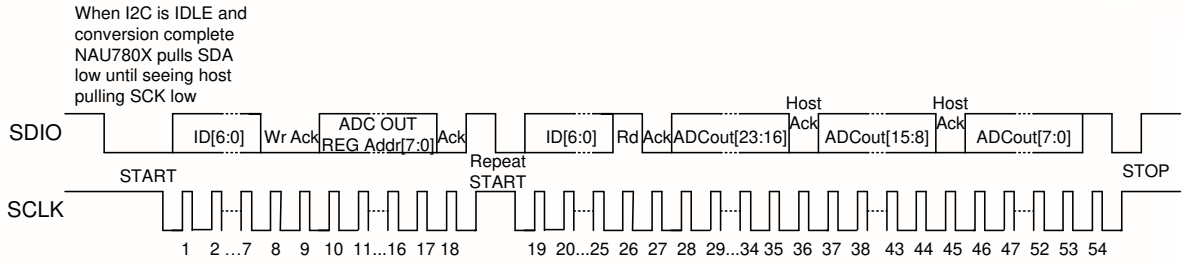
8.5 NAU7802 Streaming Data Mode

8.5.1 Enabling the Streaming I2C Mode

- Power Up the chip
  - Write 0x00 = 0x06 (PU analog and PU digital)
  - (read back 0x00 bit 3 to make sure chip is powered up)
- Enable Streaming I2C Mode
  - Write REG11[7]=1 to enable streaming mode 1, or Write REG11[7]=1 and REG11[6]=1 and REG15[7]=1 to enable streaming mode 2
  - (read back 0x1D bit 7 to make sure the streaming I2C mode is active)

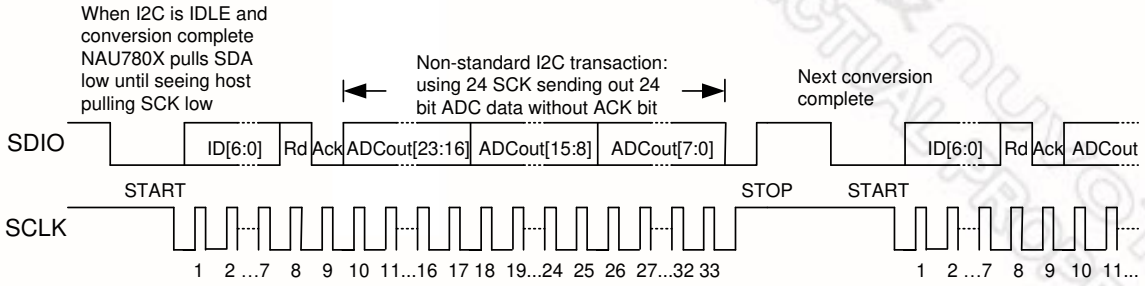
8.5.2 Streaming I2C Mode R/W Protocol 1

When REG0x11[7] CRSD=1, I2C is IDLE and a conversion is complete, NAU7802 will pull SDA/SDIO low to inform the host a conversion is complete. Host should respond by pulling SDA/SDIO low and pulling SCK low to initial an I2C "start" condition. When seeing SCK pulled low by host, NAU7802 will release the SDA/SDIO. Host can continue the standard I2C transaction with NAU7802



8.5.3 Streaming I2C Mode R/W Protocol 2

In addition to CASE1 REG11[7]=1, if REG0x11[6] FRD=1 and REG0x15[7]=1, host can direct issue a I2C read cycle (No writing register address first needed), after the Ack bit for the ID and "Read Select", the following 24 SCK is used for NAU7802 to shift out the 24 bit ADC conversion result without the ACK bit needed. So the total Read ADC conversion data cycle can be shorten to 33 SCK comparing to 54 SCK plus a repeat start by using the standard I2C.



Note: Write NAU7802 register is always allowed by using Standard I2C write NAU7802 register protocol. So these two special bits can be reset to 0 to return to Standard I2C protocol

8.6 Device Calibration Features

Calibration is not required for low accuracy applications, but may be needed in sensitive applications. When calibration is used the system designer has three options.

Calibration can be performed at the system level with an external processor or at the ADC device. Inside the ADC device both internal and external calibration can be performed.

Internal ADC device calibration only removes internal PGA gain and offset errors.
External ADC device calibration removes DC errors at the device input pins and the internal PGA gain and offset errors.

As with all devices of this type, the NAU7802 internal gain factors and offset voltages will contain small errors owing to fabrication process variations, power supply voltage changes, and temperature variations. The same types of errors exist at the external system level.

These errors can be measured by the NAU7802 device itself using the calibration features. After calibration, the stored values in the calibration registers are automatically added/subtracted to the data from the ADC before being output as the ADC resulting data. It is recommended to calibrate the NAU8702 after the following conditions:

- Initial power-up
- Power-up after long-duration register mediated power-down conditions
- PGA gain changes
- Supply changes
- Significant temperature changes (can be measured using built-in thermal sensing feature)
- Sample rate changes
- Channel select changes

Calibration is initiated by writing Logic=1 to R0x02 Bit 2. Bit 2 named “CALS” then becomes a status bit that can be read to know when calibration is complete. Internal or external calibration is performed on the Gain or Offset value and input channel as selected by other bits in R0x02. Bit 2 will remain Logic=1 until calibration is complete, and will read back as Logic=0 when calibration is completed.

After calibration, it is important to check the CAL_ERR status bit to determine if there was any problem during calibration. If there was an error, all data output could be invalid.

8.6.1 Internal or External calibration

The internal calibration disconnects the inputs from the input pins and internally connects the differential inputs to the same internal voltage reference point for calibration. the internal inputs for offset calibration. External calibration uses the inputs as-is, and it is up to the system designer to configure them appropriately for the calibration procedure. The resulting gain or offset calibration value is stored in the selected calibration register. The same register sets are used for both internal or external calibration and it is intended that only one choice of internal/external calibration is used at any given time.

At all times, when reading a value from the ADC registers, the gain and offset calibration values are added/subtracted to the ADC value before being output. The default values for the calibration registers is zero, so these have no affect on the ADC output value until after a calibration operation has been instantiated.

The resulting output value is calculated as:

ADC Output Value = Gain_Calibration* (ADC measurement - Offset_Calibration)

Calibration Equations

$$OFFSET=(1-b23) \times (b22*2^{-1}+b21*2^{-2}+b20*2^{-3}+b19*2^{-4}+b18*2^{-5}+b17*2^{-6}+b16*2^{-7}+b15*2^{-8}+b14*2^{-9}+b13*2^{-10}+b12*2^{-11}$$
$$+b11*2^{-12}+b10*2^{-13}+b9*2^{-14}+b8*2^{-15}+b7*2^{-16}+b6*2^{-17}+b5*2^{-18}+b4*2^{-19}+b3*2^{-20}+b2*2^{-21}+b1*2^{-22}+b0*2^{-23})$$

$$GAIN=b31*2^{8}+b30*2^{7}+b29*2^{6}+b28*2^{5}+b27*2^{4}+b26*2^{3}+b25*2^{2}+b24*2^{1}+b23*2^{0}+b22*2^{-1}+b21*2^{-2}+b20*2^{-3}+b19*2^{-4}+b18*2^{-5}+b17*2^{-6}+b16*2^{-7}+b15*2^{-8}$$
$$+b14*2^{-9}+b13*2^{-10}+b12*2^{-11}+b11*2^{-12}+b10*2^{-13}+b9*2^{-14}+b8*2^{-15}+b7*2^{-16}+b6*2^{-17}+b5*2^{-18}+b4*2^{-19}+b3*2^{-20}+b2*2^{-21}+b1*2^{-22}+b0*2^{-23}$$

$$DOUT<23:0>'=(DOUT<23:0>+OFFSET<23:0>) \times GAIN<31:0>$$

8.6.2 Calibration Limitations

Note that the offset that is trimmed from the input is mapped through the gain register. Additionally:

- Calibration can be limited by signal headroom in the analog path
- With the converters intrinsic gain & offset error the minimal full scale input range may be higher or lower.

8.6.3 Calibration Error

A calibration error may occur during gain calibration when one of the following happens:

- The gain required to map input to full scale is larger than the range available in the gain register ~ 256
- The offset adjusted input is negative, e.g. 256 > gain > 0

If there is a calibration error, CAL_ERR will set to Logic=1 when the calibration sequence is completed. Once CAL_ERR is set to Logic=1, it will remain in this state until either the NAU7802 is reset, or after a valid calibration sequence is completed.

When CAL_ERR = 1, the data in the calibration registers is invalid. It is recommended perform the calibration routine again, or to write a default value into the calibration registers.

8.7 Internal Band-Gap Circuit

An internal band-gap establishes accurate operation of the device over a wide temperature range. No adjustment of the bandgap is necessary. For optimum performance, the NAU7802 makes available a band-gap output pin "VBG" which should be bypassed to ground with a high quality X7R small value 0.1 uF filter capacitor.

8.8 Reset and Power-down mode

An automatic built-in power-on reset function will reset the NAU7802 after DVDD power becomes valid. After AVDD power is stable (from external power or from the built-in regulator), reset may also be initiated at any time using the register control interface. The scope of the register based reset using register 0x00 bit 0, named "RR" set to 1, is equivalent to the power-on reset.

Power-down standby mode can be selected using the register control interface using register 0x00 bits 2:1, named "PUA" and "PUD" set to 0. This mode shuts down the entire analog portion of the part, including the 24-bit ADC, voltage regulator, PGA, bandgap reference, and internal RC oscillator (or external crystal oscillator) to reduce power consumption.

The command and control interface is static and works normally in power-down mode. Power-down mode can be terminated at any time by changing the register controls to return the device to normal operating mode, using register 0x00 bits 2:1, named "PUA" and "PUD" set to 1. In this way the contents of the registers are retained for immediate normal use.

After reset or after resuming normal operating mode after power-down mode, the host should wait through six cycles of data conversion. This allows the device to stabilize all functions and to flush all old internal data for a full-accuracy output. This timing is automatically generated by the device for the DRDY pin and Data Ready device status bit.

8.9 Temperature sensor

A matched pair of on-chip diodes provides temperature sensing capability. Temperature sensing is selected by setting of the analog input multiplexer using the register control interface. A PGA gain of 2x or 1x is used for temperature sensing to prevent PGA clipping.

By measuring the difference in voltage of these diodes, temperature changes can be inferred from a baseline temperature. Please refer to the specification items "Temperature sensor output" and "Temperature sensor delta coefficient."

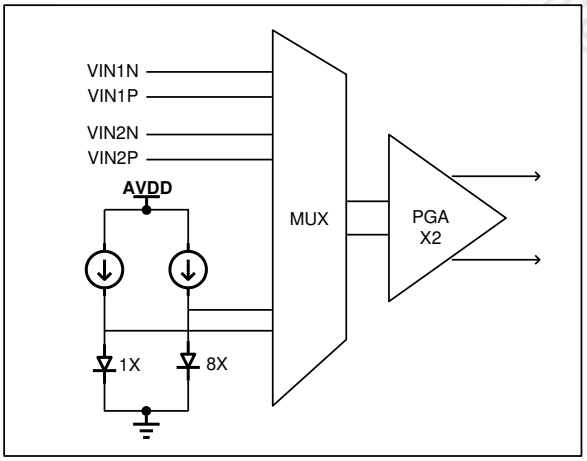


Figure 8

8.10 Oscillator Features

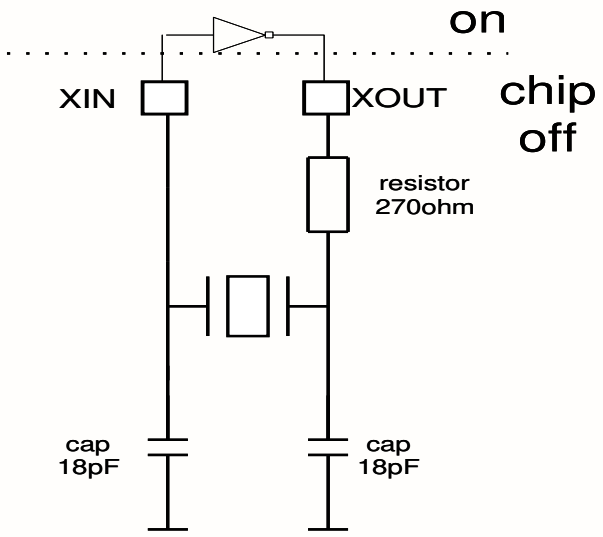
This device may either accept an external clock, use an internal RC oscillator, or use a built-in crystal oscillator for its time base. An accurate clock is important for the digital filtering of 50Hz or 60Hz components to work optimally. The internal oscillator is trimmed at the factory for good accuracy.

The internal RC or crystal oscillator frequency may be output on the DRDY pin. This is done by programming R0x06 as follows:

- Write REG00[6] = 0: Use oscillator as system clock
- Write REG01[6] = 1: Output system clock on DRDY pin

8.10.1 External Crystal Oscillator

When an external 4.9152MHz crystal oscillator is used, the preferred application circuit on the XIN & XOUT pins is as shown below. The crystal oscillator could operate without the 270 Ohm resistor and without the 18pF capacitor on XIN at a reduced performance.



8.10.2 External Clock Source

When the clock for the NAU7802 may also be provided from an external source. To use this feature, the device is configured in the same way as for using a crystal and the external clock signal is applied to the XIN pin.

9 APPLICATION INFORMATION

This section includes both circuit diagram information and recommendations for programming the device. Programming is essential, as the device will not function until various default settings are changed to values appropriate for the application.

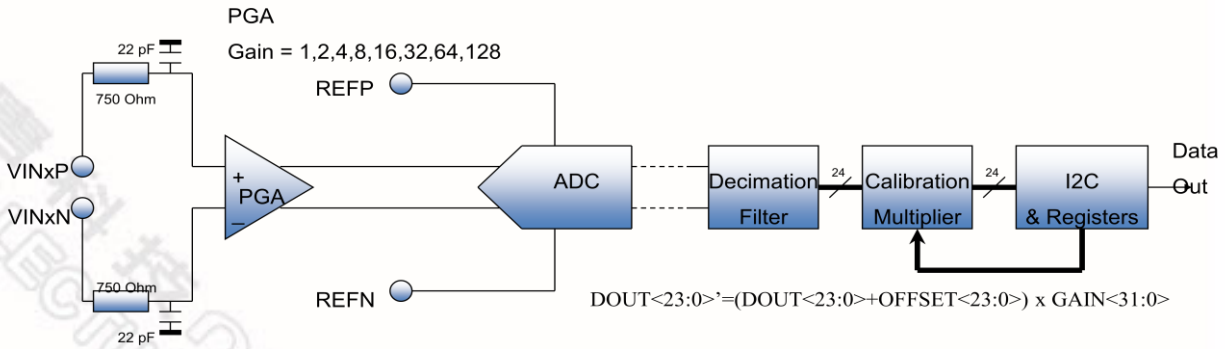
9.1 Power-On Sequencing

After the DVDD supply is valid, and after the internal power-on reset is completed, the NAU7802 is ready for host program control access. The following steps apply to most applications.

1. Set the RR bit to 1 in R0x00, to guarantee a reset of all register values.
2. Set the RR bit to 0 and PUD bit 1, in R0x00, to enter normal operation
3. After about 200 microseconds, the PWRUP bit will be Logic=1 indicating the device is ready for the remaining programming setup.
4. At this point, all appropriate device selections and configuration can be made.
    a. For example R0x00 = 0xAE
    b. R0x15 = 0x30
5. No conversion will take place until the R0x00 bit 4 “CS” is set Logic=1
6. Enter the low power standby condition by setting PUA and PUD bits to 0, in R0x00
7. Resume operation by setting PUA and PUD bits to 1, in R0x00. This sequence is the same for powering up from the standby condition, except that from standby all of the information in the configuration and calibration registers will be retained if the power supply is stable. Depending on conditions and the application, it may be desirable to perform calibration again to update the calibration registers for the best possible accuracy.

9.2 Signal path normal operation

In normal operation the input signal is full scale at the ADC input when
(VINxP - VINxN) = +/- 0.5 * (REFP - REFN) / PGA_Gain, within the PGA common mode range.



Full Scale (VINxP-VINxN) = +/- 0.5 * (REFP-REFN)/PGA