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# 24-bit Stereo Audio DAC with Speaker Driver

*emPowerAudio*™

## Description

The NAU8401 is a low power, high quality audio output system for portable applications. In addition to precision 24-bit stereo DACs, this device integrates a broad range of additional functions to simplify implementation of complete audio systems. The NAU8401 includes drivers for speaker, headphone, and stereo line outputs, and integrates mixing of the DAC outputs with analog input signals.

Advanced on-chip digital signal processing includes a 5-band equalizer, a 3-D audio enhancer, and a digital limiter/dynamic range compressor function for the playback path. The digital interface can operate as either a master or a slave. Additionally, an internal fractional-N PLL is available to generate accurate audio sample rate clocks for the DAC derived from any available system clock from 8MHz through 33MHz.

The NAU8401 operates with analog supply voltages from 2.5V to 3.6V, while the digital core can operate as low as 1.7V to reduce power. The loudspeaker BTL output pair and two auxiliary line outputs can use a 5V supply to increase output power capability, enabling the NAU8401 to drive 1 Watt into an external speaker. Internal control registers enable flexible power conserving modes, shutting down sub-sections of the chip under software control.

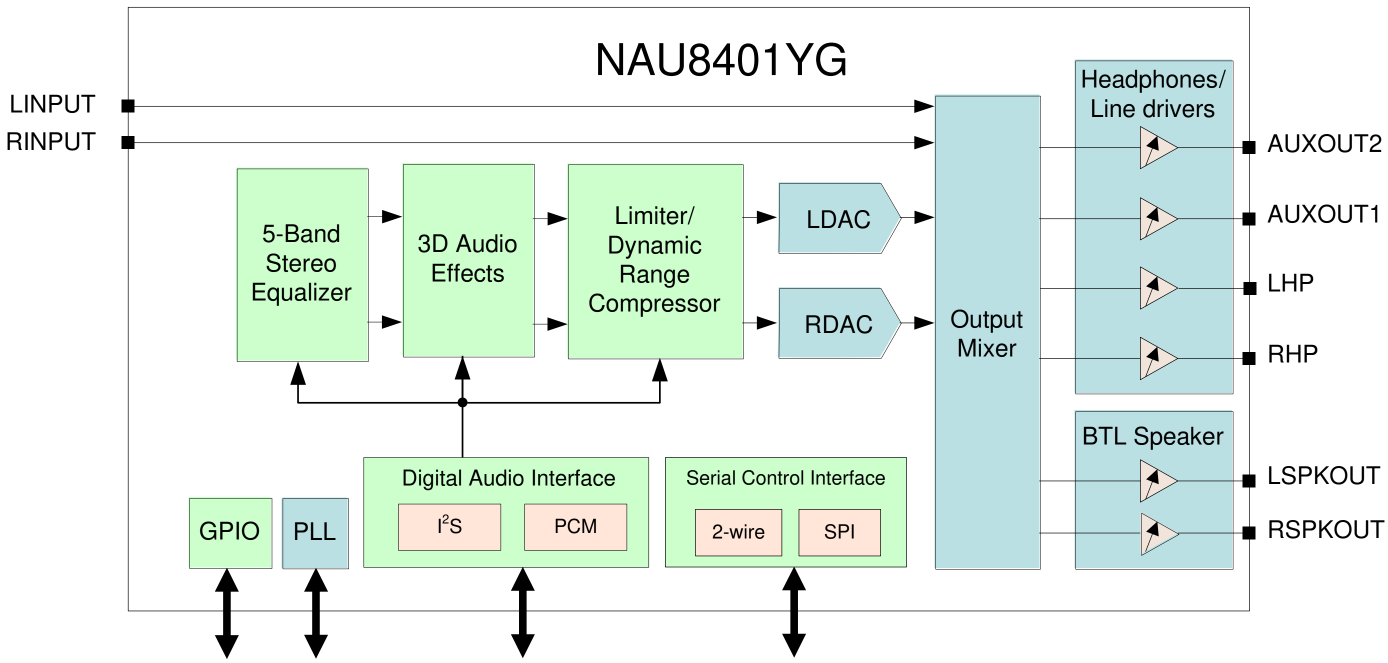
The NAU8401 is specified for operation from -40°C to +85°C. AEC-Q100 & TS16949 compliant device is available upon request.

## Key Features

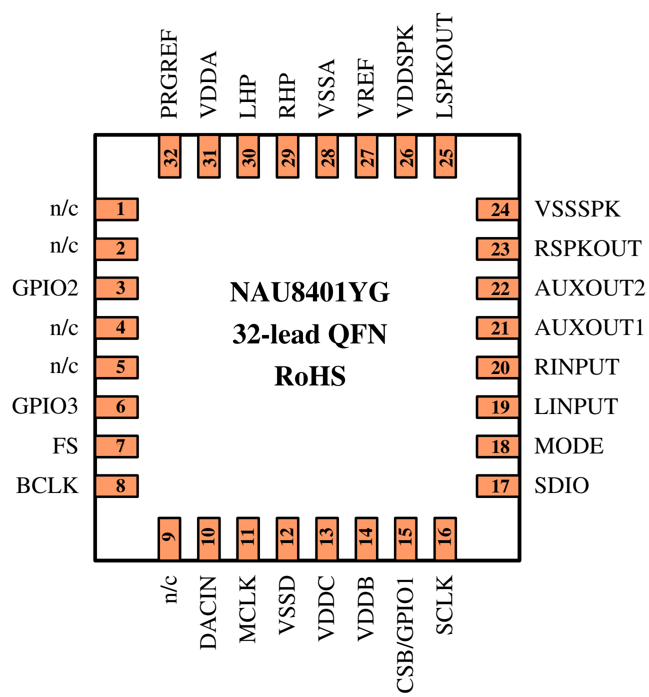
- DAC: 94dB SNR and -84dB THD (“A” weighted)
- Integrated BTL speaker driver: 1W into 8Ω
- Integrated head-phone driver: 40mW into 16Ω
- Integrated line inputs and line outputs
- On-chip high resolution fractional-N PLL
- Integrated DSP with specific functions:
  - 5-band equalizer
  - 3-D audio enhancement
  - Automatic level control
  - Audio level limiter/dynamic range compressor
- Standard audio interfaces: PCM and $I^2S$
- Serial control interfaces with read/write capability
- Supports audio sample rates from 8kHz to 48kHz

## Applications

- Personal Navigation Devices
- Personal Media Players
- Personal Navigation Devices
- Portable Game Players
- Portable TVs




## Pinout




| Part Number | Dimension | Package | Package Material |
|---|---|---|---|
| NAU8401YG | 5 x 5 mm | 32-QFN | Pb-Free |

# Pin Descriptions

| Pin # | Name | Type | Functionality |
|---|---|---|---|
| 1 | n/c | | Not internally connected |
| 2 | n/c | | Not internally connected |
| 3 | GPIO2 | Digital Input | General purpose I/O. Can be used for jack detect. |
| 4 | n/c | | Not internally connected |
| 5 | n/c | | Not internally connected |
| 6 | GPIO3 | Digital Output | General Purpose I/O. Can be used for jack detect. In 4-wire mode, must be used as output to read register data. |
| 7 | FS | Digital I/O | Digital Audio DAC and ADC Frame Sync |
| 8 | BCLK | Digital I/O | Digital Audio Bit Clock |
| 9 | n/c | | Not internally connected |
| 10 | DACIN | Digital Input | Digital Audio DAC Data Input |
| 11 | MCLK | Digital Input | Master Clock Input |
| 12 | VSSD | Supply | Digital Ground |
| 13 | VDDC | Supply | Digital Core Supply |
| 14 | VDDB | Supply | Digital Buffer (Input/Output) Supply |
| 15 | CSB/GPIO1 | Digital I/O | 3-Wire MPU Chip Select or General Purpose I/O |
| 16 | SCLK | Digital Input | 3-Wire MPU Clock Input / 2-Wire MPU Clock Input |
| 17 | SDIO | Digital I/O | 3-Wire MPU Data Input / 2-Wire MPU Data I/O |
| 18 | MODE | Digital Input | Control Interface Mode Selection Pin |
| 19 | LINPUT | Analog Input | Left Analog Input |
| 20 | RINPUT | Analog Input | Right Analog Input |
| 21 | AUXOUT1 | Analog Output | Headphone Ground / Mono Mixed Output / Line Output |
| 22 | AUXOUT2 | Analog Output | Headphone Ground / Line Output |
| 23 | RSPKOUT | Analog Output | BTL Speaker Positive Output or Right high current output |
| 24 | VSSSPK | Supply | Speaker Ground (ground pin for RSPKOUT, LSPKOUT, AUXOUT2 and AUXTOUT1 output drivers) |
| 25 | LSPKOUT | Analog Output | BTL Speaker Negative Output or Left high current output |
| 26 | VDDSPK | Supply | Speaker Supply (power supply pin for RSPKOUT, LSPKOUT, AUXOUT2 and AUXTOUT1 output drivers) |
| 27 | VREF | Reference | Decoupling for Midrail Reference Voltage |
| 28 | VSSA | Supply | Analog Ground |
| 29 | RHP | Analog Output | Headphone Positive Output / Line Output Right |
| 30 | LHP | Analog Output | Headphone Negative Output / Line Output Left |
| 31 | VDDA | Supply | Analog Power Supply |
| 32 | PRGREF | Analog Output | Programmable buffered DC voltage output |
| 33 | GPAD | Bulk Ground Pad | Electrical and Thermal pad on underside of device |

**Notes**

1. The 32-QFN package includes a bulk ground connection pad on the underside of the device. This bulk ground should be thermally tied to the PCB as much as possible, and electrically tied to the analog ground (VSSA, pin 28).
2. Unused analog input pins should be left as no-connection.
3. Unused digital input pins should be tied to ground.
4. Pins designated as "n/c" (Not Internally Connected) should be left as no-connection

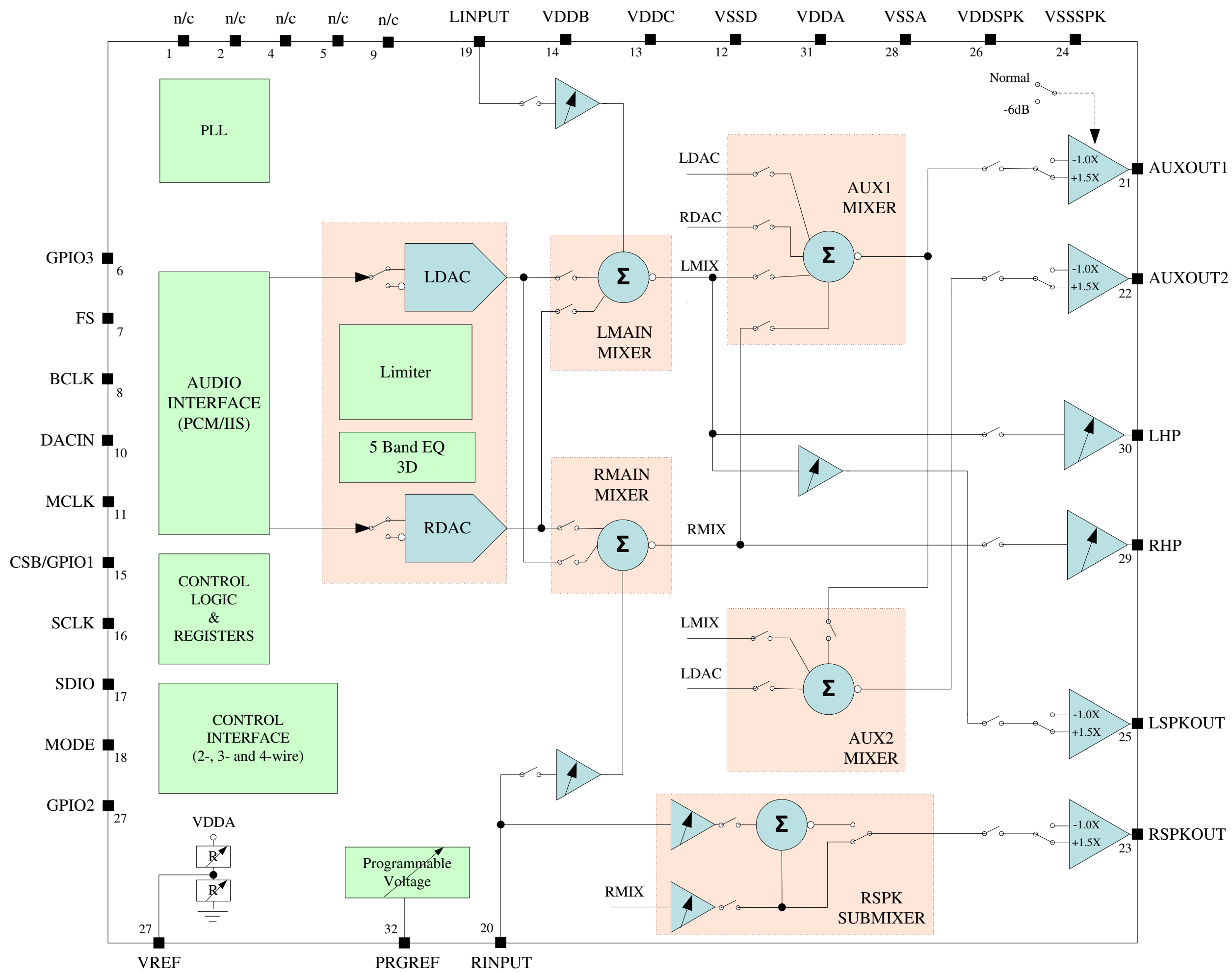



Figure 1: NAU8401 Block Diagram

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## Electrical Characteristics

Conditions: VDDC = 1.8V, VDDA = VDDB = VDDSPK = 3.3V, MCLK = 12.288MHz,
$T_A$ = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data, unless otherwise stated.

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Digital to Analog Converter (DAC) driving RHP / LHP with 10kΩ / 50pF load** | | | | | | |
| Full scale output [1] | | | | VDDA / 3.3 | | $V_{rms}$ |
| Signal-to-noise ratio | SNR | A-weighted | 88 | 94 | | dB |
| Total harmonic distortion [2] | THD+N | $R_L$ = 10kΩ; full-scale signal | | -84 | | dB |
| Channel separation | | 1kHz signal | | 99 | | dB |
| Power supply rejection ratio (50Hz - 22kHz) | PSRR | | | 53 | | dB |
| **Speaker Output (RSPKOUT / LSPKOUT with 8Ω bridge-tied-load)** | | | | | | |
| Full scale output [3] | | SPKBST = 1<br>VDDSPK = VDDA | | VDDA / 3.3 | | $V_{rms}$ |
| | | SPKBST = 0<br>VDDSPK = VDDA * 1.5 | | (VDDA / 3.3) * 1.5 | | $V_{rms}$ |
| Total harmonic distortion [2] | THD+N | $P_o$ = 320mW,<br>VDDSPK=3.3V | | -64 | | dB |
| | | $P_o$ = 400mW,<br>VDDSPK = 3.3V | | -60 | | dB |
| | | $P_o$ = 860mW,<br>VDDSPK = 5.0V | | -60 | | dB |
| | | $P_o$ = 1000mW,<br>VDDSPK = 5.0V | | -34 | | dB |
| Signal-to-noise ratio | SNR | VDDSPK = 3.3V | | 91 | | dB |
| Power supply rejection ratio (50Hz - 22kHz) | PSRR | | | 81 | | dB |
| Maximum programmable gain | | | | +6 | | dB |
| Minimum programmable gain | | | | -57 | | dB |
| Programmable gain step size | | Guaranteed monotonic | | 1 | | dB |
| Mute attenuation | | 1kHz full scale signal | | 85 | | dB |
| **Headphone Output (RHP / LHP with 32Ω load)** | | | | | | |
| 0dB full scale output voltage | | | | VDDA / 3.3 | | $V_{rms}$ |
| Signal-to-noise ratio | SNR | A-weighted | | 92 | | dB |
| Total harmonic distortion [2] | THD+N | $R_L$ = 16Ω, $P_o$ = 20mW,<br>VDDA = 3.3V | | 80 | | dB |
| | | $R_L$ = 32Ω, $P_o$ = 20mW,<br>VDDA = 3.3V | | 85 | | dB |
| Maximum programmable gain | | | | +6 | | dB |
| Minimum programmable gain | | | | -57 | | dB |
| Programmable gain step size | | Guaranteed monotonic | | 1 | | dB |
| Mute attenuation | | 1kHz full scale signal | | 85 | | dB |
| **AUXOUT1 / AUXOUT2 with 10kΩ / 50pF load** | | | | | | |
| Full scale output [3] | | AUX1BST = 1<br>AUX2BST = 1<br>VDDSPK = VDDA | | VDDA / 3.3 | | $V_{rms}$ |
| | | AUX1BST = 0<br>AUX2BST = 0<br>VDDSPK = VDDA * 1.5 | | (VDDA / 3.3) * 1.5 | | $V_{rms}$ |
| Signal-to-noise ratio | SNR | | | 87 | | dB |
| Total harmonic distortion [2] | THD+N | | | -83 | | dB |
| Channel separation | | 1kHz signal | | 99 | | dB |
| Power supply rejection ratio (50Hz - 22kHz) | PSRR | | | 53 | | dB |

**Electrical Characteristics, cont'd.**

Conditions: VDDC = 1.8V, VDDA = VDDB = VDDSPK = 3.3V, MCLK = 12.288MHz,
$T_A$ = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data, unless otherwise stated.

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Line Level Analog Inputs (LINPUT, RINPUT)** | | | | | | |
| Full scale input signal [1] | | Gain = 0dB | | 1.0<br>0 | | Vrms<br>dBV |
| Input resistance | | Aux direct-to-out path, only<br>Input gain = +6.0dB<br>Input gain = 0.0dB<br>Input gain = -12dB | | <br>20<br>40<br>159 | | <br>kΩ<br>kΩ<br>kΩ |
| Input capacitance | | | | 10 | | pF |
| **PRGREF programmable reference voltage** | | | | | | |
| Output voltage | $V_{PRGREF}$ | See Figure 3 | 0.50, 0.60,0.65, 0.70, 0.75, 0.85, or 0.90 | | | VDDA<br>VDDA |
| Output current | $I_{PRGREF}$ | | | 3 | | mA |
| Output noise voltage | $V_n$ | 1kHz to 20kHz | | 14 | | nV/√Hz |
| **Digital Input/Output** | | | | | | |
| Input HIGH level | $V_{IL}$ | | 0.7 * VDDB | | | V |
| Input LOW level | $V_{IH}$ | | | | 0.3 * VDDB | V |
| Output HIGH level | $V_{OH}$ | $I_{Load}$ = 1mA | 0.9 * VDDB | | | V |
| Output LOW level | $V_{OL}$ | $I_{Load}$ = -1mA | | | 0.1 * VDDB | V |
| Input capacitance | | | | 10 | | pF |

**Notes**

1. Full Scale is relative to the magnitude of VDDA and can be calculated as FS = VDDA/3.3.
2. Distortion is measured in the standard way as the combined quantity of distortion products plus noise. The signal level for distortion measurements is at 3dB below full scale, unless otherwise noted.
3. With default register settings, VDDSPK should be 1.5xVDDA (but not exceeding maximum recommended operating voltage) to optimize available dynamic range in the AUXOUT1 and AUXOUT2 line output stages. Output DC bias level is optimized for VDDSPK = 5.0Vdc (boost mode) and VDDA = 3.3Vdc.

## Absolute Maximum Ratings

| Condition | Min | Max | Units |
|---|---|---|---|
| VDDB, VDDC, VDDA supply voltages | -0.3 | +3.61 | V |
| VDDSPK supply voltage (default register configuration) | -0.3 | +5.80 | V |
| VDDSPK supply voltage (optional low voltage configuration) | -0.3 | +3.61 | V |
| Core Digital Input Voltage range | VSSD – 0.3 | VDDC + 0.30 | V |
| Buffer Digital Input Voltage range | VSSD – 0.3 | VDDB + 0.30 | V |
| Analog Input Voltage range | VSSA – 0.3 | VDDA + 0.30 | V |
| Industrial operating temperature | -40 | +85 | °C |
| Storage temperature range | -65 | +150 | °C |

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.*

## Operating Conditions

| Condition | Symbol | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| Digital supply range (Core) | VDDC | 1.65 | | 3.60 | V |
| Digital supply range (Buffer) | VDDB | 1.65 | | 3.60 | V |
| Analog supply range | VDDA | 2.50 | | 3.60 | V |
| Speaker supply<br>required: SPKBST=AUX1BST=AUX2BST = 0 | VDDSPK | 2.50 | | 5.50 | V |
| Speaker supply<br>if any: SPKBST, AUX1BST, or AUX2BST = 1 | VDDSPK | 2.50 | | 3.60 | V |
| Ground | VSSD<br>VSSA<br>VSSSPK | | 0 | | V |

1. VDDA must be ≥ VDDC.
2. VDDB must be ≥ VDDC.

# 1 General Description

The NAU8401 is a stereo device with identical left and right channels that share common support elements. Additionally, the right channel auxiliary output path includes a dedicated submixer that supports mixing the right auxiliary input directly into the right speaker output driver. This enables the right speaker channel to output audio that is not present on any other output.

### 1.1.1 Analog Inputs

The left and right analog inputs have available analog input gain conditioning of -15dB through +6dB in 3dB steps. These inputs include individual muting functions with excellent channel isolation and off-isolation, and are suitable for full quality, high bandwidth signals.

### 1.1.2 Analog Outputs

There are six high current analog audio outputs. These are very flexible outputs that can be used individually or in stereo pairs for a wide range of end uses. However, these outputs are optimized for specific functions and are described in this section using the functional names that are applicable to those optimized functions.

Each output receives its signal source from built-in analog output mixers. These mixers enable a wide range of signal combinations, including muting of all sources. Additionally, each output has a programmable gain function, output mute function, and output disable function.

The RHP and LHP headphone outputs are optimized for driving a stereo pair of headphones, and are powered from the main analog voltage supply rail, VDDA. These outputs may be coupled using traditional DC blocking series capacitors. Alternatively, these may be configured in a no-capacitor DC coupled design using a virtual ground at ½ VDDA provided by an AUXOUT analog output operating in the non-boost output mode.

The AUXOUT1 and AUXOUT2 analog outputs are powered from the VDDSPK supply rail and VSSSPK ground return path. The supply rail may be the same as VDDA, or may be a separate voltage up to 5.5Vdc. This higher voltage enables these outputs to have an increased output voltage range and greater output power capability.

The RSPKOUT and LSPKOUT loudspeaker outputs are powered from the VDDSPK power supply rail and VSSGND ground return path. LSPKOUT receives its audio signal via an additional submixer. This submixer supports combining a traditional alert sound (from the RINPUT input) with the right channel headphone output mixer signal. This submixer also provides the signal invert function that is necessary for the normal BTL (Bridge Tied Load) configuration used to drive a high power external loudspeaker. Alternatively, each loudspeaker output may be used individually as a separate high current analog output driver.

### 1.1.3 DAC and Digital Signal Processing

Each left and right channel has an independent high quality DAC associated with it. These are high performance, 24-bit delta-sigma converters that are suitable for a very wide range of applications.

The DAC functions are each individually supported by powerful analog mixing and routing. The DAC blocks are also supported by advanced digital signal processing subsystems that enable a very wide range of programmable signal conditioning and signal optimizing functions. All digital processing is with 24-bit precision, as to minimize processing artifacts and maximize the audio dynamic range supported by the NAU8401.

The DACs are supported by a programmable limiter/DRC (Dynamic Range Compressor). This is useful to optimize the output level for various applications and for use with small loudspeakers. This is an optional feature that may be programmed to limit the maximum output level and/or boost an output level that is too small.

Digital signal processing is also provided for a 3D Audio Enhancement function, and for a 5-Band Equalizer. These features are optional, and are programmable over wide ranges. This pair of digital processing features may be applied jointly to the DAC audio path, or be jointly disabled from the DAC audio path.

### 1.1.4 Programmable Voltage Reference

The filtered Vref pin is buffered and scaled to create a low-noise programmable DC output voltage. This output may be used for a wide range of purposes, such as providing a DC bias for other amplifiers and components in the system.

### 1.1.5 Digital Interfaces

Command and control of the device is accomplished using a 2-wire/3-wire/4-wire serial control interface. This is a simple, but highly flexible interface that is compatible with many commonly used command and control serial data protocols and host drivers.

Digital audio input/output data streams are transferred to and from the device separately from command and control. The digital audio data interface supports either I2S or PCM audio data protocols, and is compatible with commonly used industry standard devices that follow either of these two serial data formats.

### 1.1.6 Clock Requirements

The clocking signals required for the audio signal processing, audio data I/O, and control logic may be provided externally, or by optional operation of a built-in PLL (Phase Locked Loop). An external master clock (MCLK) signal must be active for analog audio logic paths to align with control register updates, and is required as the reference clock input for the PLL, if the PLL is used.

The PLL is provided as a low cost, zero external component count optional method to generate required clocks in almost any system. The PLL is a fractional-N divider type design, which enables generating accurate desired audio sample rates derived from a very wide range of commonly available system clocks.

The frequency of the system clock provided as the PLL reference frequency may be any stable frequency in the range between 8MHz and 33MHz. Because the fractional-N multiplication factor is a very high precision 24-bit value, any desired sample rate supported by the NAU8401 can be generated with very high accuracy, typically limited by the accuracy of the external reference frequency. Reference clocks and sample rates outside of these ranges are also possible, but may involve performance tradeoffs and increased design verification.

# 2 Power Supply

This device has been designed to operate reliably using a wide range of power supply conditions and power-on/power-off sequences. There are no special requirements for the sequence or rate at which the various power supply pins change. Any supply can rise or fall at any time without harm to the device. However, pops and clicks may result from some sequences. Optimum handling of hardware and software power-on and power-off sequencing is described in more detail in the Applications section of this document.

### 2.1.1 Power-On Reset

The NAU8401 does not have an external reset pin. The device reset function is automatically generated internally when power supplies are too low for reliable operation. The internal reset is generated any time that either VDDA or VDDC is lower than is required for reliable maintenance of internal logic conditions. The reset threshold voltage for VDDA and VDDC is approximately 0.5Vdc. If both VDDA and VDDC are being reduced at the same time, the threshold voltage may be slightly lower. Note that these are much lower voltages than are required for normal operation of the chip. These values are mentioned here as general guidance as to overall system design.

If either VDDA or VDDC is below its respective threshold voltage, an internal reset condition is asserted. During this time, all registers and controls are set to the hardware determined initial conditions. Software access during this time will be ignored, and any expected actions from software activity will be invalid.

When both VDDA and VDDC reach a value above their respective thresholds, an internal reset pulse is generated which extends the reset condition for an additional time. The duration of this extended reset time is approximately 50 microseconds, but not longer than 100 microseconds. The reset condition remains asserted during this time. If either VDDA or VDDC at any time becomes lower than its respective threshold voltage, a new reset condition will result. The reset condition will continue until both VDDA and VDDC again higher than their respective thresholds. After VDDA and VDDC are again both greater than their respective threshold voltage, a new reset pulse will be generated, which again will extend the reset condition for not longer than an additional 100 microseconds.

### 2.1.2 Power Related Software Considerations

There is no direct way for software to determine that the device is actively held in a reset condition. If there is a possibility that software could be accessing the device sooner than 100 microseconds after the VDDA and VDDC supplies are valid, the reset condition can be determined indirectly. This is accomplished by writing a value to any register other than register 0x00, with that value being different than the power-on reset initial values. The optimum choice of register for this purpose may be dependent on the system design, and it is recommended the system engineer choose the register and register test bit for this purpose. After writing the value, software will then read back the same register. When the register test bit reads back as the new value, instead of the power-on reset initial value, software can reliably determine that the reset condition has ended.

Although it is not required, it is strongly recommended that a Software Reset command should be issued after power-on and after the power-on reset condition is ended. This will help insure reliable operation under every power sequencing condition that could occur.

If there is any possibility that VDDA or VDDC could be unreliable during system operation, software may be designed to monitor whether a power-on reset condition has happened. This can be accomplished by writing a test bit to a register that is different from the power-on initial conditions. This test bit should be a bit that is never used for any other reason, and does not affect desired operation in any way. Then, software at any time can read this bit to determine if a power-on reset condition has occurred. If this bit ever reads back other than the test value, then software can reliably know that a power-on reset event has occurred. Software can subsequently re-initialize the device and the system as required by the system design.

### 2.1.3 Software Reset

All chip registers can be reset to power-on default conditions by writing any value to register 0, using any of the control modes. Writing valid data to any other register disables the reset, but all registers need to have the correct operating data written. See the applications section on powering NAU8401 up for information on avoiding pops and clicks after a software reset.

# 3 Input Path Detailed Description

The NAU8401 provides two analog inputs that are buffered, scaled, optionally muted, and then made available to the output mixers. The output mixers enable a wide range of possible routing of these inputs to the analog output pins, as well as mixing with the output signal from the DAC subsystem.

These inputs are maintained at a DC bias at approximately ½ of the AVDD supply voltage. Connections to these inputs should be AC-coupled by means of DC blocking capacitors suitable for the device application. If not used, these input pins should not be left not-connected and muted in the software register controls.

The RINPUT signal may additionally be routed to the Right Speaker Submixer in the analog output section. This path enables a sound to be output from the LSPKOUT speaker output, but without being audible anywhere else in the system. One purpose of this path is to support a traditional "beep" sound, such as from a microprocessor toggle bit. This is a historical application scenario which is now uncommon.

These inputs are affected by the following registers:

LMAIN MIXER or RMAIN MIXER if used (see output mixer section)
RSPK SUBMIXER if used (see Right Speaker Submixer section)

## 3.1 Analog Input Impedance and Variable Gain Stage Topology

Each analog input pin is supported by the circuit shown here as a simplified schematic. The gain value changes affect input impedance as detailed in this section. If a path is in the "not selected" condition, then the input impedance will be in a high impedance condition and the input signal will be muted. If an external input pin is not used anywhere in the system, it will be coupled to a DC tie-off of approximately 30kΩ coupled to VREF. The unused input tie-off function is explained in more detail in the Application Information section of this document.

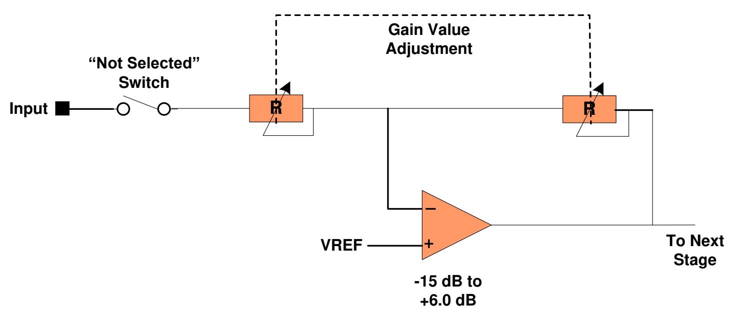



Figure 2: Variable Gain Stage Simplified Schematic

The input impedance presented to these inputs depends on the input routing choices and gain values. The nominal resistive input impedances presented to signal pins that are directly routed to an output mixer are listed in the following table. The RINPUT signal may also be connected to the Right Speaker Submixer. If both RINPUT signal paths are connected, then the RINPUT input impedance will be the parallel combination of the two paths.

| Inputs | Gain (dB) | Impedance (kΩ) |
|---|---|---|
| LINPUT & RINPUT to bypass amp<br><br>Or<br><br>RINPUT to RSPK SUBMIXER amp | -15 | 225 |
| | -12 | 159 |
| | -9 | 113 |
| | -6 | 80 |
| | -3 | 57 |
| | 0 | 40 |
| | 3 | 28 |
| | 6 | 20 |

Table 1: Analog Input and RSPK SUBMIXER Input Impedances

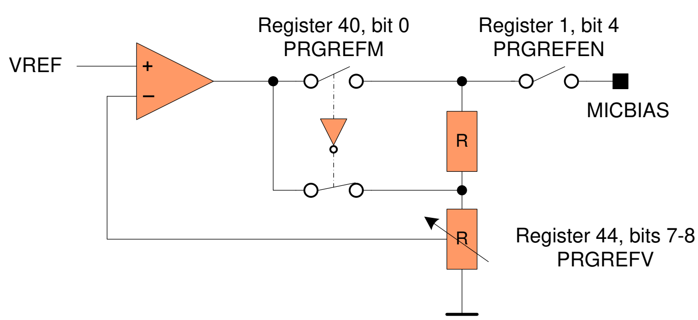
### 3.2 Programmable Reference Voltage Controls

The PRGREF pin provides a low-noise DC bias voltage as may be required for other elements in the audio subsystem. This built-in feature can typically provide up to 3mA of bias current. This DC bias voltage is also suitable for powering either traditional ECM (electret) type microphones, or for MEMS types microphones with an independent power supply pin.

Seven different bias voltages are available for optimum system performance, depending on the specific application. The bias pin normally requires an external filtering capacitor as shown on the schematic in the Application section. The programmable voltage bias function is controlled by the following registers:

R1 Power control for PRGREF feature (enabled when bit 4 = 1)
R44 Optional low-noise mode and different bias voltage levels (enabled when bit 0 = 1)
R44 Primary PRGREF voltage selection

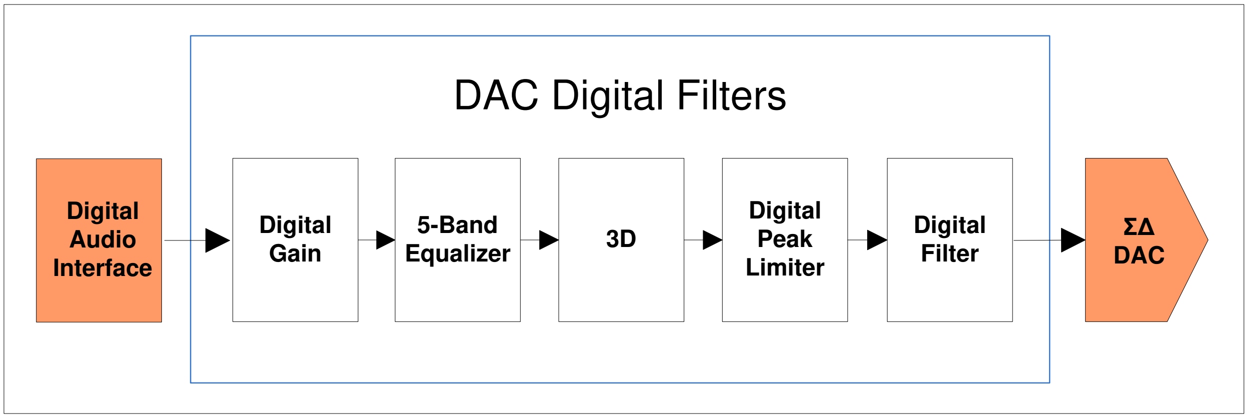
The low-noise feature results in greatly reduced noise in the external PRGREF voltage by placing a resistor of approximately 200-ohms in series with the output pin. This creates a low pass filter in conjunction with the external reference voltage filter capacitor, but without any additional external components. The low noise feature is enabled when the mode control bit 0 in register R40 is set (level = 1)




| Register 44, Bits 7-8 | Register 44, Bit 0 | Output DC Bias Voltage |
|---|---|---|
| 00 | 0 | 0.90 * VDDA |
| 01 | 0 | 0.65 * VDDA |
| 10 | 0 | 0.75 * VDDA |
| 11 | 0 | 0.50 * VDDA |
| 00 | 1 | 0.85 * VDDA |
| 01 | 1 | 0.60 * VDDA |
| 10 | 1 | 0.70 * VDDA |
| 11 | 1 | 0.50 * VDDA |

Figure 3: Programmable Reference Bias Generator

# 4 DAC Digital Block




The DAC digital block uses 24-bit signal processing to generate analog audio with a 16-bit digital sample stream input. This block consists of a sigma-delta modulator, digital decimator/filter, and optional 5-band graphic equalizer/3D effects block, and a dynamic range compressor/limiter. The DAC coding scheme is in twos complement format and the full-scale output level is proportional to VDDA. With a 3.3V supply voltage, the full-scale output level is $1.0V_{RMS}$.

Registers that affect the DAC operation are:

R3 Power management enable/disable left/right DAC
R7 Sample rate indication bits (affect filter frequency scaling)
R10 Softmute, Automute, oversampling options, polarity controls for left/right DAC
R11 Left channel DAC digital volume value; update bit feature
R12 Right channel DAC digital volume value; update bit feature

## 4.1 DAC Soft Mute

Both DACs are initialized with the SoftMute function disabled, which is a shared single control bit. Softmute automatically ramps the DAC digital volume down to zero volume when enabled, and automatically ramps the DAC digital volume up to the register specified volume level for each DAC when disabled. This feature provides a tool that is useful for using the DACs without introducing pop and click sounds.

## 4.2 DAC AutoMute

The analog output of both DACs can be automatically muted in a no signal condition. Both DACs share a single control bit for this function. When automute is enabled, the analog output of the DAC will be muted any time there are 1024 consecutive audio sample values with a zero value. If at any time there is a non-zero sample value, the DAC will be un-muted, and the 1024 count will be reinitialized to zero.

## 4.3 DAC Sampling / Oversampling Rate, Polarity Control, Digital Passthrough

The sampling rate of the DAC is determined entirely by the frequency of its input clock and the oversampling rate setting. The oversampling rate of the DAC can be changed to 128X for improved audio performance at slightly higher power consumption. Because the additional supply current is only 1mA, in most applications the 128X oversampling is preferred for maximum audio performance.

The polarity of either DAC output signal can be changed independently on either DAC analog output as a feature sometimes useful in management of the audio phase. This feature can help minimize any audio processing that may be otherwise required as the data are passed to other stages in the system.

## 4.4 DAC Digital Volume Control and Update Bit Functionality

The effective output audio volume of each DAC can be changed using the digital volume control feature. This processes the output of the DAC to scale the output by the amount indicated in the volume register setting. Included is a "digital mute" value which will completely mute the signal output of the DAC. The digital volume setting can range from 0dB through -127dB in 0.5dB steps.

***Important***: The R11 and R12 update bits are write-only bits. The primary intended purpose of the update bit is to enable simultaneous changes to both the left and right DAC volume values, even though these values must be written sequentially. When there is a write operation to either R11 or R12 volume settings, but the update bit is not set (value = 0), the new volume setting is stored as pending for the future, but does not go into effect. When there is a write operation to either R11 or R12 and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending value in the other DAC volume register is put into effect at the same time.

## 4.5 DAC Automatic Output Peak Limiter / Volume Boost

Both DACs are supported by a digital output volume limiter/boost feature which can be useful to keep output levels within a desired range without any host/processor intervention. Settings are shared by both DAC channels.

Registers that manage the peak limiter and volume boost functionality are:

R24 Limiter enable/disable, limiter attack rate, boost decay rate
R25 Limiter upper limit, limiter boost value

The operation of the peak limiter is shown in the following figure. The upper signal graphs show the time varying level of the input and output signals, and the lower graph shows the gain characteristic of the limiter. When the signal level exceeds the limiter threshold value by 0.5dB or greater, the DAC digital signal level will be attenuated at a rate set by the limiter attack rate value. When the input signal level is less than the boost lower limit by 0.5dB or greater, the DAC digital volume will be increased at a rate set by the boost decay rate value. The default boost gain value is limited not to exceed 0dB (zero attenuation).

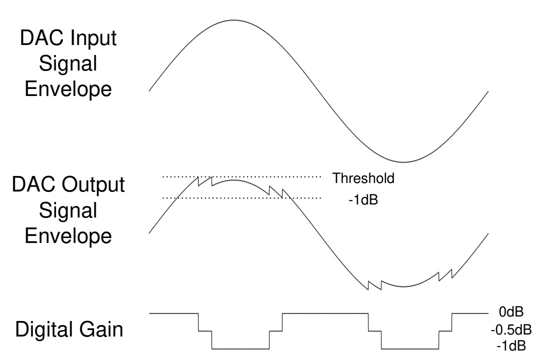



Figure 4: DAC Digital Limiter Control

The limiter may optionally be set to automatically boost the DAC digital signal level when the signal is more than 0.5dB below the limiter threshold. This can be useful in applications in which it is desirable to compress the signal dynamic range. This is accomplished by setting the limiter boost register bits to a value greater than zero. If the limiter is disabled, this boost value will be applied to the DAC digital output signal separate from other gain affecting values.

## 4.6 5-Band Equalizer

The NAU8401 includes a 5-band graphic equalizer with low distortion, low noise, and wide dynamic range. The equalizer is applied to both left and right channels. The equalizer is grouped with the 3D Stereo Enhancement signal processing function. These functions are applied to the DAC output signals, only, and do not affect the LINPUT and RINPUT analog input signals.

Registers that affect operation of the 5-Band Equalizer are:

R18 Enable / Disable Equalizer function
R18 Band 1 gain control and cut-off frequency
R19 Band 2 gain control, center cut-off frequency, and bandwidth
R20 Band 3 gain control, center cut-off frequency, and bandwidth
R21 Band 4 gain control, center cut-off frequency, and bandwidth
R22 Band 5 gain control and cut-off frequency

Each of the five equalizer bands is independently adjustable for maximum system flexibility, and each offers up to 12dB of boost and 12dB of cut with 1dB resolution. The high and the low bands are shelving filters (high-pass and low-pass, respectively), and the middle three bands are peaking filters. Details of the register value settings are described below. Response curve examples are provided in the Appendix of this document.

| Register Value | Equalizer Band | | | | |
|---|---|---|---|---|---|
| | 1 (High Pass) Register 18 Bits 5 & 6 EQ1CF | 2 (Band Pass) Register 19 Bits 5 & 6 EQ2CF | 3 (Band Pass) Register 20 Bits 5 & 6 EQ3CF | 4 (Band Pass) Register 21 Bits 5 & 6 EQ4CF | 5 (Low Pass) Register 22 Bits 5 & 6 EQ5CF |
| 00 | 80Hz | 230Hz | 650Hz | 1.8kHz | 5.3kHz |
| 01 | 105Hz | 300Hz | 850Hz | 2.4kHz | 6.9kHz |
| 10 | 135Hz | 385Hz | 1.1kHz | 3.2kHz | 9.0kHz |
| 11 | 175Hz | 500Hz | 1.4kHz | 4.1kHz | 11.7kHz |

Table 2: Equalizer Center/Cutoff Frequencies

| Register Value | | Gain | Registers |
|---|---|---|---|
| Binary | Hex | | |
| 00000 | 00h | +12db | Bits 0 to 4 in registers 18 (EQ1GC) 19 (EQ2GC) 20 (EQ3GC) 21 (EQ4GC) 22 (EQ5GC) |
| 00001 | 01h | +11dB | |
| 00010 | 02h | +10dB | |
| - - - | - - | Increments 1dB per step | |
| 01100 | 0Ch | 0dB | |
| 01101 | 17h | -11dB | |
| - - - | - - | Increments 1dB per step | |
| 11000 | 18h | -12dB | |
| 11001 to 11111 | 19h to 1Fh | Reserved | |

Table 3: Equalizer Gains

## 4.7 3D Stereo Enhancement

NAU8401 includes digital circuitry to provide flexible 3D enhancement to increase the perceived separation between the right and left channels, and has multiple options for optimum acoustic performance. The equalizer is grouped with the 3D Stereo Enhancement signal processing function. Both functions may be assigned jointly to support the DAC audio output path, or may be jointly disabled from the DAC audio output path.

Registers that affect operation of 3D Stereo Enhancement are:

R18 Enable / Disable 3D enhancement function
R41 3D Audio depth enhancement setting

The amount of 3D enhancement applied can be programmed from the default 0% (no 3D effect) to 100% in register 41, bits 0 to 3 (DEPTH3D), as shown in the following table. Note: 3D enhancement uses increased gain to achieve its effect, so that the source signal may need to be attenuated by up to 6dB to avoid clipping distortion.

| **Register 41<br>Bits 0 to 3<br>3DDEPTH** | **3D Effect** |
|---|---|
| 0000 | 0% |
| 0001 | 6.7%dB |
| 0010 | 13.4%dB |
| - - - | Increments 6.67% for each binary step in the input word |
| 1110 | 93.3% |
| 1111 | 100% |

Table 4: 3D Enhancement Depth

## 4.8 DAC Output A-law and μ-law Expansion

Companding (compression | expansion) is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates, using non-linear algorithms. NAU8401 supports the two main telecommunications expansion standards on the DAC path receive side: A-law and μ-law. The A-law algorithm is primarily used in European communication systems and the μ-law algorithm is primarily used by North America, Japan, and Australia. On the sending side of a telecommunications system, audio is converted from a linear dynamic range of approximately 13 bits (μ-law) or 12 bits (A-law) into a compressed 8-bit format using non-linear quantization. The compressed signal is an 8bit word containing sign (1-bit), exponent (3-bits) and mantissa (4-bits). The DAC can then convert the compressed back into the original 13-bit or 12-bit linear audio format.

The register affecting companding operation is:

R5 Enable 8-bit mode, enable DAC expansion

Following are the data compression equations set in the ITU-T G.711 standard and implemented in the NAU8401:

### 4.8.1 μ law

$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu) \qquad -1 \le x \le 1$

with μ=255 for the U.S. and Japan

### 4.8.2 A-law

$F(x) = A|x| / (1 + \ln A) \qquad \text{for } x \le 1/A$

$F(x) = (1 + \ln A|x|) / (1 + \ln A) \qquad \text{for } 1/A \le x \le 1$

with A=87.6 for Europe

The companded signal is an 8-bit word consisting of a sign bit, three bits for the exponent, and four bits for the mantissa. When companding is enabled, the PCM interface must be set to an 8-bit word length. When in 8-bit mode, the Register 4 word length control (WLEN) is ignored.

| Companding Mode | Register 5 | | | |
|---|---|---|---|---|
| | Bit 4 | Bit3 | Bit 2 | Bit 1 |
| No Companding (default) | 0 | 0 | 0 | 0 |
| DAC | | | | |
| A-law | 1 | 1 | | |
| μ-law | 1 | 0 | | |

Table 5: Companding Control

## 4.9 8-bit Word Length

Writing a 1 to register 5, bit 5 (CMB8), will cause the PCM interface to use 8-bit word length for data transfer, overriding the word length configuration setting in WLEN (register 4, bits 5 and 6.).

# 5 Analog Outputs

The NAU8401 features six different analog outputs. These are highly flexible and may be used individually or in pairs for many purposes. However, they are grouped in pairs and named for their most commonly used stereo application end uses. The following sections detail key features and functions of each type of output. Included is a description of the associated output mixers. These mixers are separate internal functional blocks that are important toward understanding all aspects of the analog output section.

***Important:*** For analog outputs depopping purpose, when powering up speakers, headphone, AUXOUTs, certain delays are generated after enabling sequence. However, the delays are created by MCLK and sample rate register. For correct operation, sending I2S signal no earlier than 250ms after speaker or headphone enabled and MCLK appearing.

## 5.1 Main Mixers (LMAIN MIX and RMAIN MIX)

Each left and right channel is supported by an independent main mixer. This mixer combines signals from a various available signal sources internal to the device. Each mixer may also be selectively enabled/disabled as part of the power management features. The outputs of these mixers are the only signal source for the headphone outputs, and the primary signal source for the loudspeaker outputs.

Each mixer can accept either or both the left and right digital to analog (DAC) outputs. Normally, the left and right DAC is mixed into the associated left and right main output mix. This additional capability to mix opposite DAC channels enables switching the left and right DAC outputs to the opposite channel, or mixing together the left and right DAC signals – all without any processor or host intervention and processing overhead.

Each mixer also can also combine signals directly from the respective left or right line input (LINPUT and RINPUT). Each of these analog input paths may be muted, or have an applied selectable gain between -15dB and +6dB in 3dB steps.

Registers that affect operation of the Main Mixers are:

R3 Power control for the left and right main mixer
R49 left and right DAC cross-mixing source selection options
R50 left DAC to left main mixer source selection option
R51 right DAC to right main mixer source selection option
R50 left mixer source select, and gain settings
R51 right mixer source select, and gain settings

## 5.2 Auxiliary Mixers (AUX1 MIXER and AUX2 MIXER)

Each auxiliary analog output channel is supported by an independent mixer dedicated to the auxiliary output function. This mixer combines signals from a various available signal sources internal to the device. Each mixer may also be selectively enabled/disabled as part of the power management features.

Unlike the main mixers, the auxiliary mixers are not identical and combine different signal sets internal to the device. These mixers in conjunction with the auxiliary outputs greatly increase the overall capabilities and flexibility of the NAU8401.

The AUX1 mixer combines together any or all of the following:

Left Main Mixer output
Right Main Mixer output
Left DAC output
Right DAC output

The AUX2 mixer combines together any or all of the following:

Left Main Mixer output
Left DAC output
Output from AUX1 mixer stage

Registers that affect operation of the Auxiliary Mixers are:

R1 Power control for the left and right auxiliary mixer
R56 Signal source selection for the AUX2 mixer
R57 Signal source selection for the AUX1 mixer

## 5.3 Right Speaker Submixer

The right speaker submixer serves two important functions. One is to optionally invert the output from the Right Main Mixer as an optional signal source for the right channel loudspeaker output driver. This inversion is normal and necessary in typical applications using the loudspeaker drivers.

The other function of the right speaker submixer is to mix the RINPUT input signal directly into the right channel speaker output driver. This enables the RINPUT signal to be output on the right loudspeaker channel, but not be mixed to any other output. The traditional purpose of this path is to support an old-style beep sound, such as traditionally generated by a microprocessor output toggle bit. On the NAU8401, this traditional function is supported by a full quality signal path that may be used for any purpose. The volume for this path has a selectable gain from -15dB through +6dB in 3dB step increments.

There is no separate power management control feature for the Right Speaker Submixer. The register that affects the Right Speaker Submixer is:

R43 Input mute controls, volume for RINPUT path

## 5.4 Headphone Outputs (LHP and RHP)

These are high quality, high current output drivers intended for driving low impedance loads such as headphones, but also suitable for a wide range of audio output applications. The only signal source for each of these outputs is from the associated left and right Main Mixer. Power for this section is provided from the VDDA pin. Each driver may be selectively enabled/disabled as part of the power management features.

Each output can be individually muted, or controlled over a gain range of -57dB through +6dB in 3dB steps. Gain changes for the two headphone outputs can be coordinated through use of an update bit feature as part of the register controls. Additionally, clicks that could result from gain changes can be suppressed using an optional zero crossing feature.

Registers that affect the headphone outputs are:

R2 Power management control for the left and right headphone amplifier
R52 Volume, mute, update, and zero crossing controls for left headphone driver
R53 Volume, mute, update, and zero crossing controls for right headphone driver

***Important:*** The R52 and R53 update bits are write-only bits. The primary intended purpose of the update bit is to enable simultaneous changes to both the left and right headphone output volume values, even though these two register values must be written sequentially. When there is a write operation to either R52 or R53 volume settings, but the update bit is not set (value = 0), the new volume setting is stored as pending for the future, but does not go into effect. When there is a write operation to either R52 or R53 and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending value in the other headphone output volume register is put into effect at the same time.

Zero-Crossing controls are implemented to suppress clicking sounds that may occur when volume setting changes take place while an audio input signal is active. When the zero crossing function is enabled (logic = 1), any volume change for the affected channel will not take place until the audio input signal passes through the zero point in its peak-to-peak swing. This prevents any instantaneous voltage change to the audio signal caused by volume setting changes. If the zero crossing function is disabled (logic = 0), volume changes take place instantly on condition of the Update Bit, but without regard to the instantaneous voltage level of the affected audio input signal.

## 5.5 Speaker Outputs

These are high current outputs suitable for driving low impedance loads, such as an 8-ohm loudspeaker. Both outputs may be used separately for a wide range of applications, however, the intended application is to use both outputs together in a BTL (Bridge-Tied-Load, and also, Balanced-Transformer-Less) configuration. In most applications, this configuration requires an additional signal inversion, which is a feature supported in the right speaker submixer block.
This inversion is normal and necessary when the two speaker outputs are used together in a BTL (Bridge-Tied-Load, and also, Balanced-Transformer-Less) configuration. In this physical configuration, the RSPKOUT signal is connected to one pole of the loudspeaker, and the LSPKOUT signal is connected to the other pole of the loudspeaker. Mathematically, this creates within the loudspeaker a signal equal to (Left-Right). The desired mathematical operation for a stereo signal is to drive the speaker with (Left+Right). This is accomplished by implementing an additional inversion to the right channel signal. For most applications, best performance will be achieved when care is taken to insure that all gain and filter settings in both the left and right channel paths to the loudspeaker drivers are identical.

Power for the loudspeaker outputs is supplied via the VDDSPK pin, and ground is independently provided as the VSSPK pin. This power option enables an operating voltage as high as 5Vdc and helps in a system design to prevent high current outputs from creating noise on other supply voltage rails or system grounds. VSSPK must be connected at some point in the system to VSSA, but provision of the VSSPK as a separate high current ground pin facilitates managing the flow of current to prevent “ground bounce” and other ground noise related problems.

Each loudspeaker output may be selectively enabled/disabled as part of the power management features. Registers that affect the loudspeaker outputs are:

R3 Power management control of LSPKOUT and RSPKOUT driver outputs
R3 Speaker bias control (BIASGEN) set logic = 1 for maximum power and VDDSPK > 3.60Vdc
R48 Driver distortion mode control
R49 Disable boost control for speaker outputs for VDDSPK 3.3V or lower
R54 Volume (gain), mute, update bit, and zero crossing control for left speaker driver
R55 Volume (gain), mute, update bit, and zero crossing control for right speaker driver

***Important:*** The R49 boost control option is set in the power-on reset condition for high voltage operation of VDDSPK. If VDDSPK is greater than 3.6Vdc, the R49 boost control bits should be remain at the power-on default settings. This insures reliable operation of the part, proper DC biasing, and optimum scaling of the signal to enable the output to achieve full scale output when VDDSPK is greater than VDDA. In the boost mode, the gain of the output stage is increased by a factor of 1.5 times the normal gain value.

***Important:*** The R54 and R55 update bits are write-only bits. The primary intended purpose of the update bit is to enable simultaneous changes to both the left and right headphone output volume values, even though these two register values must be written sequentially. When there is a write operation to either R54 or R55 volume settings, but the update bit is not set (value = 0), the new volume setting is stored as pending for the future, but does not go into effect. When there is a write operation to either R54 or R55 and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending value in the other headphone output volume register is put into effect at the same time.

Zero-Crossing controls are implemented to suppress clicking sounds that may occur when volume setting changes take place while an audio input signal is active. When the zero crossing function is enabled (logic = 1), any volume change for the affected channel will not take place until the audio input signal passes through the zero point in its peak-to-peak swing. This prevents any instantaneous voltage change to the audio signal caused by volume setting changes. If the zero crossing function is disabled (logic = 0), volume changes take place instantly on condition of the Update Bit, but without regard to the instantaneous voltage level of the affected audio input signal.

The loudspeaker drivers may optionally be operated in an ultralow distortion mode. This mode may require additional external passive components to insure stable operation in some system configurations. No external components are required in normal mode speaker driver operation. Distortion performance in normal operation is excellent, and already suitable for almost every application.

## 5.6 Auxiliary Outputs

These are high current outputs suitable for driving low impedance loads such as headphones or line level loads. Power for these outputs is supplied via the VDDSPK pin, and ground is also independently provided as the VSSPK pin. This power option enables an operating voltage as high as 5Vdc and helps in a system design to prevent high current outputs from creating noise on other supply voltage rails or system grounds. VSSPK must be connected at some point in the system to VSSA, but provision of the VSSPK as a separate high current ground pin facilitates managing the flow of current to prevent "ground bounce" and other ground noise related problems.

Each auxiliary output driver may be selectively enabled/disabled as part of the power management features. Registers that affect the auxiliary outputs are:

R3 Power management control of AUXOUT1 and AUXOUT2 outputs
R3 Speaker bias control (BIASGEN) set logic = 1 for maximum power and VDDSPK > 3.60Vdc
R49 Disable boost control for AUXOUT1 and AUXOUT2 for VDDSPK 3.3Vdc or lower
R56 Mute, gain control, and input selection controls for AUXOUT2
R57 Mute, gain control, and input selection controls for AUXOUT1

***Important:*** The R49 boost control option is set in the power-on reset condition for high voltage operation of VDDSPK. If VDDSPK is greater than 3.6Vdc, the R49 boost control bits should be remain at the power-on default settings. This insures reliable operation of the part, proper DC biasing, and optimum scaling of the signal to enable the output to achieve full scale output when VDDSPK is greater than VDDA. In the boost mode, the gain of the output stage is increased by a factor of 1.5 times the normal gain value.

An optional alternative function for these outputs is to provide a virtual ground for an external headphone device. This is for eliminating output capacitors for the headphone amplifier circuit in applications where this type of design is appropriate. In this type of application, the AUXOUT output is typically operated in the muted condition. In the muted condition, and with the output configured in the non-boost mode (also requiring that VDDSPK < 3.61Vdc), the AUXOUT output DC level will remain at the internal VREF level. This the same internal DC level as used by the headphone outputs. Because these DC levels are nominally the same, DC current flowing through the headphone in this mode of operation is minimized. Depending on the application, one or both of the auxiliary outputs may be used in this fashion.

# 6 Miscellaneous Functions

## 6.1 Slow Timer Clock

An internal Slow Timer Clock is supplied to automatically control features that happen over a relatively periods of time, or time-spans. This enables the NAU8401 to implement long time-span features without any host/processor management or intervention.

Two features are supported by the Slow Timer Clock. These are an optional automatic time out for the zero-crossing holdoff of PGA volume changes, and timing for debouncing of the mechanical jack detection feature. If either feature is required, the Slow Timer Clock must be enabled.

The Slow Timer Clock is initialized in the disabled state. The Slow Timer Clock is controlled by only the following register:

R7 Sample rate indication select, and Slow Timer Clock enable

The Slow Timer Clock rate is derived from MCLK using an integer divider that is compensated for the sample rate as indicated by the R7 sample rate register. If the sample rate register value precisely matches the actual sample rate, then the internal Slow Timer Clock rate will be a constant value of 128ms. If the actual sample rate is, for example, 44.1kHz and the sample rate selected in R7 is 48kHz, the rate of the Slow Timer Clock will be approximately 10% slower in direct proportion of the actual vs. indicated sample rate. This scale of difference should not be important in relation to the dedicated end uses of the Slow Timer Clock.

## 6.2 General Purpose Inputs and Outputs (GPIO1, GPIO2, GPIO3) and Jack Detection

Three pins are provided in the NAU8401 that may be used for limited logic input/output functions. GPIO1 has multiple possible functions, and may be either a logic input or logic output. GPIO2 or GPIO3 may be used as logic inputs dedicated to the purpose of jack detection. GPIO3 is used as a logic output in 4-wire SPI mode, and GPIO2 does not have any logic output capability. Only one GPIO can be selected for jack detection.

If a GPIO is selected for the jack detection feature, the Slow Timer Clock must be enabled. The jack detection function is automatically "debounced" such that momentary changes to the logic value of this input pin are ignored. The Slow Timer Clock is necessary for the debouncing feature.

Registers that control the GPIO functionality are:

R8 GPIO functional selection options
R9 Jack Detection feature input selection and functional options

If a GPIO is selected for the jack detection function, the required Slow Timer Clock determines the duration of the time windows for the input logic debouncing function. Because the logic level changes happen asynchronously to the Slow Timer Clock, there is inherently some variability in the timing for the jack detection function. A continuous and persistent logic change on the GPIO pin used for jack detection will result in a valid internal output signal within 2.5 to 3.5 periods of the Slow Timer Clock. Any logic change of shorter duration will be ignored.

The threshold voltage for a jack detection logic-low level is no higher than 1.0Vdc. The threshold voltage for a jack detection logic-high level is no lower than 1.7Vdc. These levels will be reduced as the VDDC core logic voltage pin is reduced below 1.9Vdc.

## 6.3 Automated Features Linked to Jack Detection

Some functionality can be automatically controlled by the jack detection logic. This feature can be used to enable the internal analog amplifier bias voltage generator, and/or enable analog output drivers automatically as a result of detecting a logic change at a GPIO pin assigned to the purpose of jack detection. This eliminates any requirement for the host/processor to perform these functions.

The internal analog amplifier bias generator creates the VREF voltage reference and bias voltage used by the analog amplifiers. The ability to control it is a power management feature. This is implemented as a logical "OR" function of either the debounced internal jack detection signal, or the ABIASEN control bit in Register 1. The bias generator will be powered if either of these control signals is enabled (value = 1).

Power management control of four different outputs is also optionally and selectively subject to control linked with the jack detection signal. The four outputs that can be controlled this way are the headphone driver signal pair, loudspeaker driver signal pair, AUXOUT1, and AUXOUT2. Register settings determine which outputs may be enabled, and whether they are enabled by a logic 1 or logic 0 value. Output control is a logical "AND" operation of the jack detection controls, and of the register control bits that normally control the outputs. Both controls must be in the "ON" condition for a given output to be enabled.

Registers that affect these functions are:

R9 GPIO pin selection for jack detect function, jack detection enable, VREF jack enable
R13 bit mapped selection of which outputs are to be enabled when jack detect is in a logic 1 state
R13 bit mapped selection of which outputs are to be enabled when jack detect is in a logic 0 state