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NAU8501 **Data Sheet**
24-bit Stereo Audio ADC with Differential Microphone Inputs

emPowerAudio™

Description

The NAU8501 is a low power, high quality audio input system for portable applications. In addition to precision 24-bit stereo ADCs, this device integrates a broad range of additional functions to simplify implementation of complete audio systems. The NAU8501 includes low-noise stereo differential high gain microphone inputs with wide range programmable amplifiers, separate line inputs, and an analog bypass/sidetone line level stereo output.

Advanced on-chip digital signal processing includes a limiter/ALC (Automatic Level Control), 5-band equalizer, notch filter, and a high-pass filter for speech optimization and wind noise reduction. The digital interface can operate as either a master or a slave. Additionally, an internal fractional-N PLL is available to accurately generate any audio sample rate clock for the ADCs derived using any available system clock from 8MHz through 33MHz.

The NAU8501 operates with analog supply voltages from 2.5V to 3.6V, while the digital core can operate as low as 1.7V to conserve power. Internal control registers enable flexible power conserving modes, shutting down or reducing power in sub-sections of the chip under software control.

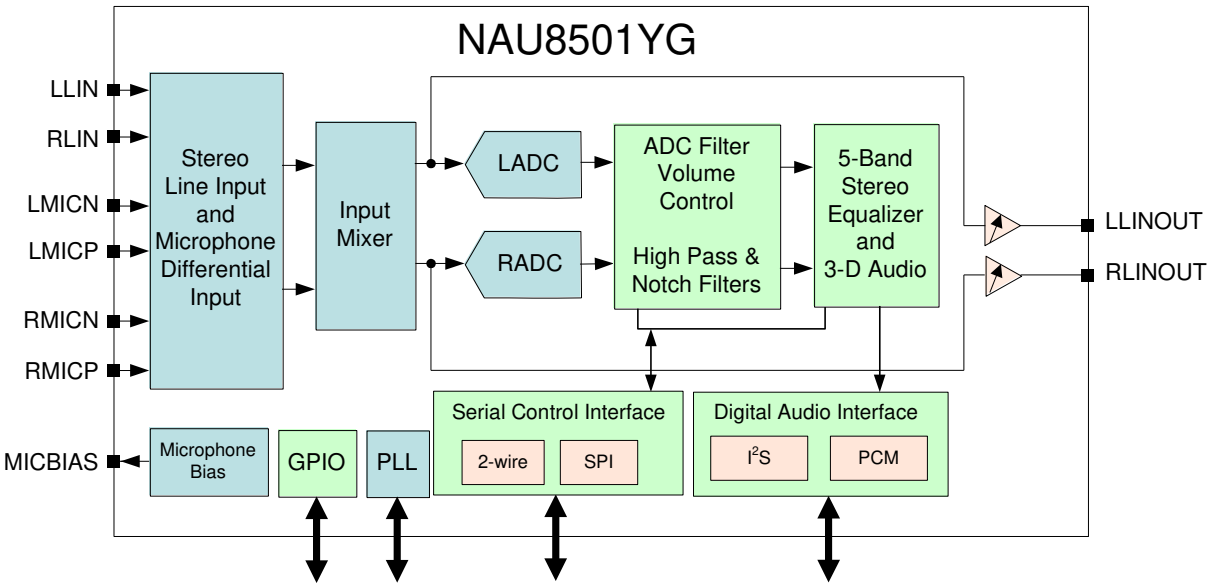
The NAU8501 is specified for operation from -40°C to +85°C. AEC-Q100 & TS16949 compliant device is available upon request.

Key Features

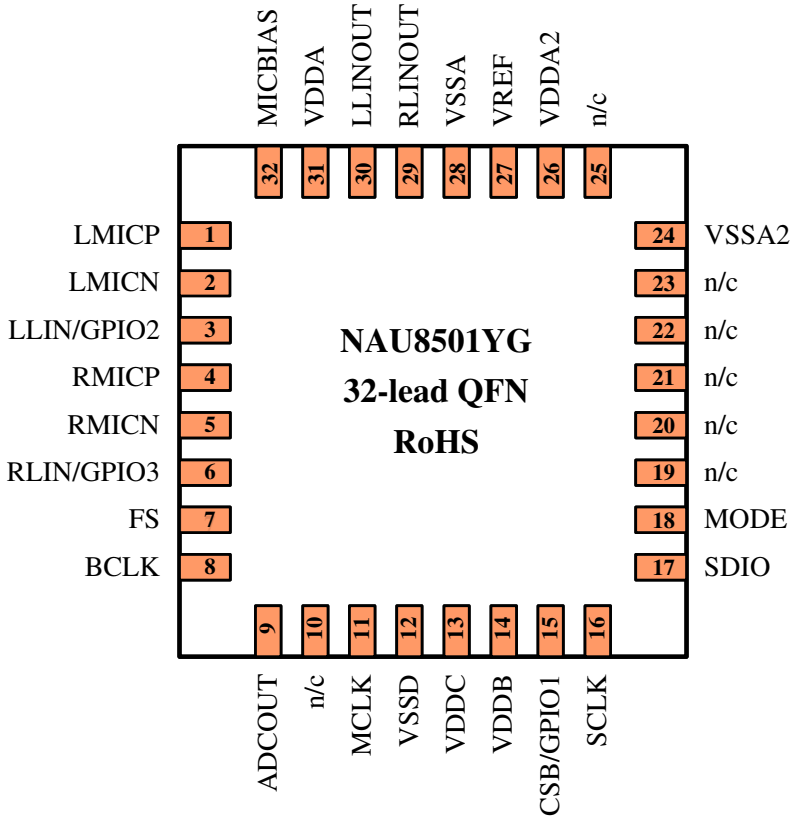
- ADC: 90dB SNR and -80dB THD ("A" weighted)
- Stereo differential input microphone amplifiers
- Very wide range programmable input amplifier
- Stereo line inputs with gain options and mixing
- Stereo line outputs with gain control and mute
- On-chip high resolution fractional-N PLL
- Integrated DSP with specific functions:
  - 5-band equalizer
  - High pass filter / wind noise reduction
  - Automatic level control / limiter
  - Programmable notch filter
- Serial control interfaces with read/write capability
- Standard audio interfaces: PCM and I^2S
- Supports any sample rate from 8kHz to 48kHz
- Read/Write control register interface

Applications

- Audio Recording Devices
- Security Systems
- Video and Still Cameras
- Enhanced Audio Inputs for SOC products
- Audio Input Accessory Products
- Gaming Systems



Pinout



Part Number	Dimension	Package	Package Material
NAU8501YG	5 x 5 mm	32-QFN	Pb-Free

Pin Descriptions

Pin #	Name	Type	Functionality
1	LMICP	Analog Input	Left MICP Input (common mode)
2	LMICN	Analog Input	Left MICN Input
3	LLIN/GPIO2	Analog Input / Digital I/O	Left Line Input / alternate Left MICP Input / GPIO2
4	RMICP	Analog Input	Right MICP Input (common mode)
5	RMICN	Analog Input	Right MICN Input
6	RLIN/GPIO3	Analog Input / Digital I/O	Right Line Input/ alternate Right MICP Input / Digital Output In 4-wire mode: Must be used for GPIO3
7	FS	Digital I/O	Digital Audio DAC and ADC Frame Sync
8	BCLK	Digital I/O	Digital Audio Bit Clock
9	ADCOUT	Digital Output	Digital Audio ADC Data Output
10	n/c		Not internally connected
11	MCLK	Digital Input	Master Clock Input
12	VSSD	Supply	Digital Ground
13	VDDC	Supply	Digital Core Supply
14	VDDB	Supply	Digital Buffer (Input/Output) Supply
15	CSB/GPIO1	Digital I/O	3-Wire MPU Chip Select or General Purpose I/O
16	SCLK	Digital Input	3-Wire MPU Clock Input / 2-Wire MPU Clock Input
17	SDIO	Digital I/O	3-Wire MPU Data Input / 2-Wire MPU Data I/O
18	MODE	Digital Input	Control Interface Mode Selection Pin
19	n/c		Not internally connected
20	n/c		Not internally connected
21	n/c		Not internally connected
22	n/c		Not internally connected
23	n/c		Not internally connected
24	VSSA2	Supply	Secondary analog ground connection for minimum noise
25	n/c		Not internally connected
26	VDDA2	Supply	Secondary analog power connection for minimum noise
27	VREF	Reference	Decoupling for Midrail Reference Voltage
28	VSSA	Supply	Analog Ground
29	RLINOUT	Analog Output	Right Line Level Output
30	LLINOUT	Analog Output	Left Line Level Output
31	VDDA	Supply	Analog Power Supply
32	MICBIAS	Analog Output	Programmable Low Noise Supply for Microphone Biasing

Notes

1. The 32-QFN package includes a bulk ground connection pad on the underside of the chip. This bulk ground should be thermally tied to the PCB as much as possible, and electrically tied to the analog ground (VSSA, pin 28).
2. Unused analog input pins should be left as no-connection.
3. Unused digital input pins should be tied to ground.
4. Pins designated as NC (Not Internally Connected) should be left as no-connection

Block Diagram

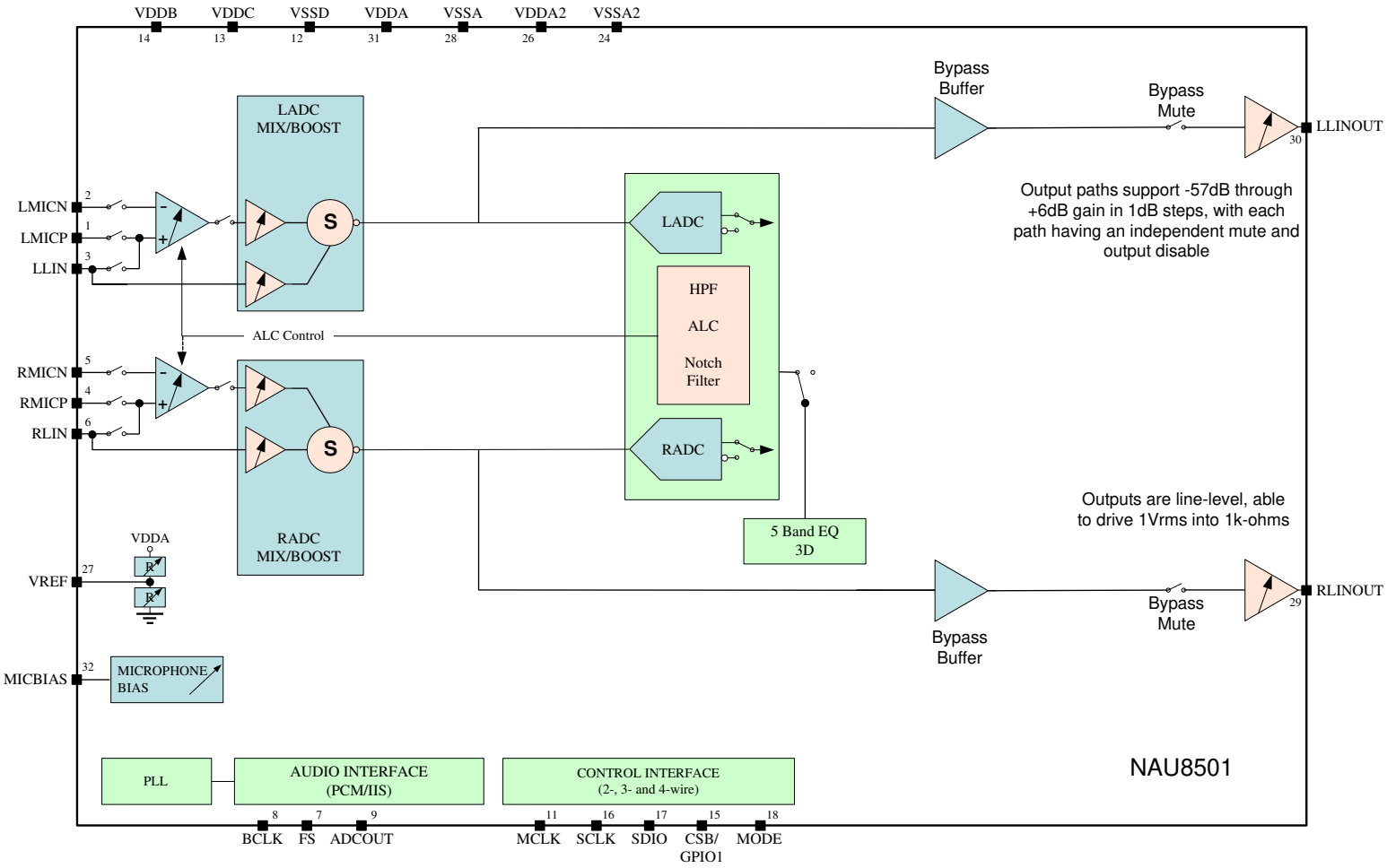


Figure 1: NAU8501 Block Diagram

Electrical Characteristics

Conditions: VDDC = 1.8V, VDDA = VDDB = VDDA2 = 3.3V, MCLK = 12.288MHz, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data, 64X oversampling rate, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Analog to Digital Converter (ADC)						
Full scale input signal [1]	V_{INFS}	PGABST = 0dB PGAGAIN = 0dB		1.0 0		Vrms dBV
Signal-to-noise ratio	SNR	Gain = 0dB, A-weighted	tbd	90		dB
Total harmonic distortion [2]	THD+N	Input = -3dB FS input		-80	tbd	dB
Channel separation		1kHz input signal		103		dB
Microphone Inputs (LMICP, LMICN, RMICP, RMICN, LLIN, RLIN) and Programmable Gain Amplifier (PGA)						
Full scale input signal [1]		PGABST = 0dB PGAGAIN = 0dB		1.0 0		Vrms dBV
Programmable gain			-12		35.25	dB
Programmable gain step size		Guaranteed Monotonic		0.75		dB
Mute Attenuation				120		dB
Input resistance		Inverting Input PGA Gain = 35.25dB PGA Gain = 0dB PGA Gain = -12dB Non-inverting Input Line Inputs Line Path Gain = +6dB Line In Gain = 0dB Line In Gain = -12dB		 1.6 47 75 94 20 40 159		 kΩ kΩ kΩ kΩ kΩ kΩ kΩ
Input capacitance				10		pF
PGA equivalent input noise		0 to 20kHz, Gain set to 35.25dB		120		µV
Input Boost Mixer						
Gain boost		Boost disabled Boost enabled		0 20		dB dB
Line Input to boost/mixer gain			-12		6	dB
Line Input step size to boost/mixer				3		dB
Microphone Bias						
Bias voltage	$V_{MICBIAS}$	See Figure 3	0.50, 0.60,0.65, 0.70, 0.75, 0.85, or 0.90			VDDA VDDA
Bias current source	$I_{MICBIAS}$			3		mA
Output noise voltage	V_n	1kHz to 20kHz		14		nV/√Hz

Electrical Characteristics, cont'd.

Conditions: VDDC = 1.8V, VDDA = VDDB = VDDA2 = 3.3V, MCLK = 12.288MHz, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data, 64X oversampling rate, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Line Output (RLINOUT and LLINOUT with 1k-Ω load)						
0dB full scale output voltage			VDDA / 3.3			V_{rms}
Signal-to-noise ratio	SNR	A-weighted		92		dB
Total harmonic distortion [2]	THD+N	VDDA = 3.3V		85		dB
Channel separation		1kHz signal		99		dB
Power supply rejection ratio (50Hz – 22kHz)	PSRR			53		dB
Automatic Level Control (ALC) and Limiter						
Target record level			-22.5		-1.5	dBFS
Programmable gain			-12		35.25	dB
Gain hold time [3]	t_{HOLD}	Doubles every gain step, with 16 steps total	0 / 2.67 / 5.33 / … / 43691			ms
Gain ramp-up (decay) [3]	t_{DCY}	ALC Mode ALC = 0	4 / 8 / 16 / … / 4096			ms
		Limiter Mode ALC = 1	1 / 2 / 4 / … / 1024			ms
Gain ramp-down (attack) [3]	t_{ATK}	ALC Mode ALC = 0	1 / 2 / 4 / … / 1024			ms
		Limiter Mode ALC = 1	0.25 / 0.5 / 1 / … / 128			ms
Mute Attenuation				120		dB
Digital Input/Output						
Input HIGH level	V_{IL}		0.7 * VDDB			V
Input LOW level	V_{IH}				0.3 * VDDB	V
Output HIGH level	V_{OH}	I_{Load} = 1mA	0.9 * VDDB			V
Output LOW level	V_{OL}	I_{Load} = -1mA			0.1 * VDDB	V
Input capacitance				10		pF

Notes

1. Full Scale is relative to the magnitude of VDDA and can be calculated as FS = VDDA/3.3.
2. Distortion is measured in the standard way as the combined quantity of distortion products plus noise. The signal level for distortion measurements is at 3dB below full scale, unless otherwise noted.
3. Time values scale proportionally with MCLK. Complete descriptions and definitions for these values are contained in the detailed descriptions of the ALC functionality.

Absolute Maximum Ratings

Condition	Min	Max	Units
VDDB, VDDC, VDDA, VDDA2 supply voltages	-0.3	+3.61	V
Core Digital Input Voltage range	VSSD – 0.3	VDDC + 0.30	V
Buffer Digital Input Voltage range	VSSD – 0.3	VDDB + 0.30	V
Analog Input Voltage range	VSSA – 0.3	VDDA + 0.30	V
Industrial operating temperature	-40	+85	°C
Storage temperature range	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Digital supply range (Core)	VDDC	1.65		3.60	V
Digital supply range (Buffer)	VDDB	1.65		3.60	V
Analog supply range	VDDA, VDDA2	2.50		3.60	V
Ground	VSSD VSSA VSSA2		0		V

1. VDDA must be ≥ VDDB.

2. VDDB must be ≥ VDDC.

Table of Contents

1 General Description

The NAU8501 is a stereo device with identical left and right channel differential microphone inputs, and also, line level inputs that share common support elements. Additionally, two line level outputs are included that enable monitoring of the analog signals present at the ADC inputs. A powerful set of integrated programmable signal processing features are included.

1.1.1 Analog Inputs

All inputs include individual muting functions with excellent channel isolation and off-isolation from all outputs. All inputs are suitable for full quality, high bandwidth signals.

Each of the left-right stereo channels includes a low noise programmable differential PGA amplifier. This may be used for a microphone level through line level source signals. Gain may be set from +35.25db through -12dB at the analog difference-amplifier type programmable amplifier input stage. A separate additional 20dB analog gain is available on this input path, between the PGA output and ADC mixer input. The output of the ADC mixer may be routed to the ADC and/or analog bypass to the analog line level output section.

Each channel also has a line level input. This input may be routed to the input PGA non-inverting input, and/or mixed directly to the ADC input mixer. The mixing path into the ADC input mixer includes programmable gain from -12dB through +6dB in 3dB steps.

1.1.2 Analog Outputs

There are two line level analog audio outputs. These outputs are useful for providing “sidetone” in telephony applications, or more generally to monitor the analog input signal that is available at the input of the ADCs. Each output has an independently programmable gain function, output mute function, and output disable function. The gain can be programmed from -57dB through +6dB in 1dB steps.

A programmable low-noise MICBIAS microphone bias supply output is included. The VREF pin voltage reference is buffered and then scaled to provide a wide range of possible low-noise microphone bias DC voltages. This microphone bias supply is suitable for both conventional electret (ECM) type microphones, and to power the newer MEMS all-silicon type microphones. A small internal series resistance is optionally programmable at the output of the device. This greatly increases the effectiveness of the external output filter capacitor in reducing high frequency noise on the microphone bias output, and is a unique feature not present in most audio codec products.

1.1.3 ADC Function and Digital Signal Processing

Each left and right channel has an independent high quality ADC associated with it. These are high performance, 24-bit delta-sigma converters that are suitable for a very wide range of applications.

Each ADC is supported by an analog input mixer to select/mix the inputs available to that ADC. The output of the ADC is supported by an advanced digital signal processing subsystem (DSP) that enables a very wide range of programmable signal conditioning and signal optimizing functions. All digital processing is with 24-bit precision, as to minimize processing artifacts and maximize the audio dynamic range supported by the NAU8501.

The available DSP features include a wide range, mixed-mode Automatic Level Control (ALC), a high pass filter, a notch filter, scaling in decibels, and a digital mute function. All of these features are optional and highly programmable. The high pass filter function includes a very low frequency DC-blocking feature, or optionally, an application mode feature for low frequency audio noise reduction, such as to reduce unwanted ambient noise or "wind noise" on a microphone input. The notch filter may be programmed over a very wide frequency range and notch depth to greatly reduce a specific frequency band or frequency. Typically, this is used to reject a certain frequency such as a 50Hz, 60Hz, or 217Hz unwanted noise, but may also be used to eliminate an unwanted housing resonance or noise such as from camera motors.

Digital signal processing is also provided for a 3D Audio Enhancement function, and for a 5-Band Equalizer. These features are optional, and are programmable over wide ranges.

1.1.4 Digital Interfaces

Command and control of the device is accomplished using a 2-wire/3-wire/4-wire serial control interface. This is a simple, but highly flexible interface that is compatible with many commonly used command and control serial data protocols and host drivers.

Digital audio input/output data streams are transferred to and from the device separately from command and control. The digital audio data interface supports either I2S or PCM audio data protocols, and is compatible with commonly used industry standard devices that follow either of these two serial data formats.

1.1.5 Clock Requirements

The clocking signals required for the audio signal processing, audio data I/O, and control logic may be provided externally, or by optional operation of a built-in PLL (Phase Locked Loop).

The PLL is provided as a low cost, zero external component count optional method to generate required clocks in almost any system. The PLL is a fractional-N divider type design, which enables generating accurate desired audio sample rates derived from a very wide range of commonly available system clocks.

The frequency of the system clock provided as the PLL reference frequency may be any stable frequency in the range between 8MHz and 33MHz. Because the fractional-N multiplication factor is a very high precision 24-bit value, any desired sample rate supported by the NAU8501 can be generated with very high accuracy, typically limited by the accuracy of the external reference frequency. Reference clocks and sample rates outside of these ranges are also possible, but may involve performance tradeoffs and increased design verification.

2 Power Supply

This device has been designed to operate reliably using a wide range of power supply conditions and power-on/power-off sequences. There are no special requirements for the sequence or rate at which the various power supply pins change. Any supply can rise or fall at any time without harm to the device. However, pops and clicks may result from some sequences. Optimum handling of hardware and software power-on and power-off sequencing is described in more detail in the Applications section of this document.

2.1.1 Power-On Reset

The NAU8501 does not have an external reset pin. The device reset function is automatically generated internally when power supplies are too low for reliable operation. The internal reset is generated any time that either VDDA or VDDC is lower than is required for reliable maintenance of internal logic conditions. The reset threshold voltage for VDDA and VDDC is approximately 0.5Vdc. If both VDDA and VDDC are being reduced at the same time, the threshold voltage may be slightly lower. Note that these are much lower voltages than are required for normal operation of the chip. These values are mentioned here as general guidance as to overall system design.

If either VDDA or VDDC is below its respective threshold voltage, an internal reset condition is asserted. During this time, all registers and controls are set to the hardware determined initial conditions. Software access during this time will be ignored, and any expected actions from software activity will be invalid.

When both VDDA and VDDC reach a value above their respective thresholds, an internal reset pulse is generated which extends the reset condition for an additional time. The duration of this extended reset time is approximately 50 microseconds, but not longer than 100 microseconds. The reset condition remains asserted during this time. If either VDDA or VDDC at any time becomes lower than its respective threshold voltage, a new reset condition will result. The reset condition will continue until both VDDA and VDDC again higher than their respective thresholds. After VDDA and VDDC are again both greater than their respective threshold voltage, a new reset pulse will be generated, which again will extend the reset condition for not longer than an additional 100 microseconds.

2.1.2 Power Related Software Considerations

There is no direct way for software to determine that the device is actively held in a reset condition. If there is a possibility that software could be accessing the device sooner than 100 microseconds after the VDDA and VDDC supplies are valid, the reset condition can be determined indirectly. This is accomplished by writing a value to any register other than register 0x00, with that value being different than the power-on reset initial values. The optimum choice of register for this purpose may be dependent on the system design, and it is recommended the system engineer choose the register and register test bit for this purpose. After writing the value, software will then read back the same register. When the register test bit reads back as the new value, instead of the power-on reset initial value, software can reliably determine that the reset condition has ended.

Although it is not required, it is strongly recommended that a Software Reset command should be issued after power-on and after the power-on reset condition is ended. This will help insure reliable operation under every power sequencing condition that could occur.

If there is any possibility that VDDA or VDDC could be unreliable during system operation, software may be designed to monitor whether a power-on reset condition has happened. This can be accomplished by writing a test bit to a register that is different from the power-on initial conditions. This test bit should be a bit that is never used for any other reason, and does not affect desired operation in any way. Then, software at any time can read this bit to determine if a power-on reset condition has occurred. If this bit ever reads back other than the test value, then software can reliably know that a power-on reset event has occurred. Software can subsequently re-initialize the device and the system as required by the system design.

2.1.3 Software Reset

All chip registers can be reset to power-on default conditions by writing any value to register 0, using any of the control modes. Writing valid data to any other register disables the reset, but all registers need to have the

correct operating data written. See the applications section on powering NAU8501 up for information on avoiding pops and clicks after a software reset.

3 Input Path Detailed Descriptions

The NAU8501 provides multiple inputs to acquire and process audio signals from microphones or other sources with high fidelity and flexibility. There are left and right input paths, each with three input pins, which can be used to capture signals from single-ended, differential or dual-differential microphones. These input channels each include a programmable gain amplifier (PGA). The outputs of the PGAs, plus two additional line level inputs, are then connected to the input boost/mix stages for maximum flexibility handling various signal sources.

All inputs are maintained at a DC bias at approximately ½ of the VDDA supply voltage. Connections to these inputs should be AC-coupled by means of DC blocking capacitors suitable for the device application.

3.1 Differential microphone input (MICN & MICP pins)

The NAU8501 features a low-noise, high common mode rejection ratio (CMRR), differential microphone input pair, MICP and MICN, which are connected to a PGA gain stage. The differential input structure is essential in noisy digital systems where amplification of low-amplitude analog signals is necessary such as in portable digital media devices and cell phones. Differential inputs very useful to reduce ground noise in systems in which there are ground voltage differences between different chips and other components. When properly implemented, the differential input architecture offers an improved power-supply rejection ratio (PSRR) and higher ground noise immunity.

3.2 Programmable Gain Amplifier (PGA)

Each PGA supports three possible inputs, MICP, MICN, and LIN. These are the microphone differential pair and a separate line level input. The PGA has a gain range of -12dB through +35.25dB in evenly spaced decibel increments of 0.75dB. Operation of the PGA is subject to control by the following registers:

R2 Power management controls for the left and right PGA
R2 Power management controls for ADC Mix/Boost (must be “on” for any PGA path to function)
R7 Zero crossing timeout control
R32 Automatic Level Control (ALC) for the left and right PGA
R44 Input selection options for the left and right PGA
R45 Volume (gain), mute, update bit, and zero crossing control for the left PGA
R46 Volume (gain), mute, update bit, and zero crossing control for the right PGA

Important: The R45 and R46 update bits are write-only bits. The primary intended purpose of the update bit is to enable simultaneous changes to both the left and right PGA volume values, even though these values must be written sequentially. When there is a write operation to either R45 or R46 volume settings, but the update bit is not set (value = 0), the new volume setting is stored as pending for the future, but does not go into effect. When there is a write operation to either R45 or R46 and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending value in the other PGA volume register is put into effect at the same time.

Note: If the ALC automatic level control is enabled, the function of the ALC is to automatically adjust the R45 or R46 volume setting. If ALC is enabled for the left or right, or both channels, then software should avoid changing the volume setting for the affected channel or channels. The reason for this is to avoid unexpected volume changes caused by competition between the ALC and the direct software control of the volume setting.

Zero-Crossing controls are implemented to suppress clicking sounds that may occur when volume setting changes take place while an audio input signal is active. When the zero crossing function is enabled (logic = 1), any volume change for the affected channel will not take place until the audio input signal passes through the zero point in its peak-to-peak swing. This prevents any instantaneous voltage change to the audio signal caused by volume setting changes. If the zero crossing function is disabled (logic = 0), volume changes take place instantly on condition of the Update Bit, but without regard to the instantaneous voltage level of the affected audio input signal.

The R7 zero crossing timeout control is an additional feature to limit the amount of time that a volume change to the PGA is delayed pending a zero crossing event. If the input signal is such that there are no zero crossing events, and the timeout control is enabled (level = 1), any new volume setting to either PGA will automatically

be put into effect after between 2.5 and 3.5 periods of the Slow Timer Clock (see description under "Miscellaneous Functions").

3.2.1 Zero Crossing Example

This drawing shows in a graphical form the problem and benefits of using the zero crossing feature. There is a major audible improvement as a result of using the zero crossing feature.

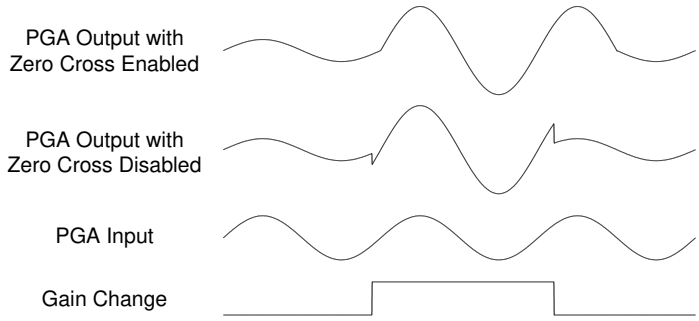


Figure 2: Zero Crossing Gain Update Operation

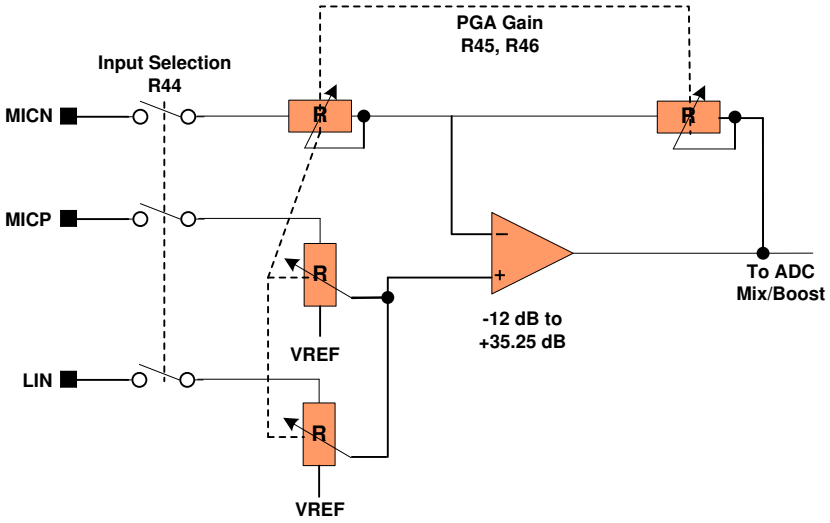


Figure 3: PGA Input Structure Simplified Schematic

3.3 Positive Microphone Input (MICP)

The positive (non-inverting) microphone input (MICP) can be used separately, or as part of a differential input configuration. This input pin connects to the positive (non-inverting) terminal of the PGA amplifier under control of register R44. When the R44 associated control bit is set (logic = 1), a switch connects MICP to the PGA input. When the associated control bit is not set (logic = 0), the MICP pin is connected to a resistor of approximately 30kΩ which is tied to VREF. The purpose of the tie to VREF is to reduce any pop or click sound by keeping the DC level of the MICP pin close to VREF at all times.

Note: If the MICP signal is not used differentially with MICN, the PGA gain values will be valid only if the MICN pin is terminated to a low impedance signal point. This termination should normally be an AC coupled path to signal ground.

This input impedance is constant regardless of the gain value. The nominal input impedance for this input is given by the following table. Impedance for specific gain values not listed in this table can be estimated through interpolation between listed values.

Nominal Input Impedance	Gain (dB)	Impedance (kΩ)
LMICP & RMICP to non-inverting PGA input or LLIN & RLIN to non-inverting PGA input	-12	94
	-9	94
	-6	94
	-3	94
	0	94
	3	94
	6	94
	9	94
	12	94
	18	94
	30	94
	35.25	94

Table 1: Microphone and Line Non-Inverting Input Impedances

3.4 Negative Microphone Input (MICN)

The negative (inverting) microphone input (MICN) can be used separately, or as part of a differential input configuration. This input pin connects to the negative (inverting) terminal of the PGA amplifier under control of register R44. When the R44 associated control bit is set (logic = 1), a switch connects MICP to the PGA input. When the associated control bit is not set (logic = 0), the MICN pin is connected to a resistor of approximately 30kΩ which is tied to VREF. The purpose of the tie to VREF is to reduce any pop or click sound by keeping the DC level of the MICN pin close to VREF at all times.

It is important for a system designer to know that the MICN input impedance varies as a function of the selected PGA gain. This is normal and expected for a difference amplifier type topology. The nominal resistive impedance values for this input over the possible gain range are given by the following table. Impedance for specific gain values not listed in this table can be estimated through interpolation between listed values.

Nominal Input Impedance	Gain (dB)	Impedance (kΩ)
LMICN or RMICN to inverting PGA input	-12	75
	-9	69
	-6	63
	-3	55
	0	47
	3	39
	6	31
	9	25
	12	19
	18	11
	30	2.9
	35.25	1.6

Table 2: Microphone Inverting Input Impedances

System designers should also note that at the highest gain values, the input impedance is relatively low. For most inputs, the best strategy if higher gain values are needed is to use the input PGA in combination with the +20dB gain boost available on the PGA Mix/Boost stage that immediately follows the PGA output. A good

guideline is to use the PGA gain for up to around 20dB of gain. If more gain than this is required and the lower input impedance of the PGA at high gains is a problem, a combination of the PGA and boost stage should be used. In this type of combined gain configuration, it is preferred to have at least 6dB gain at the PGA input stage to benefit from the PGA low noise characteristics.

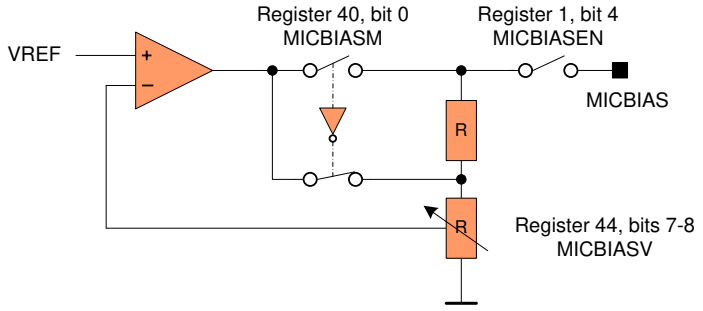
3.5 Microphone biasing

The MICBIAS pin provides a low-noise microphone DC bias voltage as may be required for operation of an external microphone. This built-in feature can typically provide up to 3mA of microphone bias current. This DC bias voltage is suitable for powering either traditional ECM (electret) type microphones, or for MEMS types microphones with an independent power supply pin.

Seven different bias voltages are available for optimum system performance, depending on the specific application. The microphone bias pin normally requires an external filtering capacitor as shown on the schematic in the Application section. The microphone bias function is controlled by the following registers:

R1 Power control for MICBIAS feature (enabled when bit 4 = 1)
R40 Optional low-noise mode and different bias voltage levels (enabled when bit 0 = 1)
R44 Primary MICBIAS voltage selection

The low-noise feature results in greatly reduced noise in the external MICBIAS voltage by placing a resistor of approximately 200-ohms in series with the output pin. This creates a low pass filter in conjunction with the external micbias filter capacitor, but without any additional external components. The low noise feature is enabled when the mode control bit 0 in register R40 is set (level = 1)



Register 44, Bits 7-8	Register 40, Bit 0	Microphone Bias Voltage
00	0	0.90 * VDDA
01	0	0.65 * VDDA
10	0	0.75 * VDDA
11	0	0.50 * VDDA
00	1	0.85 * VDDA
01	1	0.60 * VDDA
10	1	0.70 * VDDA
11	1	0.50 * VDDA

Figure 4: Microphone Bias Generator

3.6 Line Input Impedance and Variable Gain Stage Topology

Except for the input PGAs, other variable gain stages are implemented similarly to the simplified schematic shown here. The gain value changes affect input impedance in the ranges detailed in the description of each type of input path. If a path is in the “not selected” condition, then the input impedance will be in a high impedance condition. If an external input pin is not used anywhere in the system, it will be coupled to a DC tie-off of approximately 30kΩ coupled to VREF. The unused input/output tie-off function is explained in more detail in the Application Information section of this document.

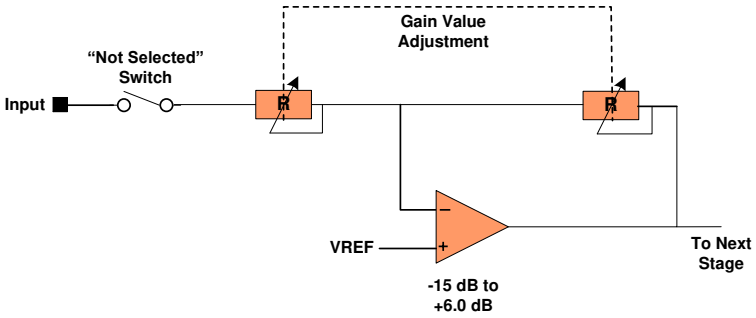


Figure 4: Variable Gain Stage Simplified Schematic

The input impedance presented to these inputs depends on the input routing choices and gain values. If an input is routed to more than one internal input node, then the effective input impedance will be the parallel combination of the impedance of the multiple nodes that are used. The impedance looking into the PGA non-inverting input is constant as listed in the section discussing the microphone input PGAs. The nominal resistive input impedances looking into the ADC Mix/Boost input inputs are listed in the following table:

Inputs	Gain (dB)	Impedance (kΩ)
LLIN & RLIN to L/RADC MIX/BOOST amp	Not Selected	High-Z
	-12	159
	-9	113
	-6	80
	-3	57
	0	40
	3	28
	6	20

Table 3: MIX/BOOST Amp Impedances

3.7 Left and Right Line Inputs (LLIN and RLIN)

A third possible input to the left or right PGA is an optional associated LIN left or right line level input. These inputs may be routed to the PGA non-inverting input, and/or connect directly to the ADC Mixer/Boost stage. If routed to the PGA, this signal is processed as an alternate pin for the MICP signal. LIN may be received differentially in relation to the MICN pin and has available the same gain range as for MICP. As in the operational case of using the MICP input, the MICN input must have a low impedance path to signal ground, so that the gain values chosen in the PGA are valid.

Note: It not recommended that both the LIN line input path to the PGA and the MICP path to the PGA be enabled at the same time. This will cause the differential gain to be unbalanced, and result in poor common mode rejection. Also, this will result in the LIN and MICP signals being connected together through internal chip resistors.

The line input pins, may alternatively be configured to operate as a GPIO (General Purpose Input/Output) logic input pin. This intended purpose is static logic voltage level sensing to determine if a headset is present or not as part of a physical detection of a possible external headset. Only one GPIO pin at any one time can be assigned for this purpose.

Registers that affect operation of the LLIN and RLIN inputs are:

R2 ADC Mix/Boost power control (must be “on” for any LIN path to function)
R9 GPIO selection for headset detect function
R44 PGA input selection control bits
If selected, all other PGA control registers (see PGA description)
R47 Left line input ADC Mix/Boost volume and mute (bits 4, 5, and 6)
R48 Right line input ADC Mix/Boost volume and mute (bits 4, 5, and 6)

3.8 ADC Mix/Boost Stage

The left and right channels each have an independent ADC Mix/Boost stage. The analog input signals must pass through the ADC Mix/Boost stage before use anywhere else in this device.

The ADC mixer stage has the LIN input and PGA output as its two inputs. The PGA input is an internal connection to the associated programmable gain amplifier servicing the microphone and line inputs.

Each input to the ADC Mix/Boost stage can be independently muted, and both inputs have independent gain controls. The LIN inputs have an available gain range of -12dB through +6dB in 3dB steps. The PGA input path has a choice of 0dB or 20dB of gain in addition to the gain in the PGA.

Registers that affect the ADC Mix/Boot stage are:

R2 Power control for left and right channels
R45 mute function for left channel PGA (bit 6 = 0 = muted condition)
R46 mute function for right channel PGA (bit 6 = 0 = muted condition)
R47 gain and mute control for left channel LIN path
R48 gain and mute control for right channel LIN path

3.9 Input Limiter / Automatic Level Control (ALC)

The input section of the NAU8501 is supported by additional combined digital and analog functionality which implement an Automatic Level Control (ALC) function. This can be very useful to automatically manage the analog input gain to optimize the signal level at the output of the programmable amplifier. The ALC can automatically amplify input signals that are too small, or decrease the amplitude if the signals are too loud. This system also helps to prevent clipping (overdrive) at the input of the ADC while maximizing the full dynamic range of the ADC.

The ALC may be operated in the normal mode just described, on in a special limiter mode of operation. The limiter mode is a faster mode of operation, the primary purpose of which is to limit too-loud signals. The limiter mode of operation is described after this section which provides details on the normal mode of operation.

The functional block architecture for the ALC is shown below. The ALC monitors the output of the ADC, measured after the digital decimator. The ADC output is fed into a peak detector, which updates the measured peak value whenever the absolute value of the input signal is higher than the current measured peak. The measured peak gradually decays to zero unless a new peak is detected, allowing for an accurate measurement of the signal envelope. The peak value is used by a logic algorithm to determine whether the PGA input gain should be increased, decreased, or remain the same.

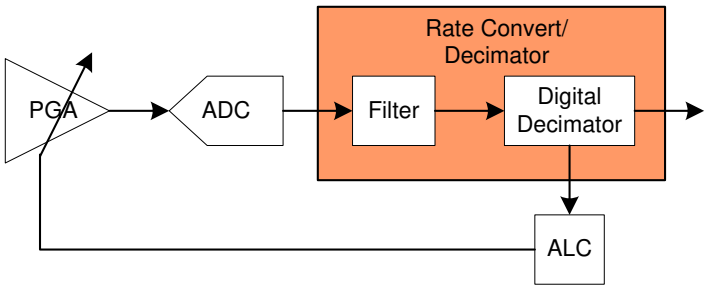


Figure 5: ALC Block Diagram

3.9.1 Normal Mode Example Operation

Immediately following is a simple example of the ALC operation. In the steady state at the beginning of the example time sequence, the PGA gain is at a steady value which results in the desired output level from the ADC. When the input signal suddenly becomes louder, the ALC reduces volume at a register determined rate and step size. This continues until the output level of the ADC is again at the desired target level. When the input signal suddenly becomes quiet, the ALC increases volume at a register determined rate and step size. When the output level from the ADC again reaches the target level, and now the input remains at a constant level, the ALC remains in a steady state.

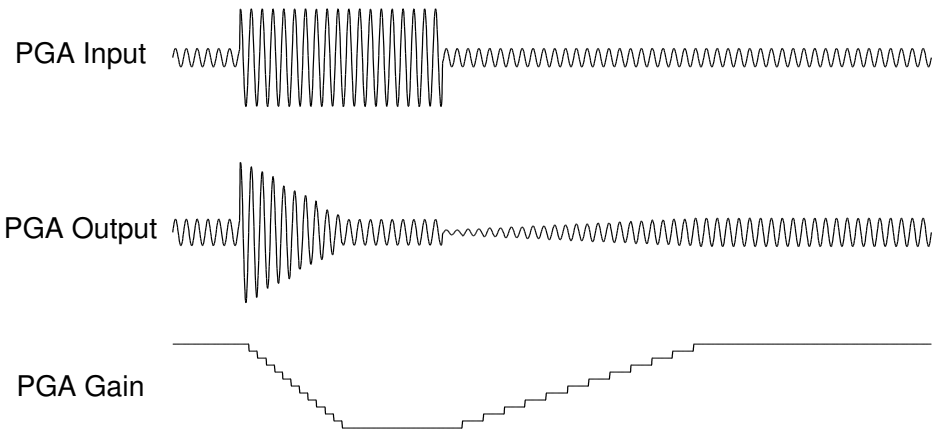


Figure 6: ALC Normal Mode Operation

3.9.2 ALC Parameter Definitions

Automatic level and volume control features are complex and have difficult to understand traditional names for many features and controls. This section defines some terms so that the explanations of this subsystem are more clear.

ALC Maximum Gain: Register 32 (ALCMXGAIN) This sets the maximum allowed gain in the PGA during normal mode ALC operation. In the Limiter mode of ALC operation, the ALCMXGAIN value is not used. In the Limiter mode, the maximum gain allowed for the PGA is set equal to the pre-existing PGA gain value that was in effect at the moment in time that the Limiter mode is enabled.

ALC Minimum Gain: Register 32 (ALCMNGAIN) This sets the minimum allowed gain in the PGA during all modes of ALC operation. This is useful to keep the AGC operating range close to the desired range for a given application scenario.

ALC Target Value: Register 33 (ALCSL) Determines the value used by the ALC logic decisions comparing this fixed value with the output of the ADC. This value is expressed as a fraction of Full Scale (FS) output from the ADC. Depending on the logic conditions, the output value used in the comparison may be either the instantaneous value of the ADC, or otherwise a time weighted average of the ADC peak output level.

ALC Attack Time: Register 34 (ALCATK) Attack time refers to how quickly a system responds to an increasing volume level that is greater than some defined threshold. Typically, attack time is much faster than decay time. In the NAU8501, when the absolute value of the ADC output exceeds the ALC Target Value, the PGA gain will be reduced at a step size and rate determined by this parameter. When the peak ADC output is at least 1.5dB lower than the ALC Target Value, the stepped gain reduction will halt.

ALC Decay Time: Register 34 (ALCDCY) Decay time refers to how quickly a system responds to a decreasing volume level. Typically, decay time is much slower than attack time. When the ADC output level is below the ALC Target value by at least 1.5dB, the PGA gain will increase at a rate determined by this parameter. The decay time constant is determined by the setting in register 34, bits 4 to 7 (ALCDCY), which sets the delay between increases in gain. In Limiter mode, the time constants are faster than in ALC mode. (See Detailed Register Map.)

ALC Hold Time Register 33 (ALCHLD) Hold time refers to a duration of time when no action is taken. This is typically to avoid undesirable sounds that can happen when an ALC responds too quickly to a changing input signal. The use and amount of hold time is very application specific. In the NAU8501, the hold time value is the duration of time that the ADC output peak value must be less than the target value before there is an actual gain increase.

3.10 ALC Peak Limiter Function

To reduce clipping and other bad audio effects, all ALC modes include a peak limiter function. This implements an emergency PGA gain reduction when the ADC output level exceeds a built-in maximum value. When the ADC output exceeds 87.5% of full scale, the ALC block ramps down the PGA gain at the maximum ALC Attack Time rate, regardless of the mode and attack rate settings, until the ADC output level has been reduced below the emergency limit threshold. This limits ADC clipping if there is a sudden increase in the input signal level.

3.10.1 ALC Normal Mode Example Using ALC Hold Time Feature

Input signals with different characteristics (e.g., voice vs. music) may require different settings for this parameter for optimum performance. Increasing the ALC hold time prevents the ALC from reacting too quickly to brief periods of silence such as those that may appear in music recordings; having a shorter hold time, may be useful in voice applications where a faster reaction time helps to adjust the volume setting for speakers with different volumes. The waveform below shows the operation of the ALCHLD parameter.

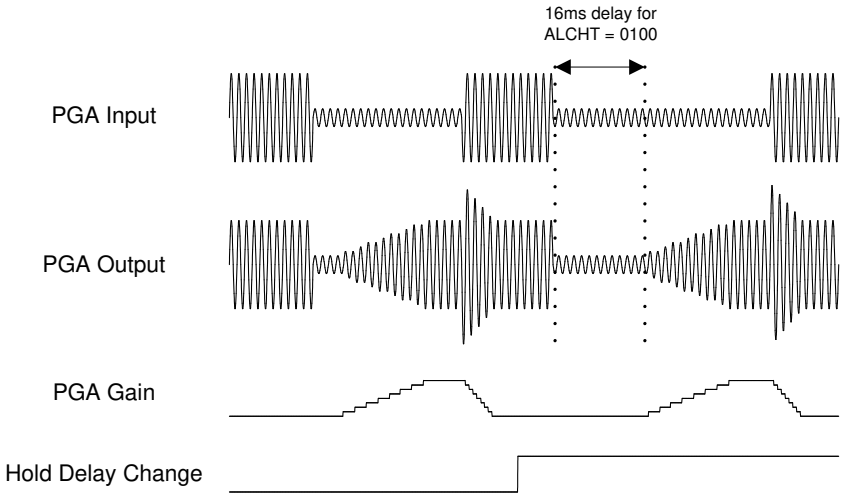


Figure 7: ALC Hold Delay Change

3.11 Noise Gate (Normal Mode Only)

A noise gate threshold prevents ALC amplification of noise when there is no input signal, or no signal above an expected background noise level. The noise gate is enabled by setting register 35, bit 3 (NGEN), HIGH, and the threshold level is set in register 35, bits 0 to 2 (NGTH). This does not remove noise from the signal; when there is no signal or a very quiet signal (pause) composed mostly of noise, the ALC holds the gain constant instead of amplifying the signal towards the target threshold. The NAU8501 accomplishes this by comparing the input signal level against the noise gate threshold. The noise gate only operates in conjunction with the ALC and only in Normal mode. The noise gate is asserted when:

Equation 1: (Signal at ADC – PGA gain – MIC Boost gain) < NGTH (Noise Gate Threshold Level)

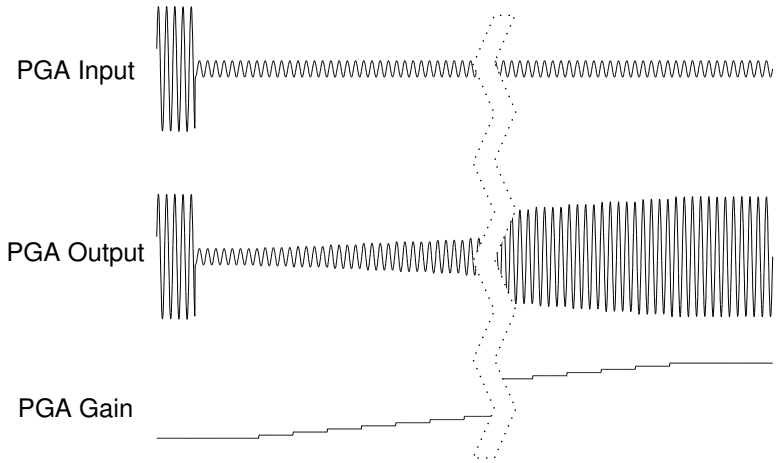


Figure 8: ALC Operation Without Noise Gate

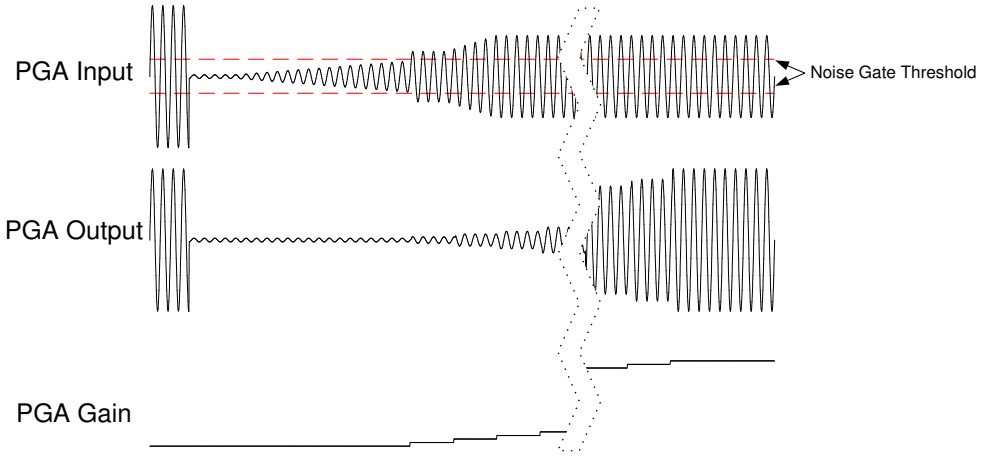
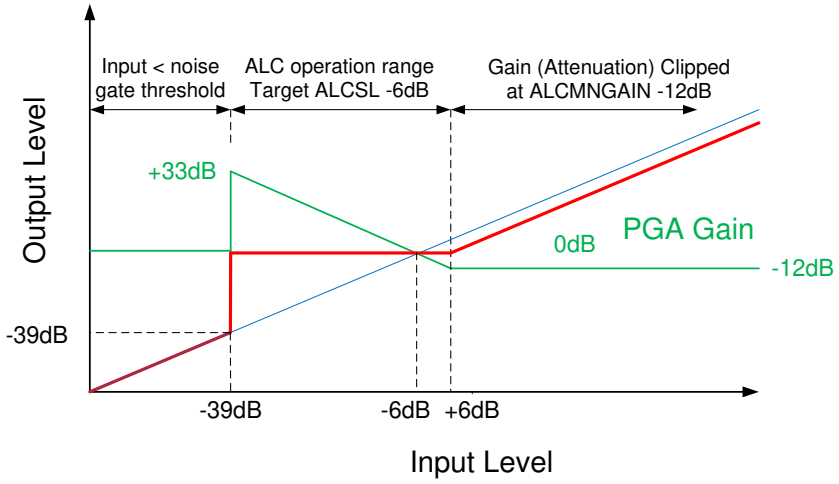


Figure 9: Noise Gate Operation

3.12 ALC Example with ALC Min/Max Limits and Noise Gate Operation

The drawing below shows the effects of ALC operation over the full scale signal range. The drawing is color coded to be more clear as follows:

Blue Original Input signal (linear line from zero to maximum)
Green PGA gain value over time (inverse to signal in target range)
Red Output signal (held to a constant value in target range)



Register	Bits	Name	Value	Description
32	7-8	ALCSEL	11	ALC enabled both channels
32	3-5	ALCMAXGAIN	111	Max ALC gain @ 35.25dB
32	0-2	ALCMINGAIN	000	Min ALC gain @ -12dB
33	0-3	ALCLVL	1011	Target ALC gain @ -6dBFS
35	3	NGEN	1	Noise gate enabled
35	0-2	NGTH	000	Noise gate @ -39dB

Figure 10: ALC Response Envelope

3.12.1 ALC Register Map Overview

ALC can be enabled for either or both the left and right ADC channels. All ALC functions and mode settings are common to the left and right channels. When either the right or left PGA is disabled, the respective PGA will remain at the most recent gain value as set by the ALC. Registers that control the ALC features and functions are:

R32 Enable left/right ALC functions; set maximum gain, minimum gain
R33 ALC hold time, ALC target signal level
R34 ALC limiter mode selection, attack parameters, decay parameters
R35 Enable noise gate, noise gate parameters
R70 Selection of signal level averaging options and ALC table options
R70 Realtime readout of left channel gain value in use by ALC (same as left in stereo operation)
R71 Realtime readout of right channel gain value in use by ALC (same as right in stereo operation)
R76 Realtime readout of input signal level from averaging peak-to-peak input signal detector
R77 Realtime readout of input signal level from averaging input signal peak detector

The following table shows some of the ALC parameter values and their ranges. The complete list of settings and values is included in the Detailed Register Map.

Parameter	Register	Bits	Name	Default Setting	Value	Programmable Range
Minimum Gain of PGA	32	0-2	ALCMINGAIN	000	-12dB	Range: -12dB to +30dB @ 6dB increments
Maximum Gain of PGA	32	3-5	ALCMAXGAIN	111	35.25dB	Range: -6.75dB to +35.25dB @ 6dB increments
ALC Function	32	7-8	ALCEN	00	Disabled	00 = Disable 01 = Enable right channel 10 = Enable left channel 11 = Enable both channels
ALC Target Level	33	0-3	ALCLVL	1011	-6dBFS	Range: -22.5dB to -1.5dBFS @ 1.5dB increments
ALC Hold Time	33	4-7	ALCHLD	0000	0ms	Range: 0ms to 1024ms at 1010 and above (times are for 0.75dB steps, and double with every step)
ALC Attack time	34	0-3	ALCATK	0010	500µs	ALCM=0 – Range: 125µs to 128ms ALCM=1 – Range: 31µs to 32ms (times are for 0.75dB steps, and double with every step)
ALC Decay Time	34	4-7	ALCDCY	0011	4ms	ALCM = 0 – Range: 500µs to 512ms ALCM = 1 – Range: 125µs to 128ms (times are for 0.75dB steps, and double with every step)
Limiter Function	34	8	ALCMODE	0	Disabled	0 = ALC mode 1 = Limiter mode

Table 4: Registers associated with ALC and Limiter Control

3.13 Limiter Mode

When register 34, bit 8, is HIGH and ALC is enabled in register 32, bits 7-8 (ALCEN), the ALC block operates in limiter mode. In this mode, the PGA gain is constrained to be less than or equal to the PGA gain setting when the limiter mode is enabled. In addition, attack and decay times are faster in limiter mode than in normal mode as indicated by the different lookup tables for these parameters for limiter mode. The following waveform illustrates the behavior of the ALC in limiter mode in response to changes in various ALC parameters.

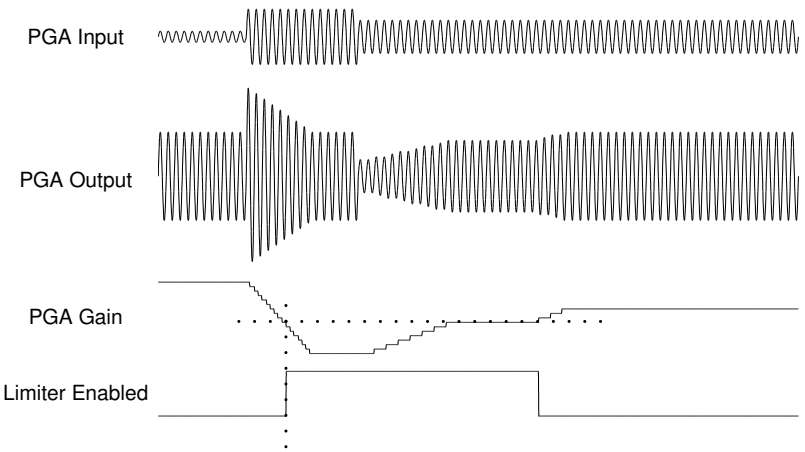


Figure 11: ALC Limiter Mode Operation