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Mono Audio Codec with SPI

emPowerAudio™

1. GENERAL DESCRIPTION

The NAU8811 is a cost effective and low power wideband MONO audio CODEC. It is designed for voice telephony related applications. Functions include Automatic Level Control (ALC) with noise gate, PGA, standard audio interface I^2S, and PCM with time slot assignment. The device provides one differential microphone input and one single ended auxiliary input (multi purpose). There are few variable gain control stages in the audio path. It also includes Headphone (Headphone) line output and integrated BTL speaker driver.

The analog inputs have PGA on the front end, allowing dynamic range optimization with a wide range of input sources. The microphone amplifiers have a programmable gain from -12dB to +35.25dB to handle both amplified microphones. In addition to a digital high pass filter to remove DC offset voltages, the ADC also features voice band digital filtering. Voice-band data is accepted by the audio interface (I^2S). The DAC converter path includes filtering and mixing, programmable-gain amplifiers (PGA), and soft muting. The digital interface SPI have independent supply voltage to allow integration into multiple supply systems. The NAU8811 operates at supply voltages from 2.5V to 3.6V, although the digital core can operate at voltage as low as 1.71V to save power.

The NAU8811 is specified for operation from -40°C to +85°C. AEC-Q100 & TS16949 compliant device is available upon request.

2. FEATURES

24-bit signal processing linear Audio CODEC
- Audio DAC: 93dB SNR and -84dB THD
- Audio ADC: 91dB SNR and -79dB THD
- Support variable sample rates from 8 - 48kHz
- Integrated BTL Speaker Driver 1W (8Ω / 5V)
- Integrated Headset Driver 40mW (16Ω / 3.3V)

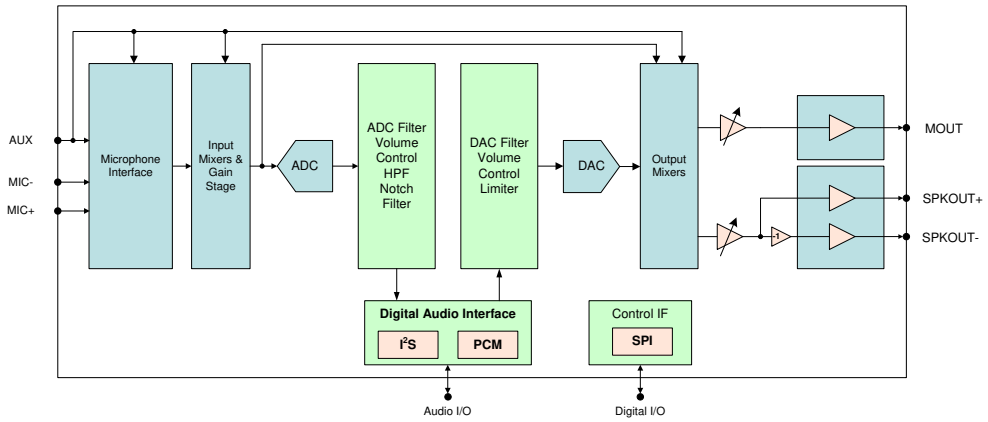
Analog I/O
- Integrated programmable Microphone Amplifier
- Integrated Line Input and Line Output
- Integrated Audio Switches
- Headphone / Speaker / Line Output selection
- Microphone / Line Inputs selection

Interfaces
- I^2S digital interface PCM time slot assignment
- SPI serial control Interface

Low Power, Low Voltage
- Analog Supply: 2.5V to 3.6V
- Digital Supply: 1.71V to 3.6V
- Nominal Operating Voltage: 3.3V

Additional features
- Programmable ALC and ADC Notch Filter
- Programmable High Pass Filter
- Digital D/A Passthrough
- AEC-Q100 & TS16949 compliant device available upon request
- Industrial temperature: range: –40°C to +85°C

Applications
- VoIP Telephones
- IP PBX
- Mobile Telephone Hands-free Kits
- Residential & Consumer Intercoms
- General Purpose low power audio CODEC



3. PIN CONFIGURATION

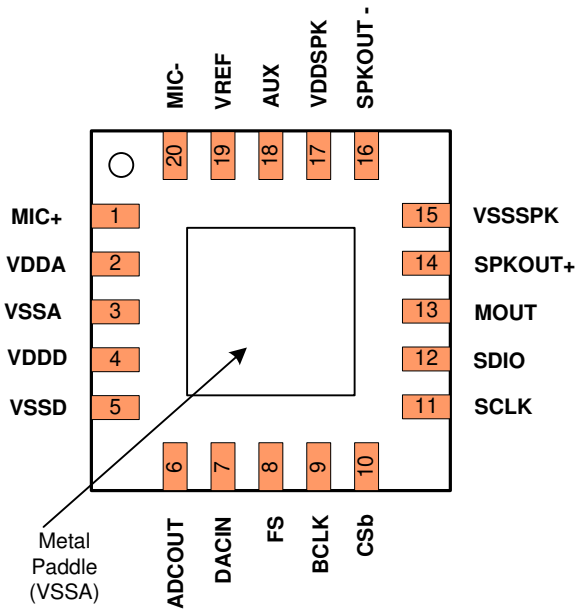


Figure 1: 20-Pin QFN Package

4. PIN DESCRIPTION

Pin Name	Pin#	Functionality	A/D	Pin Type
MIC+	1	Microphone Positive Input	A	I
VDDA	2	Analog Supply	A	I
VSSA	3	Analog Ground	A	O
VDDD	4	Digital Supply	D	I
VSSD	5	Digital Ground	D	O
ADCOUT	6	Digital Audio Data Output	D	O
DACIN	7	Digital Audio Data Input	D	I
FS	8	Frame Sync (Slave)	D	I/O
BCLK	9	Bit Clock (Slave)	D	I
CSb	10	SPI Chip Select	D	I/O
SCLK	11	SPI Serial Clock	D	I
SDIO	12	SPI Data In	D	O
MOUT	13	Headphone Output	A	O
SPKOUT+	14	Speaker Positive Output	A	O
VSSSPK	15	Speaker Ground	A	O
SPKOUT-	16	Speaker Negative Output	A	O
VDDSPK	17	Speaker Supply	A	I
AUX	18	Auxiliary Input	A	I
VREF	19	Decoupling internal analog mid supply reference voltage	A	O
MIC-	20	Microphone Negative Input	A	I
PADDLE_VSSA	PKG	The exposed metal paddle on the bottom of the IC supplies circuit ground(s) for the entire chip. It is very important that a good solder connection is made between this exposed metal paddle and the ground plane of the PCB underlying the IC.	A	O

Table 1: Pin Description

Notes

1. The 20-QFN package includes a bulk ground connection pad on the underside of the chip. This bulk ground should be thermally tied to the PCB, and electrically tied to the analog ground.
2. Unused analog input pins should be left as no-connection.
3. Under all condition when digital pins are not used they should be tied to ground.

5. BLOCK DIAGRAM

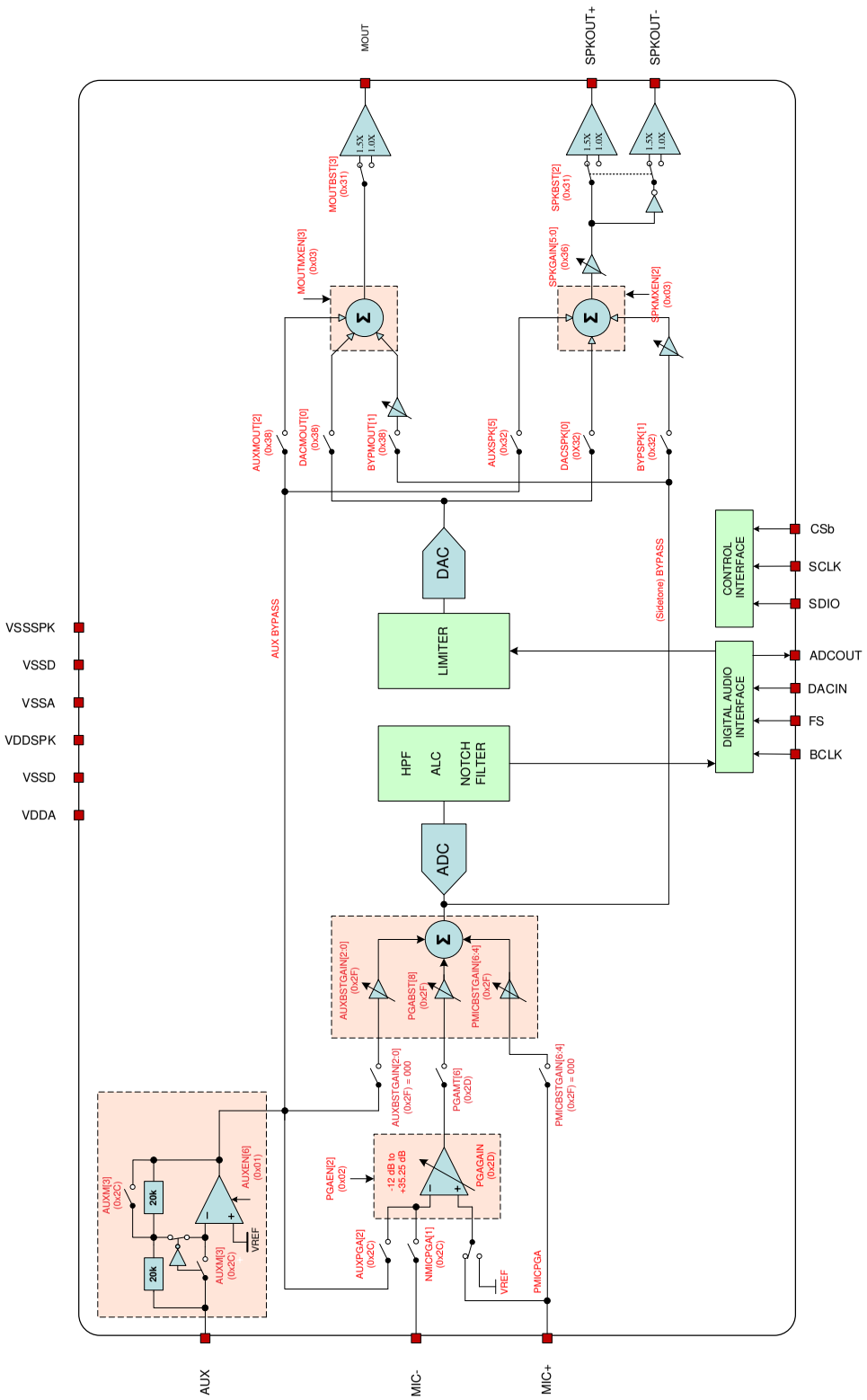


Figure 2: NAU8811 General Block Diagram

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7. List of Figures

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9. ABSOLUTE MAXIMUM RATINGS

CONDITION		MIN	MAX	Units
VDDA supply voltage		-0.3	+3.63	V
VDDSPK supply voltage	MOUTBST=0, SPKBST=0	-0.3	+3.63	V
	MOUTBST=1, SPKBST=1	-0.3	+5.50	V
Digital Input Voltage range		VSSD – 0.3	VDDD + 0.30	V
Analog Input Voltage range		VSSA – 0.3	VDDA + 0.30	V
Industrial operating temperature		-40	+85	^{0}C
Storage temperature range		-65	+150	^{0}C

CAUTION: Do not operate at or near the maximum ratings listed for extended period of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty. These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

10. OPERATING CONDITIONS

Condition	Symbol	Min Value	Typical Value	Max Value	Units
Analogue supplies range	VDDA	2.50		3.60	V
Digital supply range	VDDD	1.71		3.60	V
Speaker supply	VDDSPK	2.50		5.50	V
Ground	VSSD, VSSA, VSSSPK		0		V

1. VDDA must be ≥ VDDD

11. ELECTRICAL CHARACTERISTICS

VDDD = 1.8V, VDDA = VDDSPK = 3.3V (VDDSPK = 1.5*VDDA when Boost), T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue to Digital Converter (ADC)						
Full scale input signal [1]	V_{INFS}	PGABST = 0dB PGAGAIN = 0dB		1.0 0		V_{RMS} dBV
Signal to Noise Ratio [2]	SNR	Gain = 0dB, A-weighted	87	91		dB
Total Harmonic Distortion [3]	THD	Input = -1dBFS, Gain = 0dB		-79	-65	dB
Digital to Analogue Converter (DAC) to Headphone output (all data measured with 10kΩ / 50pF load)						
Full Scale output signal [1]		MOUTBST=0		1.0x (V_{REF})		V_{RMS}
		MOUTBST=1		1.5 x V_{REF}		
Signal to Noise Ratio [2]	SNR	A-weighted (ADC/DAC oversampling rate of 128)	90	93		dB
Total Harmonic Distortion [3]	THD	R_L = 10 kΩ; -1.5dBfs		-84	-70	dB
Auxiliary Analogue Input (AUX)						
Full-scale Input Signal Level [1]	V_{INFS}	Gain = 0dB		1 0		V_{RMS} dBV
Input Resistance	R_{AUX}	AUXM=0		20		kΩ
Input Capacitance	C_{AUX}			10		pF
Microphone Inputs (MICN & MICP) and MIC Input Programmable Gain Amplifier (PGA)						
Full-scale Input Signal Level [1]	V_{INFS}	PGABST = 0dB PGAGAIN = 0dB		1 0		V_{RMS} dBV
Programmable PGA gain			-12		35.25	dB
PGA Step Size		Guaranteed Monotonic		0.75		dB
Programmable Boost PGA gain		PGABST = 0		0		dB
		PGABST = 1		20		
Mute Attenuation				100		dB
PGA equivalent output noise		0 to 20kHz, Gain set to 35.25dB		110		µV
Auxiliary Input resistance	R_{AUX}	PGA Gain = 35.25dB		1.6		kΩ
		PGA Gain = 0dB		47		kΩ
		PGA Gain = -12dB		75		kΩ
Positive Microphone Input resistance	R_{MIC+}	PMICPGA = 1		94		kΩ
Input Capacitance	C_{MIC}			10		pF
Speaker Output PGA						
Programmable Gain			-57		6	dB
Programmable Gain Step Size		Guaranteed Monotonic		1		dB

VDDD = 1.8V, VDDA = VDDSPK = 3.3V (VDDSPK = 1.5*VDDA when Boost), T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS			MIN	TYP	MAX	UNIT
BTL Speaker Output (SPKOUT+, SPKOUT- with 8Ω bridge tied load)								
Full scale output [7]		SPKBST = 0 VDDSPK = VDDA				VDDA / 3.3		V_{RMS}
		SPKBST = 1 VDDSPK = 1.5 * VDDA				(VDDA / 3.3) * 1.5		
Output Power	PO	Output power is very closely correlated with THD						
Signal to Noise Ratio	SNR	VDDSPK=3.3V RL = 8Ω				90		dB
		VDDSPK =1.5*VDDA RL = 8Ω				90		dB
Total Harmonic Distortion	THD	PO =180mW	RL = 8Ω	VDDSPK=3.3V		-63		dB
		PO =400mW				-56		dB
		PO =360mW		VDDSPK = 1.5*VDDA		-60		dB
		PO =800mW				-61		dB
		PO =1W				-34		dB
Power Supply Rejection Ratio (50Hz - 22kHz)	PSRR	VDDSPK = 1.5*VDDA (boost)				50		dB
		VDDSPK = 3V (non-boost)				50		dB
Headphone' output (SPKOUTP, SPKOUTN with resistive load to ground)								
Full scale output [7]						VDDA / 3.3		V_{RMS}
Signal to Noise Ratio	SNR	A-weighted				90		dB
Total Harmonic Distortion	THD	Po=20mW, RL = 16Ω, VDDSPK = 3.3V				-84		dB
		Po=20mW, RL = 32Ω, VDDSPK = 3.3V				-85		dB
Automatic Level Control (ALC)/Limiter – ADC only								
Target Record Level					-28.5		-6	dB
Programmable Gain					-12		35.25	dB
Programmable Gain Step Size		Guaranteed Monotonic				0.75		dB
Gain Hold Time [4, 6]	tHOLD	BCLK=12.288MHz			0 / 2.67 / …/ 43691 (time doubles with each step)			ms
Gain Ramp-Up (Decay) Time [5, 6]	tDCY	ALC Mode ALCM=0 BCLK=12.288MHz			3.3 / 6.6 / 13.1 / … / 3360 (time doubles every step)			ms
		Limiter Mode ALCM=1 BCLK=12.288MHz			0.73 / 1.45 / 2.91 / … / 744 (time doubles every step)			ms
Gain Ramp-Down (Attack) Time [5, 6]	tATK	ALC Mode ALCM=0 BCLK=12.288MHz			0.83 / 1.66 / 3.33 / … / 852 (time doubles every step)			ms
		Limiter Mode ALCM=1 BCLK=12.288MHz			0.18 / 0.36 / 0.73 / … / 186 (time doubles every step)			ms
Digital Input / Output								

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input HIGH Level	V_{IH}		0.7 × VDDD			V
Input LOW Level	V_{IL}				0.3 × VDDD	V
Output HIGH Level	V_{OH}	I_{OL} = 1mA	0.9 × VDDD			V
Output LOW Level	V_{OL}	I_{OH} = -1mA			0.1 x VDDD	V

Notes

1. Full Scale is relative to VDDA (FS = VDDA/3.3.) Input level to RIP and LIP is limited to a maximum of -3dB so that THD+N performance will not be reduced.
2. Signal-to-noise ratio (dB) – SNR is a measure of the difference in level between the full-scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
3. THD+N (dB) – THD+N are a ratio, of the RMS values, of (Noise + Distortion)/Signal.
4. Hold Time is the length of time between a signal detected being too quiet and beginning to ramp up the gain. It does not apply to ramping down the gain when the signal is too loud, which happens without a delay.
5. Ramp-up and Ramp-Down times are defined as the time it takes to change the PGA gain by 6dB of its gain range.
6. All hold, ramp-up and ramp-down times scale proportionally with BCLK
7. The maximum output voltage can be limited by the speaker power supply. If MOUTBST or SPKBST is set then VDDSPK should be 1.5xVDDA to prevent clipping taking place in the output stage (when PGA gains are set to 0dB).

12. FUNCTIONAL DESCRIPTION

The NAU8811 is a MONO Audio CODEC with very robust ADC and DAC. The device provides one single ended auxiliary input (AUX pin) and one differential microphone input (MIC- & MIC+ pins). The auxiliary input (AUX) can be configured to sum multiple signals into a single input. It has three different amplification paths with a total gain of up to +55.25dB. The differential input also has amplification paths similar to auxiliary input.

The PGA output has programmable ADC gain. An advanced Sigma Delta DAC is used along with digital decimation and interpolation filters to give high quality audio at sample rates from 8 kHz to 48 kHz. The Digital Filter blocks include ADC high pass filters, and Notch filter. The device has two output mixers, one for Headphone output and the other for the speaker output. It also has one input mixer.

The NAU8811 has serial control interface SPI for device control. The device also supports I^2S, PCM time slotting, Left Justified and Right Justified for audio interface and can only operate in slave only. It can operate with sample rates ranging from 8 kHz to 48 kHz, depending on the values of BCLK and its prescaler. The power control registers help save power by controlling the major individual functional blocks of the NAU8811.

12.1. INPUT PATH

The NAU8811 has two different types of microphone inputs single ended and differential. Figure 3 shows the different paths that the input signals can take.

All inputs are maintained at a DC bias at approximately half of the VDDA supply voltage. Connections to these inputs should be AC-coupled by means of DC blocking capacitors suitable for the device application.

12.1.1. The Single Ended Auxiliary Input (AUX)

The single ended auxiliary input (AUX) has three different paths to Headphone output (MOUT).

- Directly connected to the Headphone Mixer or Speaker Mixer to MOUT or SPKOUT+ and SPKOUT- respectively
- Connect through the PGA Boost Mixer which has a range of -12dB to +6dB
- Connect through both the input PGA Gain (range of -12dB to +35.25 dB) and PGA Boost Mixer (range of 0db or +20dB)

The last two paths above go through the ADC filters where the ALC loop controls the amplitude of the input signal. The device also has an internal configurable biasing circuit for biasing the microphone, reducing external components.

An internal inverting operational amplifier circuit allows the auxiliary input pin to connect multiple signals for mixing. This can be achieved by setting AUXM[3] address (0x2C) to LOW. The combination of the 20k ohm resistors can vary due to process variation in the gain stage. The block can also be configured to be used as a buffer by

setting AUXM[3] address (0x2C) to HIGH. The internal inverting circuit block can be enable/disable by setting AUXEN[6] address (0x01).

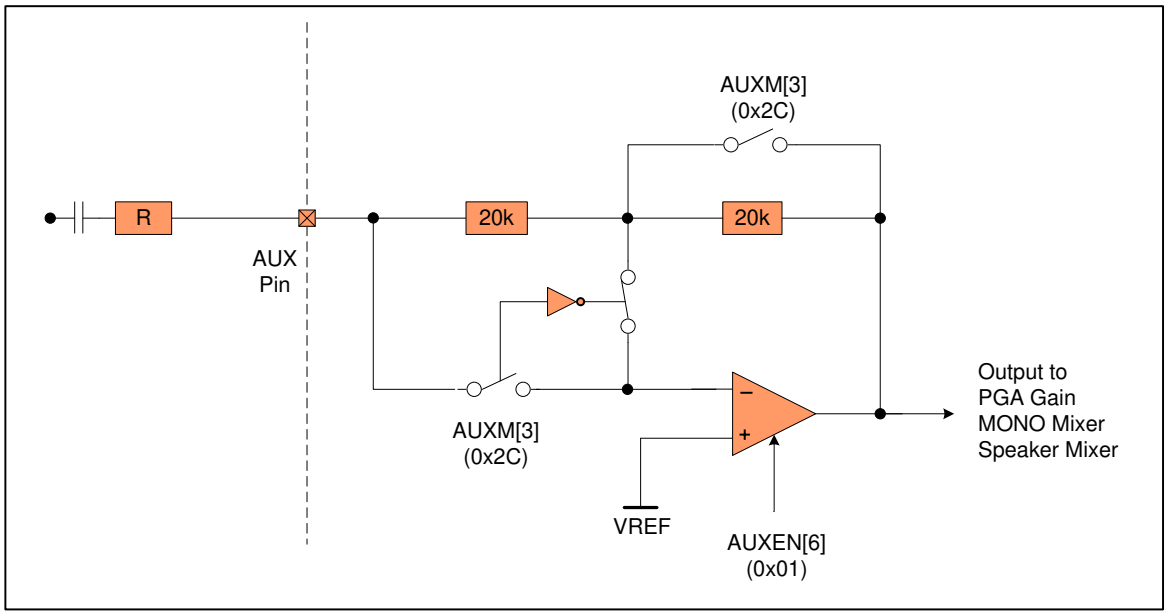

Figure 3: Auxiliary Input Circuit Block Diagram with AUXM[3] = 0

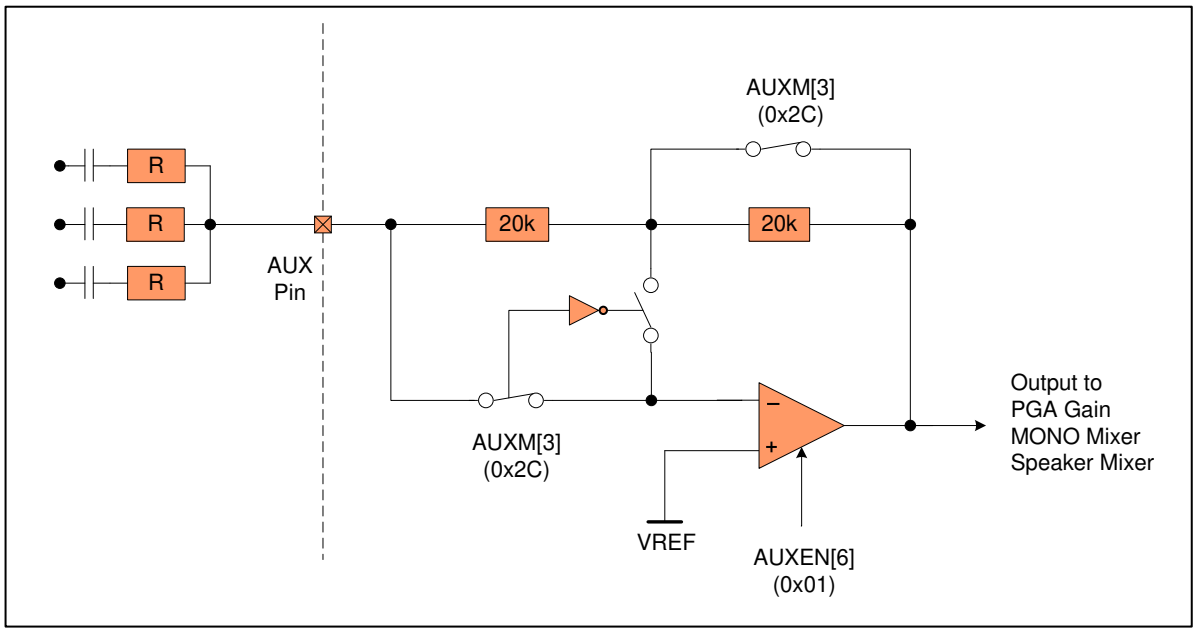

Figure 4: Auxiliary Input Circuit Block Diagram with AUXM[3] = 1

12.1.2. The differential microphone input (MIC- & MIC+ pins)

The NAU8811 features a low-noise, high common mode rejection ratio (CMRR), differential microphone inputs (MIC- & MIC+ pins) which are connected to a PGA Gain stage. The differential input structure is essential in noisy digital systems where amplification of low-amplitude analog signals is necessary such as notebooks and PDAs. When properly employed, the differential input architecture offers an improved power-supply rejection ratio (PSRR) and higher ground noise immunity.

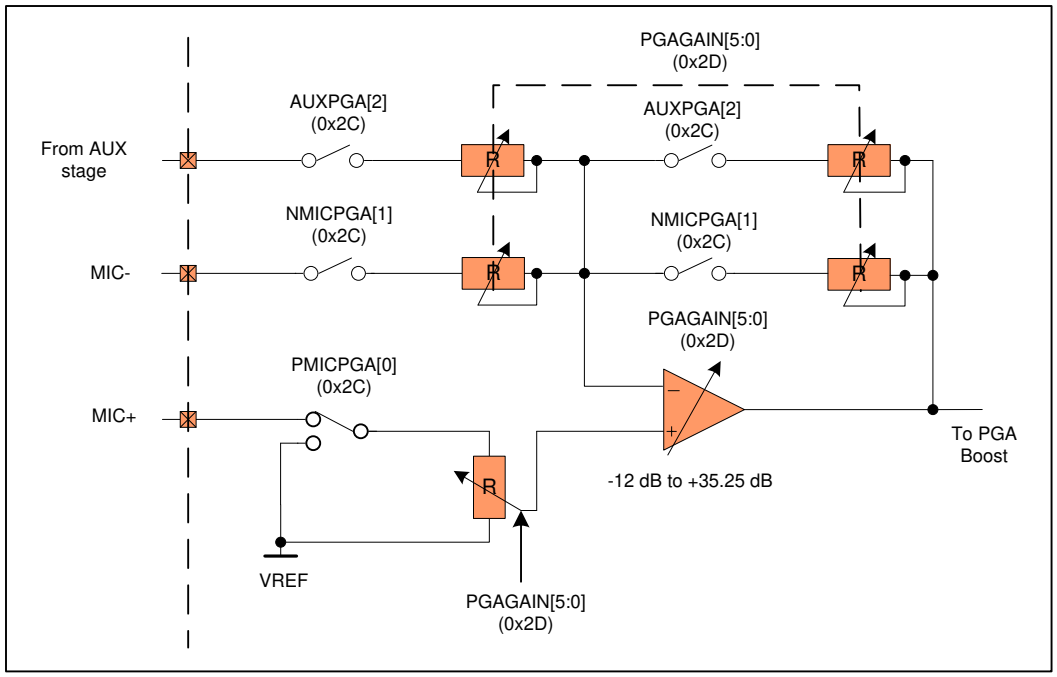

Figure 5: Input PGA Circuit Block Diagram

Bit(s)	Addr	Parameter	Programmable Range
PMICPGA[0]	0x2C	Positive Microphone to PGA	0 = Input PGA Positive terminal to VREF 1 = Input PGA Positive terminal to MICP
NMICPGA[1]	0x2C	Negative Microphone to PGA	0 = MICN not connected to input PGA 1 = MICN to input PGA Negative terminal.

Table 2: Register associated with Input PGA Control

12.1.2.1. Positive Microphone Input (MIC+)

The positive microphone input (MIC+) can be used as part of the differential input. It connects to the positive terminal of the PGA gain amplifier by setting PMICPGA[0] address (0x2C) to HIGH or can be connected to VREF by setting PMICPGA[0] address (0x2C) to LOW.

When the associated control bit is set logic = 1, the MIC+ pin is connected to a resistor of approximately 30kΩ which is tied to VREF. The purpose of the tie to VREF is to reduce any pop or click sound by keeping the DC level of the MIC+ pin close to VREF at all times.

Note: In single ended applications where the MIC+ input is used without using MIC-, the PGA gain values will be valid only if the MIC- pin is terminated to a low impedance signal point. This termination should normally be an AC coupled path to signal ground. This input impedance is constant regardless of the gain value. The following table gives the nominal input impedance for this input. Impedance for specific gain values not listed in this table can be estimated through interpolation between listed values.

MIC+ to non-inverting PGA input **Nominal Input Impedance**	
Gain (dB)	**Impedance (kΩ)**
-12	94
-9	94
-6	94
-3	94
0	94
3	94
6	94
9	94
12	94
18	94
30	94
35.25	94

Table 3: Microphone Non-Inverting Input Impedances

MIC- to inverting PGA input **Nominal Input Impedance**	
Gain (dB)	**Impedance (kΩ)**
-12	75
-9	69
-6	63
-3	55
0	47
3	39
6	31
9	25
12	19
18	11
30	2.9
35.25	1.6

Table 4: Microphone Inverting Input Impedances

12.1.2.2. Negative Microphone Input (MIC-)

The negative microphone input (MIC-) has two distinctive configuration; differential input or single ended input. This input connects to the negative terminal of the PGA gain amplifier by setting NMICPGA[1] address (0x2C) to HIGH. When the MIC- is used as a single ended input, MIC+ should be conned to VREF by setting PMICPGA[0] address (0x2C) bit to LOW. The AUX input signal can also be mixed with the MIC- input signal by setting AUXPGA[2] address (0x2C) to HIGH.

When the associated control bit is set logic = 1, the MIC- pin is connected to a resistor of approximately 30kΩ which is tied to VREF. The purpose of the tie to VREF is to reduce any pop or click sound by keeping the DC

level of the MIC- pin close to VREF at all times. It is important for a system designer to know that the MIC-input impedance varies as a function of the selected PGA gain. This is normal and expected for a difference amplifier type topology. The above table gives the nominal resistive impedance values for this input over the possible gain range. Impedance for specific gain values not listed in this table can be estimated through interpolation between listed values.

12.1.2.3. PGA Gain Control

The PGA amplification is common to all three input pins MIC-, MIC+, AUX, and enabled by PGAEN[2] address (0x02). It has a range of -12dB to +35.25dB in 0.75dB steps, controlled by PGAGAIN[5:0] address (0x2D). Input PGA gain will not be used when ALC is enabled using ALCEN[8] address (0x20).

Addr	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x2D	0	PGAZC	PGAMT	PGAGAIN[5:0]						0x010
0x20	ALCEN	0	0	ALCMXGAIN[2:0]			ALCMNGAIN[2:0]			0x038

Table 5: Registers associated with ALC and Input PGA Gain Control

12.1.3. PGA Boost Stage

The boost stage has three inputs connected to the PGA Boost Mixer. All three inputs can be individually connected or disconnected from the PGA Boost Mixer. The boost stage can be enabled by setting BSTEN[4] address (0x02) to HIGH. The following figure shows the PGA Boost stage.

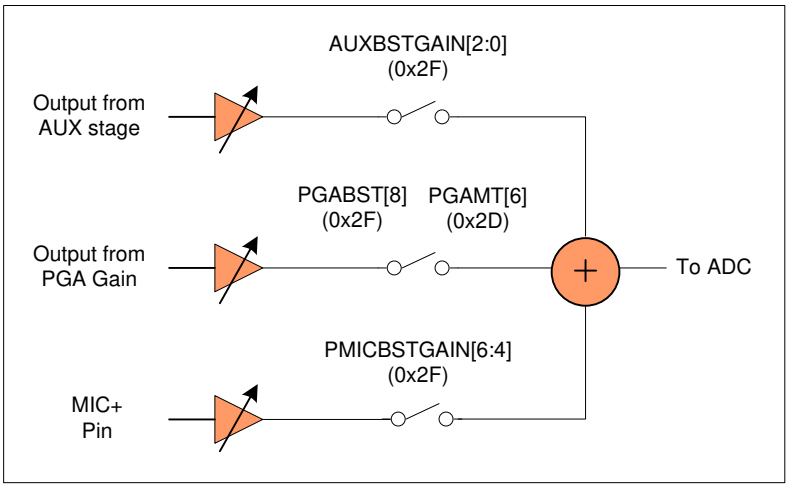

Figure 6: Boost Stage Block Diagram

The signal from AUX stage can be amplified at the PGA Boost stage before connecting to the Boost Mixer by setting a binary value from "001" – "111" to AUXBSTGAIN[2:0] address (0x2F). The path is disconnected by setting "000" to the AUXBSTGAIN bits.

Signal from PGA stage to the PGA Boost Mixer is disconnected or muted by setting PGAMT[6] address (0x2D) to HIGH. In this path the PGA boost can be a fixed value of +20dB or 0dB, controlled by the PGABST[8] address (0x2F) bit.

The signal from MIC+ pin to the PGA Boost Mixer is disconnected by setting '000' binary value to PMICBSTGAIN[6:4] address (0x2F) and any other combination connects the path.

Bit(s)	Addr	Parameter	Programmable Range
BSTEN[4]	0x02	Enable PGA Boost Block	0 = Boost stage OFF 1 = Boost stage ON
PGAMT[6]	0x2D	Mute control for input PGA	0=Input PGA not muted 1=Input PGA muted
AUXBSTGAIN[2:0]	0x2F	Boost AUX signal	Range: -12dB to +6dB @ 3dB increment
PMICBSTGAIN[6:4]	0x2F	Boost MIC+ signal	Range: -12dB to +6dB @ 3dB increment
PGABST[8]	0x2F	Boost PGA stage	0 = PGA output has +0dB 1 = PGA output has +20dB

Table 6: Registers associated with PGA Boost Stage Control

12.2. ADC DIGITAL FILTER BLOCK

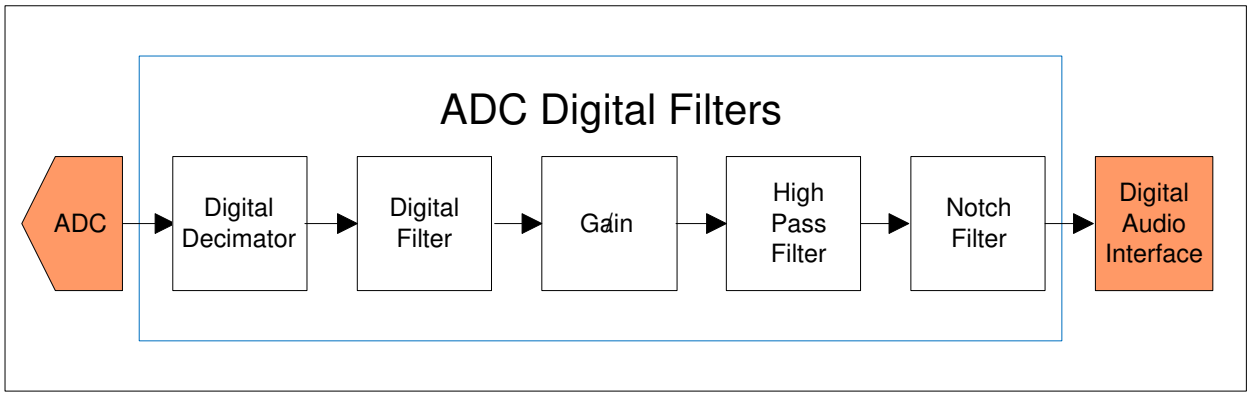

Figure 7: ADC Digital Filter Path Block Diagram

The ADC digital filter block performs a 24-bit signal processing. The block consists of an oversampled analog sigma-delta modulator, digital decimator, digital filter, high pass filter, and a notch filter. The oversampled analog sigma-delta modulator provides a bit stream to the decimation stages and filter. The ADC coding scheme is in twos-complement format and the full-scale input level is proportional to VDDA. With a 3.3V supply voltage, the full-scale level is $1.0V_{RMS}$ and any voltage greater than full scale may overload the ADC and cause distortion. The ADC is enabled by setting ADCEN[0] address (0x02) bit. Polarity and oversampling rate of the ADC output signal can be changed by ADCPL[0] address (0x0E) and ADCOS[3] address (0x0E) respectively.

Bit(s)	Addr	Parameter	Programmable Range
ADCPL[0]	0x0E	ADC Polarity	0 = Normal 1 = Inverted
ADCOS[3]	0x0E	ADC Over SampleRate	0=64x (Lowest power) 1=128x (best SNR at typical condition)
HPFEN[8]	0x0E	High Pass Filter Enable	0 = Disable 1 = Enable
HPFAM[7]	0x0E	Audio or Application Mode	0 = Audio (1^{st} order, fc ~ 3.7 Hz) 1 = Application (2^{nd} order, fc = HPF)
HPF[6:4]	0x0E	High Pass Filter frequencies	82 Hz to 612 Hz dependant on the sample rate
ADCEN[0]	0x02	Enable ADC	0 = Disable 1 = Enable
SMPLR[3:1]	0x07	Sample rate	8k Hz to 48 kHz

Table 7: Register associated with ADC

12.2.1. Programmable High Pass Filter (HPF)

The high pass filter (HPF) has two different modes that it can operate in either Audio or Application mode HPFAM[7] address (0x0E). In Audio Mode (HPFAM=0) the filter is first order, with a cut-off frequency of 3.7 Hz. In Application mode (HPFAM=1) the filter is second order, with a cut-off frequency selectable via the HPF[2:0] register bits. Cut-off frequency of the HPF depends on sample frequency selected by SMPLR[3:1] address (0x07). The HPF is enabled by setting HPFEN[8] address (0x0E) to HIGH. Table below shows the cut-off frequencies with different sampling rate.

HPF[2:0]	fs (kHz)								
	SMPLR=101/100			SMPLR=011/010			SMPLR=001/000		
	8	11.025	12	16	22.05	24	32	44.1	48
000	82	113	122	82	113	122	82	113	122
001	102	141	153	102	141	153	102	141	153
010	131	180	156	131	180	156	131	180	156
011	163	225	245	163	225	245	163	225	245
100	204	281	306	204	281	306	204	281	306
101	261	360	392	261	360	392	261	360	392
110	327	450	490	327	450	490	327	450	490
111	408	563	612	408	563	612	408	563	612

Table 8: High Pass Filter Cut-off Frequencies (HPFAM=1)

12.2.2. Programmable Notch Filter (NF)

The NAU8811 has a programmable notch filter where it passes all frequencies except those in a stop band centered on a given center frequency. The filter gives lower distortion and flattens response. The notch filter is enabled by setting NFCEN[7] address (0x1B) to HIGH. The variable center frequency is programmed by setting two's complement values to NFCA0[6:0] address (0x1C), NFCA0[13:7] address (0x1B) and NFCA1[6:0] address (0x1E), NFCA1[13:7] address (0x1D) registers. The coefficients are updated in the circuit when the NFCU[8] bit is set HIGH in a write to any of the registers NF1-NF4 address (0x1B, 0x1C, 0x1D, 0x1E).

Addr	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x1B	NFCU	NFCEN	NFCA0[13:7]							0x000
0x1C	NFCU	0	NFCA0[6:0]							0x000
0x1D	NFCU	0	NFCA1[13:7]							0x000
0x1E	NFCU	0	NFCA1[6:0]							0x000

Table 9: Registers associated with Notch Filter Function

	A_0	A_1	Notation	Register Value (DEC)
Coefficient	$\frac{1-\tan\left(\frac{2\ \pi\ f_b}{2\ f_s}\right)}{1+\tan\left(\frac{2\ \pi\ f_b}{2\ f_s}\right)}$	$-\left(1+A_0\right)\ x\ \cos\left(\frac{2\ \pi\ f_c}{f_s}\right)$	f_c = center frequency (Hz) f_b = -3dB bandwidth (Hz) fs = sample frequency (Hz)	NFCA0 = $-A_0 \times 2^{13}$ NFCA1 = $-A_1 \times 2^{12}$ (then convert to 2's complement)

Table 10: Equations to Calculate Notch Filter Coefficients

12.2.3. Digital ADC Gain Control

The digital ADC can be muted by setting "0000 0000" to ADCGAIN[7:0] address (0x0F). Any other combination digitally attenuates the ADC output signal in the range -127dB to 0dB in 0.5dB increments].

Addr	Name	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x0F	**ADCG**	0	ADCGAIN								**0x0FF**

Table 11: Register associated with ADC Gain

12.3. PROGRAMMABLE GAIN AMPLIFIER (PGA)

NAU8811 has a programmable gain amplifier (PGA) which controls the gain such that the signal level of the PGA remains substantially constant as the input signal level varies within a specified dynamic range. The PGA has two functions

- Automatic level control (ALC) or
- Input peak limiter

The Automatic Level Control (ALC) seeks to control the PGA gain in response to the amplitude of the input signal such that the PGA output maintains a constant envelope. A digital peak detector monitors the input signal amplitude and compares it to a register defined threshold level ALCSL[3:0] address (0x21). Note: When the ALC automatic level control is enabled, the function of the ALC is to automatically adjust PGAGAIN[5:0] address (0x2D) volume setting.

12.3.1. Automatic level control (ALC)

The ALC seeks to control the PGA gain such that the PGA output maintains a constant envelope. This helps to prevent clipping at the input of the sigma delta ADC while maximizing the full dynamic range of the ADC. The ALC monitors the output of the ADC, measured after the digital decimator has converted it to 1.23 fixed-point formats. The ADC output is fed into a peak detector, which updates the measured peak value whenever the absolute value of the input signal is higher than the current measured peak. The measured peak gradually decays to zero unless a new peak is detected, allowing for an accurate measurement of the signal envelope.

Based on a comparison between the measured peak value and the target value, the ALC block adjusts the gain control, which is fed back to the PGA.

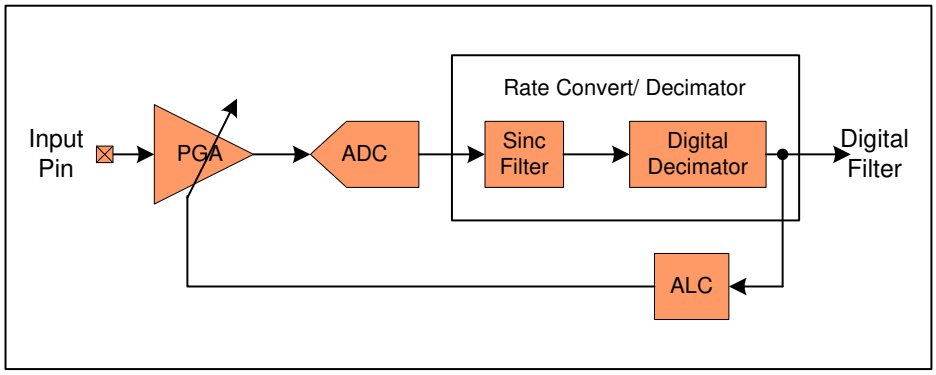

Figure 8: ALC Block Diagram

The ALC is enabled by setting ALCEN[8] address (0x20) bit to HIGH. The ALC has two functional modes, which is set by ALCM[8] address (0x22).

- Normal mode (ALCM = LOW)
- Peak Limiter mode (ALCM = HIGH)

When the ALC is disabled, the input PGA will immediately change to the value stored in PGAGAIN [5:0] address (0x2D). If it is desired that the PGA Gain match the last controlled value of the ALC, it is necessary to read the ALC gain in-use and explicitly write this gain into PGAGAIN [5:0] immediately before disabling the ALC. A digital peak detector monitors the input signal amplitude and compares it to a register defined threshold level ALCSL[3:0] address (0x21).

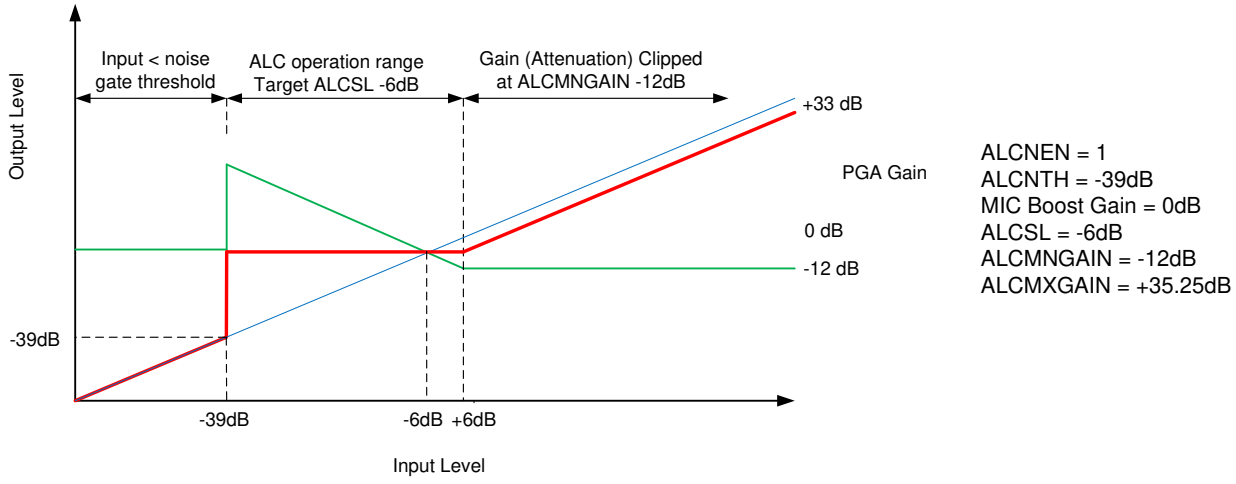

Figure 9: ALC Response Graph

The registers listed in the following section allow configuration of ALC operation with respect to:

- ALC target level
- Gain increment and decrement rates
- Minimum and maximum PGA gain values for ALC operating range
- Hold time before gain increments in response to input signal
- Inhibition of gain increment during noise inputs
- Limiter mode operation

Bit(s)	Addr	Parameter	Programmable Range
ALCMNGAIN[2:0]	0x20	Minimum Gain of PGA	Range: -12dB to +30dB @ 6dB increment
ALCMXGAIN[2:0]		Maximum Gain of PGA	Range: -6.75dB to +35.25dB @ 6dB increment
ALCEN[8]		Enable ALC function	0 = Disable 1 = Enable
ALCSL[3:0]	0x21	ALC Target	Range: -28.5dB to -6dB @ 1.5dB increment
ALCHT[3:0]		ALC Hold Time	Range: 0ms to 1s, time doubles with every step)
ALCZC[8]		ALC Zero Crossing	0 = Disable 1 = Enable
ALCATK[3:0]	0x22	ALC Attack time	ALCM=0 – Range: 125us to 128ms ALCM=1 – Range: 31us to 32ms (time doubles with every step)
ALCDCY[3:0]		ALC Decay time	ALCM=0 – Range: 500us to 512ms ALCM=1 – Range: 125us to 128ms (Both ALC time doubles with every step)
ALCM[8]		ALC Select	0 = ALC mode 1 = Limiter mode

Table 12: Registers associated with ALC Control

The operating range of the ALC is set by ALCMXGAIN[5:3] address (0x20) and ALCMNGAIN[2:0] address (0x20) bits such that the PGA gain generated by the ALC is between the programmed minimum and maximum levels. When the ALC is enabled, the PGA gain is disabled.

In Normal mode, the ALCMXGAIN bits set the maximum level for the PGA in the ALC mode but in the Limiter mode ALCMXGAIN has no effect because the maximum level is set by the initial PGA gain setting upon enabling of the ALC.

ALCMAXGAIN	Maximum Gain (dB)
111	35.25
110	29.25
ALC Max Gain Range 35.25dB to -6dB @ 6dB increments	
001	-0.75
000	-6.75

ALCMINGAIN	Minimum Gain (dB)
000	-12
001	-6
ALC Min Gain Range -12dB to 30dB @ 6dB increments	
110	24
111	30

Table 13: ALC Maximum and Minimum Gain Values