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Mono Audio Codec with Speaker Driver and Equalizer

emPowerAudio™

1. GENERAL DESCRIPTION

NAU8814 is a cost effective and low power wideband MONO audio CODEC. It is designed for voice telephony related applications. Functions include 5-band Graphic Equalizer, Automatic Level Control (ALC) with noise gate, PGA, standard audio interface I2S, PCM with time slot assignment, and on-chip PLL. The device provides one differential microphone input and one single ended auxiliary input (multi purpose). There are few variable gain control stages in the audio path. It also includes MONO line output and integrated BTL speaker driver.

The analog inputs have PGA on the front end, allowing dynamic range optimization with a wide range of input sources. The microphone amplifiers have a programmable gain from -12dB to +35.25dB to handle both amplified microphones. In addition to a digital high pass filter to remove DC offset voltages, the ADC also features voice band digital filtering. Voice band data is accepted by the audio interface (I2S). The DAC converter path includes filtering and mixing, programmable-gain amplifiers (PGA), and soft muting. The digital interfaces, 2-Wire or SPI, have independent supply voltage to allow integration into multiple supply systems. NAU8814 operates at supply voltages from 2.5V to 3.6V, although the digital core can operate at voltage as low as 1.71V to save power.

The NAU8814 is specified for operation from -40°C to +85°C, and is available with automotive AEC-Q100 qualification upon request. Please refer to ordering information for AEC-Q100 compliance part number.

2. FEATURES

24-bit signal processing linear Audio CODEC
- Audio DAC: 93dB SNR and -84dB THD
- Audio ADC: 91dB SNR and -79dB THD
- Support variable sample rates from 2.5 - 48kHz
- Integrated BTL Speaker Driver 1 W (8Ω / 5V)
- Integrated Headset Driver 40mW (16Ω / 3.3V)

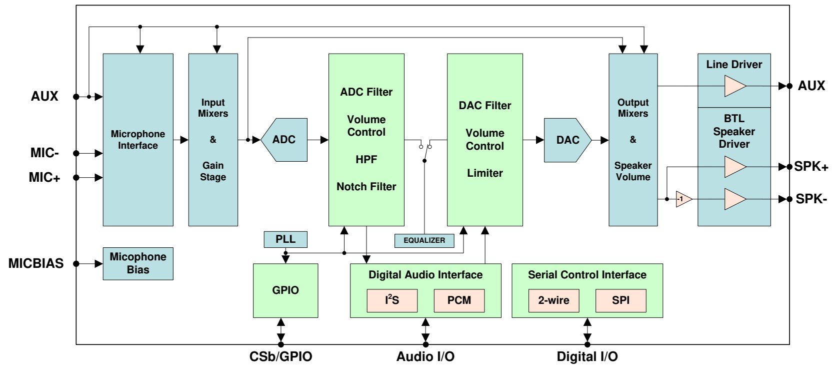
Analog I/O
- Integrated programmable Microphone Amplifier
- Integrated Line Input and Line Output
- Earphone / Speaker / Line Output selection
- Microphone / Line Inputs selection
- Low Noise bias supplied for microphone
- On-chip PLL

Interfaces
- I^2S digital interface PCM time slot assignment
- SPI & 2-Wire serial control Interface (I^2C style; /Write capable)

Low Power, Low Voltage
- Analog Supply: 2.5V to 3.6V
- Digital Supply: 1.71V to 3.6V
- Nominal Operating Voltage: 3.3V

Additional features
- 5-band Graphic Equalizer
- Programmable ALC
- ADC Notch Filter
- Programmable High Pass Filter
- Digital A/D-D/A Passthrough
- AEC-Q100 & TS16949 compliant device available upon request
- Industrial temperature: range: –40°C to +85°C

Applications
- VoIP Telephones]
- Conference speaker-phone
- IP PBX
- Mobile Telephone Hands-free Kits
- Residential & Consumer Intercoms



3. PIN CONFIGURATION

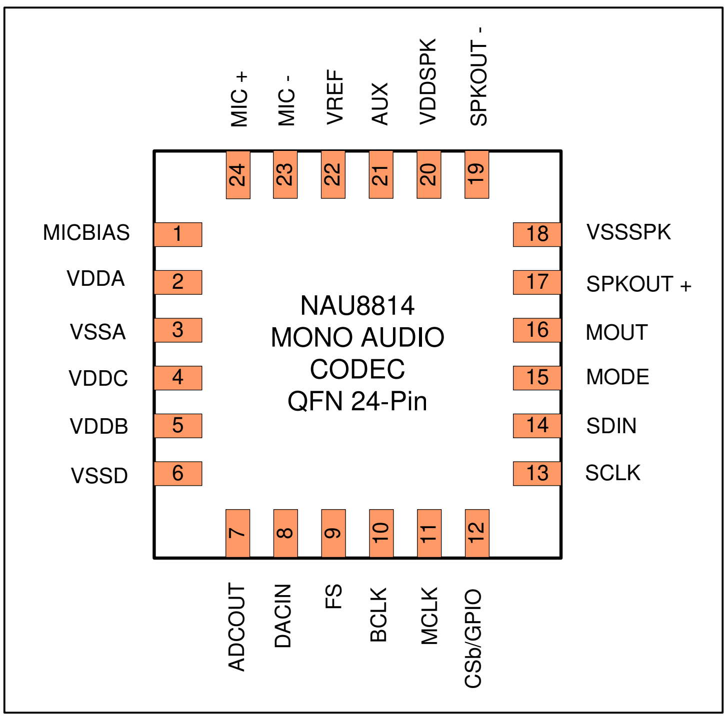


Figure 1: 24-Pin QFN Package

4. PIN DESCRIPTION

Pin Name	24-Pin	Functionality	A/D	Pin Type
MICBIAS	1	Microphone Bias	A	O
VDDA	2	Analog Supply	A	I
VSSA	3	Analog Ground	A	O
VDDC	4	Digital Supply Core	D	I
VDDB	5	Digital Supply Buffer	D	I
VSSD	6	Digital Ground	D	O
ADCOUT	7	Digital Audio Data Output	D	O
DACIN	8	Digital Audio Data Input	D	I
FS	9	Frame Sync	D	I/O
BCLK	10	Bit Clock	D	I/O
MCLK	11	Master Clock	D	I
CSb/GPIO	12	SPI Chip Select or General Purposes I/O	D	I/O
SCLK	13	SPI or 2-Wire Serial Clock	D	I
SDIO	14	SPI Data In or 2-Wire I/O	D	O
MODE	15	Interface Select (2-Wire or SPI)	D	I
MOUT	16	MONO Output	A	O
SPKOUT+	17	Speaker Positive Output	A	O
VSSSPK	18	Speaker Ground	A	O
SPKOUT-	19	Speaker Negative Output	A	O
VDDSPK	20	Speaker Supply	A	I
AUX	21	Auxiliary Input	A	I
VREF	22	Decoupling internal analog mid supply reference	A	O
MIC-	23	Microphone Negative Input	A	I
MIC+	24	Microphone Positive Input	A	I

Table 1: Pin Description

Notes

1. The 24-QFN package includes a bulk ground connection pad on the underside of the chip. This bulk ground should be thermally tied to the PCB, and electrically tied to the analog ground.
2. Unused analog input pins should be left as no-connection.
3. Under all condition when digital pins are not used they should be tied to ground.

5. BLOCK DIAGRAM

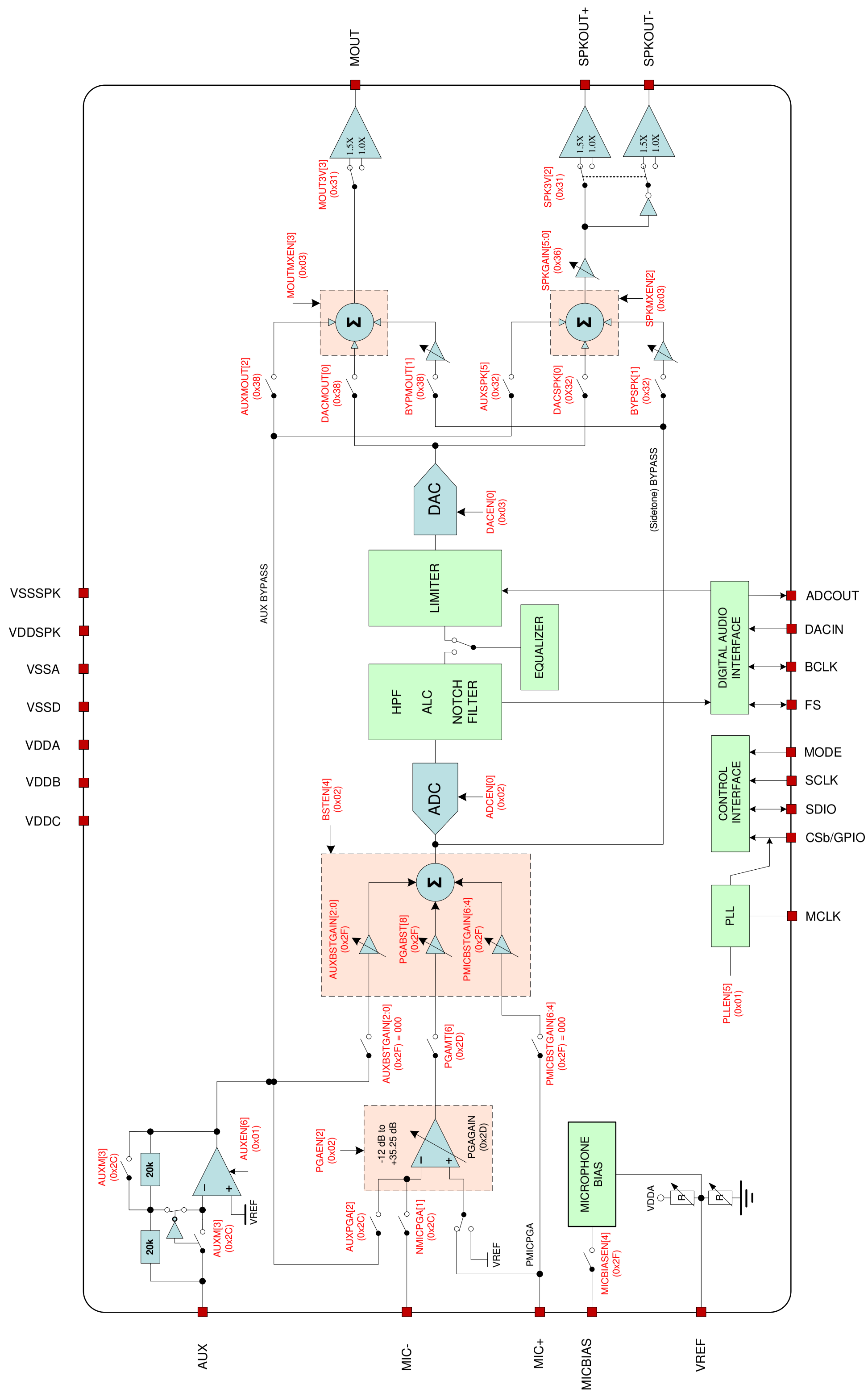


Figure 2: NAU8814 General Block Diagram

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9. ABSOLUTE MAXIMUM RATINGS

CONDITION	MIN	MAX	Units
VDDB, VDDC, VDDA supply voltages	-0.3	+3.63	V
VDDSPK supply voltage (MOUT=0, SPKBST=0)	-0.3	+3.63	V
VDDSPK supply voltage (MOUTBST=1, SPKBST=1)	-0.3	+5.50	V
Core Digital Input Voltage range	VSSD – 0.3	VDDC + 0.30	V
Buffer Digital Input Voltage range	VSSD – 0.3	VDDB + 0.30	V
Analog Input Voltage range	VSSA – 0.3	VDDA + 0.30	V
Industrial operating temperature	-40	+85	^{0}C
Storage temperature range	-65	+150	^{0}C

CAUTION: Do not operate at or near the maximum ratings listed for extended period of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty. These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

10. OPERATING CONDITIONS

Condition	Symbol	Min Value	Typical Value	Max Value	Units
Analogue supplies range	VDDA	2.50[1]		3.60	V
Digital supply range (Buffer)	VDDB	1.71[2]		3.60	V
Digital supply range (Core)	VDDC	1.71[2]		3.60	V
Speaker supply	VDDSPK	2.50		5.50	V
Ground	VSSD, VSSA, VSSSPK		0		V

1. VDDA must be ≥ VDDC.

2. VDDB must be ≥ VDDC.

11. ELECTRICAL CHARACTERISTICS

VDDC = 1.8V, VDDA = VDDB = VDDSPK = 3.3V (VDDSPK = 1.5*VDDA when Boost), T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue to Digital Converter (ADC)						
Full scale input signal [1]	V_{INFS}	PGABST = 0dB PGAGAIN = 0dB		1.0 0		V_{RMS} dBV
Signal to Noise Ratio [2]	SNR	Gain = 0dB, A-weighted	87	91		dB
Total Harmonic Distortion [3]	THD	Input = -1dBFS, Gain = 0dB		-79	-65	dB
Digital to Analogue Converter (DAC) to MONO output (all data measured with 10kΩ / 50pF load)						
Full Scale output signal [1]		MOUTBST=0		1.0x (V_{REF})		V_{RMS}
		MOUTBST=1		1.5 x V_{REF}		
Signal to Noise Ratio [2]	SNR	A-weighted (ADC/DAC oversampling rate of 128)	90	93		dB
Total Harmonic Distortion [3]	THD	R_L = 10 kΩ; -1.0dBfs		-84	-70	dB
Auxiliary Analogue Input (AUX)						
Full-scale Input Signal Level [1]	V_{INFS}	Gain = 0dB		1 0		V_{RMS} dBV
Input Resistance	R_{AUX}	AUXM=0		20		kΩ
Input Capacitance	C_{AUX}			10		pF
Microphone Inputs (MICN & MICP) and MIC Input Programmable Gain Amplifier (PGA)						
Full-scale Input Signal Level [1]	V_{INFS}	PGABST = 0dB PGAGAIN = 0dB		1 0		V_{RMS} dBV
Programmable input PGA gain			-12		35.25	dB
Programmable Gain Step Size		Guaranteed monotonic		0.75		dB
Programmable Boost PGA gain		PGABST = 0		0		dB
		PGABST = 1		20		
Mute Attenuation				100		dB
PGA equivalent output noise		0 to 20kHz, Gain set to 35.25dB		110		µV
Auxiliary Input resistance	R_{AUX}	PGA Gain = 35.25dB		1.6		kΩ
		PGA Gain = 0dB		47		kΩ
		PGA Gain = -12dB		75		kΩ
Positive Microphone Input resistance	R_{MIC+}	PMICPGA = 1		94		kΩ
Input Capacitance	C_{MIC}			10		pF
Speaker Output PGA						
Programmable Gain			-57		6	dB
Programmable Gain Step Size		Guaranteed monotonic		1		dB

VDDC = 1.8V, VDDA = VDDB = VDDSPK = 3.3V (VDDSPK = 1.5*VDDA when Boost), T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS			MIN	TYP	MAX	UNIT
BTL Speaker Output (SPKOUT+, SPKOUT- with 8Ω bridge tied load)								
Full scale output [7]		SPKBST = 0 VDDSPK = VDDA				VDDA / 3.3		V_{RMS}
		SPKBST = 1 VDDSPK = 1.5*VDDA				(VDDA / 3.3) * 1.5		V_{RMS}
Output Power	PO	Output power is very closely correlated with THD; see below						
Signal to Noise Ratio	SNR	VDDSPK = 3.3V RL = 8Ω				90		dB
		VDDSPK = 1.5*VDDA RL = 8Ω				90		dB
Total Harmonic Distortion	THD	PO =180mW	RL = 8Ω	VDDSPK=3.3V		-63		dB
		PO =400mW				-56		dB
		PO =360mW		VDDSPK = 1.5*VDDA		-60		dB
		PO =800mW				-61		dB
		PO =1W				-34		dB
Power Supply Rejection Ratio (50Hz – 22kHz)	PSRR	VDDSPK = 3V, SPKBST = 0				50		dB
		VDDSPK = 1.5*VDDA, SPKBST = 1				50		dB
Headphone' output (SPKOUTP, SPKOUTN with resistive load to ground)								
Full scale output [7]						VDDA / 3.3		V_{RMS}
Signal to Noise Ratio	SNR	A-weighted				90		dB
Total Harmonic Distortion	THD	Po = 20mW	RL=16 Ω	VDDSPK=3.3V		-84		dB
		Po = 20mW	RL=32 Ω			-85		dB
Microphone Bias								
Bias Voltage	$V_{MICBIAS}$	(MICBIASV = 0)				0.9* VDDA		V
		(MICBIASV = 1)				0.65* VDDA		V
Bias Current Source	$I_{MICBIAS}$					3		mA
Output Noise Voltage	V_N	MICBIASM = 0 (1kHz to 20kHz)				14		nV/√Hz
		MICBIASM = 1 (1kHz to 20kHz)				4		nV/√Hz
Automatic Level Control (ALC)/Limiter – ADC only								
Target Record Level					-28.5		-6	dB
Programmable Gain					-12		35.25	dB
Programmable Gain Step Size		Guaranteed Monotonic				0.75		dB
Gain Hold Time [4, 6]	t_{HOLD}	MCLK=12.288MHz				0 / 2.67 / …/ 43691		ms

			(time doubles with each step)	

VDDC = 1.8V, VDDA = VDDB = VDDSPK = 3.3V (VDDSPK = 1.5*VDDA when Boost), T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Automatic Level Control (ALC)/Limiter – ADC only						
Gain Ramp-Up (Decay) Time [5, 6]	t_{DCY}	ALC Mode ALCM=0 MCLK=12.288MHz	3.3 / 6.6 / 13.1 / … / 3360 (time doubles every step)			ms
		Limiter Mode ALCM=1 MCLK=12.288MHz	0.73 / 1.45 / 2.91 / … / 744 (time doubles every step)			ms
Gain Ramp-Down (Attack) Time [5, 6]	t_{ATK}	ALC Mode ALCM=0 MCLK=12.288MHz	0.83 / 1.66 / 3.33 / … / 852 (time doubles every step)			ms
		Limiter Mode ALCM=1 MCLK=12.288MHz	0.18 / 0.36 / 0.73 / … / 186 (time doubles every step)			ms
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7 × VDDB			V
Input LOW Level	V_{IL}				0.3 × VDDB	V
Output HIGH Level	V_{OH}	I_{OL} = 1mA	0.9 × VDDB			V
Output LOW Level	V_{OL}	I_{OH} = -1mA			0.1 x VDDB	V

Notes

1. Full Scale is relative to VDDA (FS = VDDA/3.3.). Input level to AUX is limited to a maximum of -3dB so that THD+N performance will not be reduced.
2. Signal-to-noise ratio (dB) – SNR is a measure of the difference in level between the full-scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
3. THD+N (dB) – THD+N are a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Hold Time is the length of time between a signal detected being too quiet and beginning to ramp up the gain. It does not apply to ramping down the gain when the signal is too loud, which happens without a delay.
5. Ramp-up and Ramp-Down times are defined as the time it takes to change the PGA gain by 6dB of its gain range.
6. All hold, ramp-up and ramp-down times scale proportionally with MCLK
7. The maximum output voltage can be limited by the speaker power supply. If MOUTBST or SPKBST is, set then VDDSPK should be 1.5xVDDA to prevent clipping taking place in the output stage (when PGA gains are set to 0dB).

12. FUNCTIONAL DESCRIPTION

The NAU8814 is a MONO Audio CODEC with very robust ADC and DAC. The device provides one single ended auxiliary input (AUX pin) and one differential microphone input (MIC- & MIC+ pins). The auxiliary input (AUX) can be configured to sum multiple signals into a single input. It has three different amplification paths with a total gain of up to +55.25dB. The differential input also has amplification paths similar to auxiliary input.

The device also has an internal configurable biasing circuit for biasing the microphone, which in turn reduces external components. The PGA output has programmable ADC gain. An advanced Sigma Delta DAC is used along with digital decimation and interpolation filters to give high quality audio at sample rates from 8 kHz to 48 kHz. The Digital Filter blocks include ADC high pass filters, and Notch filter, and a 5-band equalizer. The device has two output mixers, one for MONO output and the other for the speaker output. It also has one input mixer.

The NAU8814 has two different types of serial control interface 2-Wire and SPI for device control. 2-Wire and SPI are hardware selectable through MODE pin on the device. The device also supports I^2S, PCM time slotting, Left Justified and Right Justified for audio interface.

The device can operate as a master or slave device. It can operate with sample rates ranging from 8 kHz to 48 kHz, depending on the values of MCLK and its prescaler. The NAU8814 includes a PLL block, where it takes the external clock (MCLK pin) to generate other clocks for the audio data transfer such as Bit clock (BCLK), Frame sync (FS), and I^2S clocks. The PLL can also configure a separate programmable clock for the use in the system through CSb/GPIO pin. The power control registers help save power by controlling the major individual functional blocks of the NAU8814.

12.1. INPUT PATH

The NAU8814 has two different types of microphone inputs single ended and differential. Figure 3 shows the different paths that the input signals can take.

All inputs are maintained at a DC bias at approximately half of the VDDA supply voltage. Connections to these inputs should be AC-coupled by means of DC blocking capacitors suitable for the device application.

12.1.1. The Single Ended Auxiliary Input (AUX)

The single ended auxiliary input (AUX) has three different paths to MONO output (MOUT).

- Directly connected to the MONO Mixer or Speaker Mixer to MOUT or SPKOUT+ and SPKOUT- respectively
- Connect through the PGA Boost Mixer which has a range of -12dB to +6dB
- Connect through both the input PGA Gain (range of -12dB to +35.25 dB) and PGA Boost Mixer (range of 0db or +20dB)

The last two paths above go through the ADC filters where the ALC loop controls the amplitude of the input signal. The device also has an internal configurable biasing circuit for biasing the microphone, reducing external components.

An internal inverting operational amplifier circuit allows the auxiliary input pin to connect multiple signals for mixing. This can be achieved by setting AUXM[3] address (0x2C) to LOW. The combination of the 20k ohm resistors can vary due to process variation in the gain stage. The block can also be configured to be used as a buffer by setting AUXM[3] address (0x2C) to HIGH. The internal inverting circuit block can be enable/disable by setting AUXEN[6] address (0x01).

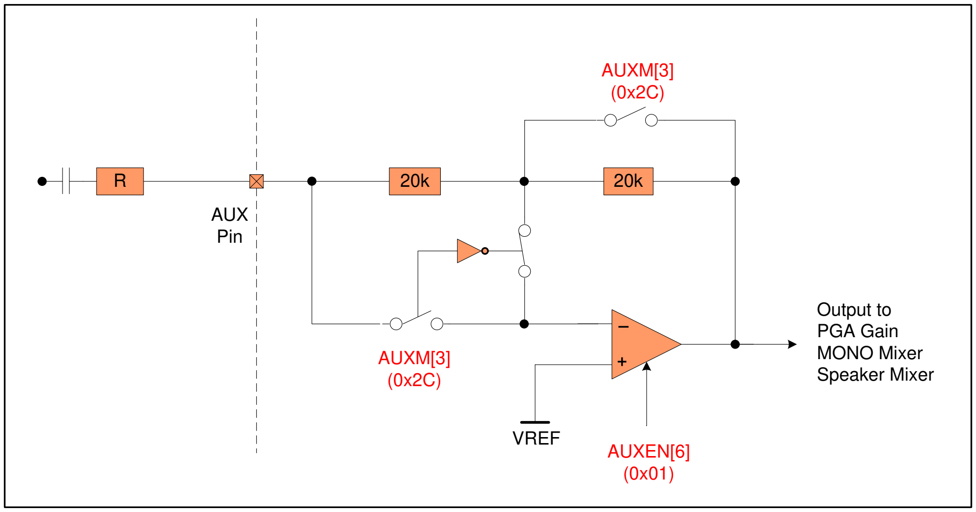

Figure 3: Auxiliary Input Circuit Block Diagram with AUXM[3] = 0

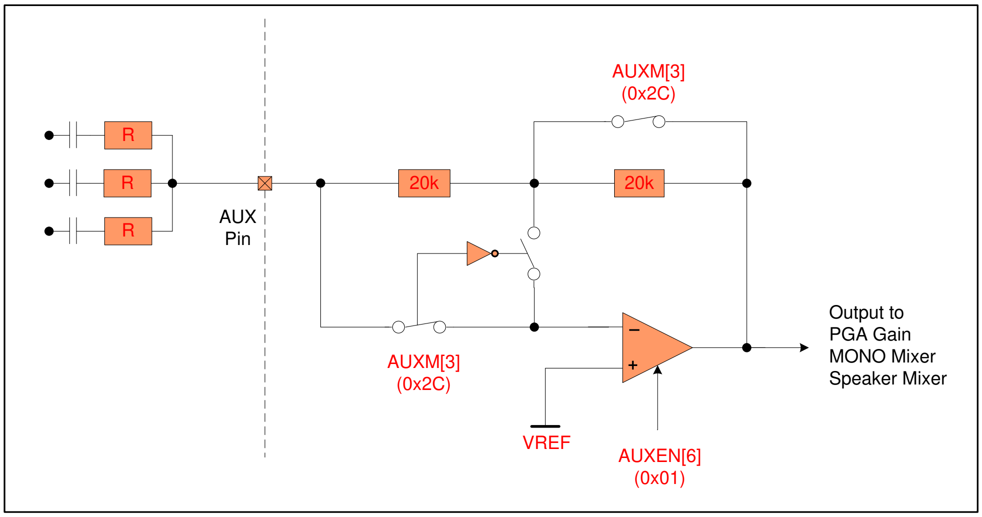

Figure 4: Auxiliary Input Circuit Block Diagram with AUXM[3] = 1

12.1.2. The differential microphone input (MIC- & MIC+ pins)

The NAU8814 features a low-noise, high common mode rejection ratio (CMRR), differential microphone inputs (MIC- & MIC+ pins) which are connected to a PGA Gain stage. The differential input structure is essential in noisy digital systems where amplification of low-amplitude analog signals is necessary such as notebooks and PDAs. When properly employed, the differential input architecture offers an improved power-supply rejection ratio (PSRR) and higher ground noise immunity.

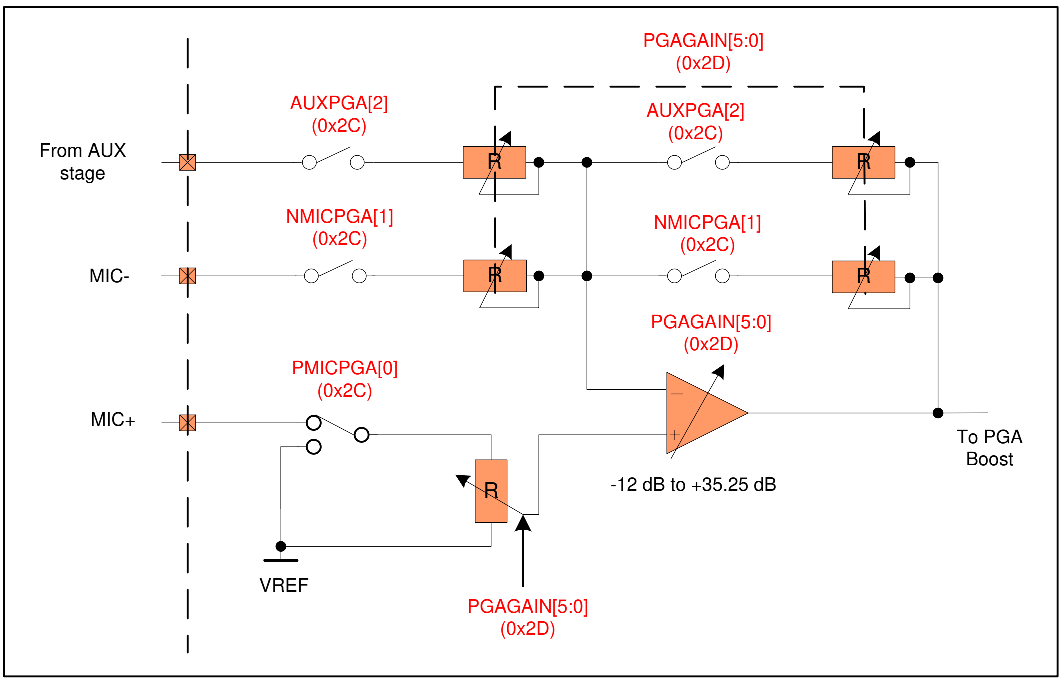

Figure 5: Input PGA Circuit Block Diagram

Bit(s)	Addr	Parameter	Programmable Range
PMICPGA[0]	0x2C	Positive Microphone to PGA	0 = Input PGA Positive terminal to VREF 1 = Input PGA Positive terminal to MICP
NMICPGA[1]	0x2C	Negative Microphone to PGA	0 = MICN not connected to input PGA 1 = MICN to input PGA Negative terminal.

Table 2: Register associated with Input PGA Contro

12.1.2.1. Positive Microphone Input (MIC+)

The positive microphone input (MIC+) can be used as part of the differential input. It connects to the positive terminal of the PGA gain amplifier by setting PMICPGA[0] address (0x2C) to HIGH or can be connected to VREF by setting PMICPGA[0] address (0x2C) to LOW.

When the associated control bit is set logic = 1, the MIC+ pin is connected to a resistor of approximately 1kΩ which is tied to VREF. The purpose of the tie to VREF is to reduce any pop or click sound by keeping the DC level of the MIC+ pin close to VREF at all times.

Note: In single ended applications where the MIC+ input is used without using MIC-, the PGA gain values will be valid only if the MIC- pin is terminated to a low impedance signal point. This termination should normally be an AC coupled path to signal ground. This input impedance is constant regardless of the gain value. The following table gives the nominal input impedance for this input. Impedance for specific gain values not listed in this table can be estimated through interpolation between listed values.

MIC+ to non-inverting PGA input **Nominal Input Impedance**	
Gain (dB)	**Impedance (kΩ)**
-12	94
-9	94
-6	94
-3	94
0	94
3	94
6	94
9	94
12	94
18	94
30	94
35.25	94

Table 3: Microphone Non-Inverting Input Impedances

MIC- to inverting PGA input **Nominal Input Impedance**	
Gain (dB)	**Impedance (kΩ)**
-12	75
-9	69
-6	63
-3	55
0	47
3	39
6	31
9	25
12	19
18	11
30	2.9
35.25	1.6

Table 4: Microphone Inverting Input Impedances

12.1.2.2. Negative Microphone Input (MIC-)

The negative microphone input (MIC-) has two distinctive configuration; differential input or single ended input. This input connects to the negative terminal of the PGA gain amplifier by setting NMICPGA[1] address (0x2C) to HIGH. When the MIC- is used as a single ended input, MIC+ should be conned to VREF by setting PMICPGA[0] address (0x2C) bit to LOW. The AUX input signal can also be mixed with the MIC- input signal by setting AUXPGA[2] address (0x2C) to HIGH.

When the associated control bit is set logic = 1, the MIC- pin is connected to a resistor of approximately 30kΩ which is tied to VREF. The purpose of the tie to VREF is to reduce any pop or click sound by keeping the DC level of the MIC- pin close to VREF at all times. It is important for a system designer to know that the MIC-input impedance varies as a function of the selected PGA gain. This is normal and expected for a difference amplifier type topology. The above table gives the nominal resistive impedance values for this input over the possible gain range. Impedance for specific gain values not listed in this table can be estimated through interpolation between listed values.

12.1.2.3. PGA Gain Control

The PGA amplification is common to all three input pins MIC-, MIC+, AUX, and enabled by PGAEN[2] address (0x02). It has a range of -12dB to +35.25dB in 0.75dB steps, controlled by PGAGAIN[5:0] address (0x2D). Input PGA gain will not be used when ALC is enabled using ALCEN[8] address (0x20).

Addr	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x2D	0	PGAZC	PGAMT	PGAGAIN[5:0]						0x010
0x20	ALCEN	0	0	ALCMXGAIN[2:0]			ALCMNGAIN[2:0]			0x038

Table 5: Registers associated with ALC and Input PGA Gain Control

12.1.3. PGA Boost Stage

The boost stage has three inputs connected to the PGA Boost Mixer. All three inputs can be individually connected or disconnected from the PGA Boost Mixer. The boost stage can be enabled by setting BSTEN[4] address (0x02) to HIGH. The following figure shows the PGA Boost stage.

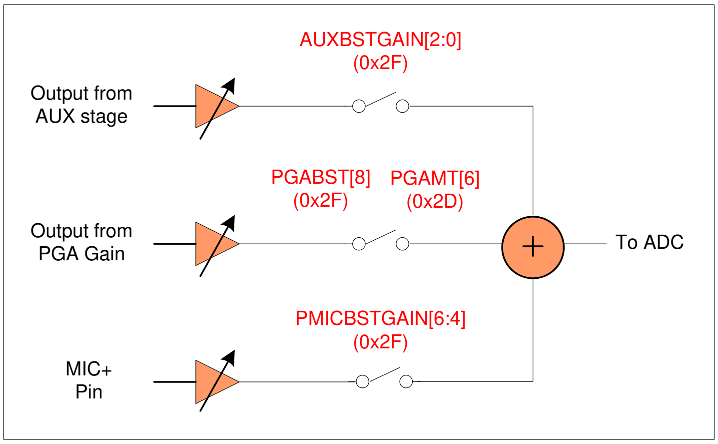

Figure 6: Boost Stage Block Diagram

The signal from AUX stage can be amplified at the PGA Boost stage before connecting to the Boost Mixer by setting a binary value from “001” – “111” to AUXBSTGAIN[2:0] address (0x2F). The path is disconnected by setting “000” to the AUXBSTGAIN bits.

Signal from PGA stage to the PGA Boost Mixer is disconnected or muted by setting PGAMT[6] address (0x2D) to HIGH. In this path the PGA boost can be a fixed value of +20dB or 0dB, controlled by the PGABST[8] address (0x2F) bit.

The signal from MIC+ pin to the PGA Boost Mixer is disconnected by setting ‘000’ binary value to PMICBSTGAIN[6:4] address (0x2F) and any other combination connects the path.

Bit(s)	Addr	Parameter	Programmable Range
BSTEN[4]	0x02	Enable PGA Boost Block	0 = Boost stage OFF 1 = Boost stage ON
PGAMT[6]	0x2D	Mute control for input PGA	0=Input PGA not muted 1=Input PGA muted
AUXBSTGAIN[2:0]	0x2F	Boost AUX signal	Range: -12dB to +6dB @ 3dB increment
PMICBSTGAIN[6:4]	0x2F	Boost MIC+ signal	Range: -12dB to +6dB @ 3dB increment
PGABST[8]	0x2F	Boost PGA stage	0 = PGA output has +0dB 1 = PGA output has +20dB

Table 6: Registers associated with PGA Boost Stage Control

12.2. MICROPHONE BIASING

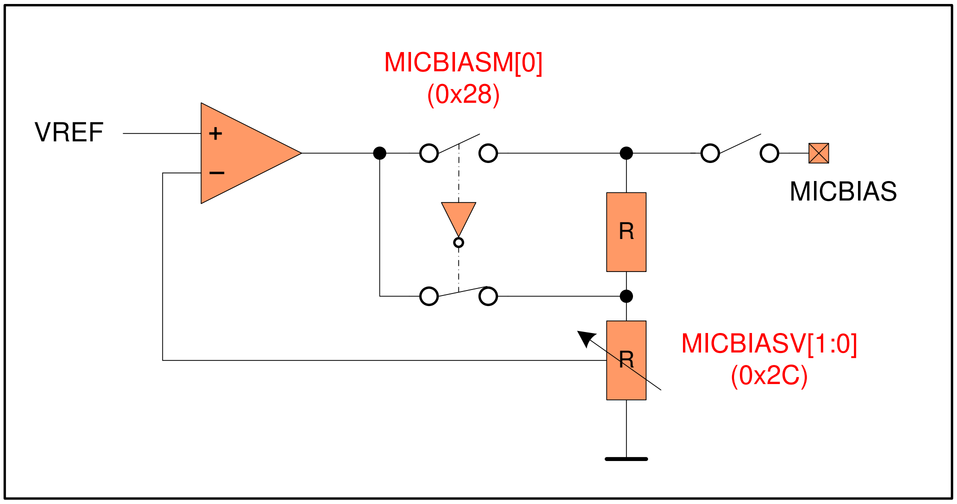

Figure 7: Microphone Bias Schematic

The MICBIAS pin is a low-noise microphone bias source for an external microphone, which can provide a maximum of 3mA of bias current. This DC bias voltage is suitable for powering either traditional ECM (electret) type microphones, or for MEMS types microphones with an independent power supply pin. Seven different bias voltages are available for optimum system performance, depending on the specific application. The microphone bias pin normally requires an external filtering capacitor as shown on the schematic in the Application section.

The output bias can be enabled by setting MICBIASEN[4] address (0x01) to HIGH. It has various voltage values selected by a combination of bits MICBIASM[4] address (0x3A) and MICBIASV[8:7] address (0x2C).

The low-noise feature results in greatly reduced noise in the external MICBIAS voltage by placing a resistor of approximately 200-ohms in series with the output pin. This creates a low pass filter in conjunction with the external microphone-bias filter capacitor, but without any additional external components.

Bit(s)	Addr	Parameter	Programmable Range
MICBIASEN[4]	0x01	Microphone bias enable	0 = Disable 1 = Enable
MICBIASM[4]	(0x3A)	Microphone bias mode selection	
MICBIASV[8:7]	(0x2C)	Microphone bias voltage selection	0 = Disable 1 = Enable

Table 7: Register associated with Microphone Bias

Below are the unloaded values when MICBIASM[4] is set to 1 and 0. When loaded, the series resistor will cause the voltage to drop, depending on the load current.

Microphone Bias Voltage Control			
MICBIASV[8:7]		MICBIASM[4] = 0	MICBIASM[4]= 1
0	0	0.9* VDDA	0.85* VDDA
0	1	0.65* VDDA	0.60* VDDA
1	0	0.75* VDDA	0.70* VDDA
1	1	0.50* VDDA	0.50* VDDA

Table 8: Microphone Bias Voltage Control

12.3. ADC DIGITAL FILTER BLOCK

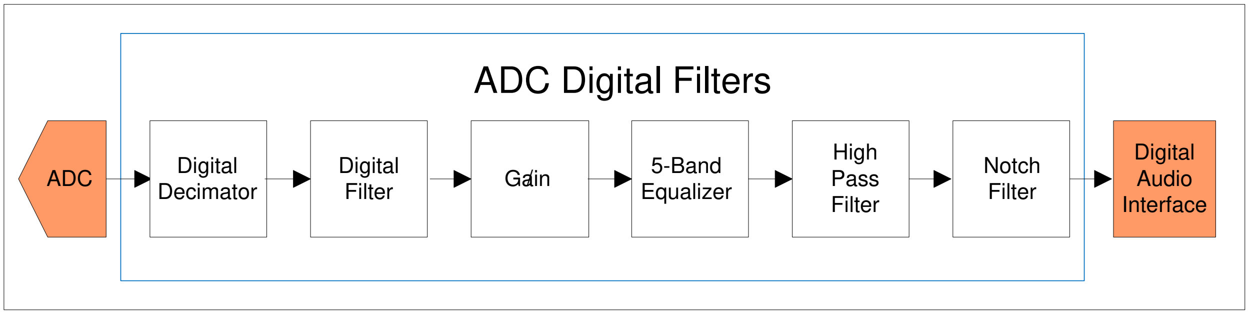

Figure 8: ADC Digital Filter Path Block Diagram

The ADC digital filter block performs a 24-bit signal processing. The block consists of an oversampled analog sigma-delta modulator, digital decimator, digital filter, 5-band graphic equalizer, high pass filter, and a notch filter. For digital decimator and 5-band graphic equalizer refer to "Output Signal Path". The oversampled analog sigma-delta modulator provides a bit stream to the decimation stages and filter. The ADC coding scheme is in twos-complement format and the full-scale input level is proportional to VDDA. With a 3.3V supply voltage, the full-scale level is $1.0V_{RMS}$ and any voltage greater than full scale may overload the ADC and cause distortion. The ADC is enabled by setting ADCEN[0] address (0x02) bit. Polarity and oversampling rate of the ADC output signal can be changed by ADCPL[0] address (0x0E) and ADCOS[3] address (0x0E) respectively.

Bit(s)	Addr	Parameter	Programmable Range
ADCPL[0]	0x0E	ADC Polarity	0 = Normal 1 = Inverted
ADCOS[3]	0x0E	ADC Over Sample Rate	0=64x (Lowest power) 1=128x (best SNR at typical condition)
HPFEN[8]	0x0E	High Pass Filter Enable	0 = Disable 1 = Enable
HPFAM[7]	0x0E	Audio or Application Mode	0 = Audio (1st order, fc ~ 3.7 Hz) 1 = Application (2nd order, fc =HPF)
HPF[6:4]	0x0E	High Pass Filter frequencies	82 Hz to 612 Hz dependant on the sample rate
ADCEN[0]	0x02	Enable ADC	0 = Disable 1 = Enable
SMPLR[3:1]	0x07	Sample rate	8k Hz to 48 kHz

Table 9: Register associated with ADC