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NC7SP17 TinyLogic[®] ULP Single Buffer with Schmitt Trigger Input

Description

3.6V V_{CC}.

The NC7SP17 is a single buffer with Schmitt trigger

input from Fairchild's Ultra Low Power (ULP) series of

TinyLogic®. Ideal for applications where battery life is

critical, this product is designed for ultra low power consumption within the V_{CC} operating range of 0.9V to

The internal circuit is composed of a minimum of

inverter stages, including the output buffer, to enable

The NC7SP17, for lower drive requirements, is uniquely

designed for optimized power and speed and is

fabricated with an advanced CMOS technology to

achieve best-in-class speed of operation, while maintaining extremely low CMOS power dissipation.

ultra low static and dynamic power.

Features

SEMICONDUCTOR

- 0.9V to 3.6V V_{CC} Supply Operation
- 3.6V Over-Voltage Tolerant I/Os at V_{CC} from 0.9V to 3.6V
- Propagation Delay (t_{PD}):
 - 4.0ns Typical for 3.0V to 3.6V V_{CC}
 - 5.0ns Typical for 2.3V to 2.7V V_{CC}
 - 6.0ns Typical for 1.65V to 1.95V V_{CC}
 - 7.0ns Typical for 1.40V to 1.60V V_{CC}
 - 11.0ns Typical for 1.10V to 1.30V V_{CC}
 - 27.0ns Typical for 0.90V V_{CC}
- Power-Off High-Impedance Inputs and Outputs
- Static Drive (I_{OH}/I_{OL}):
 - ± 2.6mA at 3.00V V_{CC}
 - ± 2.1mA at 2.30V V_{CC}
 - ± 1.5mA at 1.65V V_{CC}
 - ± 1.0mA at 1.40V V_{CC}
 - + 0.5mA at 1.10V V_{CC}
 - ± 20µA at 0.9V V_{CC}
- Quiet Series[™] Noise / EMI Reduction Circuitry
- Ultra Small MicroPak™ Packages
- Ultra Low Dynamic Power

Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7SP17P5X	P17	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3000 Units on Tape & Reel
NC7SP17L6X	K4	6-Lead MicroPak™, 1.00mm Wide	5000 Units on Tape & Reel
NC7SP17FHX	K4	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	5000 Units on Tape & Reel

NC7SP17 — TinyLogic[®] ULP Single Buffer with Schmitt Trigger Input

Pin Definitions

Pin # SC70	Pin # MicroPak	Name	Description
1	1, 5	NC	No Connect
2	2	А	Input
3	3	GND	Ground
4	4	Y	Output
5	6	V _{CC}	Supply Voltage

2

Notes:

3.

Figure 1. Battery Life vs. V_{CC} Supply Voltage

IEEE/IEC

1

Figure 2. Logic Symbol

Π

 $\mathbf{x} \, \mathbf{V}_{\mathrm{CC}}^2 \, \mathbf{x} \, \mathbf{f}.$

UHS (SZ)

2.5

Vcc Supply Voltage

3.3 5.0

Α

L = Low Logic Level H = High Logic Level

Function Table

700

600

500

300

200

100

Connection Diagrams

Pin Configurations

0

Battery Life 400

(Days)

ULP (SP)

JLP-A (SV)

0.9 1.2 1.5 1.8

Υ	=A

NC 1		5 V _{CC}	
A 🖅			
GND 3		4 Y	
Figure	3. SC70 (Top	View)	

Input

Α L

н

NC	1		6	Vcc
А	2		5	NC
GND	3		4	Y

frequency at 10MHz, with C_L=15pF load.

Figure 4. MicroPak[™] (Top Through View)

Output Y

L

н

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Para	meter	Min.	Max.	Unit
V _{cc}	Supply Voltage		-0.5	4.6	V
V _{IN}	DC Input Voltage		-0.5	4.6	V
N		HIGH or LOW State ⁽⁴⁾	-0.5	V _{CC} to +0.5	V
V _{OUT}	DC Output Voltage	V _{CC} =0V	-0.5	4.6	V
I _{IK}	DC Input Diode Current at V _{IN} <	0V		-50	mA
	DC Output Diada Currant	V _{OUT} < 0V		-50	
I _{OK}	DC Output Diode Current	$V_{OUT} > V_{CC}$		+50	mA
I _{OH} / I _{OL}	DC Output Source/Sink Current		±50	mA	
I _{CC} or Ground	DC V _{CC} or Ground Current per S	Supply Pin		±50	mA
T _{STG}	Storage Temperature Range		-65	+150	°C
TJ	Junction Temperature Under Bia	as		+150	°C
TL	Junction Lead Temperature (So	Idering, 10 Seconds)		+260	°C
		SC70-5		150	
PD	Power Dissipation at +85°C	MicroPak™-6		130	mW
		MicroPak2™-6		120	
ESD	Human Body Model	JEDEC: JESD22-A114		4000	V
ESD	Charged Device Model	JEDEC: JESD22-C101		2000	v

Note:

4. The I_{O} maximum rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
V _{CC}	Supply Voltage		0.9		3.6	V	
V _{IN}	Input Voltage ⁽⁵⁾		0		3.6	V	
V		HIGH or LOW State	0		V _{cc}	v	
V _{OUT}	Output Voltage	V _{CC} =0V	0		3.6	V	
		V _{CC} =3.0V to 3.6V		±2.6			
	Output Current in I _{OH} / I _{OL}	V _{CC} =2.3V to 2.7V		±2.1		mA	
		V _{CC} =1.65V to 1.95V		±1.5	- / 1		
I _{OH} / I _{OL}		V _{CC} =1.40V to 1.60V		±1.0			
		V _{CC} =1.10V to 1.30V		±0.5	1		
		V _{CC} =0.9V		20.0		μA	
T _A	Free Air Operating Temperature		-40		+85	°C	
Δt / ΔV	Minimum Input Edge Rate	V _{IN} =0.8V to 2.0V, V _{CC} =3.0V		10		ns/V	
		SC70-5		425			
θ_{JA}	Thermal Resistance	MicroPak™-6		500		°C/W	
		MicroPak2™-6		560		1	

Note:

5. Unused inputs must be held HIGH or LOW. They may not float.

	_			T _A =+2	25°C	T _A =-40°C	to +85°C		
Symbol	Parameter	Conditions	V _{cc} (V)	Min.	Max.	Min.	Max.	Units	
			0.90	0.30	0.60	0.30	0.60		
			1.10	0.40	1.00	0.40	1.00		
	Desitive Threshold Ve		1.40	0.50	1.20	0.50	1.20		
VP	Positive Threshold Volta	age	1.65	0.70	1.50	0.70	1.50	V	
			2.30	1.00	1.90	1.00	1.90		
			3.00	1.50	2.60	1.50	2.60		
			0.90	0.10	0.60	0.10	0.60		
			1.10	0.15	0.70	0.15	0.70		
V _N	Negative Threshold Volt	tage	1.40	0.20	0.80	0.20	0.80	v	
۷N	Negative miconola von	lage	1.65	0.25	0.90	0.25	0.90	, î	
			2.30	0.40	1.15	0.40	1.15		
			3.00	0.6	1.50	0.60	1.50		
			0.90	0.07	0.50	0.07	0.50	_	
			1.10	0.08	0.60	0.08	0.60	_	
V _H	Hysteresis Voltage		1.40	0.09	0.80	0.09	0.80	v	
- 11			1.65	0.10	1.00	0.10	1.00		
			2.30	0.25	1.10	0.25	1.10		
			3.00	0.60	1.80	0.60	1.80		
	HIGH Level Output Voltage		0.90	V _{CC} – 0.1		V _{CC} – 0.1		-	
		I _{он} =–20µА	$1.10 \leq V_{CC} \leq 1.30$	V _{CC} – 0.1		V _{cc} – 0.1			
			$1.40 \leq V_{CC} \leq 1.60$	V _{CC} – 0.1		V _{CC} – 0.1			
			$1.65 \leq V_{CC} \leq 1.95$	V _{CC} – 0.1		V _{CC} – 0.1			
		HIGH Level Output		$2.30 \leq V_{CC} \leq 2.70$	V _{CC} – 0.1		V _{CC} – 0.1		
V _{OH}			$3.00 \leq V_{CC} \leq 3.60$	$V_{CC} - 0.1$		$V_{CC} - 0.1$		V	
		I _{он} =–0.5mA	$1.10 \leq V_{CC} \leq 1.30$	$0.75 ext{ x V}_{CC}$		$0.70 \times V_{CC}$			
		I _{он} =–1mA	$1.40 \leq V_{CC} \leq 1.60$	1.07		0.99			
		I _{он} =–1.5mA	$1.65 \leq V_{CC} \leq 1.95$	1.24		1.22			
		I _{OH} =–2.1mA	$2.30 \leq V_{CC} \leq 2.70$	1.95		1.87			
		I _{он} =–2.6mА	$3.00 \leq V_{CC} \leq 3.60$	2.61		2.55			
			0.90		0.1		0.1		
			$1.10 \leq V_{CC} \leq 1.30$		0.1		0.1		
		1 -20114	$1.40 \leq V_{CC} \leq 1.60$		0.1		0.1		
		I _{οL} =20μΑ	$1.65 \leq V_{CC} \leq 1.95$		0.1		0.1		
			$2.30 \leq V_{CC} \leq 2.70$		0.1		0.1		
V _{OL}	LOW Level Output		$3.00 \leq V_{\text{CC}} \leq 3.60$		0.1		0.1	V	
• OL	Voltage	I _{OL} =0.5mA	$1.10 \leq V_{CC} \leq 1.30$		0.30 x V _{CC}		0.30 x V _{cc}		
		I _{OL} =1mA	$1.40 \leq V_{CC} \leq 1.60$		0.31		0.37	2	
		I _{OL} =1.5mA	$1.65 \leq V_{CC} \leq 1.95$		0.31		0.35		
		I _{oL} =2.1mA	$2.30 \leq V_{CC} \leq 2.70$		0.31		0.33		
		I _{OL} =2.6mA	$3.00 \leq V_{CC} \leq 3.60$		0.31		0.33]	
I _{IN}	Input Leakage Current	$0 \leq V_{IN} \leq 3.6V$	0.90 to 3.60		±0.1		±0.5	μA	
I _{OFF}	Power Off Leakage Current	$\begin{array}{l} 0 \leq (V_{\text{IN}}, V_{\text{O}}) \\ \leq 3.6 V \end{array}$	0		0.5		0.5	μA	
Icc	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND	0.90 to 3.60		0.9		0.9	μA	

Symbol Devementer				T _A =25°C		$T_{A}=25^{\circ}C$ $T_{A}=-40$ to 85°		T _A =25°C T,	5°C T _A =-40 to 8		T _A =-40 to 85°C		NC7SP1
Symbol Parameter	Conditions	V _{cc}	Min.	Тур.	Max.	Min.	Max.	Units	Figu				
			0.90		27.0								
		1.10 ≤ V _{CC} ≤ 1.30	3.5	11.0	21.8	3.0	34.3		TinyLogic [®]				
	C _L =10pF,	$1.40 \le V_{CC} \le 1.60$	2.5	7.0	14.8	2.0	15.0						
		$R_L=1M\Omega$	$1.65 \le V_{CC} \le 1.95$	2.0	6.0	12.0	1.5	12.2		D C C			
			$2.30 \le V_{CC} \le 2.70$	1.5	5.0	9.4	1.0	9.9		ក ្ល			
			$3.00 \le V_{\rm CC} \le 3.60$	1.0	4.0	8.3	1.0	9.0					
			0.90		30.0								
			1.10 ≤ V _{CC} ≤ 1.30	4.0	11.0	22.8	3.5	37.3		L.O.			
	Draw and the Dalay	C _L =15pF,	$1.40 \le V_{CC} \le 1.60$	3.0	8.0	15.5	2.5	16.5					
t_{PHL}, t_{PLH}	Propagation Delay	$R_L = 1M\Omega$	1.65 ≤ V _{CC} ≤ 1.95	2.5	6.0	12.6	2.0	13.6	ns	Figur			
			2.30 ≤ V _{CC} ≤ 2.70	2.0	5.0	9.9	1.5	10.8		Β			
			$3.00 \le V_{CC} \le 3.60$	1.5	4.0	8.7	1.0	9.5		l E			
			0.90		32.0					P			
			1.10 ≤ V _{CC} ≤ 1.30	5.0	13.0	25.9	4.0	46.3		≦			
	1	C _L =30pF, R _L =1MΩ	$1.40 \le V_{CC} \le 1.60$	4.0	9.0	17.8	3.5	18.2		5			
			1.65 ≤ V _{CC} ≤ 1.95	3.0	7.0	14.4	2.0	15.9		ပ္သ			
			2.30 ≤ V _{CC} ≤ 2.70	2.0	6.0	11.3	1.5	12.8		lΞ			
			$3.00 \le V_{CC} \le 3.60$	1.5	5.0	9.2	1.0	10.7	-	ULP Shing be Buffer with Schmitt			
CIN	Input Capacitance		0		2				р				
C_{PD}	Power Dissipation Capacitance	V_{IN} =0V or V_{CC} , f=10MHz	0.90 to 3.60		8				р	rigg			
S			Input	GND V _o ut	он	 3ns 90% 50% t_{PHL} 50 	90%	= 3ns	-	Trigger Input			
	Finung	5. AC Test Circui					. fau luu	erting an					

Symbol		V _{cc}								
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V	1.5V ± 0.1V	1.2V ± 0.1V	0.9V				
V _{mi}	1.5V	V _{CC} / 2								
V _{mo}	1.5V	V _{CC} / 2								

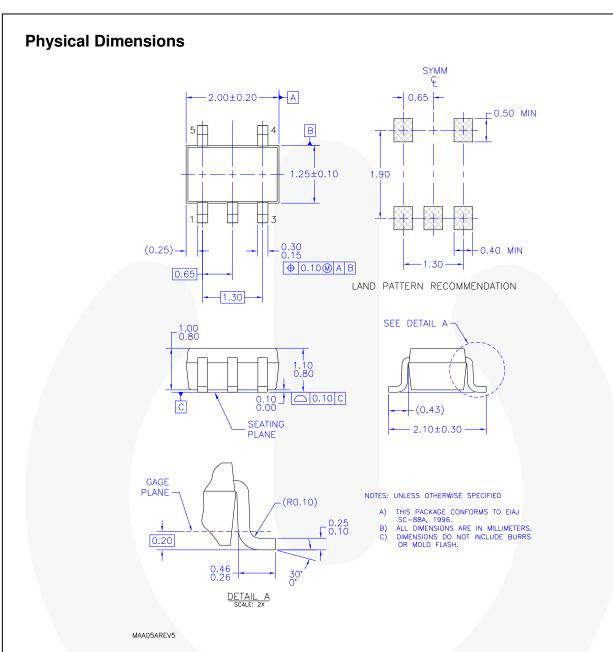


Figure 7. 5-Lead, SC70, EIAJ SC-88a, 1.25mm Wide

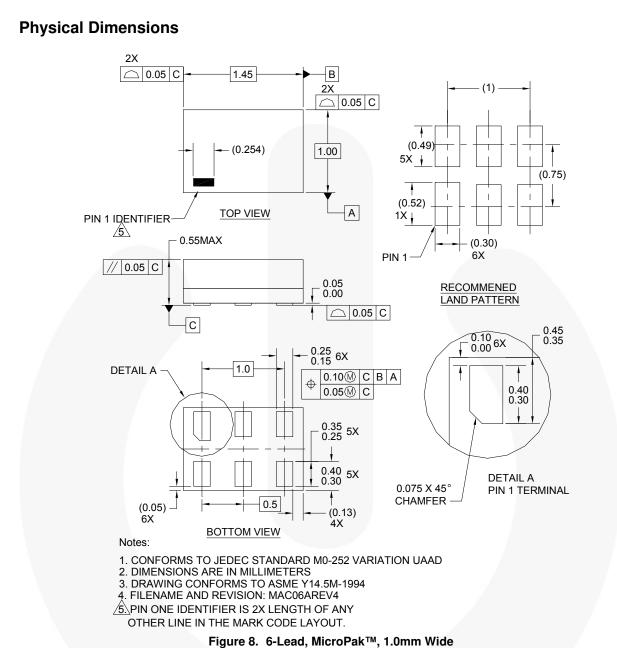
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Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
P5X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed



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Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
L6X	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

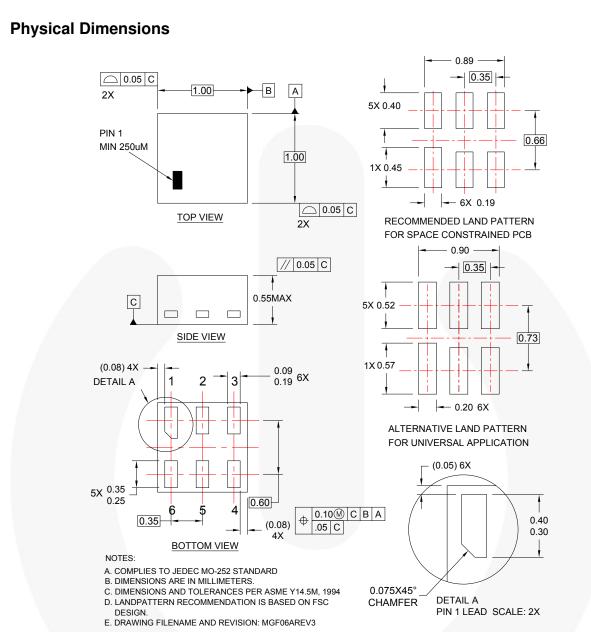


Figure 9. 6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch

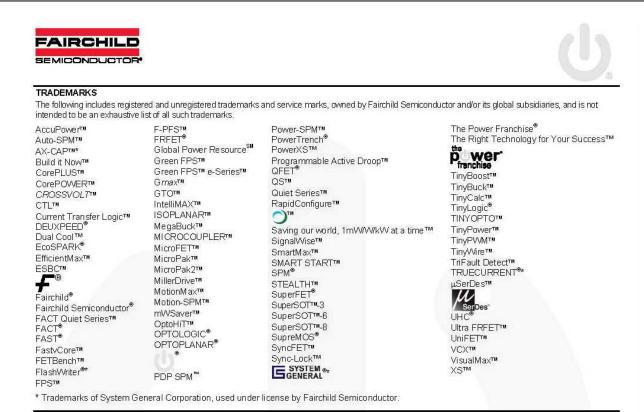
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Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: <u>http://www.fairchildsemi.com/packaging/MicroPAK2_6L_tr.pdf.</u>

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed



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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchil Semiconductor reserves the right to make changes at any time without notice to improve design.	
No Identification Needed	tion Needed Full Production Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.		
		Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.	

Rev. 153

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