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NC7ST32 TinyLogic® HST 2-Input OR Gate

General Description

The NC7ST32 is a single 2-Input high performance CMOS OR Gate, with TTL-compatible inputs. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation. ESD protection diodes inherently guard both inputs and output with respect to the V_{CC} and GND rails. High gain circuitry offers high noise immunity and reduced sensitivity to input edge rate. The TTL-compatible inputs facilitate TTL to NMOS/CMOS interfacing. Device performance is similar to MM74HCT but with ½ the output current drive of HC/HCT.

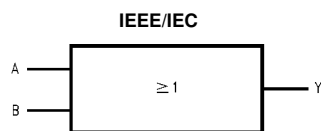
Features

- Space saving SOT23 or SC70 5-lead package
- Ultra small MicroPak™ leadless package
- High Speed; $t_{PD} < 7$ ns typ, $V_{CC} = 5V$, $C_L = 15$ pF
- Low Quiescent Power; $I_{CC} < 1$ μA typ, $V_{CC} = 5.5V$
- Balanced Output Drive; 2 mA I_{OL} , -2 mA I_{OH}
- TTL-compatible inputs

Ordering Code:

| Order Number | Package Number | Product Code Top Mark | Package Description | Supplied As |
|--------------|----------------|-----------------------|---------------------------------------|---------------------------|
| NC7ST32M5X | MA05B | 8S32 | 5-Lead SOT23, JEDEC MO-178, 1.6mm | 3k Units on Tape and Reel |
| NC7ST32P5X | MAA05A | T32 | 5-Lead SC70, EIAJ SC-88a, 1.25mm Wide | 3k Units on Tape and Reel |
| NC7ST32L6X | MAC06A | D7 | 6-Lead MicroPak, 1.0mm Wide | 5k Units on Tape and Reel |

Logic Symbol



Pin Descriptions

| Pin Names | Description |
|-----------|-------------|
| A, B | Inputs |
| Y | Output |
| NC | No Connect |

Function Table

$$Y = A + B$$

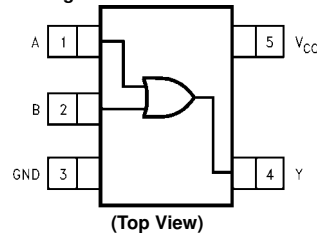
| Inputs | | Output |
|--------|---|--------|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | H |

H = HIGH Logic Level
L = LOW Logic Level

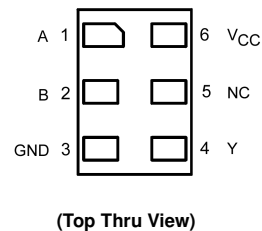
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MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

Connection Diagrams

Pin Assignments for SOT23 and SC70



Pad Assignments for MicroPak



Absolute Maximum Ratings(Note 1)

| | |
|--|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Input Diode Current (I_{IK}) | |
| $V_{IN} < -0.5V$ | -20 mA |
| $V_{IN} \geq V_{CC} + 0.5V$ | +20 mA |
| DC Input Voltage (V_{IN}) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Diode Current (I_{OK}) | |
| $V_{OUT} < -0.5V$ | -20 mA |
| $V_{OUT} > V_{CC} + 0.5V$ | +20 mA |
| Output Voltage (V_{OUT}) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Source or Sink Current (I_{OUT}) | ± 12.5 mA |
| DC V_{CC} or Ground Current per Supply Pin (I_{CC} or I_{GND}) | ± 25 mA |
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Junction Temperature (T_J) | 150°C |
| Lead Temperature (T_L); (Soldering, 10 seconds) | 260°C |
| Power Dissipation (P_D) @+85°C | |
| SOT23-5 | 200 mW |
| SC70-5 | 150 mW |

Recommended Operating Conditions (Note 2)

| | |
|---|----------------|
| Supply Voltage | 4.5V–5.5V |
| Input Voltage (V_{IN}) | 0V– V_{CC} |
| Output Voltage (V_{OUT}) | 0V– V_{CC} |
| Operating Temperature (T_A) | -40°C to +85°C |
| Input Rise and Fall Time (t_r, t_f) | |
| $V_{CC} = 5.0V$ | 0–500 ns |
| Thermal Resistance (θ_{JA}) | |
| SOT23-5 | 300°C/W |
| SC70-5 | 425°C/W |

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of circuits outside the databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

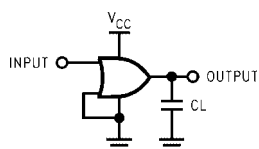
| Symbol | Parameter | V_{CC} (V) | $T_A = +25^\circ\text{C}$ | | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | Units | Conditions |
|-----------|---------------------------|-----------------|---------------------------|------|-----------|---|-----------|---------------|--|
| | | | Min | Typ | Max | Min | Max | | |
| V_{IH} | HIGH Level Input Voltage | 4.5–5.5 | 2.0 | | | 2.0 | | V | |
| V_{IL} | LOW Level Input Voltage | 4.5–5.5 | | | 0.8 | | 0.8 | V | |
| V_{OH} | HIGH Level Output Voltage | 4.5 | 4.4 | 4.5 | | 4.4 | | V | $I_{OH} = -20 \mu\text{A}, V_{IN} = V_{IH}$ |
| | | 4.5 | 4.18 | 4.35 | | 4.13 | | V | $I_{OH} = -2 \text{ mA}$ |
| V_{OL} | LOW Level Output Voltage | 4.5 | | 0 | 0.1 | | 0.1 | V | $I_{OL} = 20 \mu\text{A}, V_{IN} = V_{IL}$ |
| | | 4.5 | | 0.10 | 0.26 | | 0.33 | V | $I_{OL} = 2 \text{ mA}$ |
| I_{IN} | Input Leakage Current | 5.5 | | | ± 0.1 | | ± 1.0 | μA | $0 \leq V_{IN} \leq 5.5V$ |
| I_{CC} | Quiescent Supply Current | 5.5 | | | 1.0 | | 10.0 | μA | $V_{IN} = V_{CC}$ or GND |
| I_{CCT} | I_{CC} per Input | 5.5 | | | 2.0 | | 2.9 | mA | One Input $V_{IN} = 0.5V$ or 2.4V, Other Input V_{CC} or GND |

AC Electrical Characteristics

| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | | T _A = -40°C to +85°C | | Units | Conditions | Fig. No. |
|--|-------------------------------|------------------------|------------------------|------|-----|---------------------------------|-----|-------|------------------------|-----------------|
| | | | Min | Typ | Max | Min | Max | | | |
| t _{PLH} , t _{PHL} | Propagation Delay | 5.0 | | 4.3 | 12 | | | ns | C _L = 15 pF | Figures 1, 3 |
| | | | | 6.1 | 17 | | | | | |
| | | 4.5 | | 6.5 | 16 | | 20 | ns | C _L = 50 pF | |
| | | | | 12.0 | 27 | | 31 | | | |
| | | 5.5 | | 5.4 | 14 | | 18 | | | |
| | | | | 10.7 | 26 | | 30 | | | |
| t _{TLH} , t _{THL} | Output Transition Time | 5.0 | | 4 | 10 | | | ns | C _L = 15 pF | Figures 1, 3 |
| | | 4.5 | | 11 | 25 | | 31 | ns | C _L = 50 pF | |
| | | 5.5 | | 10 | 21 | | 26 | | | |
| C _{IN} | Input Capacitance | Open | | 2 | 10 | | | pF | | |
| C _{PD} | Power Dissipation Capacitance | 5.0 | | 6 | | | | pF | (Note 3) | Figure 2 |

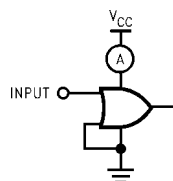
Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:
 $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CCstatic})$.

AC Loading and Waveforms



C_L includes load and stray capacitance
 Input PRR = 1.0 MHz, t_w = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveform; PRR = Variable; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

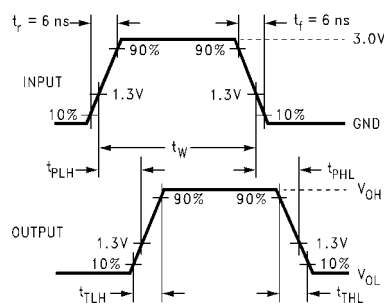


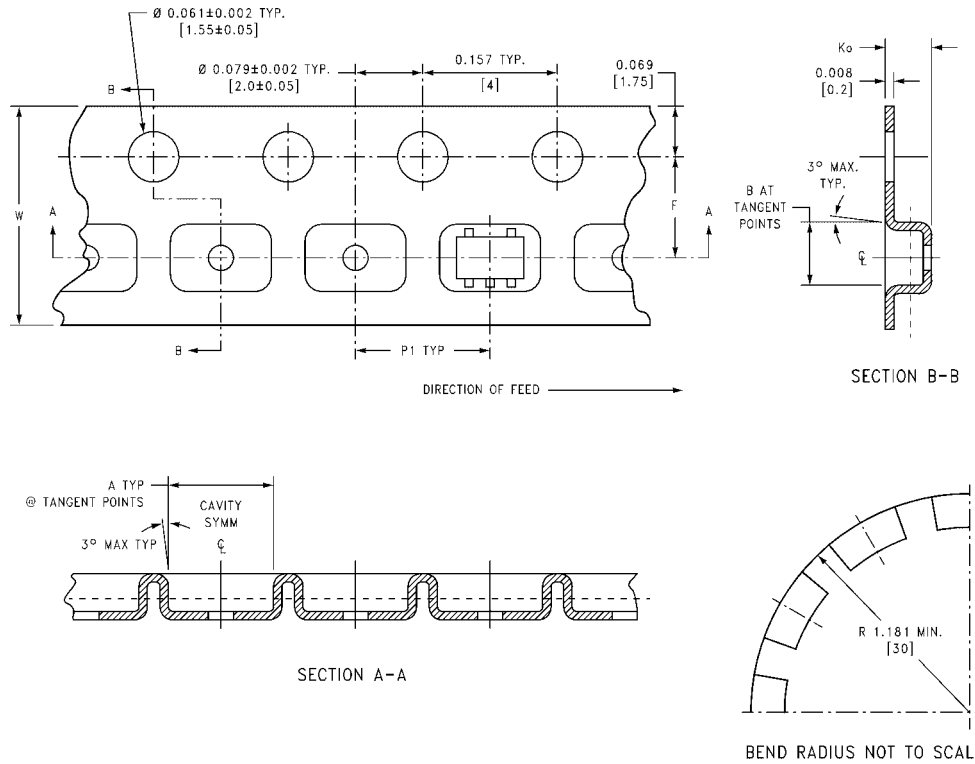
FIGURE 3. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for SOT23 and SC70

| Package Designator | Tape Section | Number Cavities | Cavity Status | Cover Tape Status |
|--------------------|--------------------|-----------------|---------------|-------------------|
| M5X, P5X | Leader (Start End) | 125 (typ) | Empty | Sealed |
| | Carrier | 3000 | Filled | Sealed |
| | Trailer (Hub End) | 75 (typ) | Empty | Sealed |

TAPE DIMENSIONS inches (millimeters)

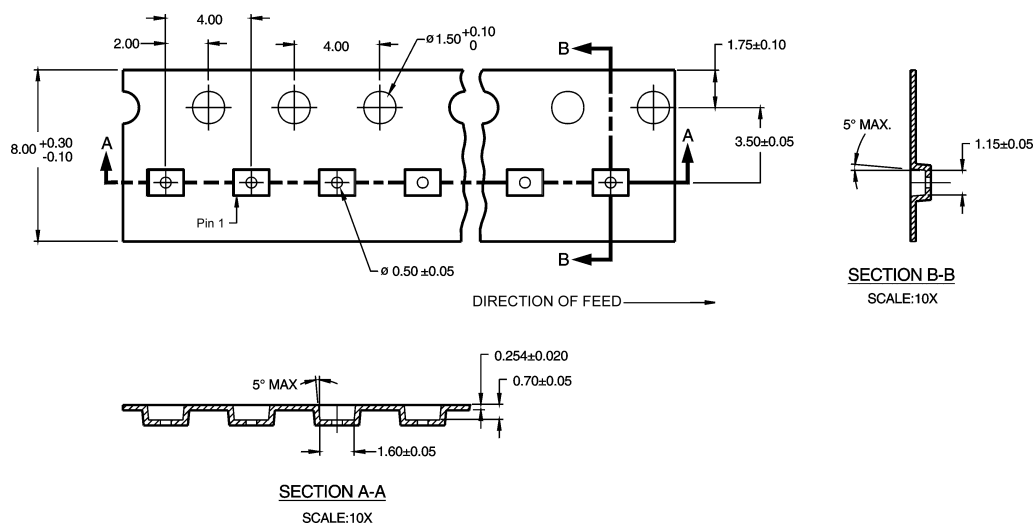


| Package | Tape Size | DIM A | DIM B | DIM F | DIM K ₀ | DIM P1 | DIM W |
|---------|-----------|-----------------|-----------------|-------------------------------|--------------------------------|--------------|----------------------------|
| SC70-5 | 8 mm | 0.093 (2.35) | 0.096 (2.45) | 0.138 ± 0.004 (3.5 ± 0.10) | 0.053 ± 0.004 (1.35 ± 0.10) | 0.157 (4) | 0.315 ± 0.004 (8 ± 0.1) |
| SOT23-5 | 8 mm | 0.130 (3.3) | 0.130 (3.3) | 0.138 ± 0.002 (3.5 ± 0.05) | 0.055 ± 0.004 (1.4 ± 0.11) | 0.157 (4) | 0.315 ± 0.012 (8 ± 0.3) |

Tape and Reel Specification (Continued)

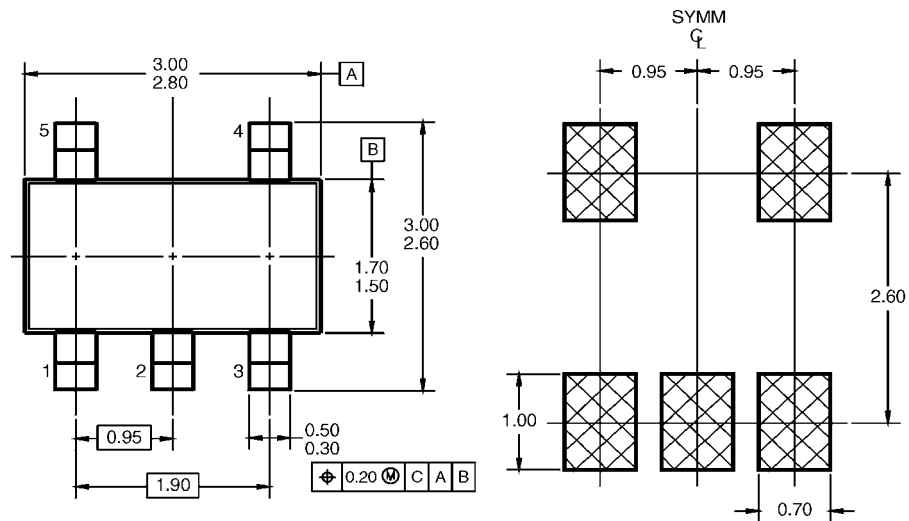
TAPE FORMAT for MicroPak

| Package Designator | Tape Section | Number Cavities | Cavity Status | Cover Tape Status |
|--------------------|--------------------|-----------------|---------------|-------------------|
| L6X | Leader (Start End) | 125 (typ) | Empty | Sealed |
| | Carrier | 5000 | Filled | Sealed |
| | Trailer (Hub End) | 75 (typ) | Empty | Sealed |

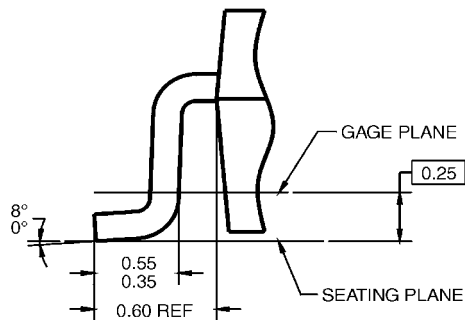
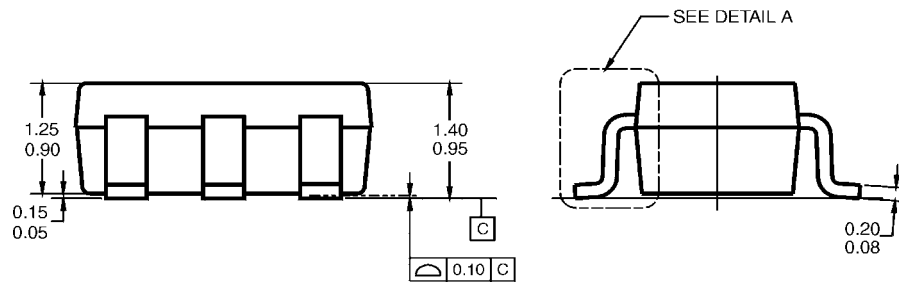


| Tape Size | A | B | C | D | N | W1 | W2 | W3 |
|-----------|----------------|-----------------|------------------|------------------|------------------|---|------------------|--|
| 8 mm | 7.0 (177.8) | 0.059 (1.50) | 0.512 (13.00) | 0.795 (20.20) | 2.165 (55.00) | 0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00) | 0.567 (14.40) | W1 + 0.078/-0.039 (W1 + 2.00/-1.00) |

Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

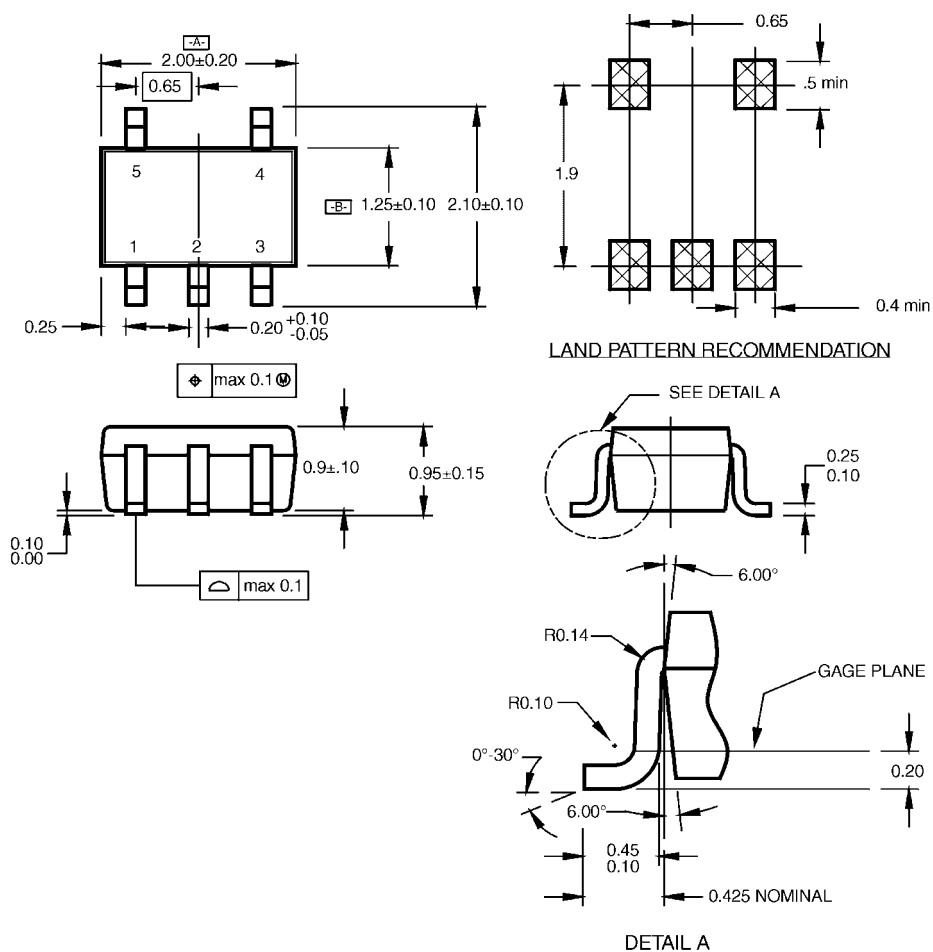
- A) THIS PACKAGE CONFORMS TO JEDEC MO-178, ISSUE B, VARIATION AA, DATED JANUARY 1999.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.

MA05BRevC

DETAIL A

5-Lead SOT23, JEDEC MO-178, 1.6mm
Package Number MA05B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



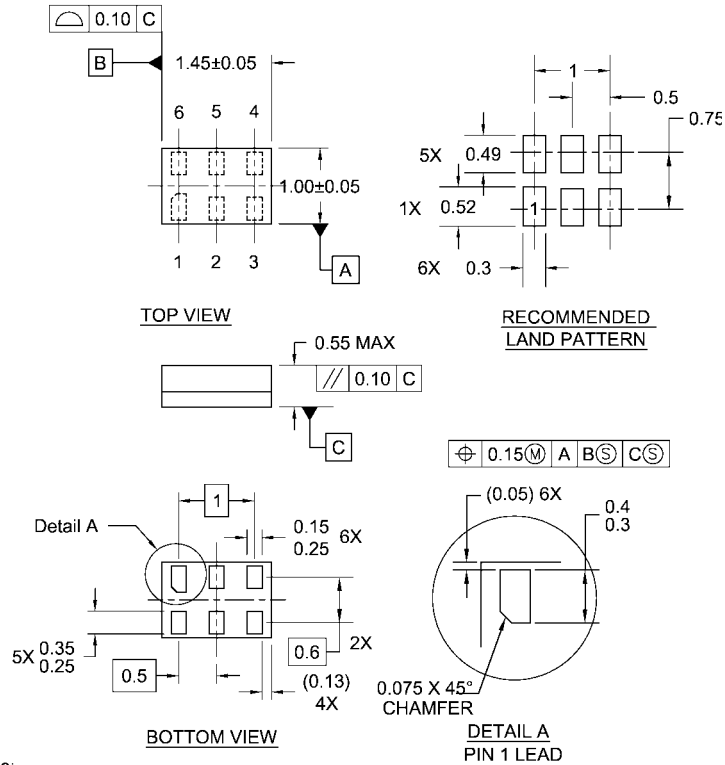
NOTES:

- A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88A.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
- C. DIMENSIONS ARE IN MILLIMETERS.

MAA05ARevC

**5-Lead SC70, EIAJ SC-88a, 1.25mm Wide
Package Number MAA05A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

**6-Lead MicroPak, 1.0mm Wide
Package Number MAC06A**

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