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June 1998
Revised August 2004

NC7SZ373
TinyLogic® UHS D-Type Latch with 3-STATE Output

General Description

The NC7SZ373 is a single positive edge-triggered D-type CMOS Latch with 3-STATE output from Fairchild's Ultra High Speed Series of TinyLogic® in the space saving SC70 6-lead package. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V range. The inputs and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V independent of V_{CC} operating voltage. The latch appears transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. The output tolerates voltages above V_{CC} in the 3-STATE condition.

Features

- Space saving SC70 6-lead package
- Ultra small MicroPak™ leadless package
- Ultra High Speed; t_{PD} 2.6 ns Typ into 50 pF at 5V V_{CC}
- High Output Drive; ±24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.65V to 5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/output
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SZ373P6X	MAA06A	Z73	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ373L6X	MAC06A	D4	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

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MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

Logic Symbol

IEEE/IEC

$\overline{OE}$
LE
D ── Q

Pin Descriptions

Pin Names	Description
D	Data Input
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
Q	Latch Output

Function Table

Inputs			Output
LE	**D**	**$\overline{OE}$**	**Q**
H	L	L	L
H	H	L	H
L	X	L	Q_{n-1}
X	X	H	Z

H = HIGH Logic Level   X = Immaterial
L = LOW Logic Level   Z = HIGH Impedance
Q_{n-1} = Previous state prior to HIGH-to-LOW transition of latch enable

Connection Diagrams

Pin Assignments for SC70

LE 1 | LE | 6 $\overline{OE}$
GND 2 | | 5 V_{CC}
D 3 | D Q | 4 Q

(Top View)
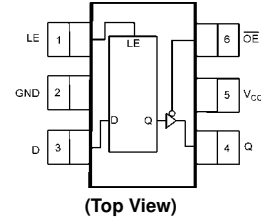
Pin One Orientation Diagram

(Top View)   AAA
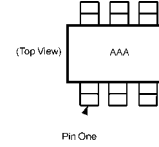
Pin One

AAA = Product Code Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin.(see diagram).

Pad Assignments for MicroPak

LE 1 | | 6 $\overline{OE}$
GND 2 | | 5 V_{CC}
D 3 | | 4 Q

(Top Thru View)

Absolute Maximum Ratings (Note 1)

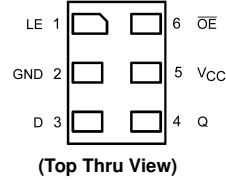|	
Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_{IN} < 0V$	−50 mA
DC Output Diode Current (I_{OK})	
$V_{OUT} < 0V$	−50 mA
DC Output (I_{OUT}) Source/Sink Current	±50 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Junction Temperature under Bias (T_J)	150°C
Junction Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C
Power Dissipation (P_D) @+85°C	180 mW

Recommended Operating Conditions (Note 2)

Power Supply	
Operating (V_{CC})	1.65V to 5.5V
Data Retention	1.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	
Active State	0V to V_{CC}
3-STATE	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
$V_{CC} = 1.8V$, $2.5V \pm 0.2V$	0 to 20 ns/V
$V_{CC} = 3.3V \pm 0.3V$	0 to 10 ns/V
$V_{CC} = 5.5V \pm 0.5V$	0 to 5 ns/V
Operating Temperature (T_A)	−40°C to +85°C
Thermal Resistance (θ_{JA})	350° C/W

Note 1: The "Absolute Maximum Ratings": are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = −40°C$ to $+85°C$		Unit	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Control	1.65 to 1.95	0.75 V_{CC}			0.75 V_{CC}		V		
	Input Voltage	2.3 to 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Control	1.65 to 1.95			0.25 V_{CC}		0.25 V_{CC}	V		
	Input Voltage	2.3 to 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level Control	1.65	1.55	1.65		1.55		V	$V_{IN} = V_{IH}$	$I_{OH} = −100$ µA
	Output Voltage	1.8	1.7	1.8		1.7				
		2.3	2.2	2.3		2.2				
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		1.65	1.24	1.52		1.29				$I_{OH} = −4$ mA
		2.3	1.9	2.15		1.9				$I_{OH} = −8$ mA
		3.0	2.4	2.8		2.4				$I_{OH} = −16$ mA
		3.0	2.3	2.68		2.3				$I_{OH} = −24$ mA
		4.5	3.8	4.2		3.8				$I_{OH} = −32$ mA
V_{OL}	LOW Level Control	1.65		0.0	0.08		0.0	V	$V_{IN} = V_{IL}$	$I_{OL} = 100$ µA
	Output Voltage	1.8		0.0	0.1		0.1			
		2.3		0.0	0.1		0.1			
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		1.65		0.08	0.24		0.24			$I_{OL} = 4$ mA
		2.3		0.10	0.3		0.3			$I_{OL} = 8$ mA
		3.0		0.15	0.4		0.4			$I_{OL} = 16$ mA
		3.0		0.22	0.55		0.55			$I_{OL} = 24$ mA
		4.5		0.22	0.55		0.55			$I_{OL} = 32$ mA
I_{IN}	Input Leakage Current	0 to 5.5			±0.1		±1.0	µA	$0 \leq V_{IN} \leq 5.5V$	
I_{OZ}	3-STATE Output Leakage	1.65 to 5.5			±0.5		±5.0	µA	$V_{IN} = V_{IL}$ or V_{IH} $0 \leq V_{OUT} \leq 5.5V$	
I_{OFF}	Power-Off Leakage Current	0.0			1.0		10	µA	V_{IN} or $V_{OUT} = 5.5V$	
I_{CC}	Quiescent Supply Current	1.65 to 5.5			1.0		10	µA	$V_{IN} = 5.5V$, GND	

AC Electrical Characteristics

Symbol	Parameter	V_CC (V)	T_A = +25°C Min	T_A = +25°C Typ	T_A = +25°C Max	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units	Conditions	Figure Number
t_{PLH} t_{PHL}	Propagation Delay D to Q	1.65	2.0	9.0	15.0	2.0	16.0	ns	C_L = 15 pF R_D = 1 MΩ S_1 = Open	Figures 1, 3
		1.8	2.0	6.1	10.0	2.0	10.5			
		2.5 ± 0.2	1.5	3.6	6.5	1.6	6.8			
		3.3 ± 0.3	1.0	2.7	4.6	1.2	5.0			
		5.0 ± 0.5	1.0	2.0	3.4	1.0	3.7			
		3.3 ± 0.3	1.5	3.3	5.5	1.5	6.2		C_L = 50 pF R_D = 500Ω, S_1 = Open	Figures 1, 3
		5.0 ± 0.5	1.0	2.6	4.3	1.3	4.8			
t_{PLH} t_{PHL}	Propagation Delay LE to Q	1.65	2.0	9.0	1.45	2.0	15.0	ns	C_L = 15 pF R_D = 1 MΩ S_1 = Open	Figures 1, 3
		1.8	2.0	6.0	9.6	2.0	10.0			
		2.5 ± 0.2	1.8	3.5	6.1	1.5	6.6			
		3.3 ± 0.3	1.3	2.6	4.4	1.0	4.8			
		5.0 ± 0.5	1.0	2.0	3.2	0.8	3.5			
		3.3 ± 0.3	1.5	3.3	5.3	1.5	6.2		C_L = 50 pF R_D = 500Ω, S_1 = Open	Figures 1, 4
		5.0 ± 0.5	1.3	2.6	4.2	1.2	4.6			
t_{PZL} t_{PZH}	Output Enable Time	1.65	2.0	9.0	13.5	2.0	14.6	ns	C_L = 50 pF, V_I = 2x V_{CC} R_U, R_D = 500Ω S1 = GND for t_{PZH} S1 = V_I for t_{PZL}	Figures 1, 4
		1.8	2.0	6.0	9.0	2.0	9.5			
		2.5 ± 0.2	2.0	3.7	6.0	1.8	6.6			
		3.3 ± 0.3	1.5	2.8	5.0	1.4	5.3			
		5.0 ± 0.5	1.0	2.2	3.7	1.0	3.9			
t_{PLZ} t_{PHZ}	Output Disable Time	1.65	2.0	7.7	12.0	2.0	13.0	ns	C_L = 50 pF, V_I = 2x V_{CC} R_U, R_D = 500Ω S_1 = GND for t_{PHZ} S_1 = V_I for t_{PLZ}	Figures 1, 4
		1.8	2.0	5.1	8.0	2.0	8.5			
		2.5 ± 0.2	2.0	3.5	6.0	1.8	6.3			
		3.3 ± 0.3	1.5	2.8	4.5	1.4	4.7			
		5.0 ± 0.5	1.0	2.3	3.7	1.0	3.9			
t_S	Setup Time, D to LE	2.5 ± 0.2			2.0			ns	C_L = 50 pF R_D = 500 Ω, S_1 = Open	Figures 1, 5
		3.3 ± 0.3			1.5					
		5.0 ± 0.5			1.5					
t_H	Hold Time, D to LE	2.5 ± 0.2			1.5			ns	C_L = 50 pF R_D = 500 Ω, S_1 = Open	Figures 1, 5
		3.3 ± 0.3			1.5					
		5.0 ± 0.5			1.5					
t_W	Pulse Width, LE	2.5 ± 0.2			3.0			ns	C_L = 50 pF R_D = 500 Ω, S_1 = Open	Figures 1, 5
		3.3 ± 0.3			3.0					
		5.0 ± 0.5			3.0					

Capacitance (Note 3)

| Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	3		pF	V_{CC} = Open, V_{IN} = 0V or V_{CC}
C_{OUT}	Output Capacitance	4		pF	V_{CC} = 3.3V, V_{IN} = 0V or V_{CC}
C_{PD}	Power Dissipation Capacitance (Note 4)	14		pF	V_{CC} = 3.3V
		17			V_{CC} = 5.0V

Note 3: T_A = +25C, f = 1 MHz.

Note 4: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2) C_{PD} is related to I_{CCD} dynamic operating current by the expression:
$I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}static)$.

AC Loading and Waveforms
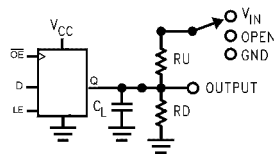
C_L includes load and stray capacitance

Input PRR = 1.0 MHz, t_w = 500 ns

FIGURE 1. AC Test Circuit
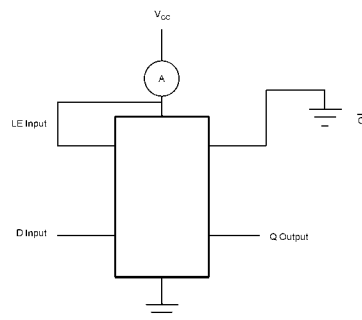
D Input = AC Waveform; $t_r = t_f$ = 1.8 ns;

D Input PRR = 10 MHz; Duty Cycle = 50%
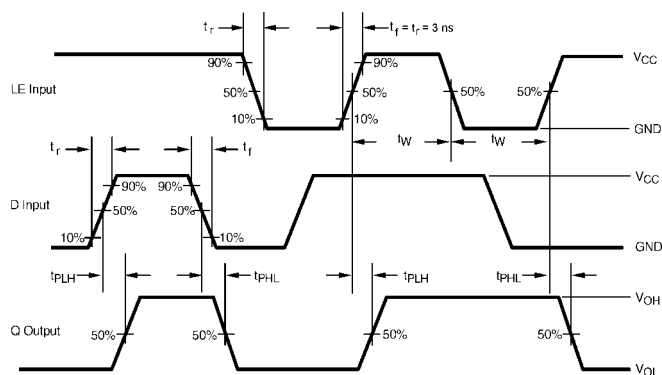
FIGURE 2. I_{CCD} Test Circuit
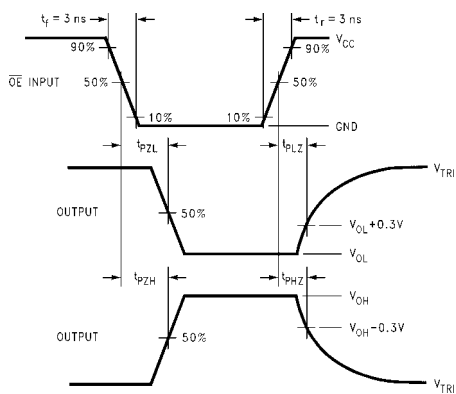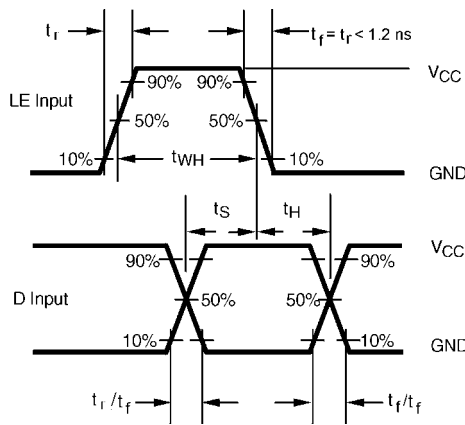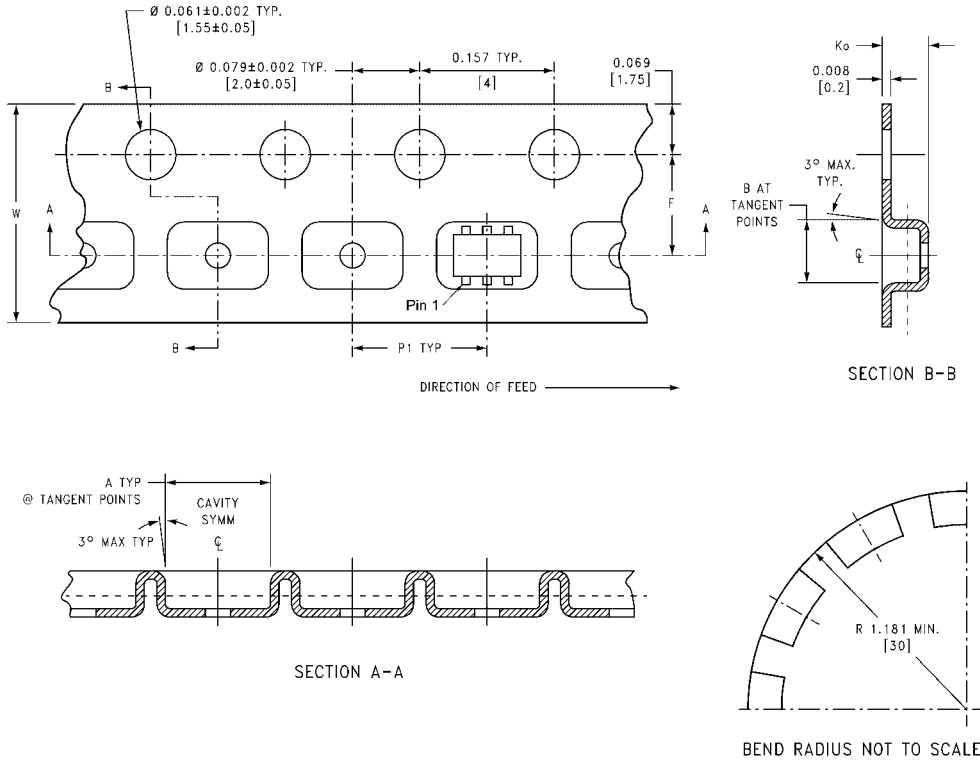

FIGURE 3. AC Waveforms

FIGURE 4. AC Waveforms

FIGURE 5. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for SC70

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
P6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

Package	Tape Size	DIM A	DIM B	DIM F	DIM K_o	DIM P1	DIM W
SC70-6	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)

Tape and Reel Specification (Continued)

TAPE FORMAT for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

SECTION B-B
SCALE:10X

SECTION A-A
SCALE:10X

REEL DIMENSIONS inches (millimeters)

DETAIL X

DETAIL X
SCALE: 3X
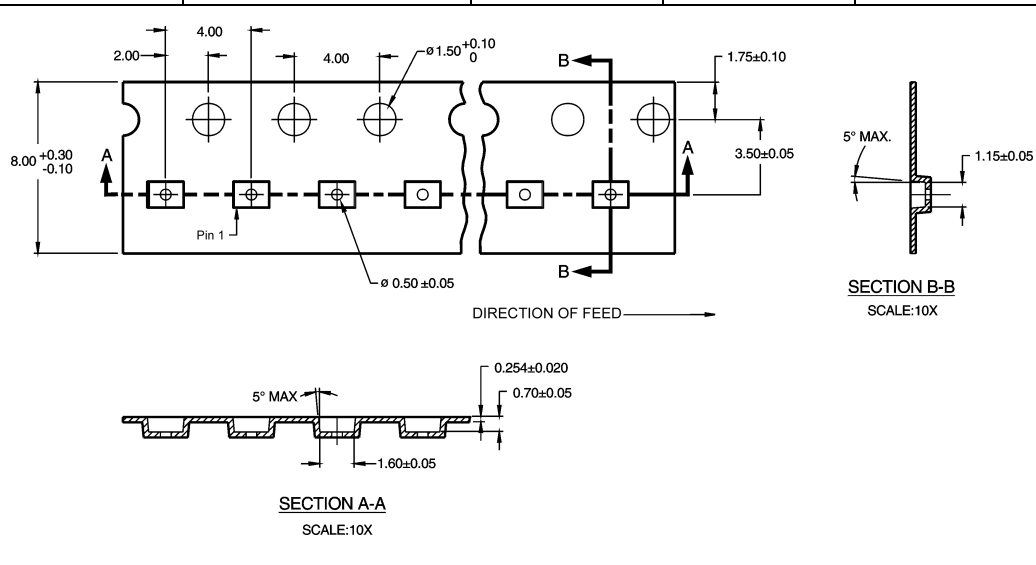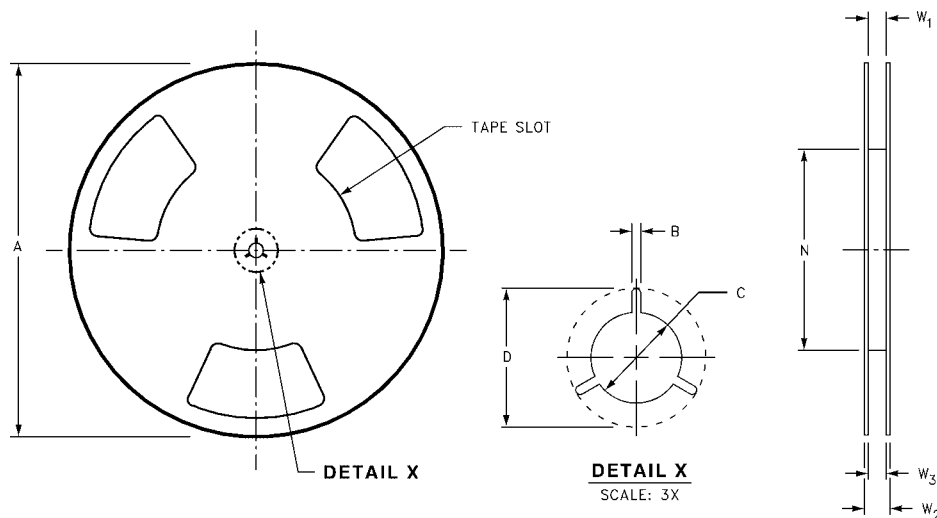
Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

Physical Dimensions inches (millimeters) unless otherwise noted

-A-
2.00±0.20

0.65

| 6 | 5 | 4 |
| 1 | 2 | 3 |

-B- 1.25±0.10   2.10±0.10

0.25   0.20 +0.10 −0.05

⊕ max 0.1 Ⓜ

0.9±.10   0.95±0.15

0.10 0.00

◁ max 0.1

0.65

.5 min

1.9

0.4 min

LAND PATTERN RECOMMENDATION

SEE DETAIL A

0.25 0.10

6.00°

R0.14

GAGE PLANE

R0.10

0°-30°

0.20

6.00°

0.45 0.10

0.425 NOMINAL

DETAIL A
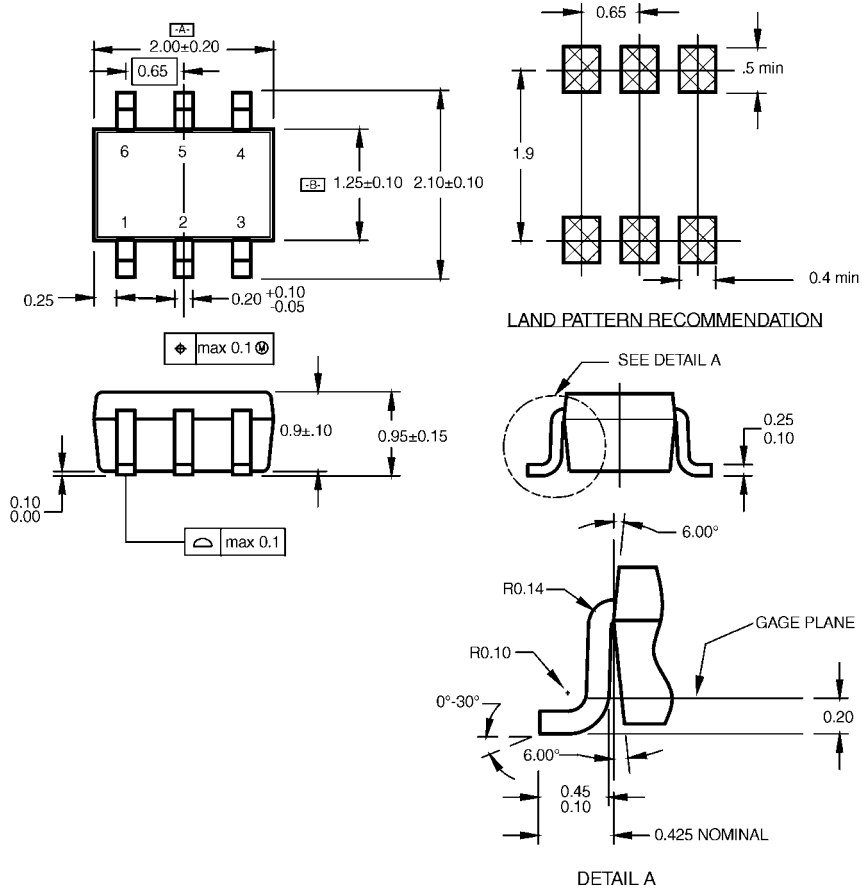
NOTES:
A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88.
B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
C. DIMENSIONS ARE IN MILLIMETERS.

MAA06ARevC

**6-Lead SC70, EIAJ SC88, 1.25mm Wide
Package Number MAA06A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

⌓ 0.10 C

B

1.45±0.05

6 5 4

1.00±0.05

1 2 3

A

TOP VIEW

RECOMMENDED
LAND PATTERN

1
0.5
0.75

5X 0.49

1X 0.52

6X 0.3

0.55 MAX

// 0.10 C

C

⊕ 0.15Ⓜ A BⓈ CⓈ

Detail A

1

0.15
0.25 6X

5X 0.35
    0.25

0.5

0.6 2X

(0.13)
4X

(0.05) 6X
0.4
0.3

0.075 X 45°
CHAMFER

DETAIL A
PIN 1 LEAD

BOTTOM VIEW
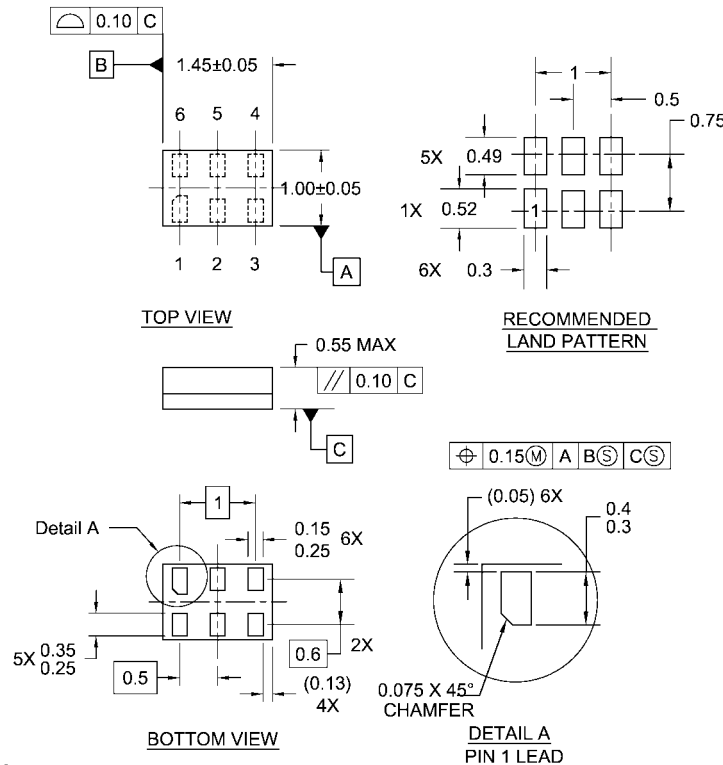
Notes:
1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

**6-Lead MicroPak, 1.0mm Wide
Package Number MAC06A**

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