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August 2011

NC7SZ74 TinyLogic[®] UHS D-Type, Flip-Flop with Preset and Clear

Features

- Ultra-High Speed: t_{PD} 2.6ns (Typical) into 50pF at 5V V_{CC}
- High Output Drive: ±24mA at 3V V_{CC}
- Broad V_{CC} Operating Range: 1.65V to 5.5V
- Power Down High-Impedance Inputs/Outputs
- Over-Voltage Tolerance Inputs Facilitate 5V to 3V Translation
- Proprietary Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak™ Package
- Space-Saving US8 Surface Mount Package

Description

The NC7SZ74 is a single, D-type, CMOS flip-flop with preset and clear from Fairchild's ultra high-speed series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive, while maintaining low static power dissipation over a very broad $V_{\rm CC}$ operating range of 1.65V to 5.5V $V_{\rm CC}$. The inputs and outputs are high impedance when $V_{\rm CC}$ is 0V. Inputs tolerate voltages up to 7V, independent of $V_{\rm CC}$ operating voltage.

The signal level applied to the D input is transferred to the Q output during the positive-going transition of the CLK pulse.

Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7SZ74K8X	SZ74	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide-	3000 Units on Tape & Reel
NC7SZ74L8X	N9	8-Lead MicroPak, 1.6 mm Wide	5000 Units on Tape & Reel

Connection Diagrams

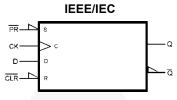
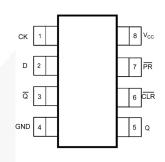


Figure 1. Logic Symbol

Pin Configurations





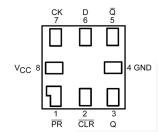


Figure 3. MicroPak™ (Top Through View)

Pin Definitions

Pin # US8	Pin # MicroPak	Name	Description
1	7	CK	Clock Pulse Input
2	6	D	Data Input
3	5	/Q	Flip-Flop Output
4	4	GND	Ground
5	3	Q	Flip-Flop Output
6	2	/CLR	Direct Clear Input
7	1	/PR	Direct Preset Input
8	8	V _{CC}	Supply Voltage

Function Table

	Inp	uts		Out	Function	
/CLR	/PR	D	СК	Q	/Q	Function
L	Н	Х	Х	L	Н	Clear
Н	L	X	Х	Н	L	Preset
L	L	X	Х	Н	Н	
Н	Н	L	1	L	Н	
Н	Н	Н	↑	Н	L	
Н	Н	X	\	Qn	/Q _n	No Change

H = HIGH Logic Level

Qn = No change in data

X = Immaterial

↓= Falling Edge

L = LOW Logic Level

Z = High Impedance

↑ = Rising Edge

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Pai	Parameter			
V _{CC}	Supply Voltage		-0.5	7.0	V
V _{IN}	DC Input Voltage		-0.5	7.0	V
V _{OUT}	DC Output Voltage		-0.5	7.0	V
I _{IK}	DC Input Diode Current	V _{IN} < 0V		-50	mA
I _{OK}	DC Output Diode Current	V _{OUT} < 0V		-50	mA
I _{OUT}	DC Output Source/Sink Curre	DC Output Source/Sink Current			
I _{CC} or I _{GND}	DC V _{CC} or Ground Current			±50	mA
T _{STG}	Storage Temperature Range		-65	+150	°C
TJ	Junction Temperature Under I	Bias		+150	°C
TL	Junction Lead Temperature (S	Soldering, 10 Seconds)		+260	°C
P_D	Power Dissipation at +85°C		250	mW	
ECD	Human Body Model, JEDEC:	Human Body Model, JEDEC:JESD22-A114			
ESD	Charge Device Model: JEDEC	:JESD22-C101		2000	V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit	
\/	Supply Voltage Operating		1.65	5.50	V	
V _{CC}	Supply Voltage Data Retention		1.50	5.50	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	
V_{IN}	Input Voltage		0	5.5	V	
\/	Output Valtage	Active State	0	V _{CC}	V	
V_{OUT}	Output Voltage	3-State	0	5.5		
		V _{CC} =1.8V, 2.5V ± 0.2V	0	20		
t_r , t_f	Input Rise and Fall Times	V _{CC} =3.3V ± 0.3V	0	10	ns/V	
		V _{CC} =5.0V ± 0.5V	0	5		
T _A	Operating Temperature		-40	+85	°C	
0	The word Desistance	US8	4.5	250	°C/M	
$ heta_{\sf JA}$	Thermal Resistance	MicroPak™-8		280	°C/W	

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

		.,		T,	_A =+25°	°C	T _A =-40			
Symbol	Parameter	V _{cc}	Conditions	Min.	Тур.	Max.	Min.	Max.	Units	
.,	HIGH Level Control	1.65 to 1.95		0.75V _{CC}			0.75V _{CC}		.,	
V_{IH}	Input Voltage	2.30 to 5.50		0.70V _{CC}			0.70V _{CC}		V	
	LOW Level Control	1.65 to 1.95				0.25V _{CC}		0.25V _{CC}	V	
V_{IL}	Input Voltage	2.30 to 5.50				0.30V _{CC}		0.30V _{CC}	V	
		1.65		1.55	1.65		1.55			
		2.30	V _{IN} =V _{IH} ,	2.20	2.30		2.20			
		3.00	I _{OH} =-100μA	2.90	3.00		2.90			
		4.50		4.40	4.50		4.40			
V_{OH}	HIGH Level Output Voltage	1.65	I _{OH} =-4mA	1.29	1.52		1.29		V	
	Voltago	2.30	I _{OH} =-8mA	1.90	2.15		1.90			
		3.00	I _{OH} =-16mA	2.40	2.80		2.40			
		3.00	I _{OH} =-24mA	2.30	2.68		2.30			
		4.50	I _{OH} =-32mA	3.80	4.20		3.80			
		1.65				0.10		0.10		
		2.30	V _{IN} =V _{IH} ,			0.10		0.10		
		3.00	I _{OL} =100μA			0.10		0.10		
		4.50				0.10		0.10		
V_{OL}	LOW Level Control Output Voltage	1.65	I _{OL} =4mA		0.80	0.24		0.24	V	
	output voitage	2.30	I _{OL} =8mA		0.10	0.30		0.30		
		3.00	I _{OL} =16mA		0.15	0.40		0.40		
		3.00	I _{OL} =24mA		0.22	0.55		0.55		
		4.50	I _{OL} =32mA		0.22	0.55		0.55		
I _{IN}	Input Leakage Current	0 to 5.5	$0 \leq V_{IN} \leq 5.5V$			±0.1		±1.0	μΑ	
I _{OFF}	Power Off Leakage Current	0	V _{IN} or V _{OUT} =5.5V			1		10	μΑ	
I _{cc}	Quiescent Supply Current	1.65 to 5.50	V _{IN} =5.5V, GND			1		10	μΑ	

AC Electrical Characteristics

Symbol	Parameter	V CC	V _{cc} Conditions	T _A =+25°C		T _A =-40 to +85°C		Units	Eiguro	
			Conditions	Min.	Тур.	Max.	Min.	Max.	Units	Figure
		1.80 ± 0.15		75			75			
		2.50 ± 0.20	C _L =15pF	150			150			
f _{MAX} Maximum Clock Frequency	3.30 ± 0.30	$R_D=1M\Omega$ $S_1=Open$	200			200			Figure 4	
	5.00 ± 0.50		250			250			Figure 8	
		3.30 ± 0.50	C _L =50pF	175			175			
		5.00 ± 0.50	R_D =500Ω, S_1 =Open	200			200			
		1.80 ± 0.15	·	2.5	6.5	12.5	2.5	13.0		
		2.50 ± 0.20	C _L =15pF,	1.5	3.8	7.5	1.5	8.0	1	
	Propagation Dolay	3.30 ± 0.30	$R_D=1M\Omega$ $S_1=Open$	1.0	2.8	6.5	1.0	7.0	1	Figure 4
$t_{\text{PLH}},t_{\text{PHL}}$	Propagation Delay CK to Q, /Q	5.00 ± 0.50	. О1-Орсп	0.8	2.2	4.5	0.8	5.0	ns	Figure 4
	2,112	3.30 ± 0.30	C _L =50pF	1.0	3.4	7.0	1.0	7.5		l iguio o
		5.00 ± 0.50	$R_D=500\Omega$, $S_1=Open$	Ω , 10 26 50 10 55						
		1.80 ± 0.15	от-орен	2.5	6.5	14.0	2.5	14.5		
		2.50 ± 0.20	C _L =15pF,	1.5	3.8	9.0	1.5	9.5		
- A			$R_L=1M\Omega$	1.0	2.8	6.5	1.0	7.0		F:
t _{PLH} , t _{PHL}	Propagation Delay /CLR, /PR to Q, /Q	5.00 ± 0.50	S₁=Open	0.8	2.2	5.0	0.8	5.5	ns	Figure 4 Figure 6
	TOER, IT IT IS Q, TQ	3.30 ± 0.30	C _L =50pF,	1.0	3.4	7.0	1.0	7.5		i igule o
		5.00± 0.50	R _D =500Ω∋ S₁=Open	1.0	2.6	5.0	1.0	5.5	Í	
	t _S Setup Time CK to D	1.80 ± 0.15	от орон	6.5			6.5			
		2.50 ± 0.20	C _L =15pF,	3.5			3.5		İ	
ts		3.30 ± 0.30	R _L =1MΩ S₁=Open	2.0			2.0		1	F: 4
		5.00 ± 0.50	. 3₁–Open	1.5			1.5		ns	Figure 4 Figure 7
		3.30 ± 0.30 C _L =50pF	C _L =50pF,	2.0			2.0			riguic r
		5.00± 0.50	$R_D=500\Omega$ 3 S ₁ =Open	1.5			1.5			
		1.80 ± 0.15	от-орен	0.5			0.5			
		2.50 ± 0.20	C _L =15pF,	0.5			0.5		†	
		3.30 ± 0.30	R _L =1MΩ	0.5			0.5		1	
t _H	Hold Time, CK to D	5.00 ± 0.50	S₁=Open	0.5			0.5		ns	Figure 4 Figure 7
		3.30 ± 0.30	C ₁ =50pF,	0.5			0.5			i igule /
		5.00± 0.50	$R_D=500\Omega$ 3 S ₁ =Open	0.5			0.5		1	
		1.80 ± 0.15	31-Ореп	6.0			6.0			
		2.50 ± 0.20	C _L =15pF,	4.0			4.0			
		3.30 ± 0.30	$R_L=1M\Omega$	3.0			3.0			
t_{W}	Pulse Width, CK, /PR, /CLR	5.00 ± 0.50	S₁=Open	2.0			2.0		ns	Figure 4 Figure 8
	III, IOLIK	3.30 ± 0.30	C ₁ =50pF,	3.0			3.0			rigule o
		5.00± 0.50	R _D =500Ωэ	2.0			2.0			
		1.80 ± 0.15	S₁=Open	8.0			8.0			
		2.50 ± 0.20	C _L =15pF,	4.5			4.5			
		3.30 ± 0.30	$R_L=1M\Omega$	3.0			3.0			
t _{REC}	Recover Time /CLR, /PR to CK	5.00 ± 0.50	S₁=Open	3.0			3.0	ns	ns	Figure 4
-	I /PK to UK	3.30 ± 0.30	C ₁ =50pF,	3.0			3.0		-	Figure 7
	$3.30 \pm 0.$ $5.00 \pm 0.$	J.00 ± 0.00	R _D =500Ω∋	3.0			3.0		1	

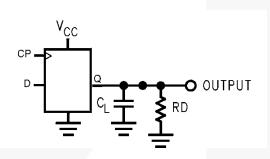
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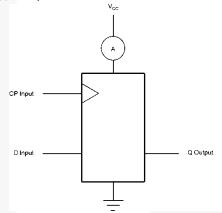
AC Electrical Characteristics

Symbol	Parameter	V	V _{CC} Conditions T _A =+25°C		T _A =-40 to +85°C		Units	Figure		
Syllibol	Parameter	V _{cc}	Conditions	Min.	Тур.	Min.	Тур.	Min.	Units	rigule
C _{IN}	Input Capacitance	0			3				pF	
C _{OUT}	Output Capacitance	0			4				pF	
	Power Dissipation	3.30			10				, F	
	Capacitance ⁽²⁾	5.00			12				pF	

Note:

2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD}=(C_{PD})(V_{CC})(f_{IN})+(I_{CC}static).





Note:

3. C_L includes load and stray capacitance. Input PRR=1.0MHz t_w =500ns.

Figure 4. AC Test Circuit

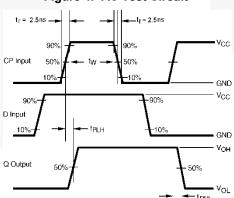


Figure 6. AC Waveforms

Notes:

- 4. CP input=AC Waveforms t_r=t_f=2.5ns.
- 5. CP input PRR=10MHz; Duty Cycle=50%.
- 6. D input PRR=5MHz; Duty Cycle=50%.

Figure 5. ICCD Test Circuit

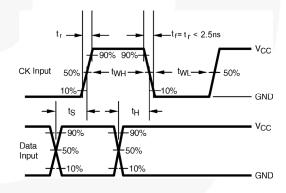


Figure 7. AC Waveforms

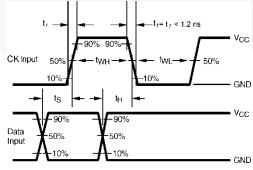
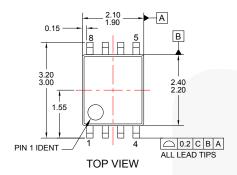
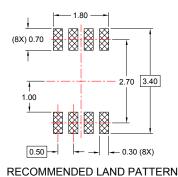
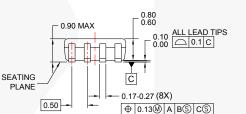


Figure 8. AC Waveforms

Physical Dimensions



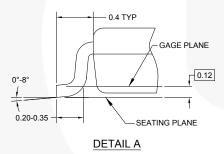




SIDE VIEW

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-187
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1994.
- E. FILE DRAWING NAME: MKT-MAB08Arev4



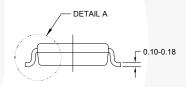


Figure 9. 8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide

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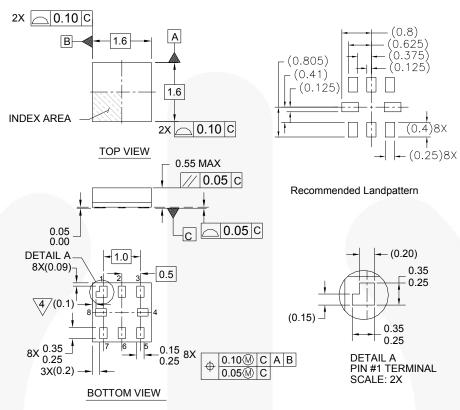
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Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/products/analog/pdf/sc70-5 tr.pdf.

Package Des	signator	Tape Section	Tape Section Cavity Number		Cover Type Status
	Leader (Start End)		125 (Typical)	Empty	Sealed
K8X		Carrier	3000	Filled	Sealed
		Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions



Notes:

- 1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
- 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y.14M-1994
- 4/PIN 1 FLAG, END OF PACKAGE OFFSET
- 5. DRAWING FILE NAME: MKT-MAC08AREV4

MAC08AREV4

Figure 10.8-Lead, MicroPak™, 1.6mm Wide

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Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf.

Package Designator	Tape Section	Tape Section Cavity Number		Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
L8X	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed





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Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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