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NCL30001

High-Efficiency Single Stage Power Factor Correction and Step-Down Offline LED Driver

The NCL30001 is a highly integrated controller for implementing power factor correction (PFC) and isolated step down ac−dc power conversion in a single stage, resulting in a lower cost and reduced part count solution. This controller is ideal for LED Driver power supplies with power requirements between 40 W and 150 W. The single stage is based on the flyback converter and it is designed to operate in continuous conduction (CCM).

The NCL30001 can be configured as as constant current driver or a fixed output driver for two stage LED lighting applications. In addition, the controller features a proprietary Soft−Skip™ to reduce acoustic noise at light loads. Other features found in the NCL30001 include a high voltage startup circuit, voltage feedforward, brown out detector, internal overload timer, latch input and a high accuracy multiplier. The multi−function latch off pin can also be used to implement an overtemperature shutdown circuit.

Features

- Voltage Feedforward Improves Loop Response
- Frequency Jittering Reduces EMI Signature
- Proprietary Soft−Skip at Light Loads Reduces Acoustic Noise
- Brown Out Detector
- Internal 160 ms Fault Timer
- Independent Latch−Off Input Facilitates Implementation of Overvoltage and Overtemperature Fault Detectors
- Average Current Mode Control (ACMC), Fixed Frequency Operation
- High Accuracy Multiplier Reduces Input Line Harmonics
- Adjustable Operating Frequency from 20 kHz to 250 kHz
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- LED Street Lights
- Low Bay LED Lighting
- High Power LED Drivers
- Architectural LED Lighting

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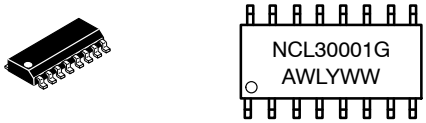
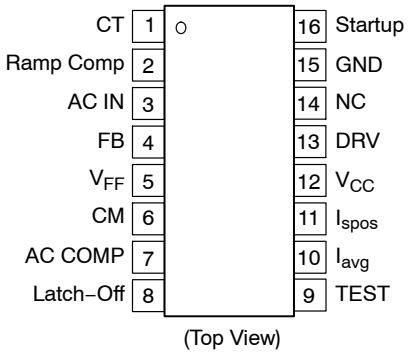
MARKING DIAGRAM



SOIC−16
D SUFFIX
CASE 751B

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 30 of this data sheet.

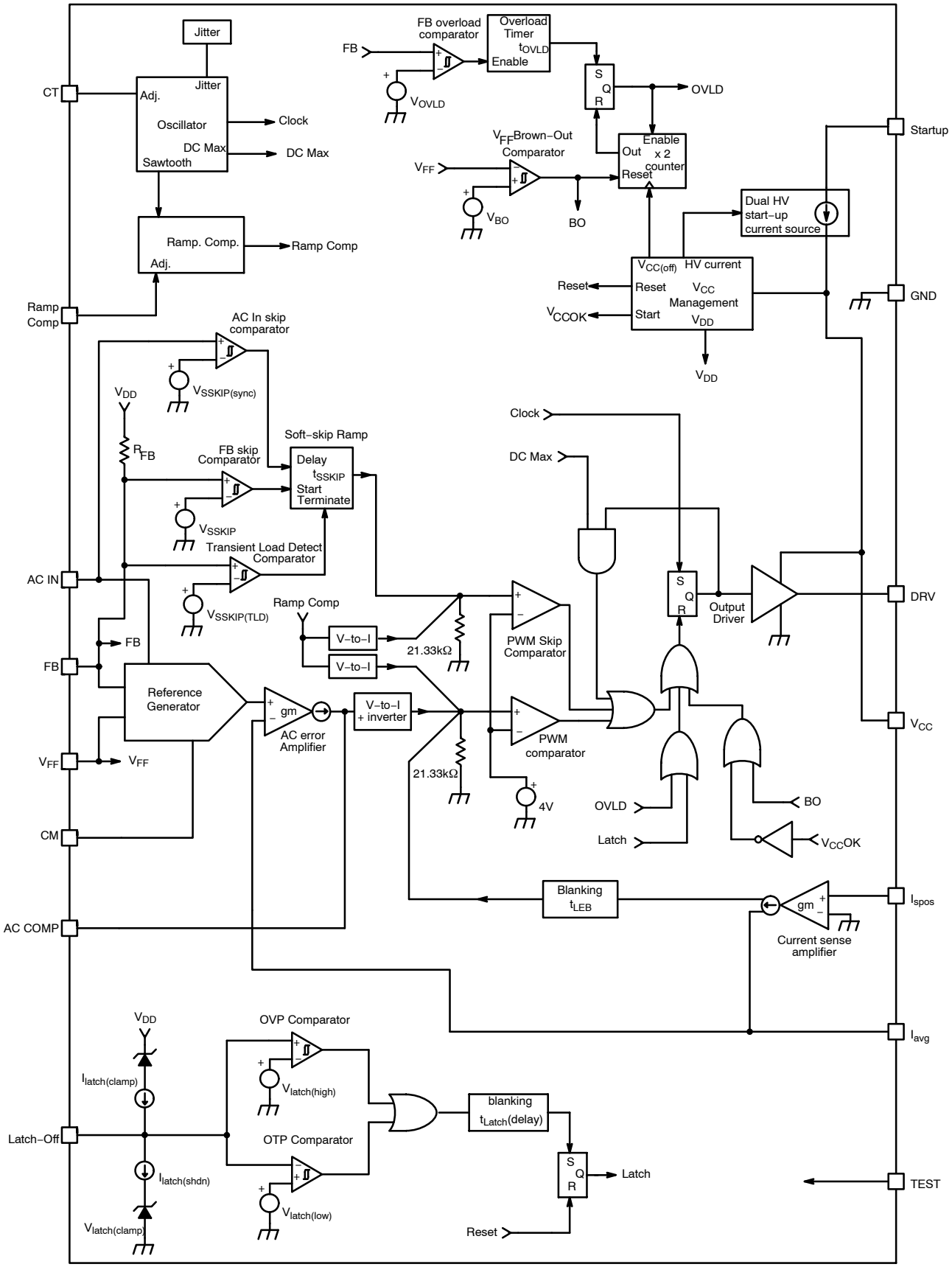


Figure 1. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	C_T	An external timing capacitor (C_T) sets the oscillator frequency. A sawtooth between 0.2 V and 4 V sets the oscillator frequency and the gain of the multiplier.
2	RAMP COMP	A resistor (R_{RC}) between this pin and ground adjust the amount of ramp compensation that is added to the current signal. Ramp compensation is required to prevent subharmonic oscillations. This pin should not be left open.
3	AC IN	The scaled version of the full wave rectified input ac wave is connected to this pin by means of a resistive voltage divider. The line voltage information is used by the multiplier.
4	FB	An error signal from an external error amplifier circuit is fed to this pin via an optocoupler or other isolation circuit. The FB voltage is a proportional of the load of the converter. If the voltage on the FB pin drops below 0.41 V (typical) the controller enters Soft−Skip to reduce acoustic noise.
5	VFF	Feedforward input. A scaled version of the filtered rectified line voltage is applied by means of a resistive divider and an averaging capacitor. The information is used by the Reference Generator to regulate the controller.
6	CM	Multiplier output. A capacitor is connected between this pin and ground to filter the modulated output of the multiplier.
7	AC COMP	Sets the pole for the ac reference amplifier. The reference amplifier compares the low frequency component of the input current to the ac reference signal. The response must be slow enough to filter out most of the high frequency content of the current signal that is injected from the current sense amplifier, but fast enough to cause minimal distortion to the line frequency information. The pin should not be left open.
8	Latch	Latch−Off input. Pulling this pin below 1.0 V (typical) or pulling it above 7.0 V (typical) latches the controller. This input can be used to implement an overvoltage detector, an overtemperature detector or both. Refer to Figure 60 for a typical implementation.
9	TEST	This pin is a TEST pin. A nominal 50K $\pm$10% resistor must be connected to GND for proper operation.
10	I_{AVG}	An external resistor and capacitor connected from this terminal to ground, to set and stabilizes the gain of the current sense amplifier output that drives the ac error amplifier.
11	I_{Spos}	Positive current sense input. Connects to the positive side of the current sense resistor.
12	V_{CC}	Positive input supply. This pin connects to an external capacitor for energy storage. An internal current source supplies current from the STARTUP pin V_{CC}. Once the voltage on V_{CC} reaches approximately 15.3 V, the current source turns off and the outputs are enabled. The drivers are disabled once V_{CC} reaches approximately 10.2 V. If V_{CC} drops below 0.83 V (typical), the startup current is reduced to less than 500 μA.
13	DRV	Drive output for the main flyback power MOSFET or IGBT. DRV has a source resistance of 10.8 Ω (typical) and a sink resistance of 8 Ω (typical).
14	NC	No Connect
15	GND	Ground reference for the circuit.
16	HV	Connect the rectified input line voltage directly to this pin to enable the internal startup regulator. A constant current source supplies current from this pin to the capacitor connected to the V_{CC} pin, eliminating the need for a startup resistor. The charge current is typically 5.5 mA. Maximum input voltage is 500 V.

MAXIMUM RATINGS (Notes 1 and 2)

Rating	Symbol	Value	Unit
Start_up Input Voltage Start_up Input Current	V_{HV} I_{HV}	−0.3 to 500 ±100	V mA
Power Supply Input Voltage Power Supply Input Current	V_{CC} I_{CC}	−0.3 to 20 ±100	V mA
Latch Input Voltage Latch Input Current	V_{Latch} I_{Latch}	−0.3 to 10 ±100	V mA
All Other Pins Voltage All Other Pins Current		−0.3 to 6.5 ±100	V mA
Thermal Resistance, Junction−to−Air 0.1 in" Copper 0.5 in" Copper	θ_{JA}	 130 110	°C/W
Thermal Resistance, Junction−to−Lead	$R_{\Theta JL}$	50	°C/W
Maximum Power Dissipation @ T_A = 25°C	P_{MAX}	0.77	W
Operating Temperature Range	T_J	−40 to 125	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains ESD protection and exceeds the following tests:
   Pin 1−15: Human Body Model 2000 V per JEDEC Standard JESD22, Method A114E.
   Machine Model Method 200 V per JEDEC Standard JESD22, Method A114A.
   Pin 16 is the high voltage startup of the device and is rated to the maximum rating of the part, 500 V.
2. This device contains Latchup protection and exceeds ±100 mA per JEDEC Standard JESD78.

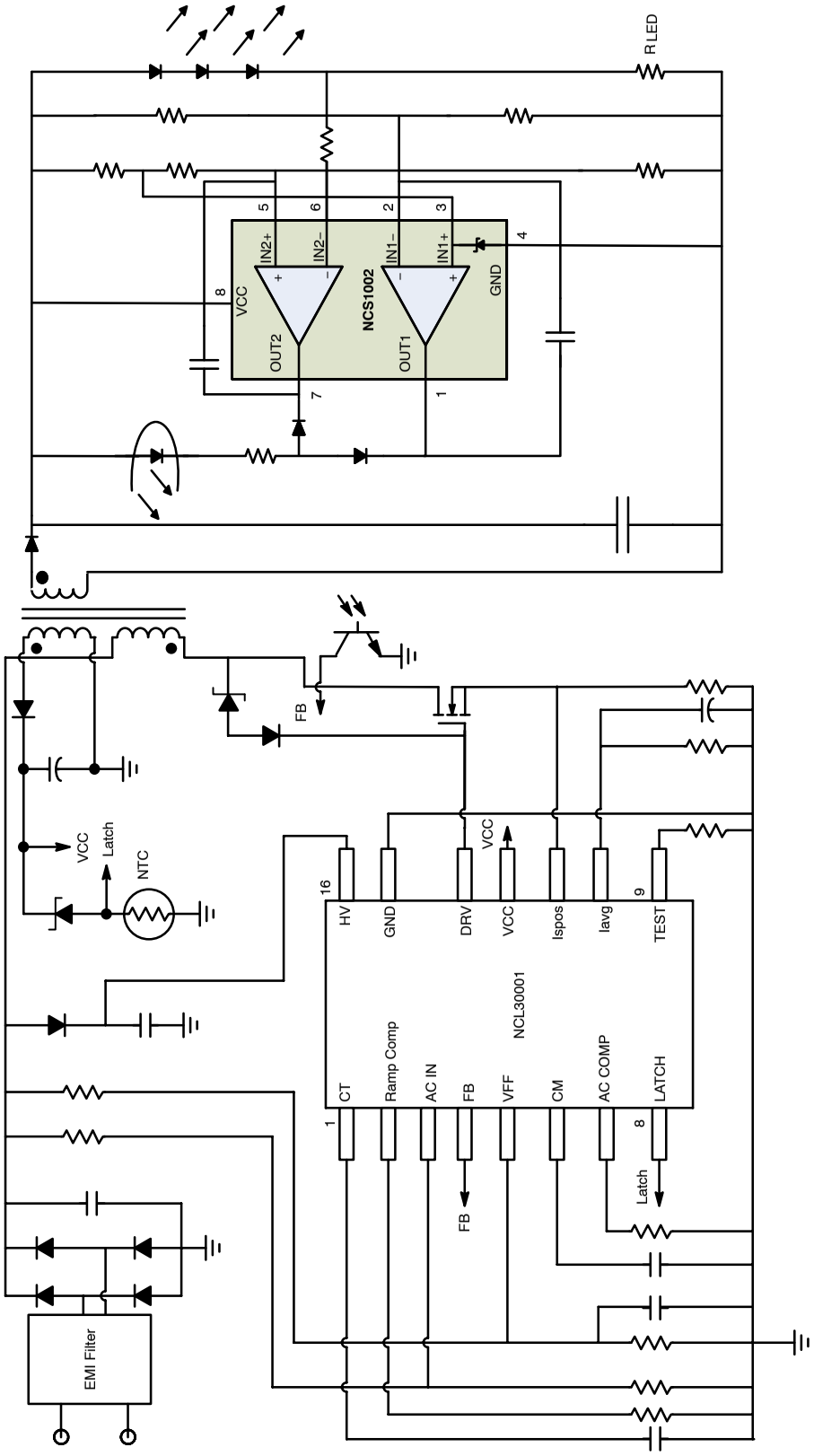


Figure 2. Typical Application Schematic

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, $V_{AC\ IN}$ = 3.8 V, V_{FB} = 2.0 V, V_{FF} = 2.4 V, V_{Latch} = open, V_{ISPOS} = −100 mV, C_{DRV} = 1 nF, C_T = 470 pF, C_{IAVG} = 0.27 nF, C_{Latch} = 0.1 nF, C_M = 10 nF, R_{IAVG} = 76.8 kΩ, R_{TEST} = 50 kΩ, R_{RC} = 43 kΩ, For typical Value T_J = 25°C, for min/max values T_J = −40°C to 125°C, unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
OSCILLATOR						
Frequency		f_{osc}	90	100	110	kHz
Frequency Modulation in Percentage of f_{OSC}			–	6.8	–	%
Frequency Modulation Period			–	6.8	–	ms
Ramp Peak Voltage		$V_{CT(peak)}$	–	4.0	–	V
Ramp Valley Voltage		$V_{CT(valley)}$	–	0.10	–	V
Maximum Duty Ratio	R_{TEST} = open	D	94	–	–	%
Ramp Compensation Peak Voltage		$V_{RCOMP(peak)}$	–	4	–	V
AC ERROR AMPLIFIER						
Input Offset Voltage (Note 3)	Ramp I_{AVG}, V_{FB} = 0 V	ACV_{IO}		40	–	mV
Error Amplifier Transconductance		g_m	–	100	–	μS
Source Current	$V_{AC\ COMP}$ = 2.0 V, $V_{AC\ IN}$ = 2.0 V, V_{FF} = 1.0 V	$I_{EA(source)}$	25	70	–	μA
Sink Current	$V_{AC\ COMP}$ = 2.0 V, V_{AC_IN} = 2.0 V, V_{FF} = 5.0 V	$I_{EA(sink)}$	−25	−70	–	μA
CURRENT AMPLIFIER						
Input Bias Current	V_{ISPOS} = 0 V	CAI_{bias}	40	53	80	μA
Input Offset Voltage	$V_{AC\ COMP}$ = 5.0 V, V_{ISpos} = 0 V	CAV_{IO}	−20	0	20	mV
Current Limit Threshold	force DRV high, $V_{AC\ COMP}$ = 3.0 V, ramp V_{ISPOS}, V_{Ramp_Comp} = open	V_{ILIM}	0.695	0.74	0.77	V
Leading Edge Blanking Duration		t_{LEB}	–	200	–	ns
Bandwidth			–	1.5	–	MHz
PWM Output Voltage Gain	$PWMk = \frac{4}{(V_{ILIM} - C_{AVIO})}$	PWMk	4.0	5.3	6.0	V/V
Current Limit Voltage Gain (See Current Sense Section)	$ISVK = \frac{V_{(AVG)}}{VI_{SPOS}}$	ISVk	15.4	18.5	23	V/V
REFERENCE GENERATOR						
Reference Generator Gain	$k = \frac{V_{AC\_REF} \cdot V_{FF}^{\ 2}}{V_{FB} \cdot V_{AC\_IN}}$	k	–	0.55	–	V
Reference Generator output voltage (low input ac line and full load)	$V_{AC\ IN}$ = 1.2 V, V_{FF} = 0.765 V, V_{FB} = 4 V	RG_{out1}	3.61	4.36	4.94	Vpk
Reference Generator output voltage (high input ac line and full load)	$V_{AC\ IN}$ = 3.75 V, V_{FF} = 2.39 V, V_{FB} = 4.0 V	RG_{out2}	1.16	1.35	1.61	Vpk
Reference Generator output Voltage (low input as line and minimum load)	$V_{AC\ IN}$ = 1.2 V, V_{FF} = 0.765 V, V_{FB} = 2.0 V	RG_{out3}	1.85	2.18	2.58	Vpk
Reference Generator output voltage (high input ac line and minimum load)	$V_{AC\ IN}$ = 3.75 V, V_{FF} = 2.39 V, V_{FB} = 2.0 V	RG_{out4}	0.55	0.65	0.78	Vpk
Reference Generator output offset voltage		RG_{offset}	−100	–	100	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by Design

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, $V_{AC\ IN}$ = 3.8 V, V_{FB} = 2.0 V, V_{FF} = 2.4 V, V_{Latch} = open, V_{ISPOS} = −100 mV, C_{DRV} = 1 nF, C_T = 470 pF, C_{IAVG} = 0.27 nF, C_{Latch} = 0.1 nF, C_M = 10 nF, R_{IAVG} = 76.8 kΩ, R_{TEST} = 50 kΩ, R_{RC} = 43 kΩ, For typical Value T_J = 25°C, for min/max values T_J = −40°C to 125°C, unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
AC INPUT						
Input Bias Current Into Reference Multiplier & Current Compensation Amplifier		$I_{AC\ IN(IB)}$	–	0.01	–	μA
DRIVE OUTPUT						
Drive Resistance (Thermally Limited) DRV Sink DRV Source	 V_{DRV} = 1 V I_{DRV} = 100 mA	 R_{SNK} R_{SRC}	 – –	 8 10.8	 18 24	Ω
Rise Time (10% to 90%) DRV		t_r	–	40	–	ns
Fall Time (90% to 10%) DRV		t_f	–	20	–	ns
Driver Out Low Voltage DRV	I_{DRV} = 100 μA	$V_{DRV(low)}$	–	1.0	100	mV
Soft−Skip						
Skip Synchronization to ac Line Voltage Threshold	V_{ACIN} Increasing, V_{FB} = 1.5 V	$V_{SSKIP(SYNC)}$	210	267	325	mV
Skip Synchronization to ac Line Voltage Threshold Hysteresis	V_{ACIN} Decreasing	$V_{SSKIP\ (SYNCHYS)}$	–	40	–	mV
Skip Ramp Period (Note 3)		t_{SSKIP}	–	2.5	–	ms
Skip Voltage Threshold		V_{SSKIP}	360	410	460	V
Skip Voltage Hysteresis		$V_{SSKIP(HYS)}$	45	90	140	mV
Skip Transient Load Detect Threshold (Note 3)		$V_{SSKIP(TLD)}$	–	1.75	–	V
FEEDBACK INPUT						
Pull−Up Current Source	V_{FB} = 0.5 V	I_{FB}	600	750	920	μA
Pull−Up Resistor		R_{FB}	–	6.7	–	kΩ
Open Circuit Voltage		$V_{FB(open)}$	5.3	5.7	6.3	V
STARTUP AND SUPPLY CIRCUITS						
Supply Voltage Startup Threshold Minimum Operating Voltage Logic Reset Voltage	 V_{CC} Increasing V_{CC} Decreasing V_{CC} Decreasing	 $V_{CC(on)}$ $V_{CC(off)}$ $V_{CC(reset)}$	 14.3 9.3 –	 15.4 10.2 7.0	 16.3 11.3 –	V
Inhibit Threshold Voltage	V_{HV} = 40 V, $I_{inhibit}$ = 500 μA	$V_{inhibit}$	–	0.83	1.15	V
Inhibit Bias Current	V_{HV} = 40 V, V_{CC} = 0.8 * $V_{inhibit}$	$I_{inhibit}$	40	-	500	μA
Minimum Startup Voltage	I_{start} = 0.5 mA, V_{CC} = $V_{CC(on)}$ − 0.5 V	$V_{start(min)}$	–	–	40	V
Startup Current	V_{CC} = $V_{CC(on)}$ − 0.5 V, V_{FB} = Open	I_{start}	3.0	5.62	8.0	mA
Off−State Leakage Current	V_{HV} = 400 V, T_J = 25°C T_J = −40°C to 125°C	$I_{HV(off)}$	 – –	 17 15	 40 80	μA
Supply Current Device Disabled (Overload) Device Switching	 V_{FB} = Open f_{OSC} ≈ 100 kHz	 I_{CC1} I_{CC2}	 – –	 0.72 6.25	 1.2 7.2	mA
FAULT PROTECTION						
Overload Timer		t_{OVLD}	120	160	360	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by Design

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, $V_{AC\ IN}$ = 3.8 V, V_{FB} = 2.0 V, V_{FF} = 2.4 V, V_{Latch} = open, V_{ISPOS} = −100 mV, C_{DRV} = 1 nF, C_T = 470 pF, C_{IAVG} = 0.27 nF, C_{Latch} = 0.1 nF, C_M = 10 nF, R_{IAVG} = 76.8 kΩ, R_{TEST} = 50 kΩ, R_{RC} = 43 kΩ, For typical Value T_J = 25°C, for min/max values T_J = −40°C to 125°C, unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
FAULT PROTECTION						
Overload Detect Threshold		V_{OVLD}	4.7	4.9	5.2	V
Brown−Out Detect Threshold (entering fault mode)	V_{FF} Decreasing, V_{FB} = 2.5 V, $V_{AC\ IN}$ = 2.0 V	$V_{BO(low)}$	0.41	0.45	0.49	V
Brown−Out Exit Threshold (exiting fault mode)	V_{FF} Increasing, V_{FB} = 2.5 V, $V_{AC\ IN}$ = 2.0 V	$V_{BO(high)}$	0.57	0.63	0.69	V
Brown−Out Hysteresis		$V_{BO(HYS)}$	–	174	–	mV
LATCH INPUT						
Pull−Down Latch Voltage Threshold	V_{Latch} Decreasing	$V_{latch(low)}$	0.9	0.98	1.1	V
Pull−Up Latch Voltage Threshold	V_{Latch} Increasing	$V_{latch(high)}$	5.6	7.0	8.4	V
Latch Propagation Delay	V_{Latch} = $V_{latch(high)}$	$t_{latch(delay)}$	30	56	90	μs
Latch Clamp Current (Going Out)	V_{Latch} = 1.5 V	$I_{latch(clamp)}$	42	51	58	μA
Latch Clamp Voltage (I_{Latch} Going In)	I_{Latch} = 50 μA	$V_{latch(clamp)}$	2.5	3.27	4.5	V
Latch−Off Current Shutdown (Going In)	V_{Latch} Increasing	$I_{latch(shdn)}$	–	95	–	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by Design

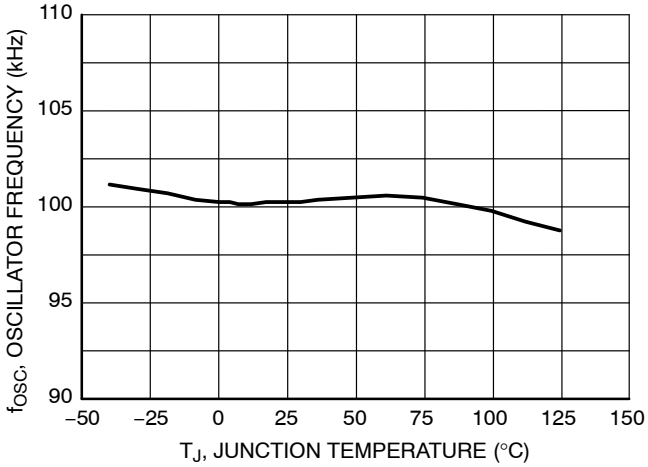


Figure 3. Oscillator Frequency (f_{OSC}) vs. Junction Temperature

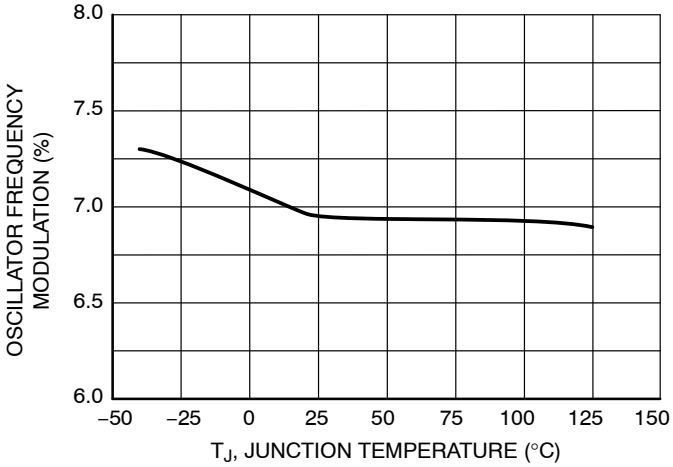


Figure 4. Oscillator Frequency Modulation in Percentage of f_{OSC} vs. Junction Temperature

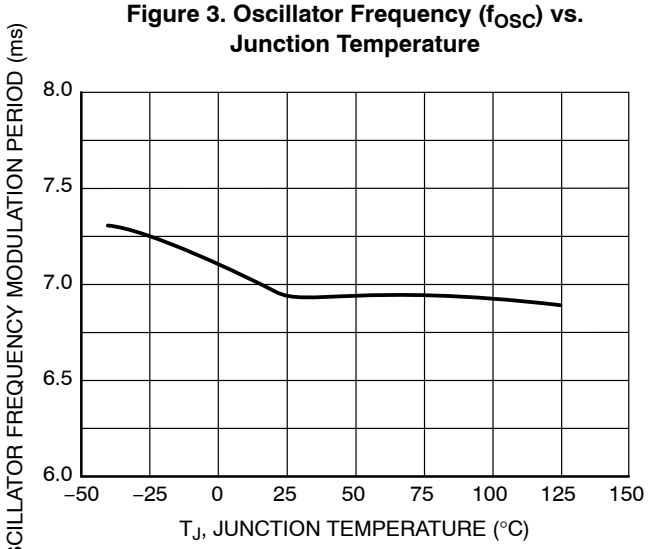


Figure 5. Oscillator Frequency Modulation Period vs. Junction Temperature

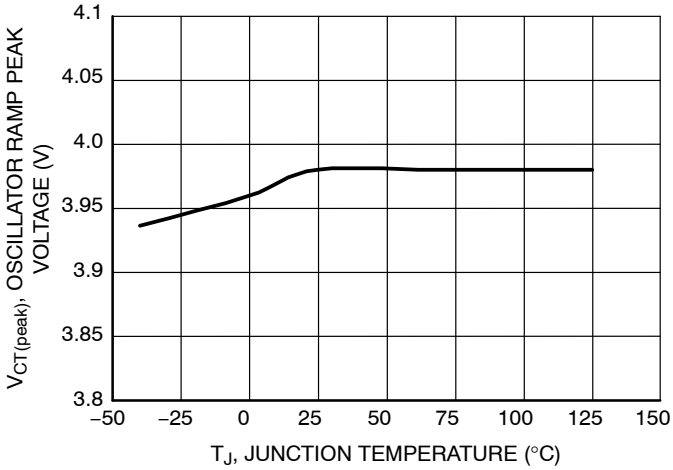


Figure 6. Ramp Peak Voltage vs. Junction Temperature

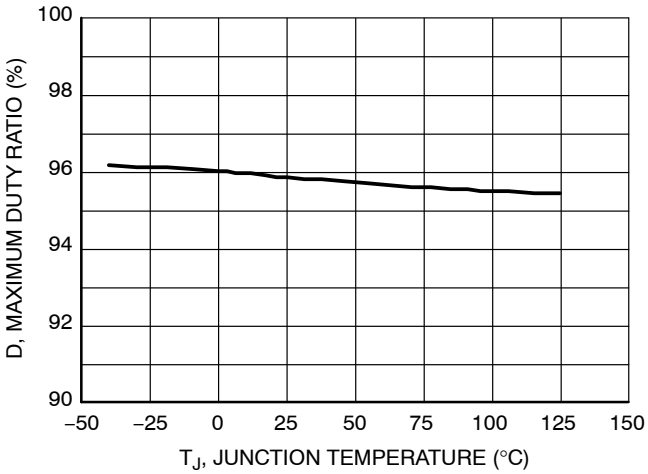


Figure 7. Maximum Duty Ratio vs. Junction Temperature

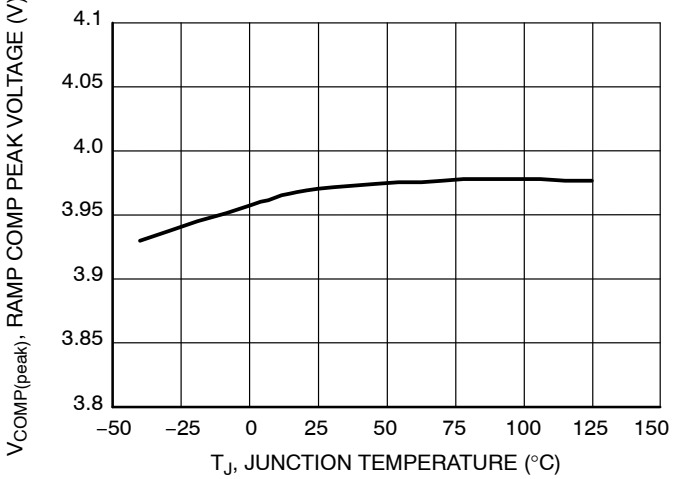


Figure 8. Ramp Compensation Peak Voltage vs. Junction Temperature

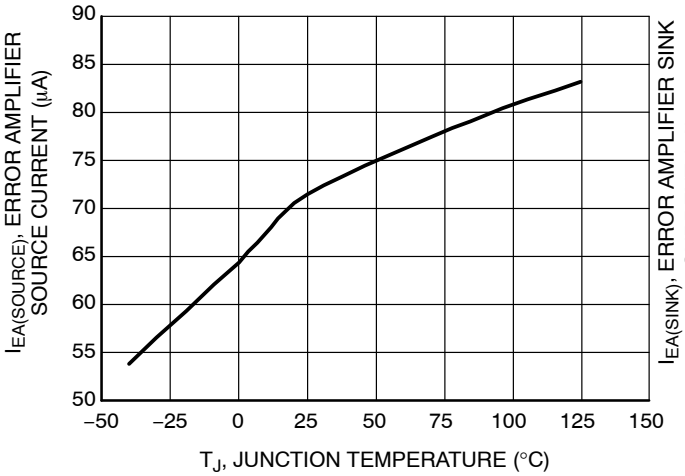


Figure 9. Error Amplifier Source Current vs. Junction Temperature

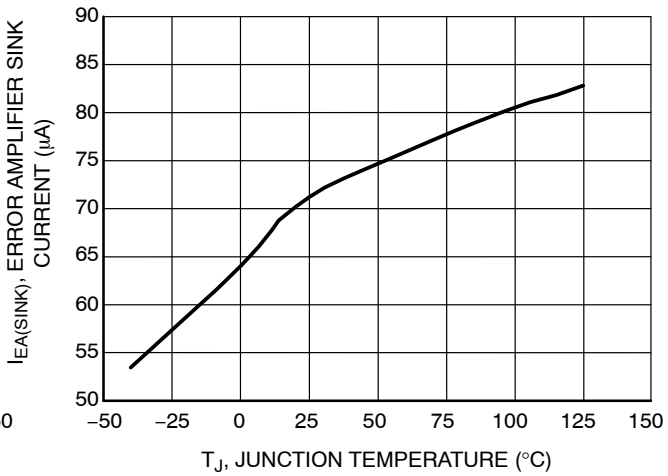


Figure 10. Error Amplifier Sink Current vs. Junction Temperature

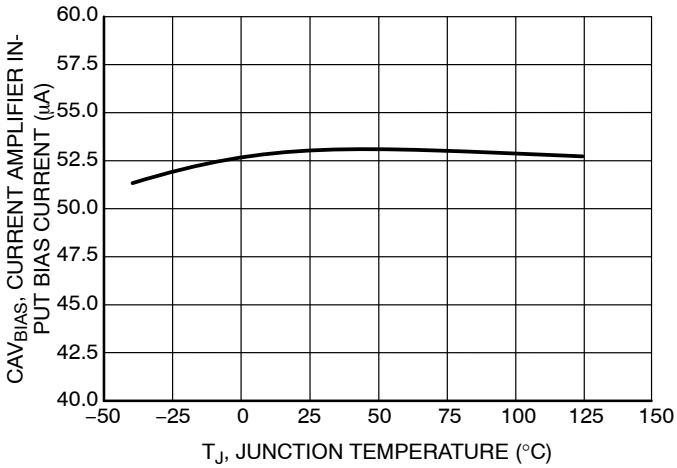


Figure 11. Current Amplifier Input Bias Current vs. Junction Temperature

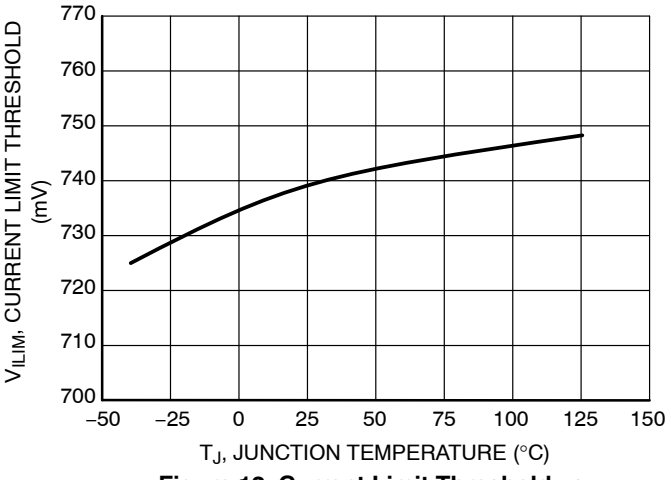


Figure 12. Current Limit Threshold vs. Junction Temperature

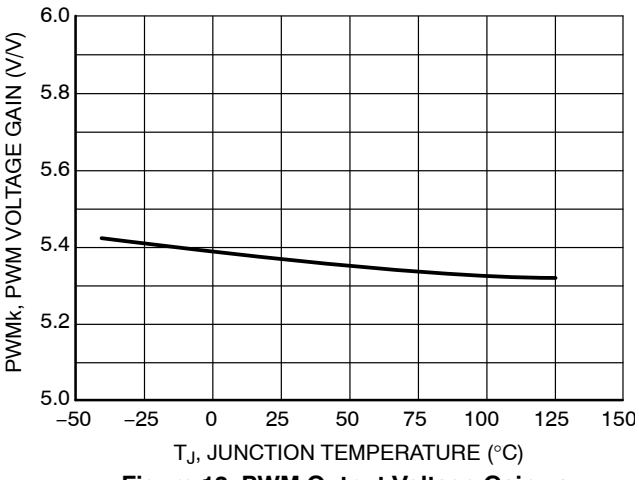


Figure 13. PWM Output Voltage Gain vs. Junction Temperature

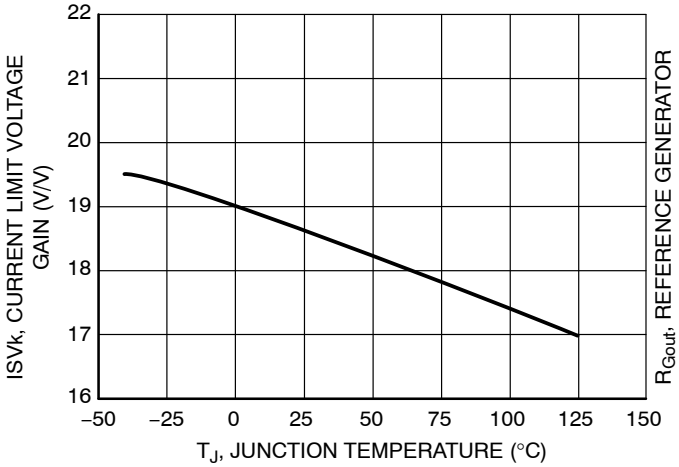


Figure 14. Oscillator CS Limit Voltage Gain vs. Junction Temperature

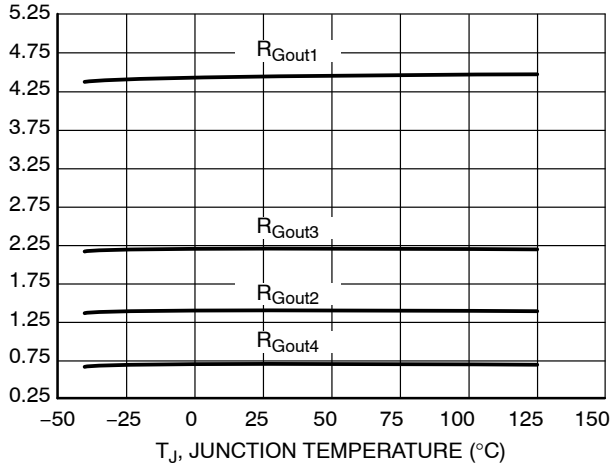


Figure 15. Oscillator Reference Generator Output Voltage vs. Junction Temperature

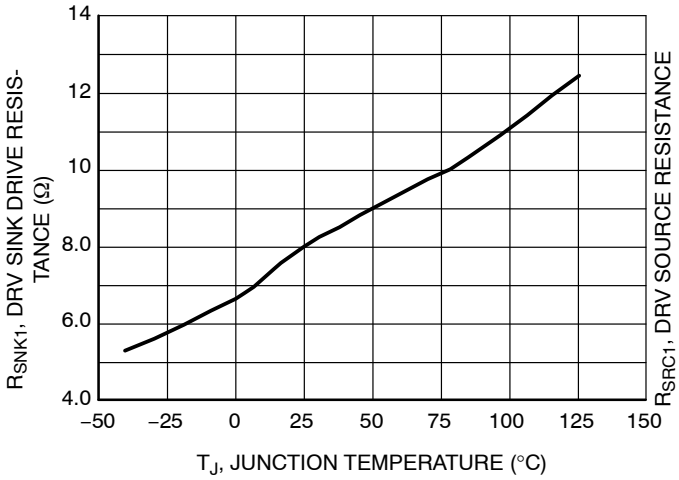


Figure 16. DRV Sink Resistance vs. Junction Temperature

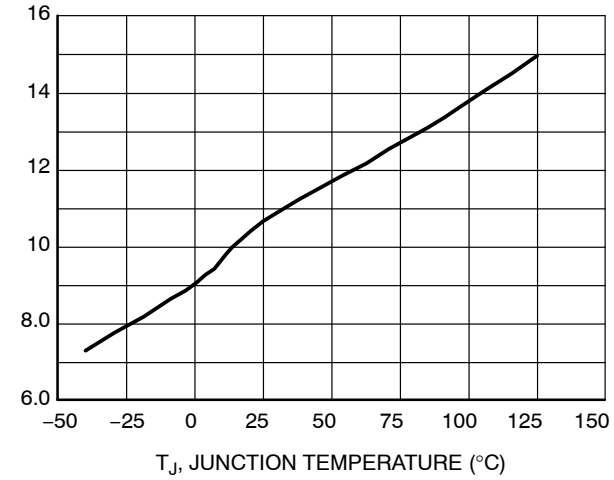


Figure 17. DRV Source Drive Resistance vs. Junction Temperature

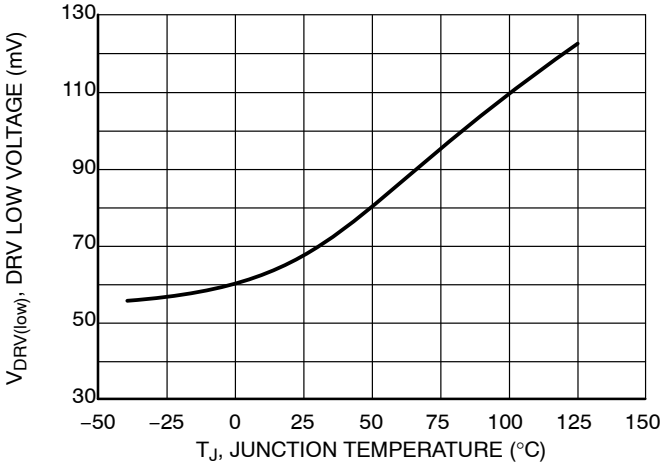


Figure 18. DRV Low Voltage vs. Junction Temperature

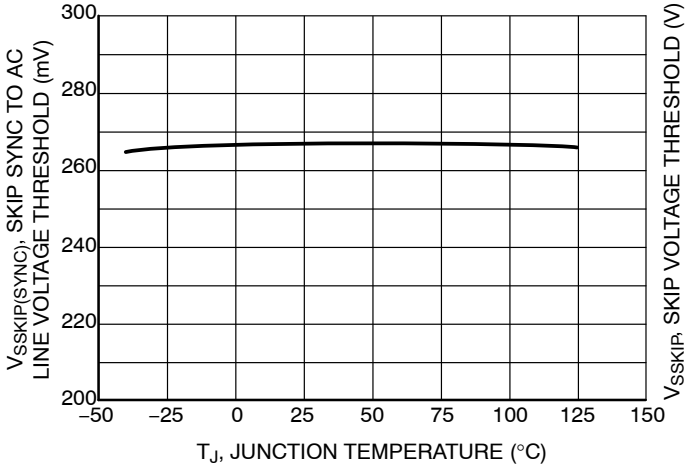


Figure 19. Skip Synchronization to ac Line Voltage Threshold vs. Junction Temperature

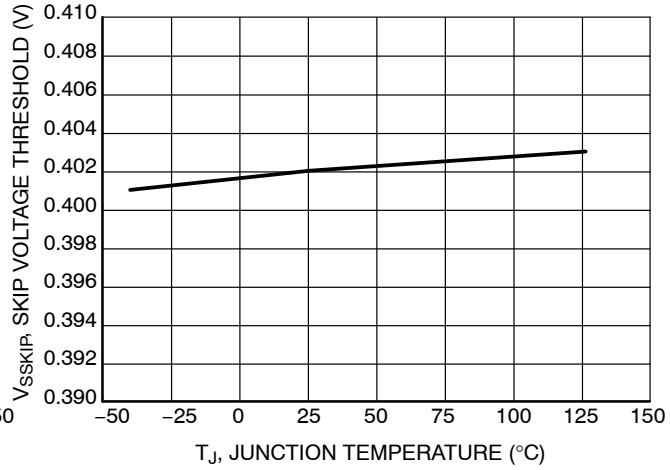


Figure 20. Skip Voltage Threshold vs. Junction Temperature

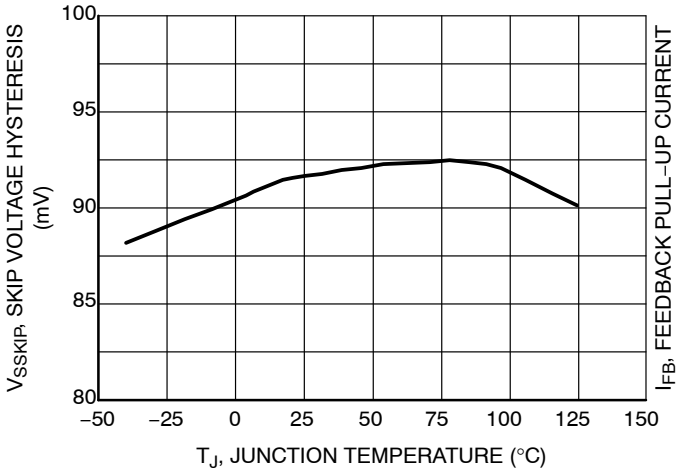


Figure 21. Skip Voltage Hysteresis vs. Junction Temperature

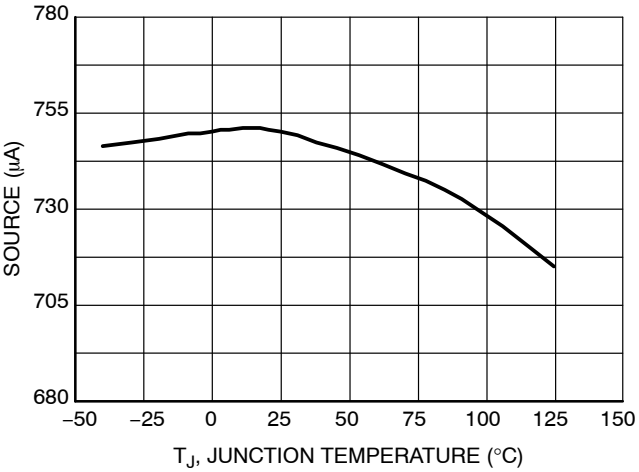


Figure 22. Feedback Pull−Up Current Source vs. Junction Temperature

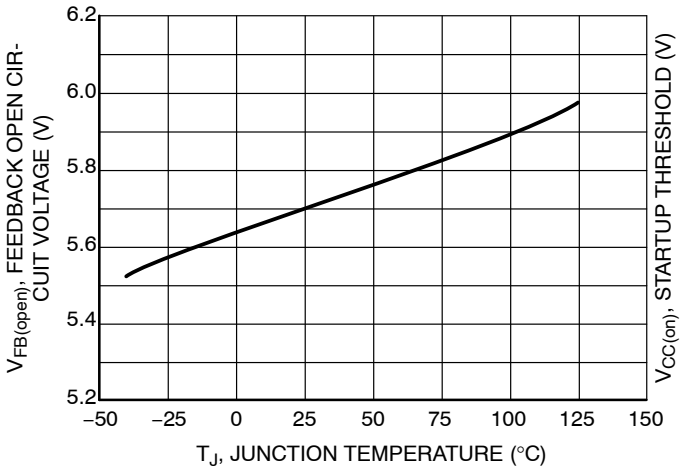


Figure 23. Feedback Open Circuit Voltage vs. Junction Temperature

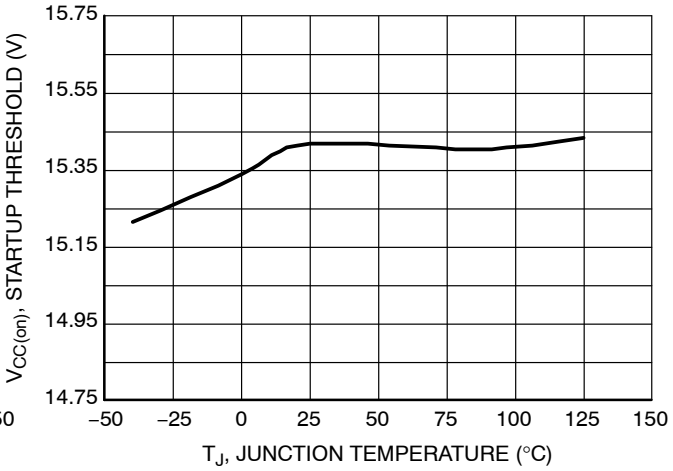


Figure 24. Startup Threshold vs. Junction Temperature

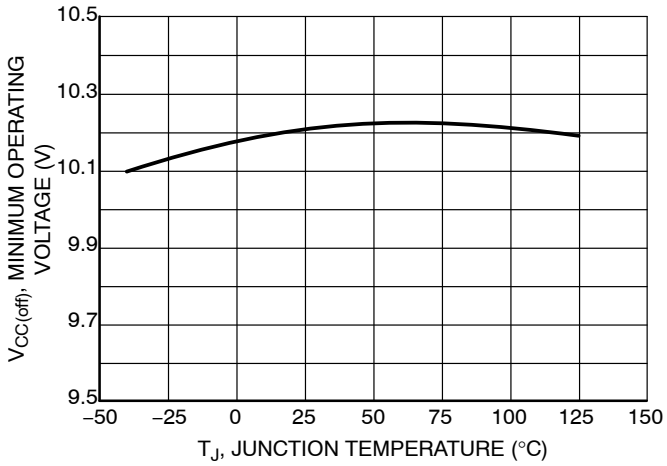


Figure 25. Minimum Operating Voltage vs. Junction Temperature

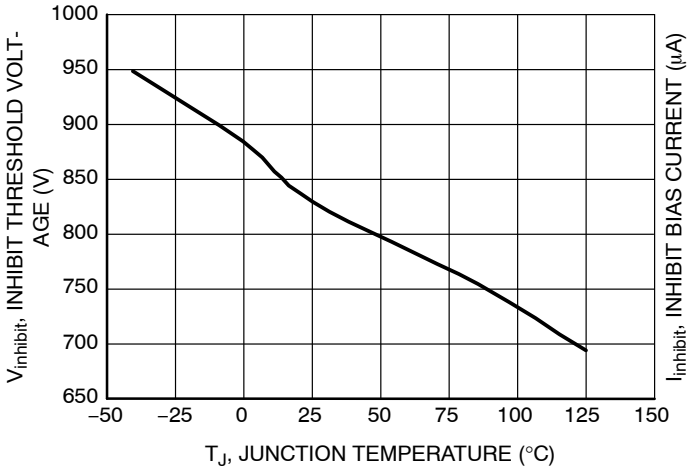


Figure 26. Inhibit Threshold Voltage vs. Junction Temperature

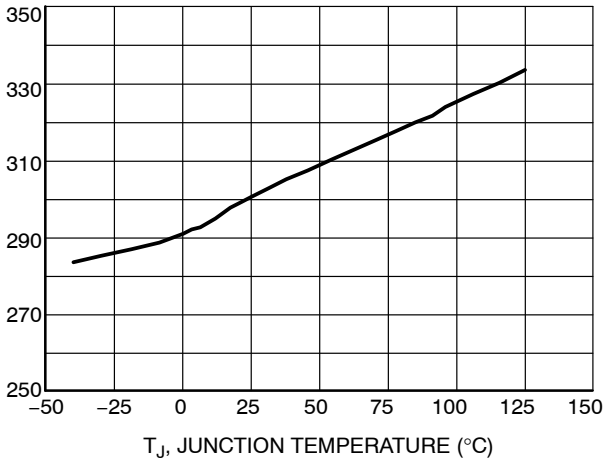


Figure 27. Inhibit Bias Current vs. Junction Temperature

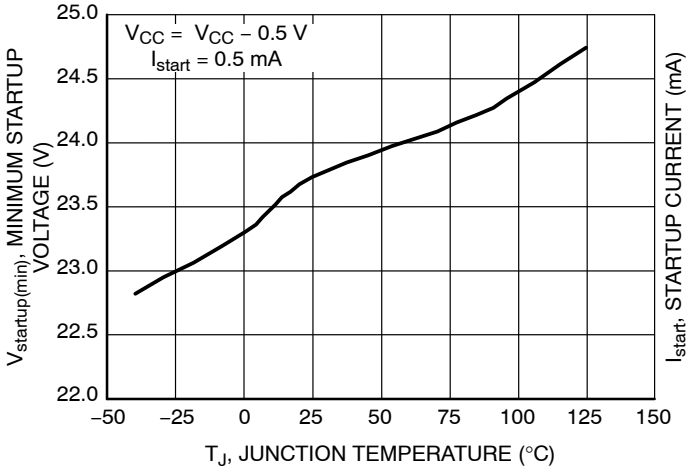


Figure 28. Minimum Startup Voltage vs. Junction Temperature

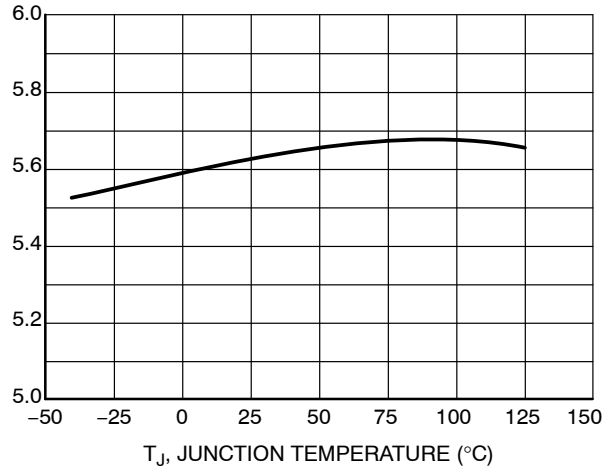


Figure 29. Startup Current vs. Junction Temperature

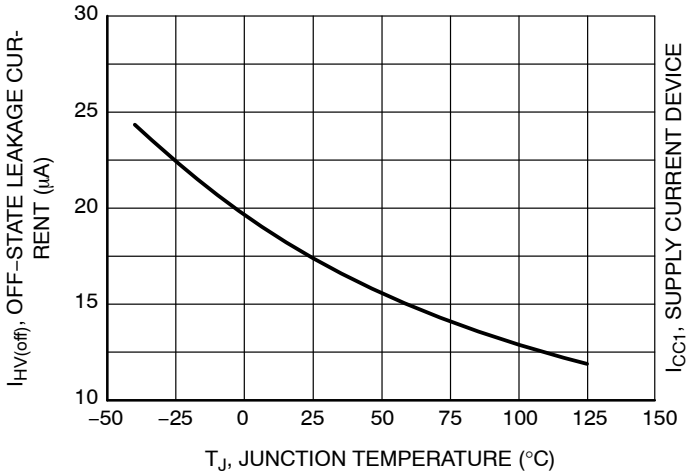


Figure 30. Off−State Leakage Current vs. Junction Temperature

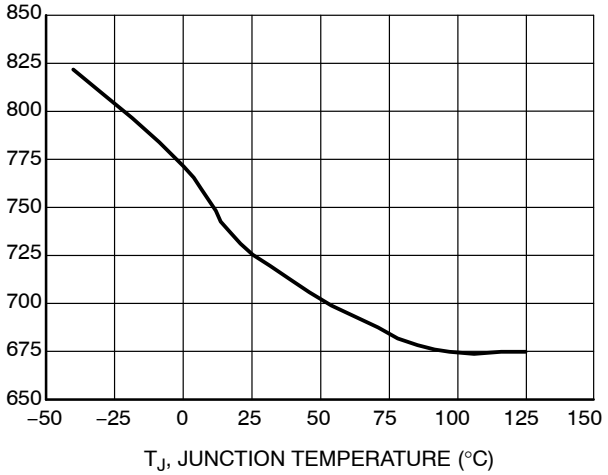


Figure 31. Supply Current Device Disabled (Overload) vs. Junction Temperature

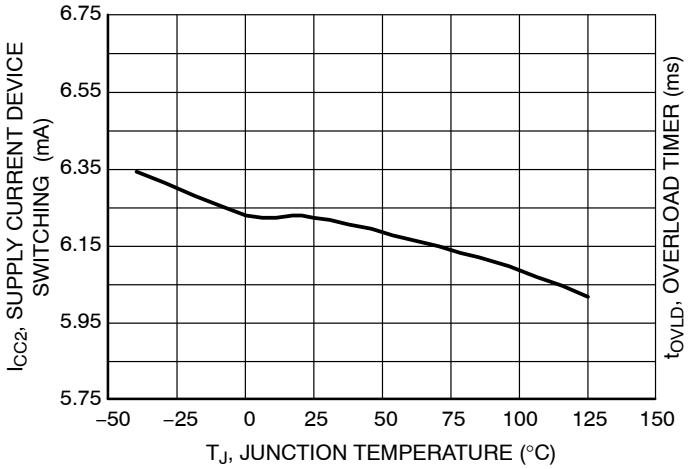


Figure 32. Supply Current Device Switching vs. Junction Temperature

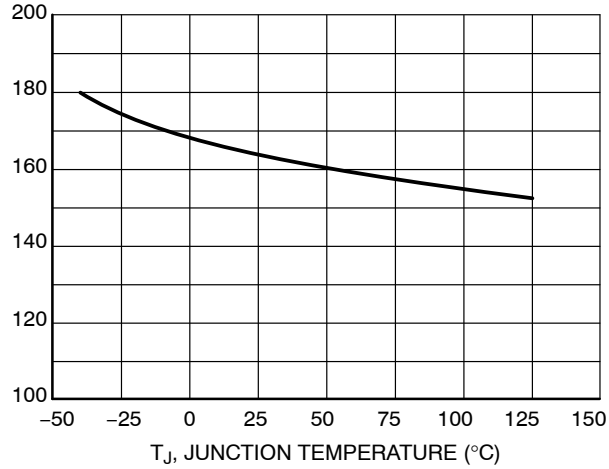


Figure 33. Overload Timer vs. Junction Temperature

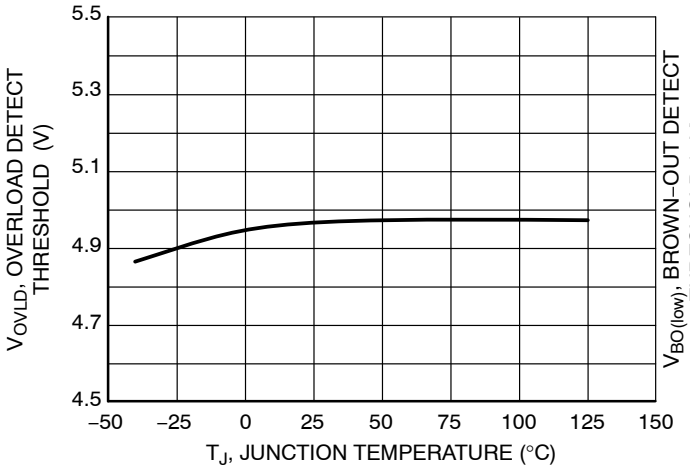


Figure 34. Overload Detect Threshold vs. Junction Temperature

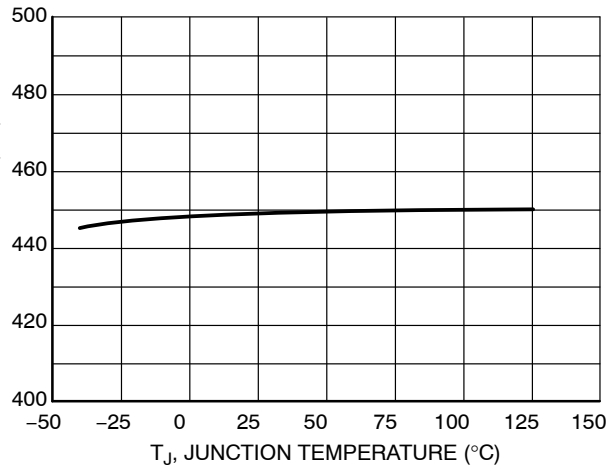


Figure 35. Brown−Out Detect Threshold vs. Junction Temperature

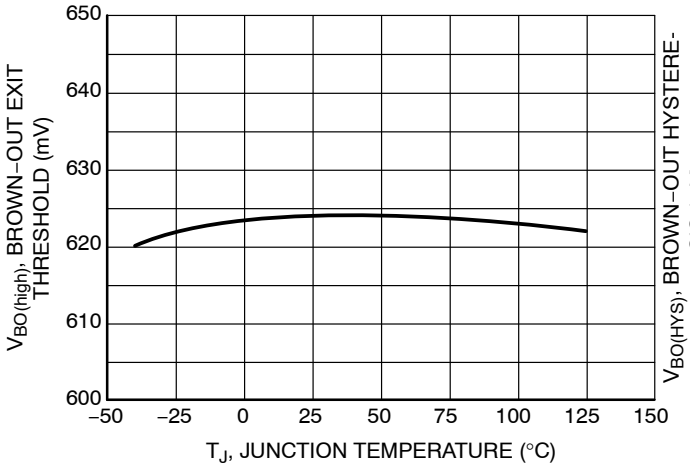


Figure 36. Brown−Out Exit Threshold vs. Junction Temperature

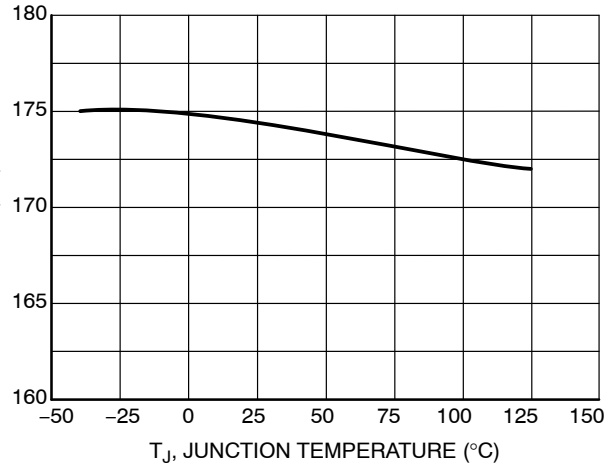


Figure 37. Brown−Out Hysteresis vs. Junction Temperature

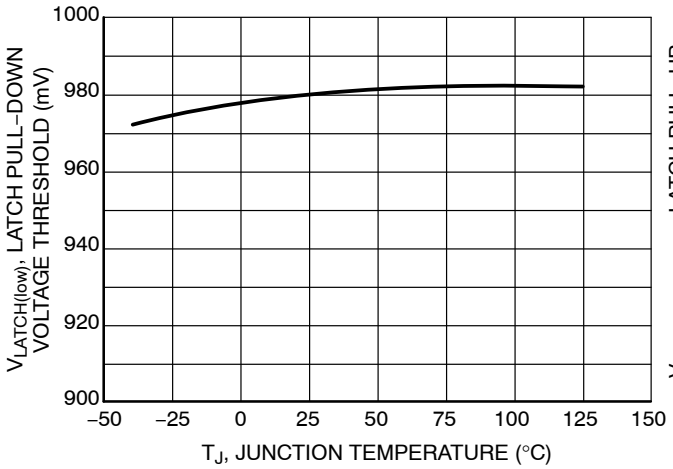


Figure 38. Latch Pull−Down Voltage Threshold vs. Junction Temperature

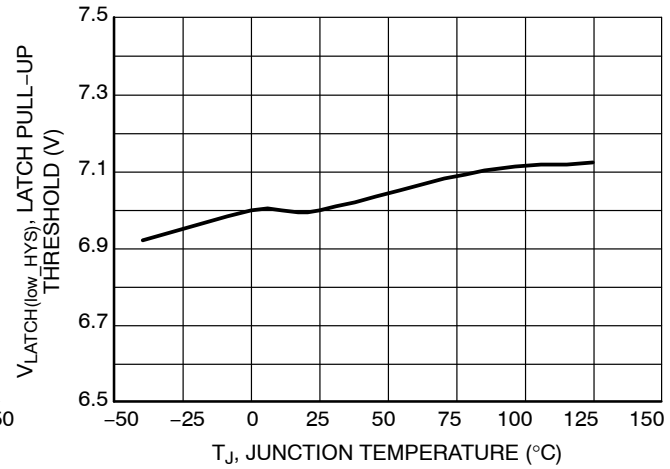


Figure 39. Latch Pull−Up Threshold vs. Junction Temperature

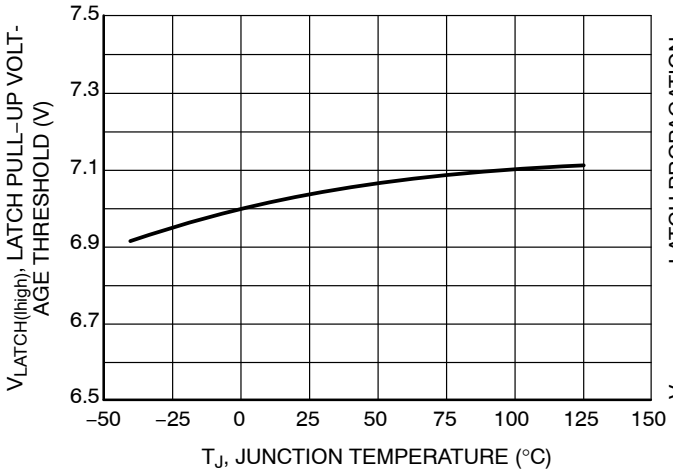


Figure 40. Latch Pull−Up Voltage Threshold vs. Junction Temperature

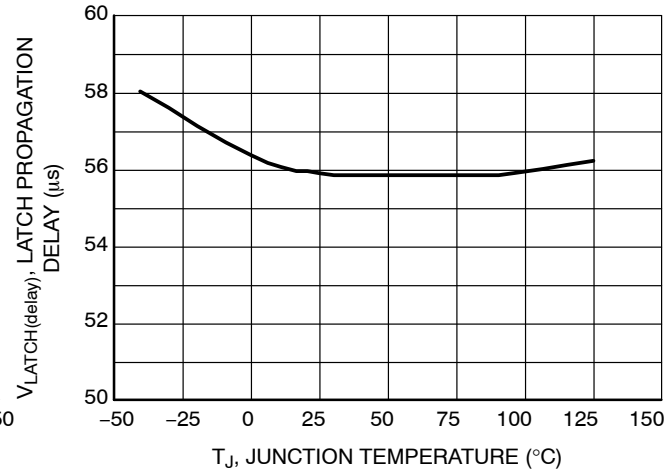


Figure 41. Latch Propagation Delay vs. Junction Temperature

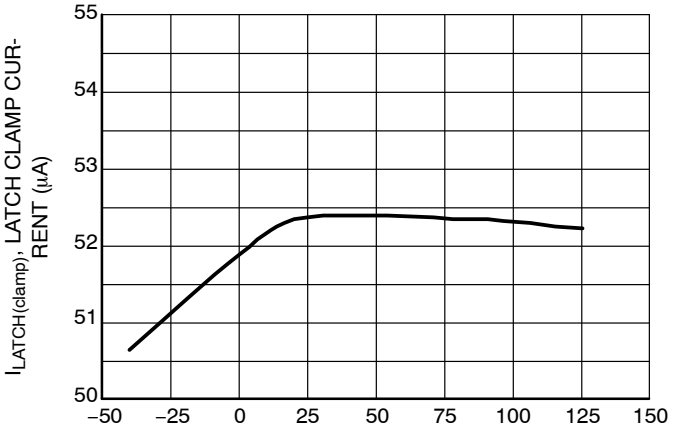


Figure 42. Latch Clamp Current vs. Junction Temperature

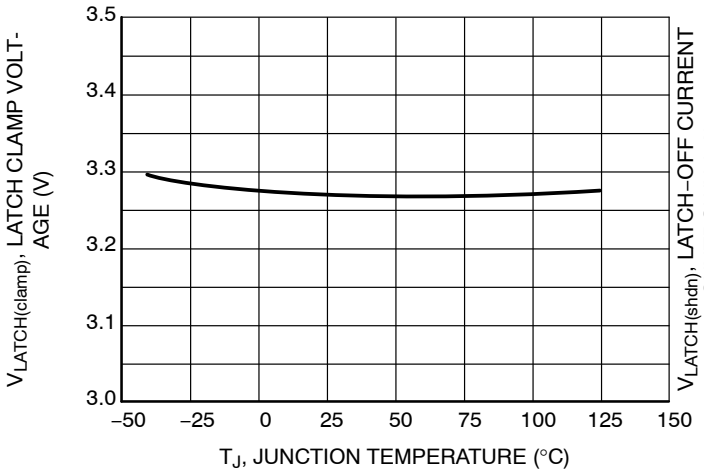


Figure 43. Latch Clamp Voltage vs. Junction Temperature

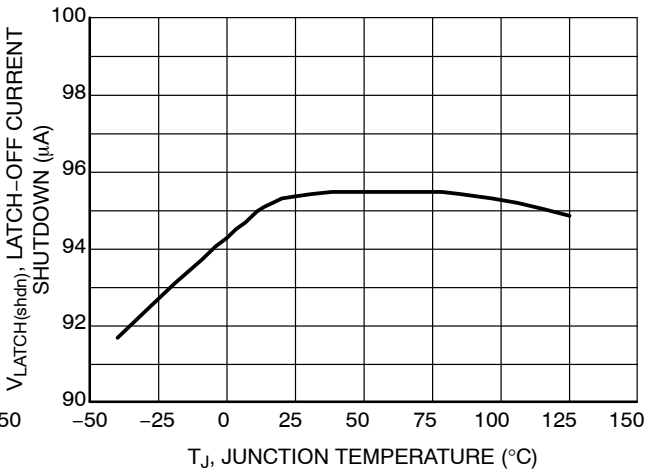


Figure 44. Latch−Off Current Shutdown vs. Junction Temperature

DETAILED DEVICE DESCRIPTION

Introduction

The NCL30001 is a highly integrated controller combining PFC and isolated step down power conversion in a single stage, resulting in a lower cost and reduced part count solution. This controller is ideal for LED Lighting applications with power requirements between 40 W and 150 W with an output voltage greater than 12 V. The single stage is based on the flyback converter and it is designed to operate in CCM mode.

Power Factor Correction (PFC) Introduction

Power factor correction shapes the input current of off−line power supplies to maximize the real power available from the mains. Ideally, the electrical appliance should present a load that emulates a pure resistor, in which case the reactive power drawn by the device is zero. Inherent in this scenario is the freedom from input current harmonics. The current is a perfect replica of the input voltage (usually a sine wave) and is exactly in phase with it. In this case the current drawn from the mains is at a minimum for the real power required to perform the needed work, and this minimizes losses and costs associated not only with the distribution of the power, but also with the generation of the power and the capital equipment involved in the process. The freedom from harmonics also minimizes interference with other devices being powered from the same source.

Another reason to employ PFC in many of today's power supplies is to comply with regulatory requirements. Today, lighting equipment in Europe must comply with IEC61000−3−2 Class C. This requirement applies to most lighting applications with input power of 25 W or greater, and it specifies the maximum amplitude of line−frequency harmonics up to and including the 39th harmonic. Moreover power factor requirements for commercial lighting is included within the ENERGY STAR® Solid State Lighting Luminaire standard regardless of the applications power level.

Typical Power Supply with PFC

A typical power supply consists of a boost PFC preregulator creating an intermediate ~400 V bus and an isolated dc−dc converter producing the desired output voltage as shown in Figure 45. This architecture has two power stages.

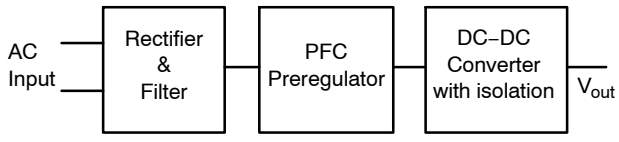


Figure 45. Typical Two Stage Power Converter

A two stage architecture allows optimization of each individual power stage. It is commonly used because of designer familiarity and a vast range of available components. But, because it processes the power twice, the search is always on for a more compact and power efficient solution.

The NCL30001 controller offers the convenience of shrinking the front−end converter (PFC preregulator) and the dc−dc converter into a single power processing stage as shown in Figure 46.

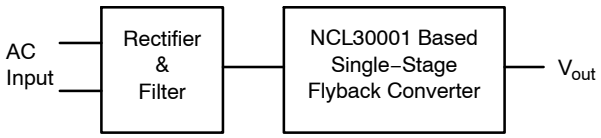


Figure 46. Single Stage Power Converter

This approach significantly reduces the component count. The NCL30001 based solution requires only one each of MOSFET, magnetic element, output rectifier (low voltage) and output capacitor (low voltage). In contrast, the 2−stage solution requires two or more of the above−listed components. Elimination of certain high−voltage components (e.g. high voltage capacitor and high voltage PFC diode) has significant impact on the system design. The resultant cost savings and reliability improvement are often worth the effort of designing a new converter.

Single PFC Stage

While the single stage offers certain benefits, it is important to recognize that it is not a recommended solution for all requirements. The following three limitations apply to the single stage approach:

- The output voltage ripple will have a 2x line frequency component (120 Hz for North American applications) that can not be eliminated easily. The cause of this ripple is the elimination of the energy storage element that is typically the boost output capacitor in the 2−stage solution. The only way to reduce the ripple is to increase the output filter capacitance. The required value of capacitance is inversely proportional to the output voltage. Normally the presence of this ripple is not a issue for most LED lighting applications.
- The hold−up time will not be as good as the 2−stage approach – again due to the lack of an intermediate energy storage element.
- In a single stage converter, one FET processes all the power – that is both a benefit and a limitation as the stress on that main MOSFET is relatively higher. Similarly, the magnetic component (flyback transformer/inductor) can not be optimized as well as in the 2−stage solution. As a result, potentially higher leakage inductance induces higher voltage spikes (like the one shown in Figure 47) on the MOSFET drain. This may require a MOSFET with a higher voltage

rating compared to similar dc−input flyback applications.

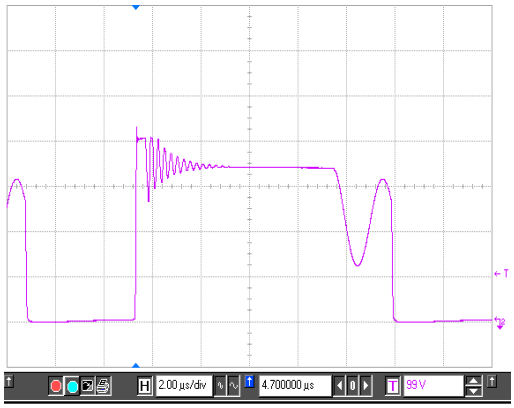


Figure 47. Typical Drain Voltage Waveform of a Flyback Main Switch

There are two methods to clamp the voltage spike on the main switch, a resistor−capacitor−diode (RCD) clamp or a transient voltage suppressor (TVS).

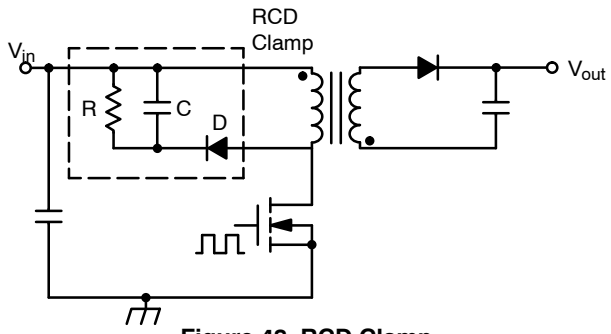


Figure 48. RCD Clamp

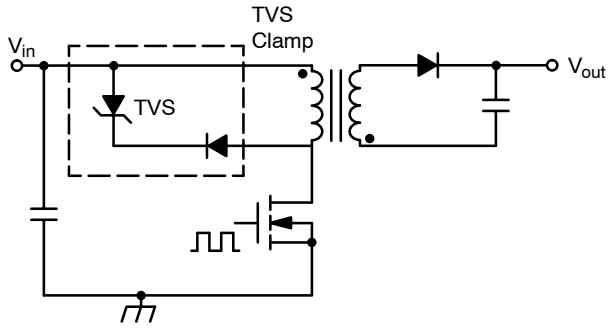


Figure 49. TVS Clamp

Both methods result in dissipation of the leakage energy in the clamping circuits – the dissipation is proportional to LI^2 where L is the leakage inductance of the transformer and I is the peak of the switch current at turn−off. An RCD snubber is simple and has the lowest cost, but constantly dissipates power. A TVS provides good voltage clamping at a slightly higher cost and dissipates power only when the drain voltage exceeds the voltage rating of the TVS.

Other features found in the NCL30001 include a high voltage startup circuit, voltage feedforward, brown out detector, internal overload timer, latch input and a high accuracy multiplier.

NCL30001 PFC Loop

The NCL30001 incorporates a modified version of average current mode control used for achieving the unity power factor. The PFC section includes a variable reference generator, a low frequency voltage regulation error amplifier (AC error AMP), ramp compensation (Ramp Comp) and current shaping network. These blocks are shown in the lower portion of the bock diagram (Figure 45).

The inputs to the reference generator include feedback signal (FB), scaled AC input signal (AC_IN) and feedforward input (V_{FF}). The output of the reference generator is a rectified version of the input sine−wave scaled by the FB and V_{FF} values. The reference amplitude is proportional to the FB and inversely proportional to the square of the V_{FF}. This, for higher load levels and/or lower input voltage, the signal would be higher.

The function of the AC error amp is to force the average current output of the current sense amplifier to match the reference generator output. The output of the AC error amplifier is compensated to prevent response to fast events. This output (V_{error}) is fed into the PWM comparator through a reference buffer. The PWM comparator sums the V_{error} and the instantaneous current and compares it to a 4.0 V threshold to provide the desired duty cycle control. Ramp compensation is also added to the input signal to allow CCM operation above 50% duty cycle.

High Voltage Startup Circuit

The NCL30001 internal high voltage startup circuit eliminates the need for external startup components and provides a faster startup time compared to an external startup resistor. The startup circuit consists of a constant current source that supplies current from the HV pin to the supply capacitor on the V_{CC} pin (C_{CC}). The startup current (I_{start}) is typically 5.5 mA.

The DRV driver is enabled and the startup current source is disabled once the V_{CC} voltage reaches $V_{CC(on)}$, typically 15.4 V. The controller is then biased by the V_{CC} capacitor. The drivers are disabled if V_{CC} decays to its minimum operating threshold ($V_{CC(off)}$) typically 10.2 V. Upon reaching $V_{CC(off)}$ the gate driver is disabled. The V_{CC} capacitor should be sized such V_{CC} is kept above $V_{CC(off)}$ while the auxiliary voltage is building up. Otherwise, the system will not start.

The controller operates in double hiccup mode while in overload or $V_{CC(off)}$. A double hiccup fault disables the drivers, sets the controller in a low current mode and allows V_{CC} to discharge to $V_{CC(off)}$. This cycle is repeated twice to minimize power dissipation in external components during

a fault event. Figure 50 shows double hiccup mode operation. A soft−start sequence is initiated the second time V_{CC} reaches $V_{CC(on)}$. If the controller is latched upon reaching $V_{CC(on)}$, the controller stays in hiccup mode. During this mode, V_{CC} never drops below $V_{CC(reset)}$, the controller logic reset level. This prevents latched faults to be cleared unless power to the controller is completely removed (i.e. unplugging the supply from the AC line).

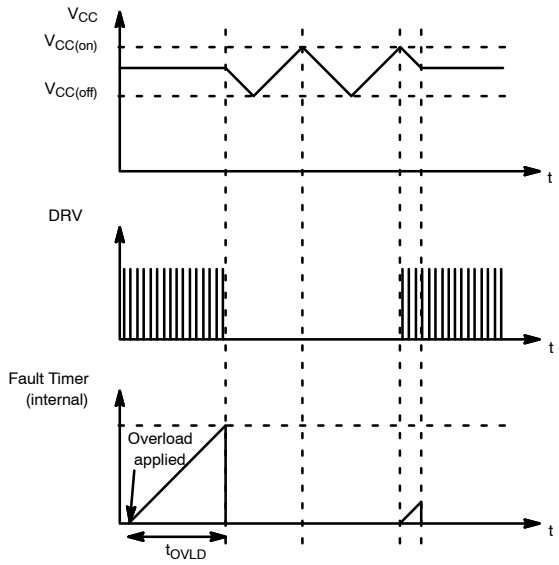


Figure 50. V_{CC} Double Hiccup Operation with a Fault Occurring while the Startup Circuit is Disabled

An internal supervisory circuit monitors the V_{CC} voltage to prevent the controller from dissipating excessive power if the V_{CC} pin is accidentally grounded. A lower level current source ($I_{inhibit}$) charges C_{CC} from 0 V to $V_{inhibit}$, typically 0.85 V. Once V_{CC} exceeds $V_{inhibit}$, the startup current source is enabled. This behavior is illustrated in Figure 51. This slightly increases the total time to charge V_{CC}, but it is generally not noticeable.

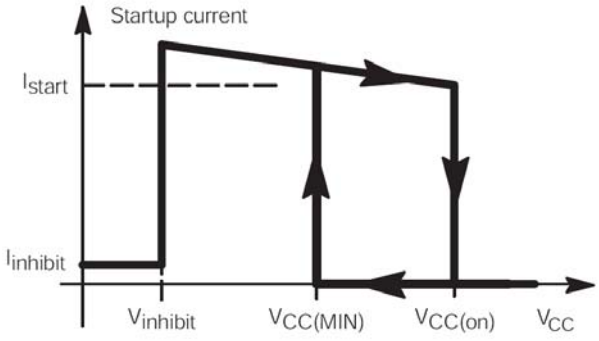


Figure 51. Startup Current at Various V_{CC} Levels

The rectified ac line voltage is provided to the power stage to achieve accurate PFC. Filtering the rectified ac line voltage with a large bulk capacitor distorts the PFC in a single stage PFC converter. A peak charger is needed to bias the HV pin as shown in Figure 52. Otherwise, the HV pin follows the ac line and the startup circuit is disabled every time the ac line voltage approaches 0 V. The V_{CC} capacitor is sized to bias the controller during power up.

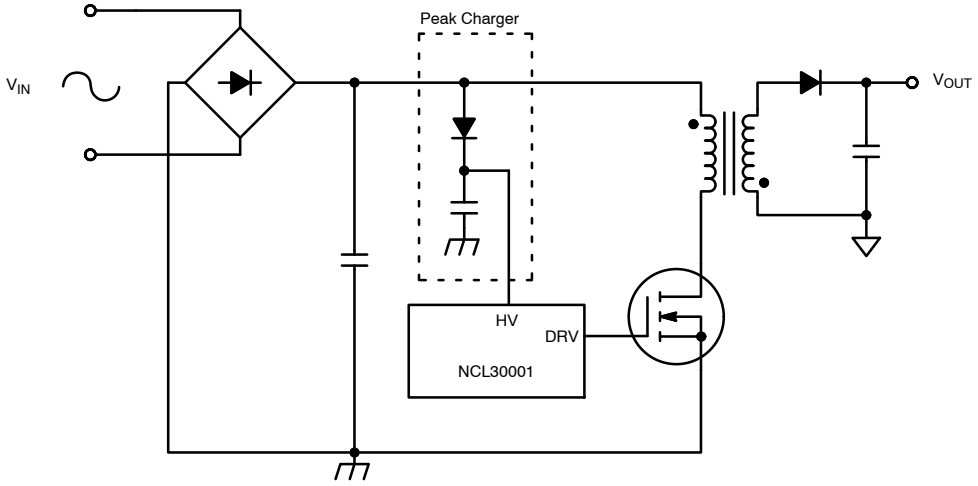


Figure 52. Peak charger

The startup circuit is rated at a maximum voltage of 500 V. Power dissipation should be controlled to avoid exceeding the maximum power dissipation of the controller. If dissipation on the controller is excessive, a resistor can be placed in series with the HV pin. This will reduce power dissipation on the controller and transfer it to the series resistor.

Drive Output

DRV has a source resistance of 10.8 Ω (typical) and a sink resistance of 8.0 Ω (typical). The driver is enabled once V_{CC} reaches $V_{CC(on)}$ and there are no faults present. They are disabled once V_{CC} discharges to $V_{CC(off)}$. The high current drive capability of DRV may generate voltage spikes during switch transitions due to parasitic board inductance. Shortening the connection length between the driver and the load and using wider connections will reduce inductance−induced spikes.

AC Error Amplifier and Buffer

The AC error amplifier (EA) shapes the input current into a high quality sine wave by forcing the filtered input current to follow the output of the reference generator. The output of the reference generator is a full wave rectified ac signal and it is applied to the non inverting input of the EA. The filtered input current, I_{in}, is the current sense signal at the ISpos pin multiplied by the current sense amplifier gain. It is applied to the inverting input of the AC EA.

The AC EA is a transconductance amplifier. A transconductance amplifier generates an output current proportional to its differential input voltage. This amplifier has a nominal gain of 100 μS (or 0.0001 A/V). That is, an input voltage difference of 10 mV causes the output current to change by 1.0 μA. The AC EA has typical source and sink currents of 70 μA.

The filtered input current is a high frequency signal. A low frequency pole forces the average input current to follow the reference generator output. A pole-zero pair is created by placing a (R_{COMP}) and capacitor (C_{COMP}) series combination at the output of the AC EA. The AC COMP pin provides access to the AC EA output.

The output of the AC EA is inverted and converted into a current using a second transconductance amplifier. The output of the inverting transconductance amplifier is $V_{ACEA(buffer)}$. Figure 53 shows the circuit schematic of the AC EA buffer. The AC EA buffer output current, $I_{ACEA(out)}$, is given by Equation 1.

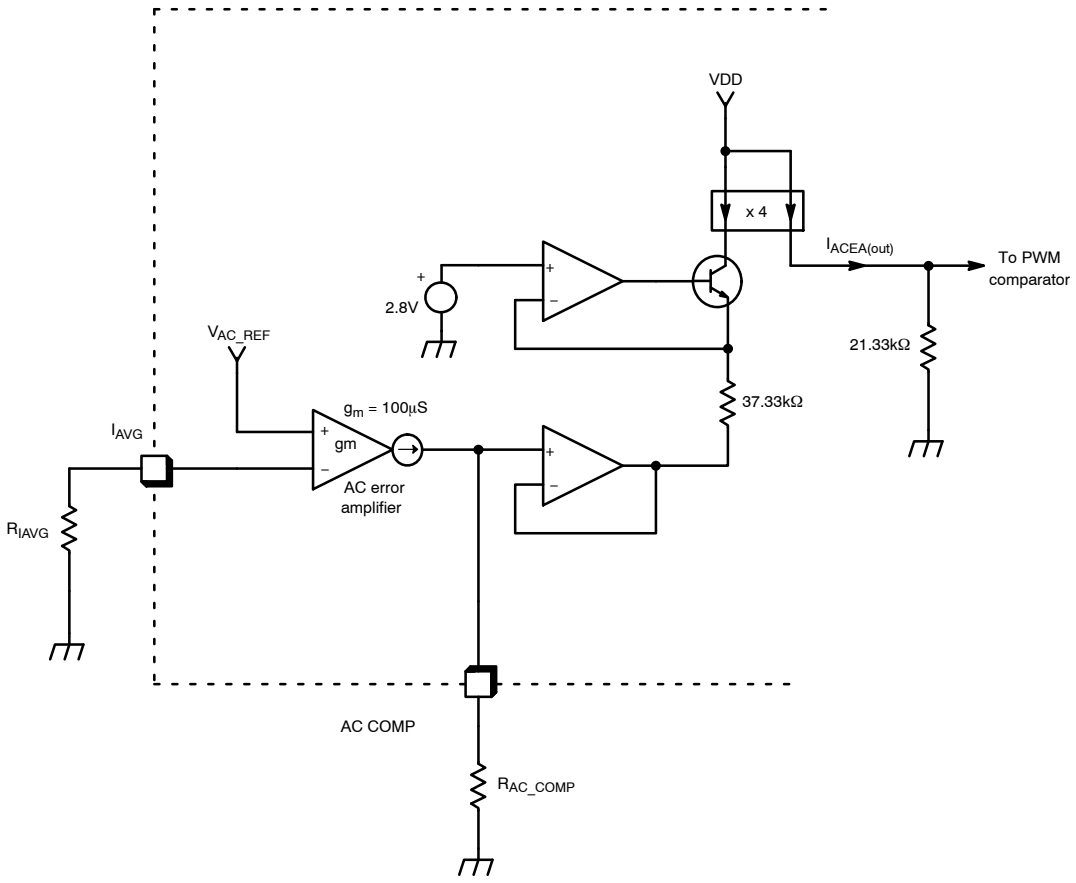


Figure 53. AC EA Buffer Amplifier

$$I_{ACEA(out)} = \left(\frac{2.8 - V_{ACEA}}{37.33k}\right) \cdot 4 \qquad \text{(eq. 1)}$$

The voltage at the PWM non-inverting input is determined by $I_{ACEA(out)}$, the instantaneous switch current along and the ramp compensation current. DRV is terminated once the voltage at the PWM non-inverting input reaches 4 V.

Current Sense Amplifier

A voltage proportional to the main switch current is applied to the current sense input, IS_{POS}. The current sense amplifier is a wide bandwidth amplifier with a differential input. The current sense amplifier has two outputs, PWM Output and I_{AVG} Output. The PWM Output is the instantaneous switch current which is filtered by the internal leading edge blanking (LEB) circuitry prior to applying it to the PWM Comparator non inverting input. The second output is a filtered current signal resembling the average value of the input current. Figure 54 shows the internal architecture of the current sense amplifier.

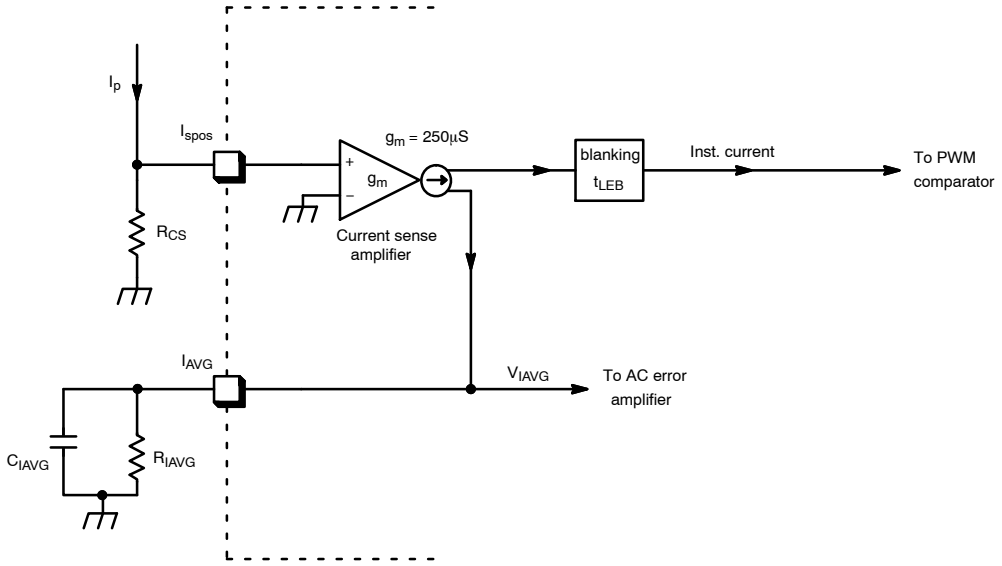


Figure 54. Current Sense Amplifier

Caution should be exercised when designing a filter between the current sense resistor and the IS_{POS} input, due to the low impedance of this amplifier. Any series resistance due to a filter creates a voltage offset (V_{OS}) due to its input bias current, CA_{Ibias}. The input bias current is typically 60 μA. The voltage offset is given by Equation 2.

$$V_{OS} = CA_{Ibias} \cdot R_{external} \qquad \text{(eq. 2)}$$

The offset adds a positive offset to the current sense signal. The ac error amplifier will then try to compensate for the average output current which appears never to go to zero and cause additional zero crossing distortion.

A voltage proportional to the main switch current is applied to the IS_{POS} pin. The IS_{POS} pin voltage is converted into a current, i_1, and internally mirrored. Two internal currents are generated, I_{CS} and I_{AVG}. I_{CS} is a high frequency signal which is a replica of the instantaneous switch current. I_{AVG} is a low frequency signal. The relationship between V_{ISPOS} and I_{CS} and I_{AVG} is given by Equation 3.

$$I_{CS} = I_{IN} = \frac{V_{ISPOS}}{4k} \qquad \text{(eq. 3)}$$

The PWM Output delivers current to the positive input of the PWM input where it is added to the AC EA and ramp compensation signal.

The I_{AVG} Output generates a voltage signal to a buffer amplifier. This voltage signal is the product of I_{AVG} and an external R_{IAVG} resistor filtered by the capacitor on the I_{AVG} pin, C_{IAVG}. The pole frequency, f_P, set by C_{IAVG} should be significantly below the switching frequency to remove the high frequency content. But, high enough to not to cause significant distortion to the input full wave rectified sinewave waveform. A properly filtered average current signal has twice the line frequency. Equation 4 shows the relationship between C_{IAVG} (in nF) and f_P (in kHz).

$$C_{IAVG} = \frac{1}{2 \cdot \pi \cdot R_{IAVG} \cdot f_P} \qquad \text{(eq. 4)}$$

The gain of the low frequency current buffer is set by the resistor at the I_{AVG} pin, R_{IAVG}. R_{IAVG} sets the scaling factor between the primary peak and primary average currents. The gain of the current sense amplifier, A_{CA}, is given by Equation 5.

$$A_{CA} = \frac{RI_{AVG}}{4k} \quad \text{(eq. 5)}$$

The current sense signal is prone to leading edge spikes during the switch turn on due to parasitic capacitance and inductance. This spike may cause incorrect operation of the PWM Comparator. The NCL30001 incorporates LEB circuitry to block the first 200 ns (typical) of each current pulse. This removes the leading edge spikes without filtering the current signal waveform.

Oscillator

The oscillator controls the switching frequency, *f*, the jitter frequency and the gain of the multiplier. The oscillator ramp is generated by charging the timing capacitor on the CT Pin, C_T, with a 200 μA current source. This current source is tightly controlled during manufacturing to achieve a controlled and repeatable oscillator frequency. The current source turns off and C_T is immediately discharged with a pull down transistor once the oscillator ramp reaches its peak voltage, $V_{CT(peak)}$, typically 4.0 V. The pull down transistor turns off and the charging current source turns on once the oscillator ramp reaches its valley voltage, $V_{CT(valley)}$. Figure 55 shows the resulting oscillator ramp and control circuitry.

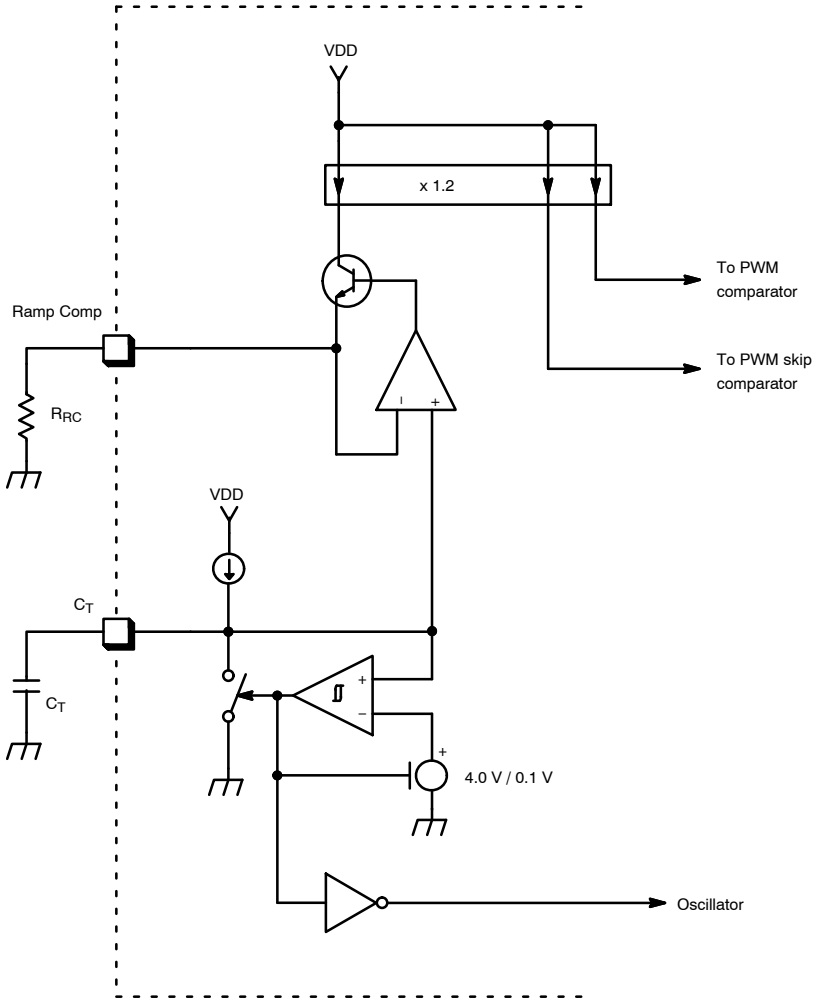


Figure 55. Oscillator Ramp and Control Circuitry

The relationship between the oscillator frequency in kHz and timing capacitor in pF is given by Equation 6.

$$C_T = \frac{47000}{f} \quad \text{(eq. 6)}$$

A low frequency oscillator modulates the switching frequency, reducing the controller EMI signature and allowing the use of a smaller EMI filter. The frequency modulation or jitter is typically ±6.8% of the oscillator frequency.

Output Overload

The Feedback Voltage, V_{FB}, is directly proportional to the output power of the converter. An internal 6.7 kΩ resistor pulls−up the FB voltage to the internal 6.5 V reference. An external optocoupler pulls down the FB voltage to regulate the output voltage of the system. The optocoupler is off during power up and output overload conditions allowing the FB voltage to reach its maximum level.

The NCL30001 monitors the FB voltage to detect an overload condition. A typical startup time of a single PFC stage converter is around 100 ms. If the converter is out of regulation (FB voltage exceeds 5.0 V) for more that 160 ms (typical) the drivers are disabled and the controller enters the double hiccup mode to reduce the average power dissipation. A new startup sequence is initiated after the double hiccup is complete. This protection feature is critical to reduce power during an output short condition.

Soft−Skip™ Cycle Mode

The FB voltage reduces as the output power demand of the converter reduces. Once V_{FB} drops below the skip threshold, V_{SSKIP}, 410 mV (typical) the driver is disabled. The skip comparator hysteresis is typically 90 mV.

The converter output voltage starts to decay because no additional output power is delivered. As the output voltage decreases the feedback voltage increases to maintain the output voltage in regulation. This mode of operation is known as skip mode. The skip mode frequency is dependent of load loop gain and output capacitance and can create audible noise due to mechanical resonance in the transformer and snubber capacitor. A proprietary Soft−Skip mode reduces audible noise by slowly increasing the primary peak current until it reaches its maximum value. The minimum skip ramp period, t_{SSKIP}, is 2.5 ms. Figure 56 shows the relationship between V_{FB}, V_{SSKIP} and the primary current.

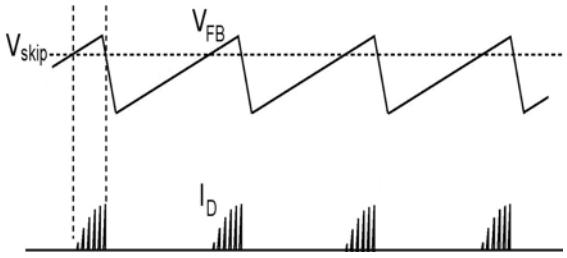


Figure 56. Soft−Skip Operation

Skip mode operation is synchronized to the ac line voltage. The NCL30001 disables Soft−Skip when the rectified ac line voltage drops to its valley level. This ensures the primary current always ramp up reducing audible noise. A skip event occurring as the ac line voltage is decreasing, causes the primary peak current to ramp down instead of ramp up. Once the skip period is over the primary current is only determined by the ac line voltage. A Soft−Skip event terminates once the AC−IN pin voltage decreases below 260 mV. A new Soft−Skip period starts once the voltage on the AC−IN pin increases to 260 mV.

An increase in output load current terminates a Soft−Skip event. A transient load detector terminates a Soft−Skip period once V_{FB} voltage exceeds V_{SSKIP} (1.75 V nominal). This ensures the required output power is delivered during a load transient and the output voltage does not fall out of regulation. Figure 57 shows the relationship between Soft−Skip and the transient load detector.

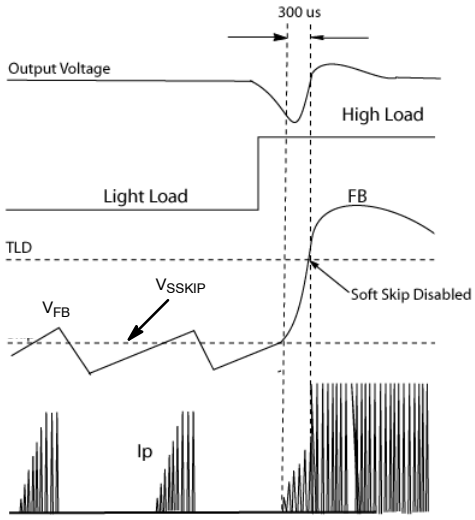


Figure 57. Load transient during Soft−Skip

The output of the Soft−Skip Comparator is or−ed with the PWM Comparator output to control the duty ratio. The Soft−Skip Comparator controls the duty ratio in skip mode and the PWM Comparator controls the duty cycle during normal operation. In skip mode, the non−inverting input of the Soft−Skip Comparator exceeds 4 V, disabling the drivers. As the FB voltage increases, the voltage at the non−inverting input is ramp down from 4 V to 0.2 V to enable the drivers.

Multiplier and Reference Generator

The NCL30001 uses a multiplier to regulate the average output power of the converter. This controller uses a proprietary concept for the multiplier used within the reference generator. This innovative design allows greatly improved accuracy compared to a conventional linear analog multiplier. The multiplier uses a PWM switching circuit to create a scalable output signal, with a very well defined gain.

The output of the multiplier is the ac-reference signal. The ac-reference signal is used to shape the input current. The multiplier has three inputs, the error signal from an external error amplifier (V_{FB}), the full wave rectified ac input (AC_IN) and the feedforward input (V_{FF}).

The FB signal from an external error amplifier circuit is applied to the V_{FB} pin via an optocoupler or other isolation circuit. The FB voltage is converted to a current with a V-I

V_{CC}