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NCL30082

Dimmable Quasi-Resonant Primary Side Current-Mode Controller for LED Lighting with Thermal Fold-back

The NCL30082 is a PWM current mode controller targeting isolated flyback and non-isolated constant current topologies. The controller operates in a quasi-resonant mode to provide high efficiency. Thanks to a novel control method, the device is able to precisely regulate a constant LED current from the primary side. This removes the need for secondary side feedback circuitry, biasing and an optocoupler.

The device is highly integrated with a minimum number of external components. A robust suite of safety protection is built in to simplify the design. This device supports analog/digital dimming as well as thermal current fold-back. While the NCL30082 has integrated fixed overvoltage protection, the designer has the flexibility to program a lower OVP level.

Features

- Quasi-resonant Peak Current-mode Control Operation
- Primary Side Sensing (no optocoupler needed)
- Wide V_{CC} Range
- Source 300 mA / Sink 500 mA Totem Pole Driver with 12 V Gate Clamp
- Precise LED Constant Current Regulation $\pm 1\%$ Typical
- Line Feed-forward for Enhanced Regulation Accuracy
- Low LED Current Ripple
- 250 mV $\pm 2\%$ Guaranteed Voltage Reference for Current Regulation
- ~ 0.9 Power Factor with Valley Fill Input Stage
- Low Start-up Current (13 μ A typ.)
- Analog or Digital Dimming
- Thermal Fold-back
- Wide Temperature Range of -40 to $+125^{\circ}\text{C}$
- Pb-Free, Halide-Free MSL1 Product
- Robust Protection Features
 - ◆ Over Voltage / LED Open Circuit Protection
 - ◆ Over Temperature Protection
 - ◆ Secondary Diode Short Protection
 - ◆ Output Short Circuit Protection
 - ◆ Shorted Current Sense Pin Fault Detection
 - ◆ Latched and Auto-recoverable Versions
 - ◆ Brown-out
 - ◆ V_{CC} Under Voltage Lockout
 - ◆ Thermal Shutdown
- These Devices are Pb-Free and Halogen Free/BFR Free

Typical Applications

- Integral LED Bulbs
- LED Power Driver Supplies
- LED Light Engines

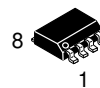


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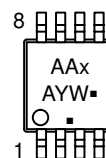


Micro8
DM SUFFIX
CASE 846A

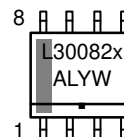


SOIC-8
D SUFFIX
CASE 751

MARKING DIAGRAMS

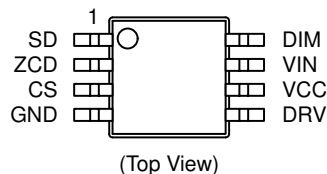


AAx = Specific Device Code
x = C, D or H
A = Assembly Location
Y = Year
W = Work Week
■ = Pb-Free Package
(Note: Microdot may be in either location)



L30082x = Specific Device Code
x = B, B1, B2, B3, D
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 33 of this data sheet.

NCL30082

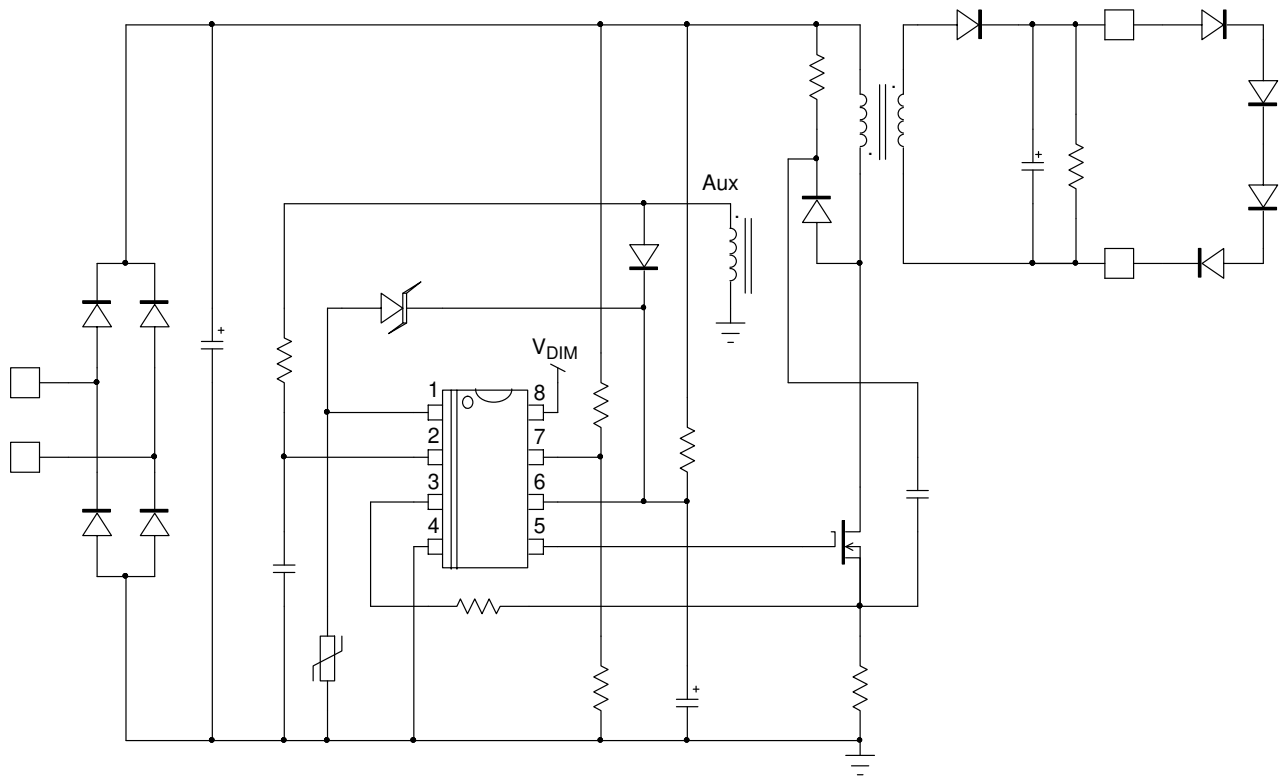


Figure 1. Typical Application Schematic for NCL30082

Table 1. PIN FUNCTION DESCRIPTION

Pin No	Pin Name	Function	Pin Description
1	SD	Thermal Fold-back and shutdown	Connecting an NTC to this pin allows reducing the output current down to 50% of its fixed value before stopping the controller. A Zener diode can also be used to pull-up the pin and stop the controller for adjustable OVP protection
2	ZCD	Zero Crossing Detection	Connected to the auxiliary winding, this pin detects the core reset event.
3	CS	Current sense	This pin monitors the primary peak current
4	GND	-	The controller ground
5	DRV	Driver output	The current capability of the totem pole gate drive (+0.3/-0.5 A) makes it suitable to effectively drive a broad range of power MOSFETs.
6	VCC	Supplies the controller	This pin is connected to an external auxiliary voltage.
7	VIN	Input voltage sensing Brown-Out	This pin observes the HV rail and is used in valley selection. This pin also monitors and protects for low mains conditions.
8	DIM	Analog / PWM dimming	This pin is used for analog or PWM dimming control. An analog signal than can be varied between $V_{DIM(EN)}$ and V_{DIM100} can be used to vary the current, or a PWM signal with an amplitude greater than V_{DIM100} .

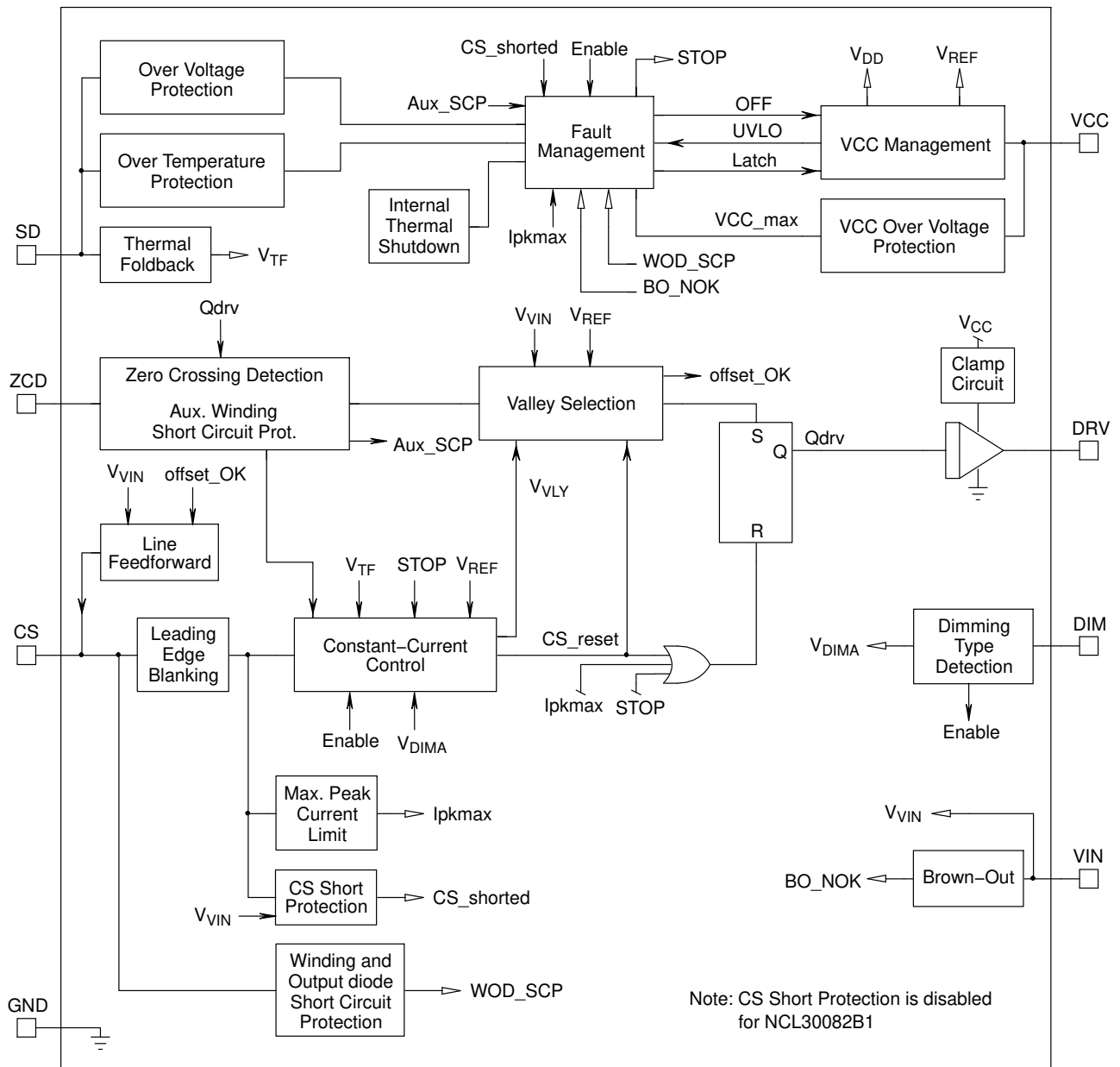


Figure 2. Internal Circuit Architecture

Table 2. MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
$V_{CC(MAX)}$ $I_{CC(MAX)}$	Maximum Power Supply voltage, VCC pin, continuous voltage Maximum current for VCC pin	-0.3, +35 Internally limited	V mA
$V_{DRV(MAX)}$ $I_{DRV(MAX)}$	Maximum driver pin voltage, DRV pin, continuous voltage Maximum current for DRV pin	-0.3, V_{DRV} (Note 1) -500, +800	V mA
V_{MAX} I_{MAX}	Maximum voltage on low power pins (except pins ZCD, DIM, DRV and VCC) Current range for low power pins (except pins ZCD, DRV and VCC)	-0.3, +5.5 -2, +5	V mA
$V_{ZCD(MAX)}$ $I_{ZCD(MAX)}$	Maximum voltage for ZCD pin Maximum current for ZCD pin	-0.3, +10 -2, +5	V mA
$V_{DIM(MAX)}$	Maximum voltage for DIM pin	-0.3, +10	V
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 4) Micro8 version SOIC-8 version	228 180	°C/W
Ψ_{JC}	Thermal Characterization Parameter, Junction-to-Case Top Micro8 version SOIC-8 version	50 45	°C/W
$T_J(MAX)$	Maximum Junction Temperature	150	°C
	Operating Temperature Range	-40 to +125	°C
	Storage Temperature Range	-60 to +150	°C
	ESD Capability, HBM model (Note 2)	4	kV
	ESD Capability, MM model (Note 2)	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- V_{DRV} is the DRV clamp voltage $V_{DRV(high)}$ when V_{CC} is higher than $V_{DRV(high)}$. V_{DRV} is V_{CC} unless otherwise noted.
- This device series contains ESD protection and exceeds the following tests: Human Body Model 4000 V per JEDEC JESD22-A114-F and Machine Model Method 200 V per JEDEC JESD22-A115-A.
- This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78 except for VIN pin which passes 60 mA.
- With a 100 mm², 2 oz copper area based on JEDEC EIA/JESD51-3 board design.

Table 3. ELECTRICAL CHARACTERISTICS (Unless otherwise noted: For typical values $T_J = 25^\circ\text{C}$, $V_{CC} = 12\text{ V}$; For min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, Max $T_J = 150^\circ\text{C}$, $V_{CC} = 12\text{ V}$)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Supply Voltage						V
Startup Threshold	V_{CC} increasing	$V_{CC(on)}$	16	18	20	
Minimum Operating Voltage	V_{CC} decreasing	$V_{CC(off)}$	8.2	8.8	9.4	
Hysteresis $V_{CC(on)} - V_{CC(off)}$	V_{CC} decreasing	$V_{CC(HYS)}$	8	-	-	
Internal logic reset		$V_{CC(reset)}$	3.5	4.5	5.5	
Over Voltage Protection		$V_{CC(OVP)}$	26	28	30	V
$V_{CC(off)}$ noise filter		$t_{VCC(off)}$	-	5	-	μs
$V_{CC(reset)}$ noise filter-		$t_{VCC(reset)}$	-	20	-	
Startup current		$I_{CC(start)}$	-	13	30	μA
Startup current in fault mode		$I_{CC(sFault)}$	-	46	60	μA
Supply Current						mA
Device Disabled/Fault	$V_{CC} > V_{CC(off)}$	I_{CC1}	0.8	1.2	1.4	
Device Enabled/No output load on pin 5	$F_{sw} = 65\text{ kHz}$	I_{CC2}	-	2.3	4.0	
Device Switching ($F_{sw} = 65\text{ kHz}$)	$C_{DRV} = 470\text{ pF}$, $F_{sw} = 65\text{ kHz}$	I_{CC3}	-	2.7	5.0	

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Description	Test Condition	Symbol	Min	Typ	Max	Unit
CURRENT SENSE						
Maximum Internal current limit		V_{ILIM}	0.95	1	1.05	V
Leading Edge Blanking Duration for V_{ILIM} ($T_J = -25^\circ\text{C}$ to 125°C) (Not applicable for NCL30082D)		t_{LEB}	250	300	350	ns
Leading Edge Blanking Duration for V_{ILIM} ($T_J = -40^\circ\text{C}$ to 125°C)		t_{LEB}	240	300	350	ns
Input Bias Current	DRV high	I_{bias}	–	0.02	–	μA
Propagation delay from current detection to gate off–state		t_{LIM}	–	50	150	ns
Threshold for immediate fault protection activation		$V_{CS(stop)}$	1.35	1.5	1.65	V
Leading Edge Blanking Duration for $V_{CS(stop)}$		t_{BCS}	–	120	–	ns
Blanking time for CS to GND short detection $V_{pinVIN} = 1\text{ V}$		$t_{CS(blank1)}$	6	–	12	μs
Blanking time for CS to GND short detection $V_{pinVIN} = 1\text{ V}$ NCL30082D		$t_{CS(blank1)D}$	8	10.7	14	μs
Blanking time for CS to GND short detection $V_{pinVIN} = 3.3\text{ V}$		$t_{CS(blank2)}$	2	–	4	μs
Blanking time for CS to GND short detection $V_{pinVIN} = 3.3\text{ V}$ NCL30082D		$t_{CS(blank2)D}$	2.6	3.6	4.6	μs
GATE DRIVE						
Drive Resistance DRV Sink DRV Source		R_{SNK} R_{SRC}	– –	13 30	– –	Ω
Drive current capability DRV Sink (Note 6) DRV Source (Note 6)		I_{SNK} I_{SRC}	– –	500 300	– –	mA
Rise Time (10% to 90%)	$C_{DRV} = 470\text{ pF}$	t_r	–	40	–	ns
Fall Time (90% to 10%)	$C_{DRV} = 470\text{ pF}$	t_f	–	30	–	ns
DRV Low Voltage	$V_{CC} = V_{CC(off)} + 0.2\text{ V}$ $C_{DRV} = 470\text{ pF}$, $R_{DRV} = 33\text{ k}\Omega$	$V_{DRV(low)}$	8	–	–	V
DRV High Voltage	$V_{CC} = 30\text{ V}$ $C_{DRV} = 470\text{ pF}$, $R_{DRV} = 33\text{ k}\Omega$	$V_{DRV(high)}$	10	12	14	V

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Description	Test Condition	Symbol	Min	Typ	Max	Unit
ZERO VOLTAGE DETECTION CIRCUIT						
ZCD threshold voltage	V_{ZCD} increasing	$V_{ZCD(THI)}$	25	45	65	mV
ZCD threshold voltage (Note 6)	V_{ZCD} decreasing	$V_{ZCD(THD)}$	5	25	45	mV
ZCD hysteresis (Note 6)	V_{ZCD} increasing	$V_{ZCD(HYS)}$	10	–	–	mV
Threshold voltage for output short circuit or aux. winding short circuit detection		$V_{ZCD(short)}$	0.8	1	1.2	V
Short circuit detection Timer	$V_{ZCD} < V_{ZCD(short)}$	$t_{OVL D}$	70	90	110	ms
Auto-recovery timer duration		$t_{recovery}$	3	4	5	s
Input clamp voltage High state Low state	$I_{pin1} = 3.0\text{ mA}$ $I_{pin1} = -2.0\text{ mA}$	V_{CH} V_{CL}	– –0.9	9.5 –0.6	– –0.3	V
Propagation Delay from valley detection to DRV high	V_{ZCD} decreasing	t_{DEM}	–	–	150	ns
Equivalent time constant for ZCD input (Note 6)		t_{PAR}	–	20	–	ns
Blanking delay after on-time		t_{BLANK}	2.25	3	3.75	μs
Blanking delay after on-time NCL30082B2 and NCL30082B3		$t_{BLANKB2}$	1.2	1.6	2.0	μs
Timeout after last demag transition		t_{TIMO}	5	6.5	8	μs

CONSTANT CURRENT CONTROL

Reference Voltage at $T_J = 25^\circ\text{C}$		V_{REF}	245	250	255	mV
Reference Voltage $T_J = -40^\circ\text{C}$ to 125°C		V_{REF}	242.5	250	257.5	mV
Reference Voltage NCL30082D ($T_J = 25^\circ\text{C}$)		V_{REFD}	495	500	505	mV
Reference Voltage NCL30082D ($T_J = 0^\circ\text{C}$ to 85°C)		V_{REFD}	492	500	508	mV
Reference Voltage NCL30082D ($T_J = -40^\circ\text{C}$ to 125°C)		V_{REFD}	488	500	512	mV
Reference Voltage NCL30082B3 ($T_J = 25^\circ\text{C}$)		V_{REFB3}	329	333	337	mV
Reference Voltage NCL30082B3 ($T_J = 0^\circ\text{C}$ to 85°C)		V_{REFB3}	325	333	341	mV
Reference Voltage NCL30082B3 ($T_J = -40^\circ\text{C}$ to 125°C)		V_{REFB3}	321	333	345	mV
50% reference voltage (for thermal foldback)		V_{REF50}	–	125	–	mV
25% reference voltage (for thermal foldback) NCL30082D		V_{REF25D}	–	125	–	mV
Current sense lower threshold for detection of the leakage inductance reset time		$V_{CS(low)}$	30	55	80	mV

LINE FEED-FORWARD

V_{VIN} to $I_{CS(offset)}$ conversion ratio		K_{LFF}	15	17	19	$\mu\text{A/V}$
Offset current maximum value	$V_{pinVIN} = 4.5\text{ V}$	$I_{offset(MAX)}$	67.5	76.5	85.5	μA
V_{REF} value below which the offset current source is turned off	V_{REF} decreases	$V_{REF(off)}$	–	37.5	–	mV
V_{REF} value above which the offset current source is turned on	V_{REF} increases	$V_{REF(on)}$	–	50	–	mV

VALLEY SELECTION

Threshold for line range detection V_{in} increasing (1 st to 2 nd valley transition for $V_{REF} > 0.75\text{ V}$)	V_{VIN} increases	V_{HL}	2.28	2.4	2.52	V
Threshold for line range detection V_{in} decreasing (2 nd to 1 st valley transition for $V_{REF} > 0.75\text{ V}$)	V_{VIN} decreases	V_{LL}	2.18	2.3	2.42	V
Blanking time for line range detection		$t_{HL(blank)}$	15	25	35	ms

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Description	Test Condition	Symbol	Min	Typ	Max	Unit
VALLEY SELECTION						
Valley thresholds						mV
1 st to 2 nd valley transition at LL and 2 nd to 3 rd valley HL	V_{REF} decreases	$V_{VLY1-2/2-3}$	177.5	187.5	197.5	
2 nd to 1 st valley transition at LL and 3 rd to 2 nd valley HL	V_{REF} increases	$V_{VLY2-1/3-2}$	185.0	195.0	205.0	
2 nd to 4 th valley transition at LL and 3 rd to 5 th valley HL	V_{REF} decreases	$V_{VLY2-4/3-5}$	117.5	125.0	132.5	
4 th to 2 nd valley transition at LL and 5 th to 3 rd valley HL	V_{REF} increases	$V_{VLY4-2/5-3}$	125.0	132.5	140.0	
4 th to 7 th valley transition at LL and 5 th to 8 th valley HL	V_{REF} decreases	$V_{VLY4-7/5-8}$	–	75.0	–	
7 th to 4 th valley transition at LL and 8 th to 5 th valley HL	V_{REF} increases	$V_{VLY7-4/8-5}$	–	82.5	–	
7 th to 11 th valley transition at LL and 8 th to 12 th valley HL	V_{REF} decreases	$V_{VLY7-11/8-12}$	–	37.5	–	
11 th to 7 th valley transition at LL and 12 th to 8 th valley HL	V_{REF} increases	$V_{VLY11-7/12-8}$	–	50.0	–	
11 th to 13 th valley transition at LL and 12 th to 15 th valley HL	V_{REF} decreases	$V_{VLY11-13/12-15}$	–	15.0	–	
13 th to 11 th valley transition at LL and 15 th to 12 th valley HL	V_{REF} increases	$V_{VLY13-11/15-12}$	–	20.0	–	
DIMMING SECTION						
DIM pin voltage for zero output current (OFF voltage)		$V_{DIM(EN)}$	0.66	0.7	0.74	V
DIM pin voltage for maximum output current		V_{DIM100}	2.25	2.45	2.65	V
Dimming range		$V_{DIM(range)}$	–	1.75	–	V
Clamping voltage for DIM pin		$V_{DIM(CLP)}$	–	7.8	–	V
Dimming pin pull-up current source		$I_{DIM(pullup)}$	–	280	–	nA
THERMAL FOLD-BACK AND OVP						
Reference current for direct connection of an NTC (Note 6)		$I_{OTP(REF)}$	80	85	90	
SD pin voltage at which thermal fold-back starts		$V_{TF(start)}$	0.9	1	1.1	V
SD pin voltage at which thermal fold-back stops ($I_{out} = 50\% I_{out(nom)}$)		$V_{TF(stop)}$	0.64	0.68	0.72	V
SD pin voltage at which thermal fold-back stops NCL30082D ($I_{out} = 25\% I_{out(nom)}$)		$V_{TF(stop)D}$	0.86	0.90	0.94	V
Reference current for direct connection of an NTC		$I_{OTP(REF)}$	80	85	90	μA
Fault detection level for OTP	V_{SD} decreasing	$V_{OTP(off)}$	0.47	0.5	0.53	V
Fault detection level for OTP NCL30082D		$V_{OTP(off)D}$	0.81	0.85	0.89	V
SD pin level at which controller re-start switching after OTP detection	V_{SD} increasing	$V_{OTP(on)}$	0.64	0.68	0.72	V
SD pin level at which controller re-start switching after OTP detection NCL30082D		$V_{OTP(on)D}$	0.86	0.9	0.94	V
SD pin Over temperature Protection Hysteresis NCL30082D		$V_{OTP(hys)D}$	15	50	100	mV
$V_{TF(start)}$ over $I_{OTP(REF)}$ ratio (Note 5)	$T_J = +25^\circ\text{C}$ to $+125^\circ\text{C}$	$R_{TF(start)}$	10.8	11.7	12.6	$\text{k}\Omega$
$V_{TF(stop)}$ over $I_{OTP(REF)}$ ratio (Note 5)	$T_J = +25^\circ\text{C}$ to $+125^\circ\text{C}$	$R_{TF(stop)}$	7.4	8.0	8.6	$\text{k}\Omega$
$V_{OTP(off)}$ over $I_{OTP(REF)}$ ratio (Note 5)	$T_J = +25^\circ\text{C}$ to $+125^\circ\text{C}$	$R_{OTP(off)}$	5.4	5.9	6.4	$\text{k}\Omega$
$V_{OTP(on)}$ over $I_{OTP(REF)}$ ratio (Note 5)	$T_J = +25^\circ\text{C}$ to $+125^\circ\text{C}$	$R_{OTP(on)}$	7.4	8.0	8.6	$\text{k}\Omega$
$V_{TF(stop)}$ over $I_{OTP(REF)}$ ratio NCL30082D (Note 5)	$T_J = +25^\circ\text{C}$ to $+125^\circ\text{C}$	$R_{TF(stop)D}$	9.9	10.5	11.1	$\text{k}\Omega$
$V_{OTP(off)}$ over $I_{OTP(REF)}$ ratio NCL30082D (Note 5)	$T_J = +25^\circ\text{C}$ to $+125^\circ\text{C}$	$R_{OTP(off)D}$	9.4	10.0	10.6	$\text{k}\Omega$
$V_{OTP(on)}$ over $I_{OTP(REF)}$ ratio NCL30082D (Note 5)	$T_J = +25^\circ\text{C}$ to $+125^\circ\text{C}$	$R_{OTP(on)D}$	9.9	10.5	11.1	$\text{k}\Omega$

5. A NTC is generally placed between the SD and GND pins. Parameters $R_{TF(start)}$, $R_{TF(stop)}$, $R_{OTP(off)}$ and $R_{OTP(on)}$ give the resistance the NTC must exhibit to respectively, enter thermal foldback, stop thermal foldback, trigger the OTP limit and allow the circuit recovery after an OTP situation.

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NCL30082

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Description	Test Condition	Symbol	Min	Typ	Max	Unit
THERMAL FOLD-BACK AND OVP						
Timer duration after which the controller is allowed to start pulsing		$t_{OTP(\text{start})}$	180	–	300	μs
Clamped voltage (SD pin left open)	SD pin open	$V_{SD(\text{clamp})}$	1.13	1.35	1.57	V
Clamp series resistor		$R_{SD(\text{clamp})}$	–	1.6	–	$\text{k}\Omega$
SD pin detection level for OVP	V_{SD} increasing	V_{OVP}	2.35	2.5	2.65	V
Delay before OVP or OTP confirmation (OVP and OTP)		$T_{SD(\text{delay})}$	15	30	45	μs
THERMAL SHUTDOWN						
Thermal Shutdown (Note 6)	Device switching (F_{SW} around 65 kHz)	T_{SHDN}	130	150	170	$^\circ\text{C}$
Thermal Shutdown Hysteresis (Note 6)		$T_{SHDN(\text{HYS})}$	–	50	–	$^\circ\text{C}$
BROWN-OUT						
Brown-Out ON level (IC start pulsing)	V_{SD} increasing	$V_{BO(\text{on})}$	0.90	1	1.10	V
Brown-Out OFF level (IC shuts down)	V_{SD} decreasing	$V_{BO(\text{off})}$	0.85	0.9	0.95	V
BO comparators delay		$t_{BO(\text{delay})}$	–	30	–	μs
Brown-Out blanking time		$t_{BO(\text{blank})}$	35	50	65	ms
Brown-Out blanking time NCL30082D		$t_{BO(\text{blank})D}$	10.5	15	19.5	ms
Brown-out pin bias current		$I_{BO(\text{bias})}$	–250	–	250	nA

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TYPICAL CHARACTERISTICS

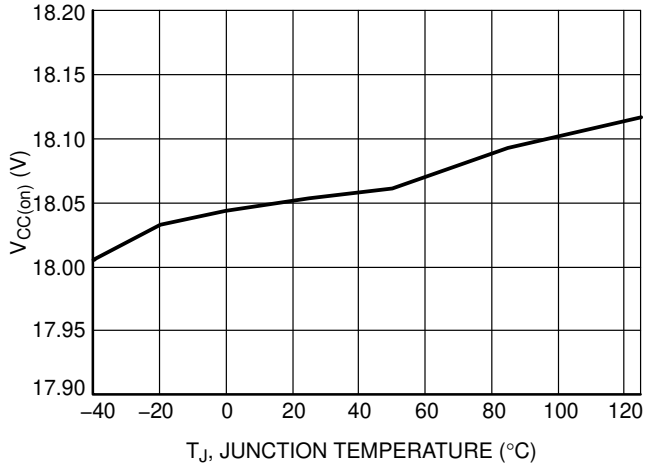


Figure 3. V_{CC(on)} vs. Junction Temperature

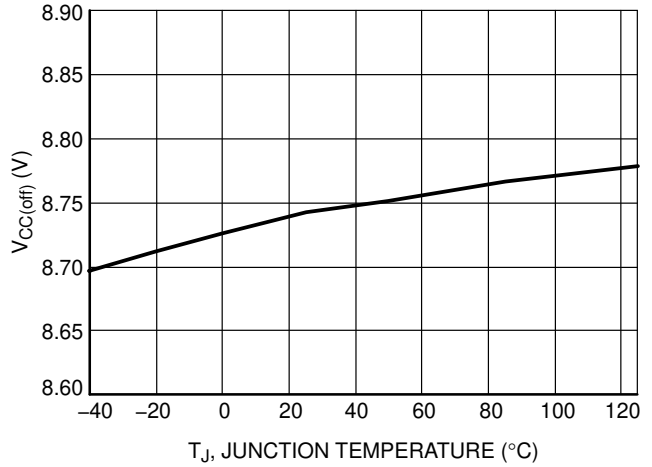


Figure 4. V_{CC(off)} vs. Junction Temperature

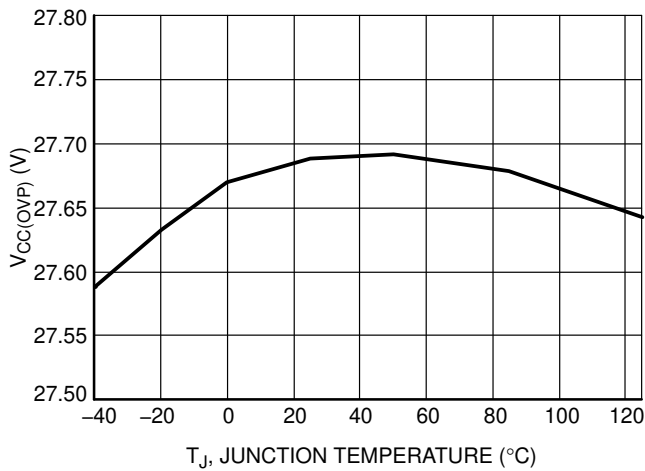


Figure 5. V_{CC(OVP)} vs. Junction Temperature

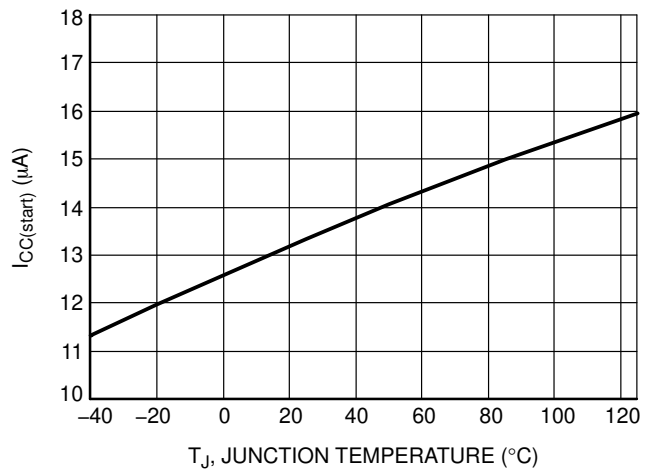


Figure 6. I_{CC(start)} vs. Junction Temperature

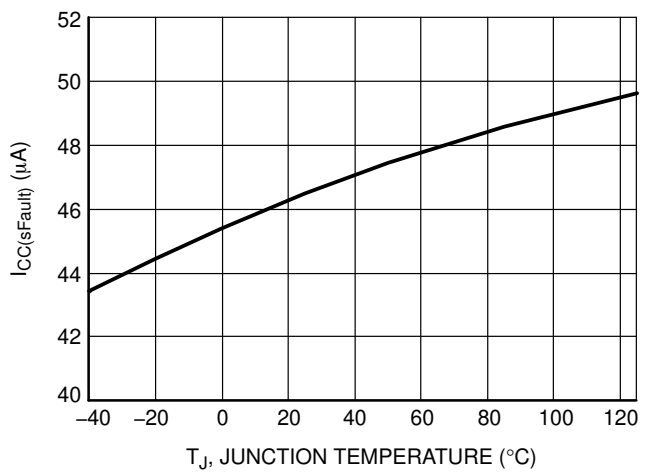


Figure 7. I_{CC(sFault)} vs. Junction Temperature

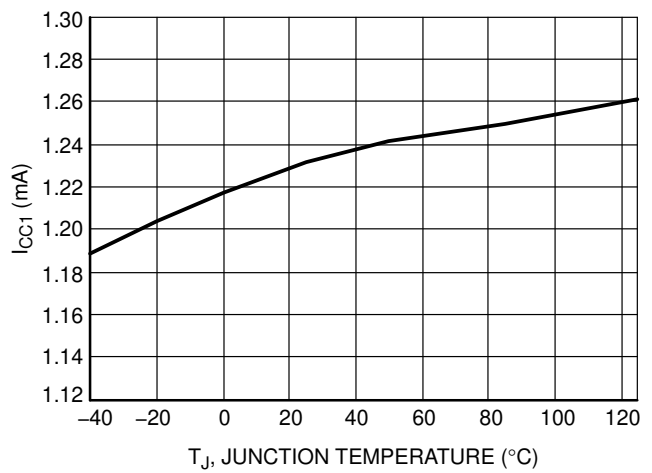


Figure 8. I_{CC1} vs. Junction Temperature

TYPICAL CHARACTERISTICS

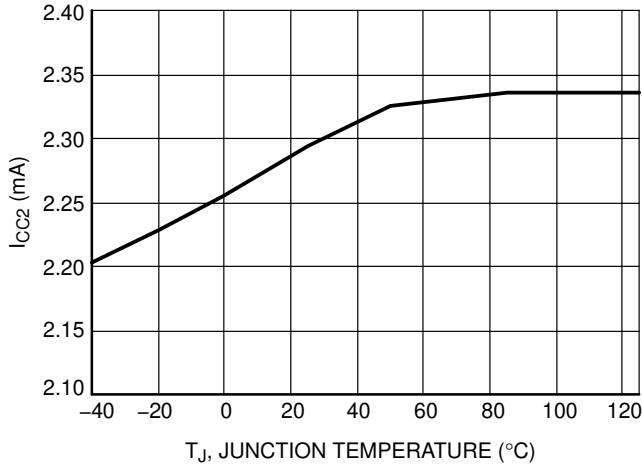


Figure 9. I_{CC2} vs. Junction Temperature

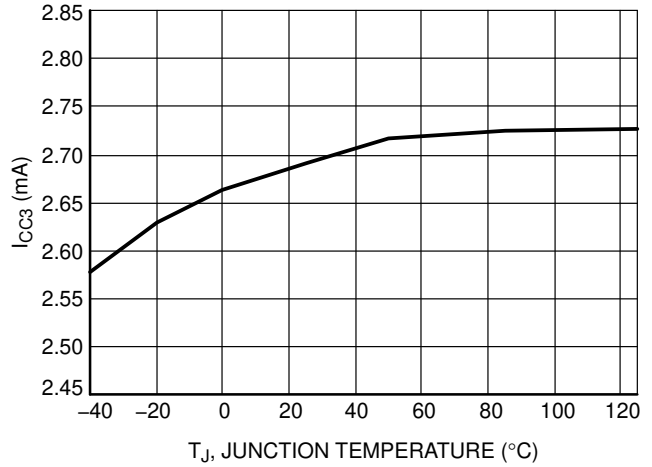


Figure 10. I_{CC3} vs. Junction Temperature

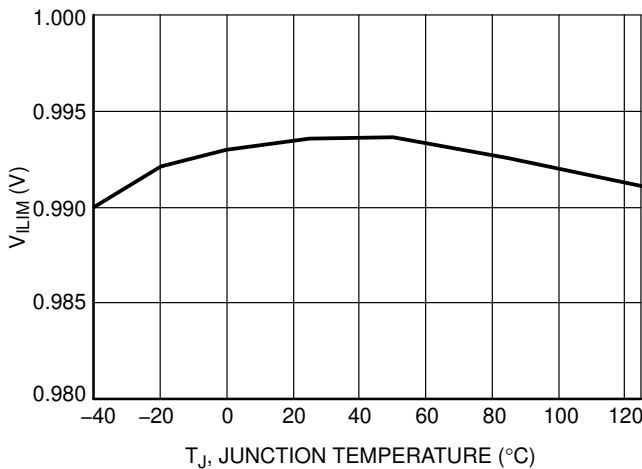


Figure 11. V_{ILIM} vs. Junction Temperature

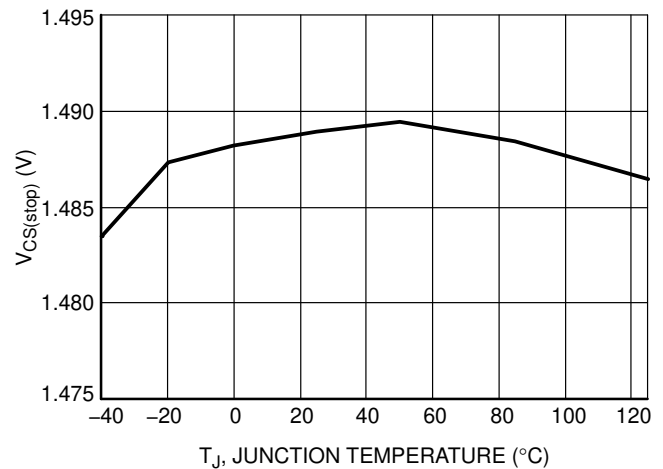


Figure 12. $V_{CS(stop)}$ vs. Junction Temperature

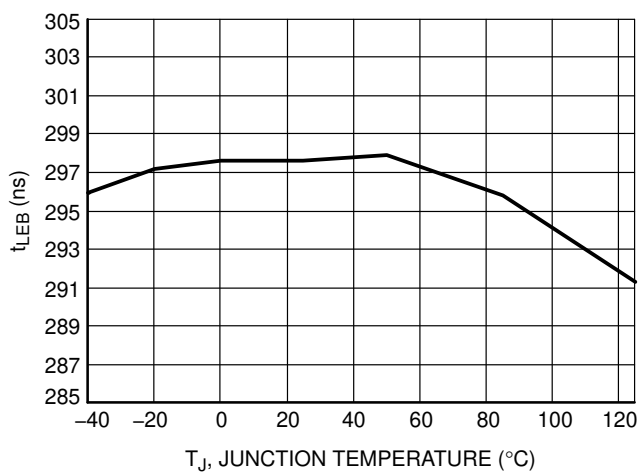


Figure 13. t_{LEB} vs. Junction Temperature

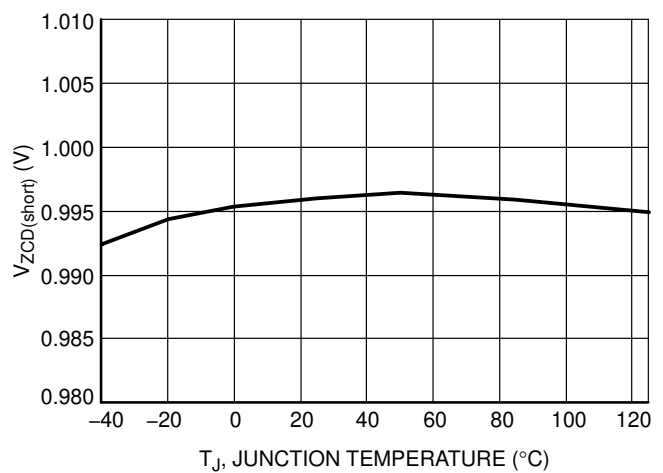


Figure 14. $V_{ZCD(short)}$ vs. Junction Temperature

TYPICAL CHARACTERISTICS

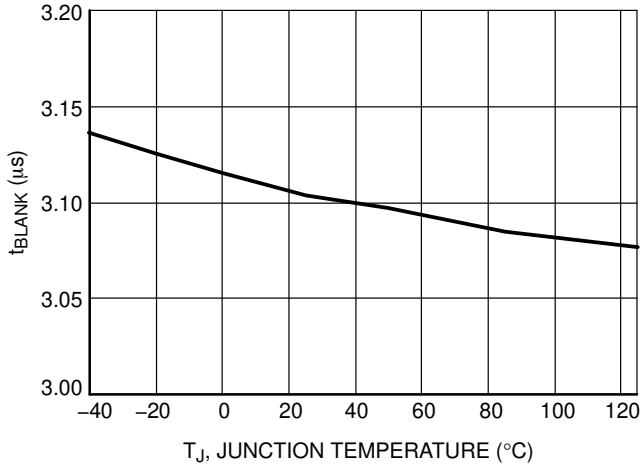


Figure 15. t_{BLANK} vs. Junction Temperature

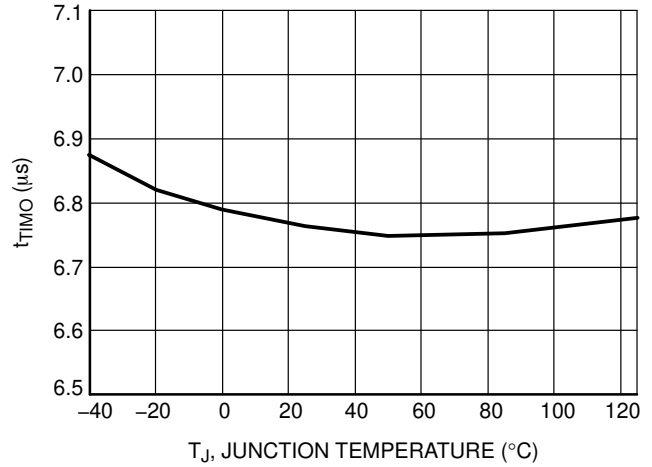


Figure 16. t_{TIMO} vs. Junction Temperature

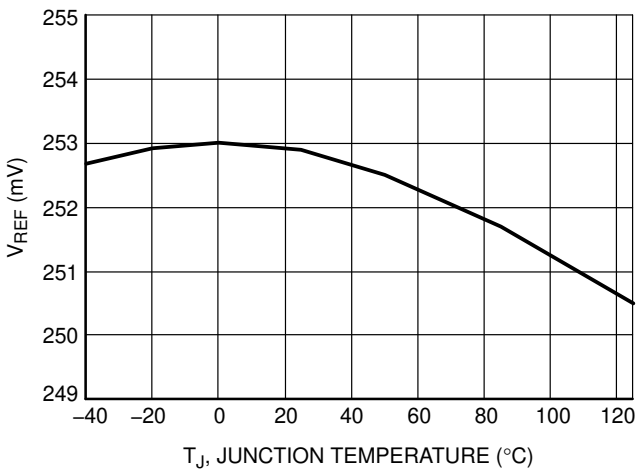


Figure 17. V_{REF} vs. Junction Temperature

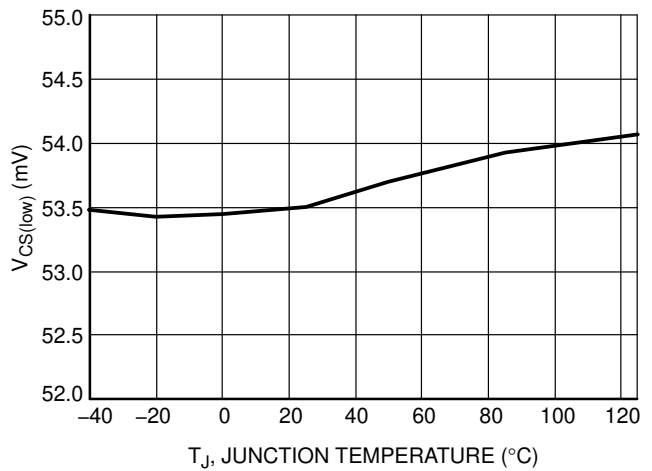


Figure 18. $V_{CS(low)}$ vs. Junction Temperature

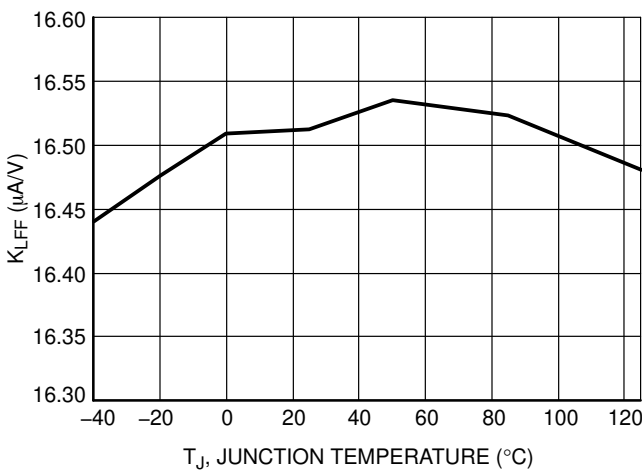


Figure 19. K_{LFF} vs. Junction Temperature

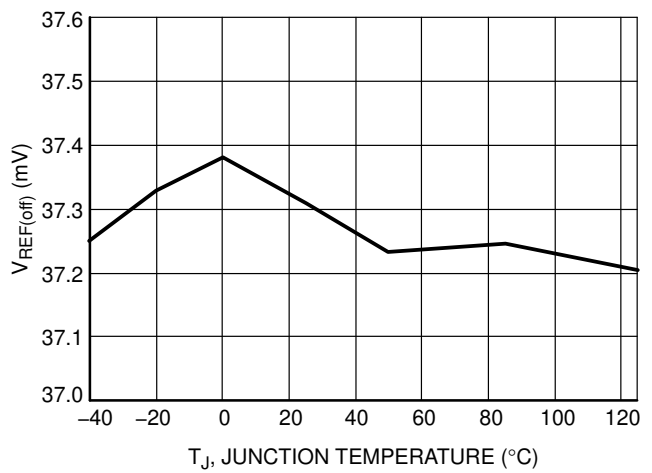


Figure 20. $V_{REF(off)}$ vs. Junction Temperature

TYPICAL CHARACTERISTICS

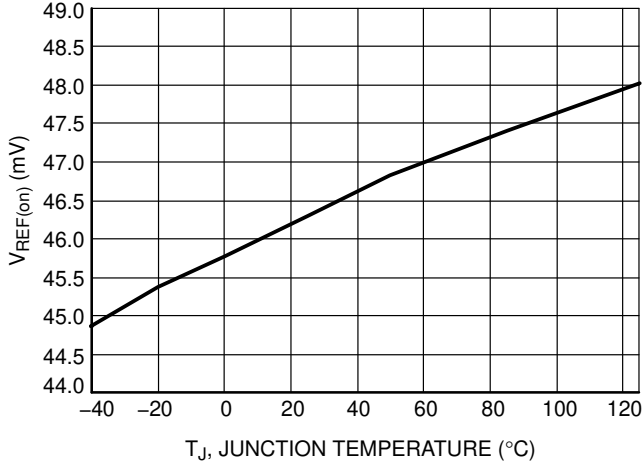


Figure 21. V_{REF(on)} vs. Junction Temperature

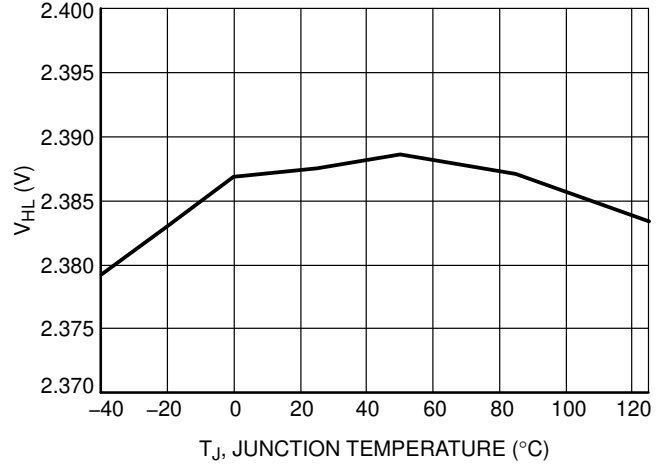


Figure 22. V_{HL} vs. Junction Temperature

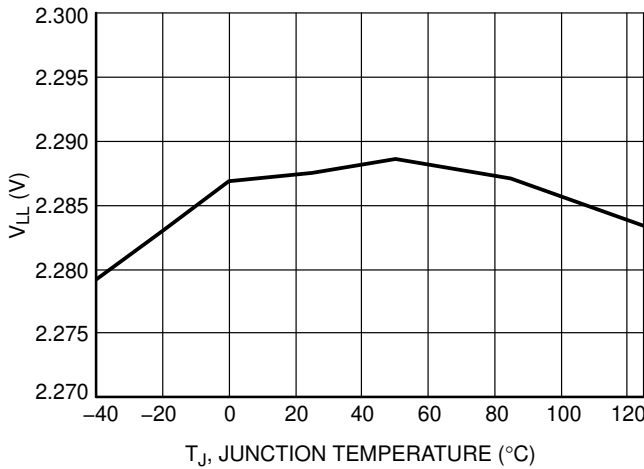


Figure 23. V_{LL} vs. Junction Temperature

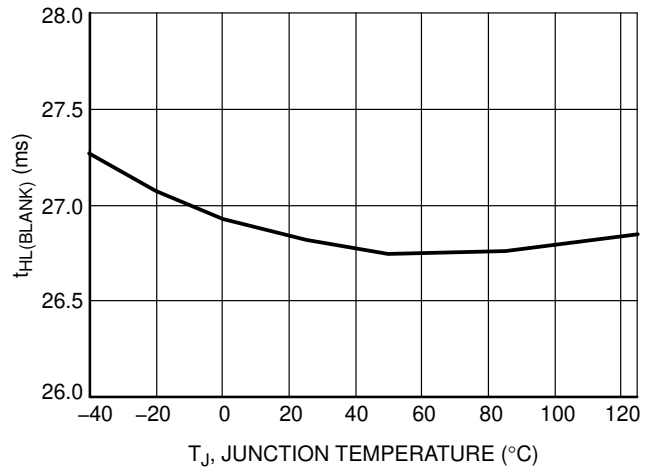


Figure 24. t_{HL(BLANK)} vs. Junction Temperature

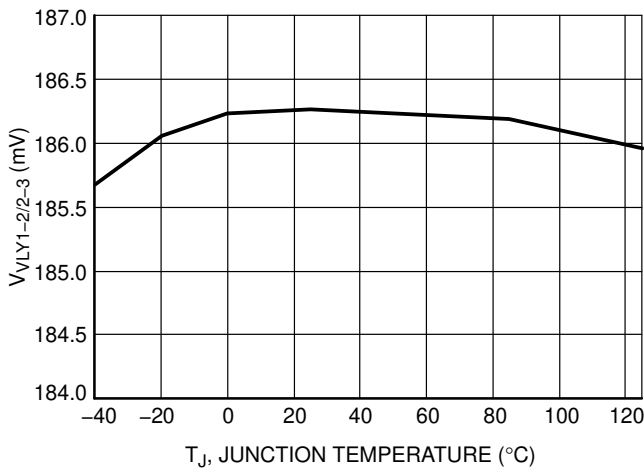


Figure 25. V_{VLY1-2/2-3} vs. Junction Temperature

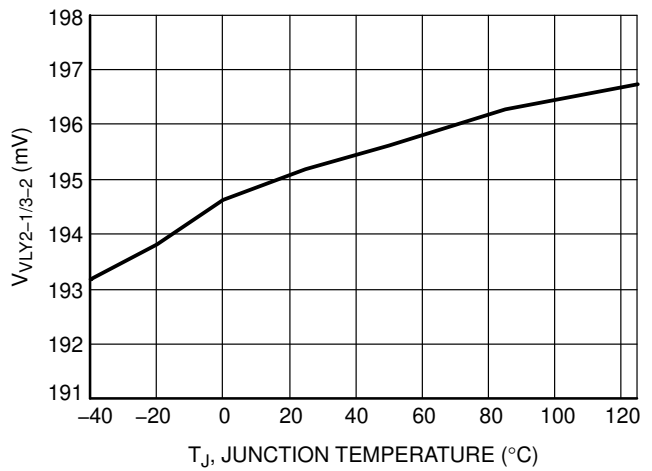


Figure 26. V_{VLY2-1/3-2} vs. Junction Temperature

TYPICAL CHARACTERISTICS

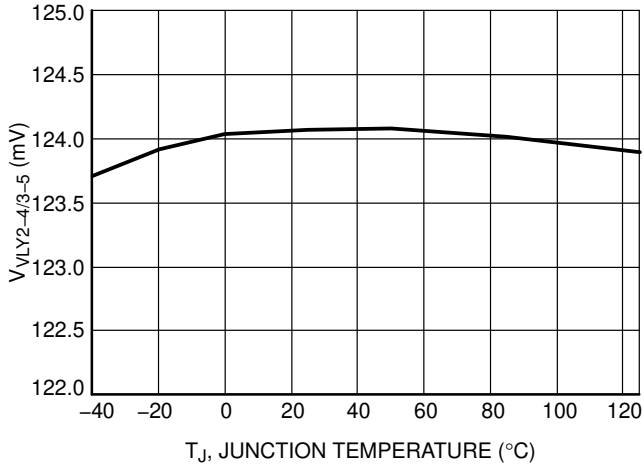


Figure 27. $V_{VLY2-4/3-5}$ vs. Junction Temperature

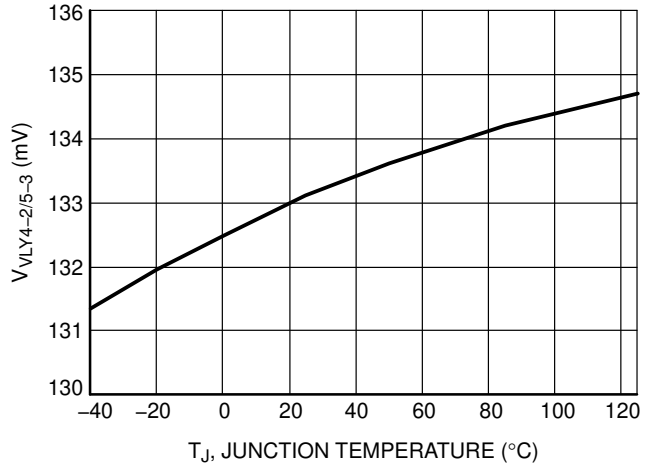


Figure 28. $V_{VLY4-2/5-3}$ vs. Junction Temperature

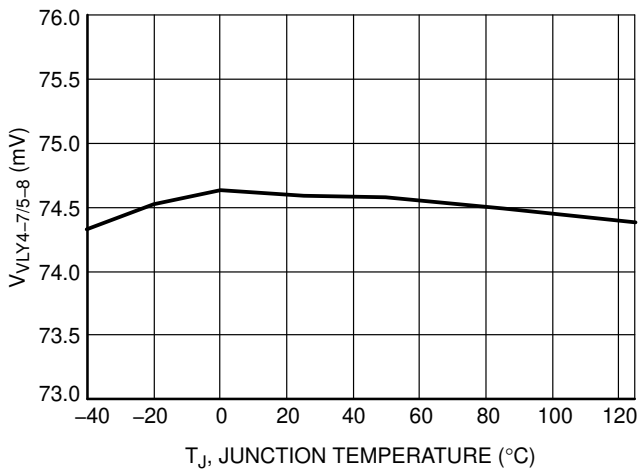


Figure 29. $V_{VLY4-7/5-8}$ vs. Junction Temperature

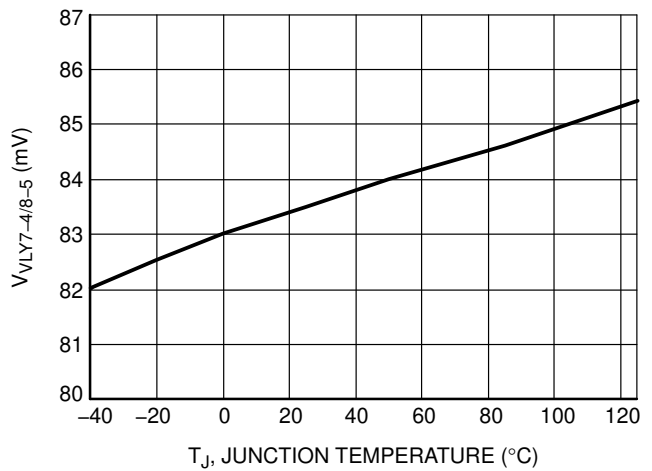


Figure 30. $V_{VLY7-4/8-5}$ vs. Junction Temperature

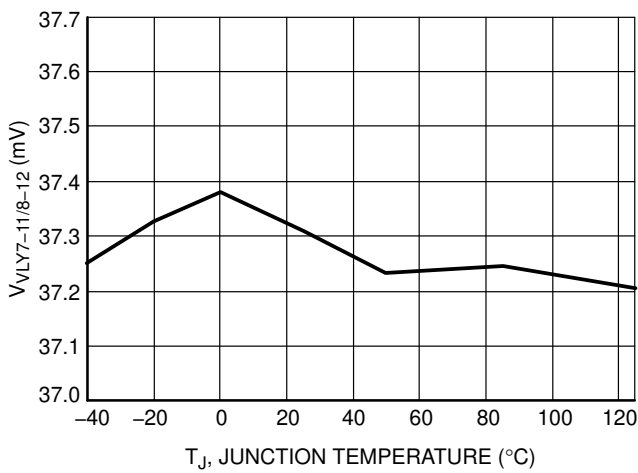


Figure 31. $V_{VLY7-11/8-12}$ vs. Junction Temperature

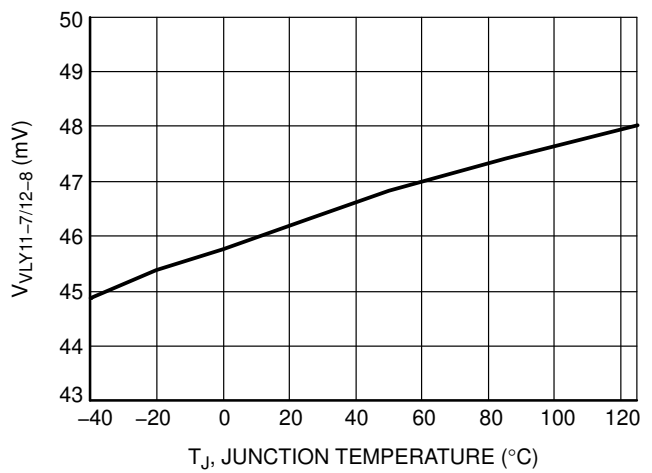


Figure 32. $V_{VLY11-7/12-8}$ vs. Junction Temperature

TYPICAL CHARACTERISTICS

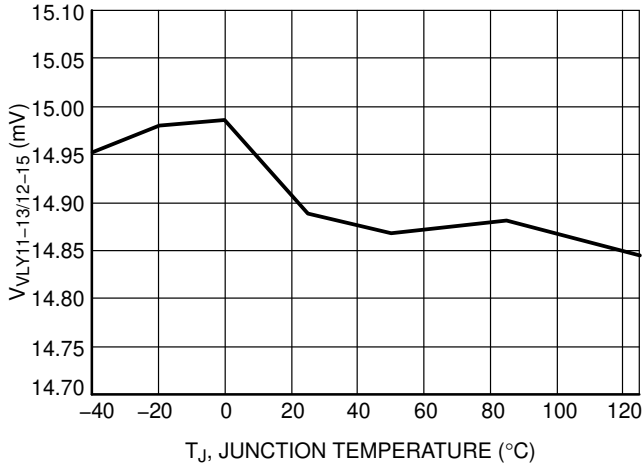


Figure 33. V_{VLY11-13/12-15} vs. Junction Temperature

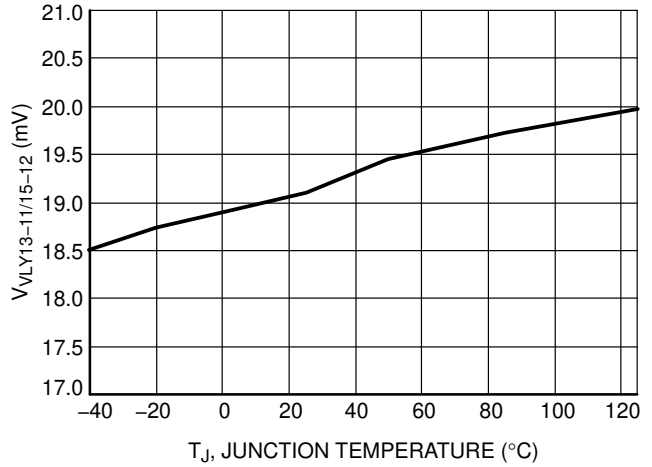


Figure 34. V_{VLY13-11/15-12} vs. Junction Temperature

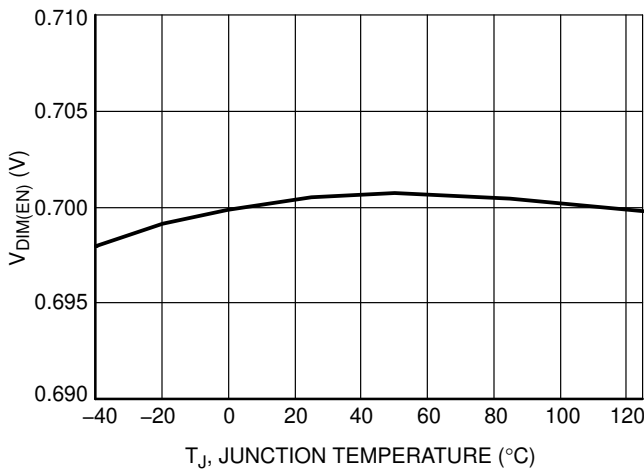


Figure 35. V_{DIM(EN)} vs. Junction Temperature

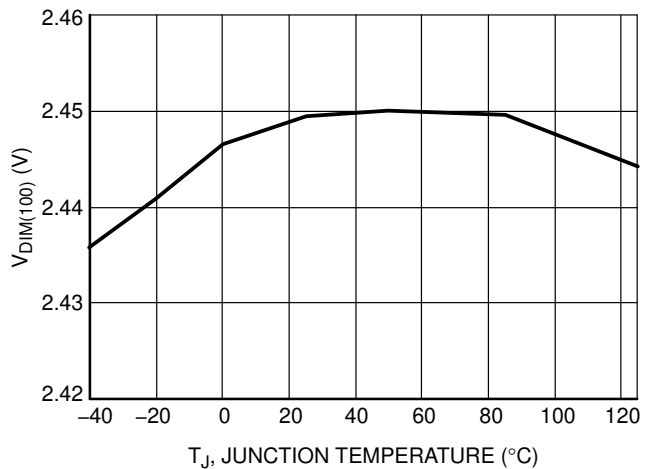


Figure 36. V_{DIM(100)} vs. Junction Temperature

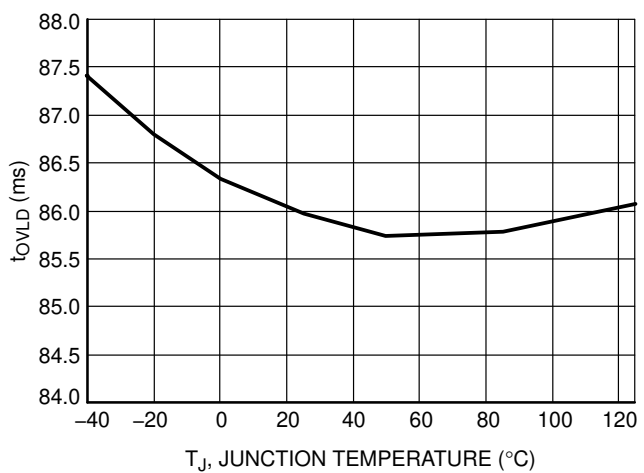


Figure 37. t_{OVLD} vs. Junction Temperature

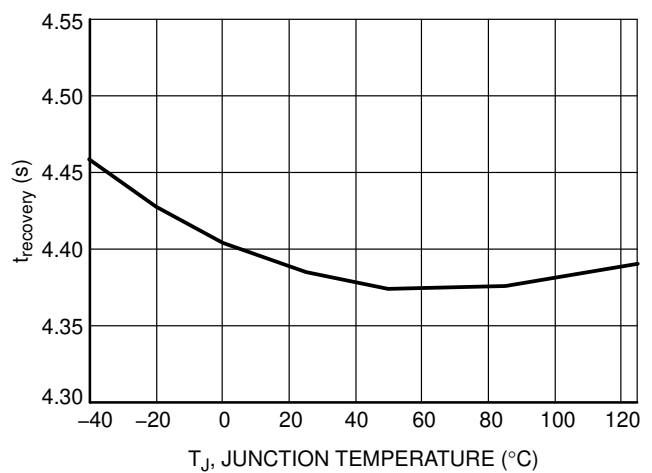


Figure 38. t_{recovery} vs. Junction Temperature

TYPICAL CHARACTERISTICS

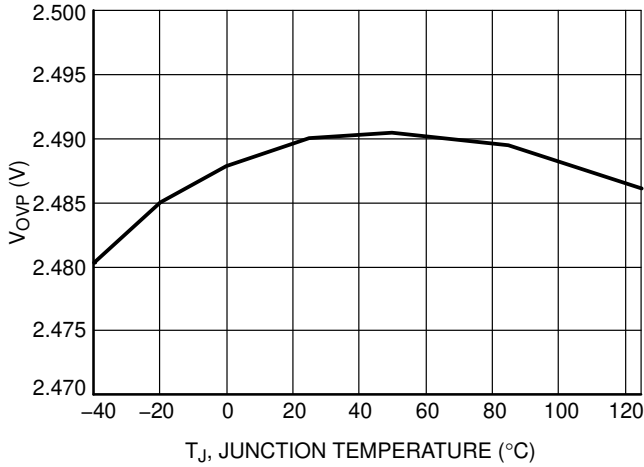


Figure 39. V_{OVP} vs. Junction Temperature

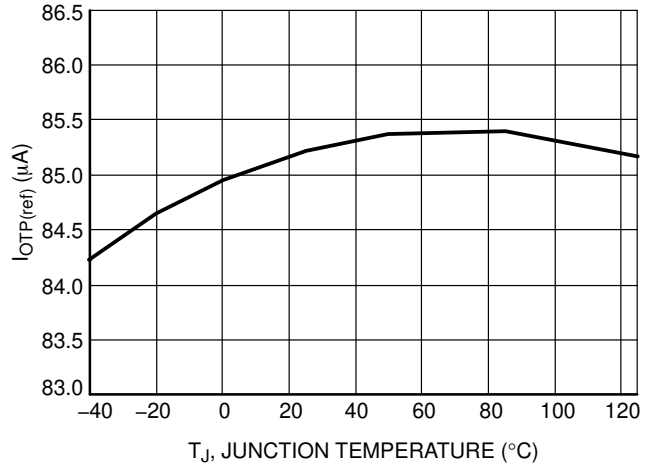


Figure 40. $I_{OTP(ref)}$ vs. Junction Temperature

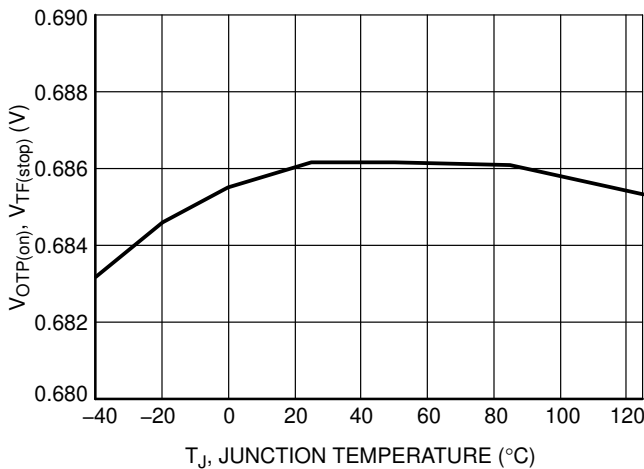


Figure 41. $V_{OTP(on)}$, $V_{TF(stop)}$ vs. Junction Temperature

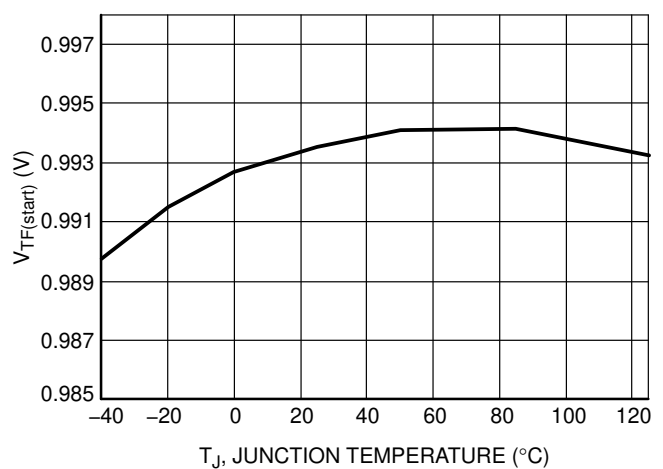


Figure 42. $V_{TF(start)}$ vs. Junction Temperature

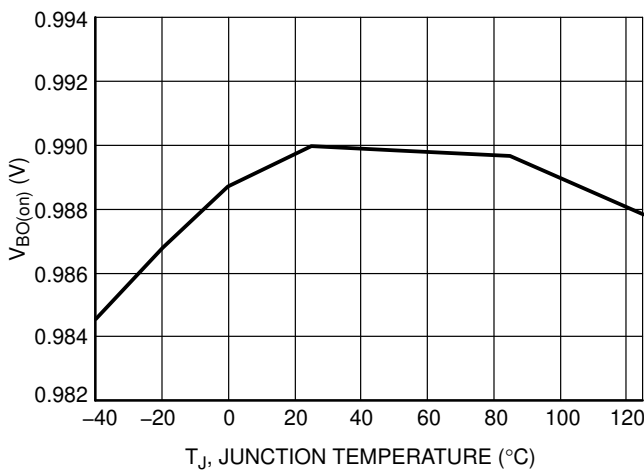


Figure 43. $V_{BO(on)}$ vs. Junction Temperature

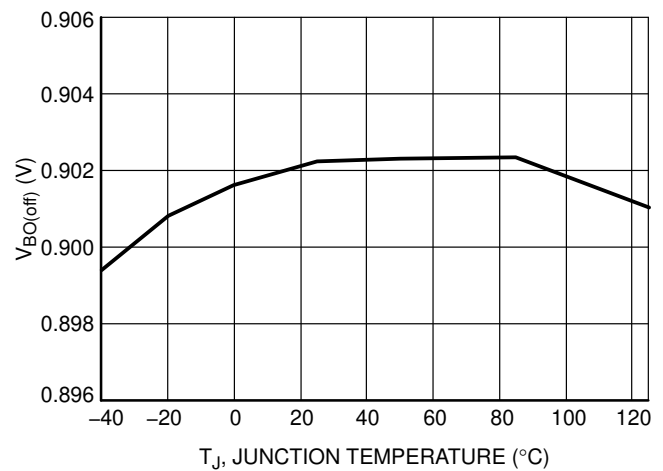


Figure 44. $V_{BO(off)}$ vs. Junction Temperature

TYPICAL CHARACTERISTICS

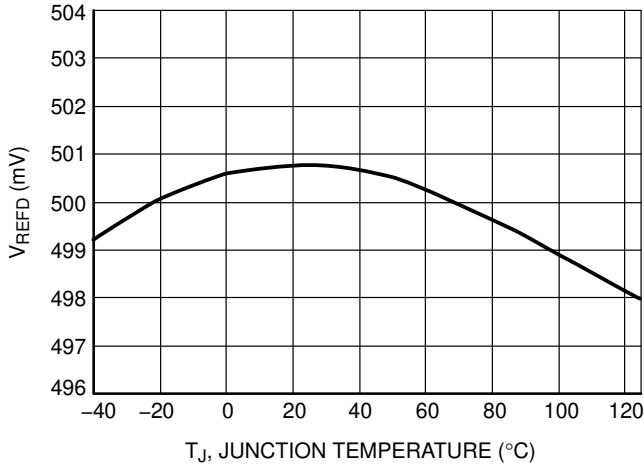


Figure 45. V_{REFD} vs. Junction Temperature

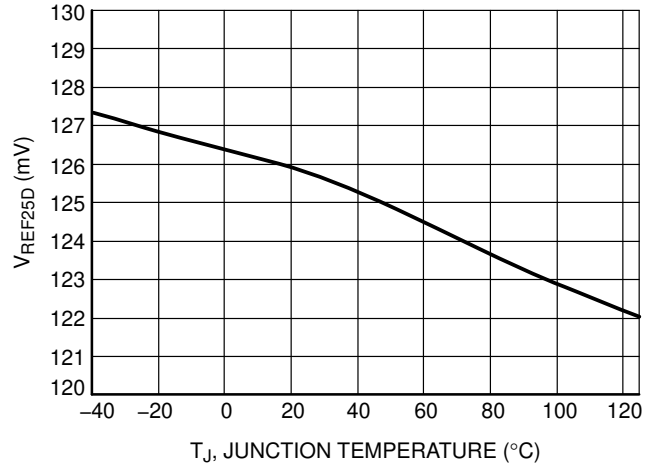


Figure 46. V_{REF25D} vs. Junction Temperature

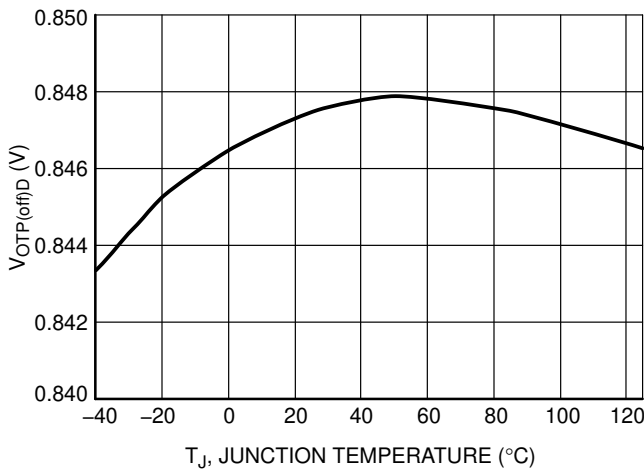


Figure 47. V_{OTP(off)D} vs. Junction Temperature

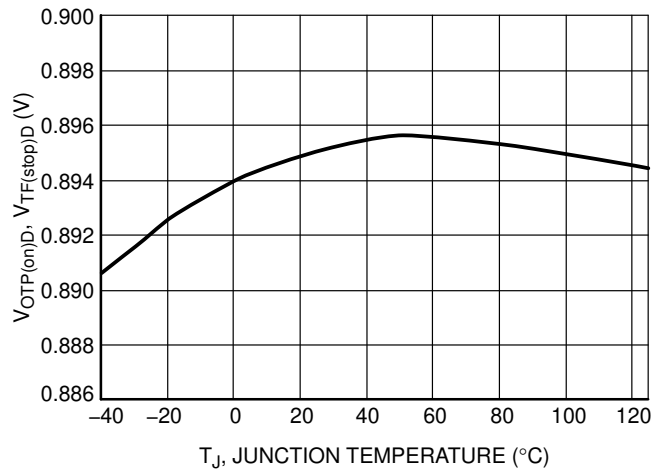


Figure 48. V_{OTP(on)D}, V_{TF(stop)D} vs. Junction Temperature

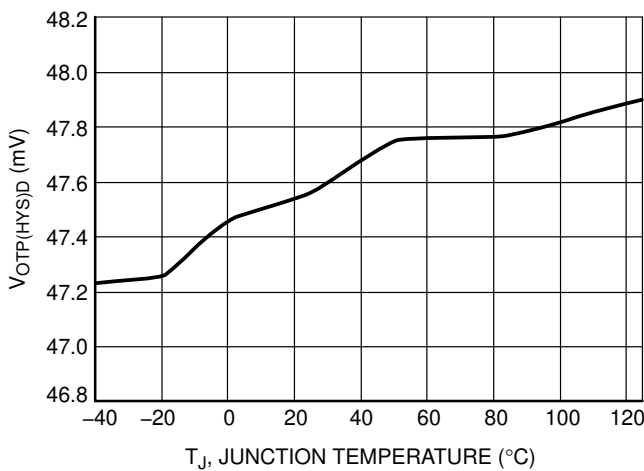


Figure 49. V_{OTP(HYS)D} vs. Junction Temperature

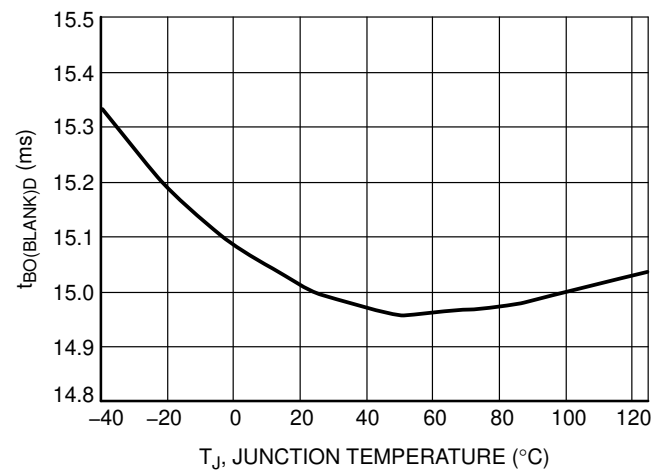
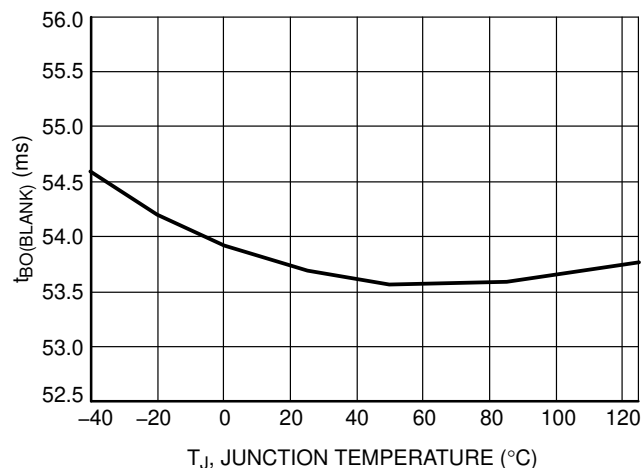


Figure 50. t_{BO(BLANK)D} vs. Junction Temperature

TYPICAL CHARACTERISTICS

Figure 51. t_{BO(BLANK)} vs. Junction Temperature

APPLICATION INFORMATION

The NCL30082 implements a current-mode architecture operating in quasi-resonant mode. Thanks to proprietary circuitry, the controller is able to accurately regulate the secondary side current of the flyback converter without using any opto-coupler or measuring directly the secondary side current.

- **Quasi-Resonance Current-Mode Operation:** implementing quasi-resonance operation in peak current-mode control, the NCL30082 optimizes the efficiency by switching in the valley of the MOSFET drain-source voltage. Thanks to a smart control algorithm, the controller locks-out in a selected valley and remains locked until the input voltage or the output current set point significantly changes.
- **Primary Side Constant Current Control:** thanks to a proprietary circuit, the controller is able to compensate for the leakage inductance of the transformer and allow accurate control of the secondary side current.
- **Line Feed-forward:** compensation for possible variation of the output current caused by system slew rate variation.
- **Open LED protection:** if the voltage on the VCC pin exceeds an internal limit, the controller shuts down and waits 4 seconds before restarting switching.
- **Thermal Fold-back / Over Temperature / Over Voltage Protection:** by combining a dual threshold on the SD pin, the controller allows the direct connection of an NTC to ground plus a Zener diode to a monitored voltage. The temperature is monitored and the output current is linearly reduced in the event that the

temperature exceeds a prescribed level. If the temperature continues to increase, the current will be further reduced until the controller is stopped. The control will automatically restart if the temperature is reduced. This pin can implement a programmable OVP shutdown that can also auto-restart the device.

- **Brown-Out:** the controller includes a brown-out circuit which safely stops the controller in case the input voltage is too low. The device will automatically restart if the line recovers.
- **Cycle-by-cycle peak current limit:** when the current sense voltage exceeds the internal threshold V_{ILIM}, the MOSFET is turned off for the rest of the switching cycle.
- **Winding Short-Circuit Protection:** an additional comparator with a short LEB filter (t_{BCS}) senses the CS signal and stops the controller if V_{CS} reaches 1.5 x V_{ILIM}. For noise immunity reasons, this comparator is enabled only during the main LEB duration t_{LEB}.
- **Output Short-circuit protection:** If a very low voltage is applied on ZCD pin for 90 ms (nominal), the controllers assume that the output or the ZCD pin is shorted to ground and enters shutdown. The auto-restart version (B suffix) waits 4 seconds, then the controller restarts switching. In the latched version (A suffix), the controller is latched as long as V_{CC} stays above the V_{CC(reset)} threshold.
- **Linear or PWM dimming:** the DIM pin allows implementing both analog and PWM dimming.

Constant Current Control

Figure 53 portrays the primary and secondary current of a flyback converter in discontinuous conduction mode (DCM). Figure 52 shows the basic circuit of a flyback converter.

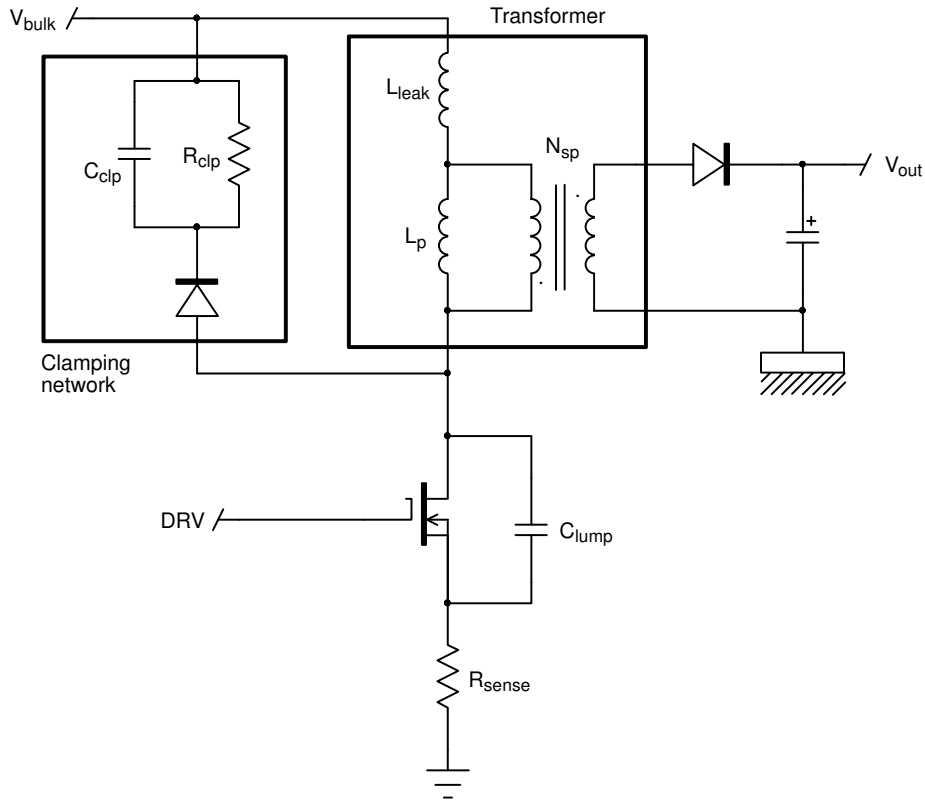


Figure 52. Basic Flyback Converter Schematic

During the on-time of the MOSFET, the bulk voltage V_{bulk} is applied to the magnetizing and leakage inductors L_p and L_{leak} and the current ramps up.

When the MOSFET is turned-off, the inductor current first charges C_{lump} . The output diode is off until the voltage across L_p reverses and reaches:

$$N_{sp}(V_{out} + V_f) \tag{eq. 1}$$

The output diode current increase is limited by the leakage inductor. As a consequence, the secondary peak current is reduced:

$$I_{D,pk} < \frac{I_{L,pk}}{N_{sp}} \tag{eq. 2}$$

The diode current reaches its peak when the leakage inductor is reset. Thus, in order to accurately regulate the output current, we need to take into account the leakage inductor current. This is accomplished by sensing the clamping network current. Practically, a node of the clamp capacitor is connected to R_{sense} instead of the bulk voltage V_{bulk} . Then, by reading the voltage on the CS pin, we have an image of the primary current (red curve in Figure 53).

When the diode conducts, the secondary current decreases linearly from $I_{D,pk}$ to zero. When the diode current has turned off, the drain voltage begins to oscillate because of the resonating network formed by the inductors ($L_p + L_{leak}$) and the lump capacitor. This voltage is reflected on the auxiliary winding wired in flyback mode. Thus, by looking at the auxiliary winding voltage, we can detect the end of the conduction time of secondary diode. The constant current control block picks up the leakage inductor current, the end of conduction of the output rectifier and controls the drain current to maintain the output current constant.

We have:

$$I_{out} = \frac{V_{REF}}{2N_{sp}R_{sense}} \tag{eq. 3}$$

The output current value is set by choosing the sense resistor:

$$R_{sense} = \frac{V_{ref}}{2N_{sp}I_{out}} \tag{eq. 4}$$

From Equation 3, the first key point is that the output current is independent of the inductor value. Moreover, the leakage inductance does not influence the output current value as the reset time is taken into account by the controller.

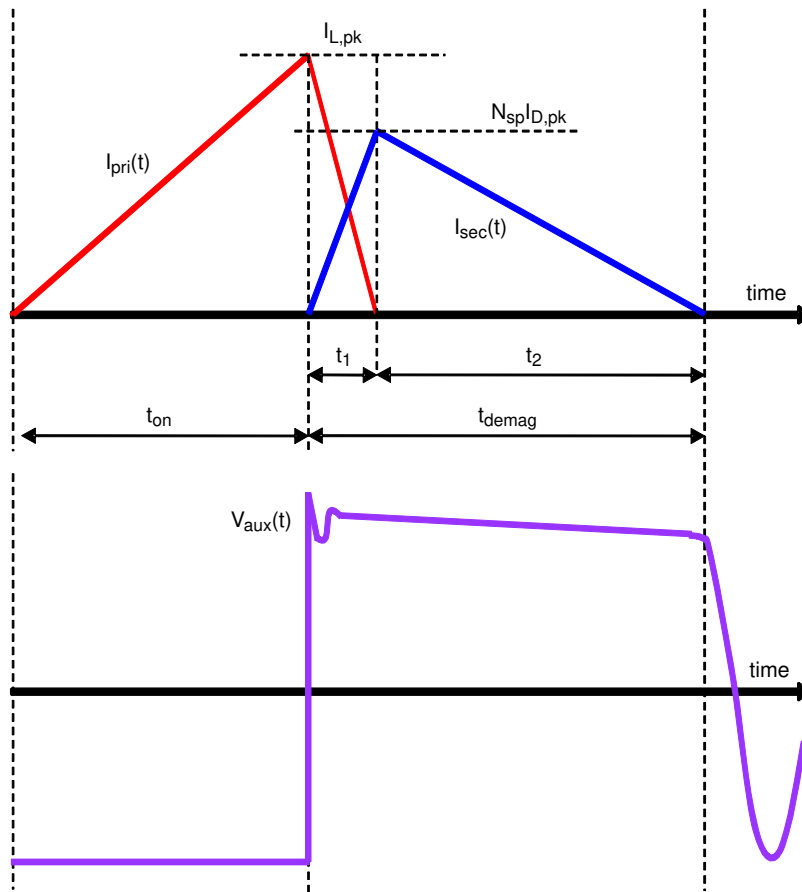


Figure 53. Flyback Currents and Auxiliary Winding Voltage in DCM

Internal Soft-Start

At startup or after recovering from a fault, there is a small internal soft-start of 40 μ s.

In addition, during startup, as the output voltage is zero volts, the demagnetization time is long and the constant

current control block will slowly increase the peak current towards its nominal value as the output voltage grows. Figure 54 shows a soft-start simulation example for a 9 W LED power supply.

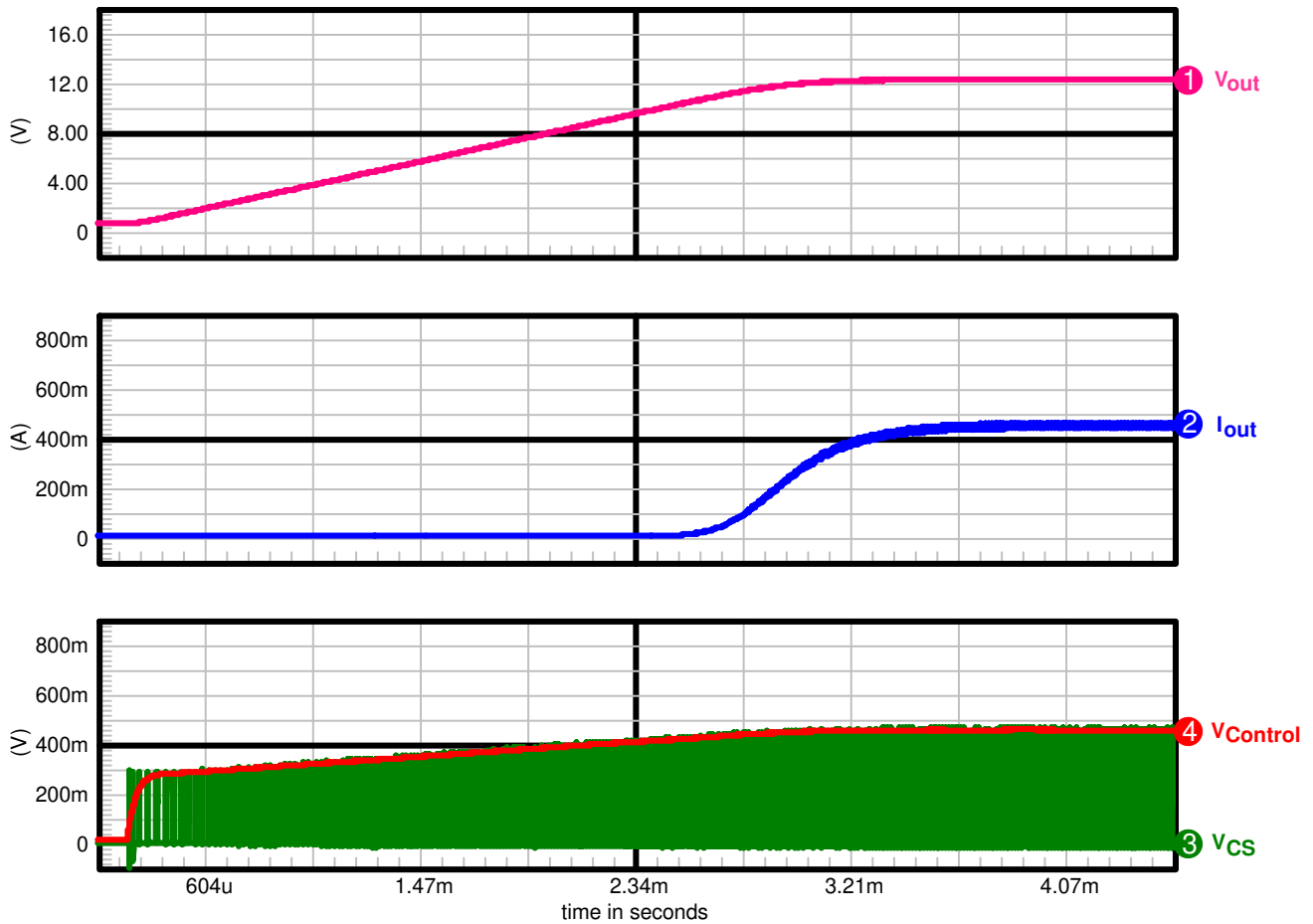


Figure 54. Startup Simulation Showing the Natural Soft-start

Cycle-by-Cycle Current Limit

When the current sense voltage exceeds the internal threshold V_{ILIM} , the MOSFET is turned off for the rest of the switching cycle (Figure 55).

Winding and Output Diode Short-Circuit Protection

In parallel with the cycle-by-cycle sensing of the CS pin, another comparator with a reduced LEB (t_{BCS}) and a higher threshold (1.5 V typical) is able to sense winding short-circuit and immediately stops the DRV pulses. The controller goes into auto-recovery mode in version B, B1, B2, B3 and D.

In version A, the controller is latched. In latch mode, the DRV pulses stop and VCC ramps up and down. The circuit un-latches when VCC pin voltage drops below $V_{CC(reset)}$ threshold.

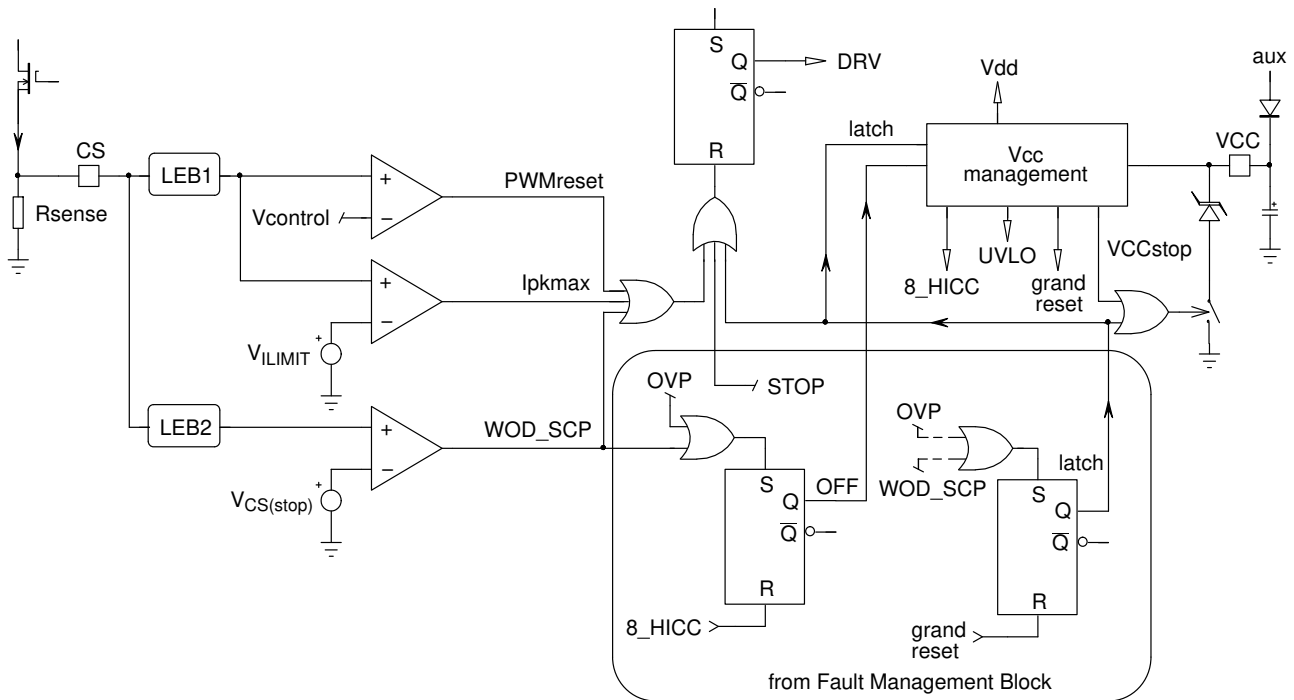


Figure 55. Winding Short Circuit Protection, Max. Peak Current Limit Circuits

Thermal Fold-back and Over Voltage / Over Temperature Protection

The thermal fold-back circuit reduces the current in the LED string when the ambient temperature exceeds a set point. The current is gradually reduced to 50% of its nominal value if the temperature continues to rise. (Figure 56). The thermal foldback starting temperature depends of the Negative Coefficient Temperature (NTC) resistor chosen by the power supply designer.

Indeed, the SD pin allows the direct connection of an NTC to sense the ambient temperature. When the SD pin voltage V_{SD} drops below $V_{TF(start)}$, the internal reference for the

constant current control V_{REF} is decreased proportionally to V_{SD} . When V_{SD} reaches $V_{TF(stop)}$, V_{REF} is clamped to V_{REF50} , corresponding to 50% of the nominal output current (versions A, B, B1, B2, B3). For the NCL30082D, the output current is decreased to 25% of the nominal output current.

If V_{SD} drops below V_{OTP} , the controller enters into the auto-recovery fault mode for version B, B1, B2, B3 and D meaning that the 4-s timer is activated. The controller will re-start switching after the 4-s timer has elapsed and when $V_{SD} > V_{OTP(on)}$ to provide some temperature hysteresis.

For version A, this protection is latched: reset occurs when $V_{CC} < V_{CC(reset)}$.

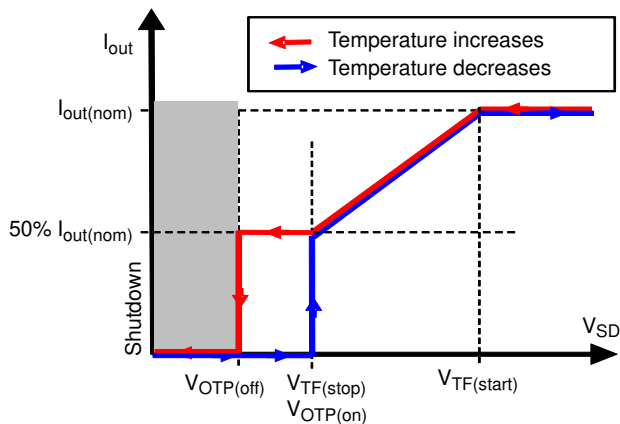


Figure 56. Output Current Reduction vs. SD Pin Voltage for NCL30082 Versions A, B, B1, B2, B3

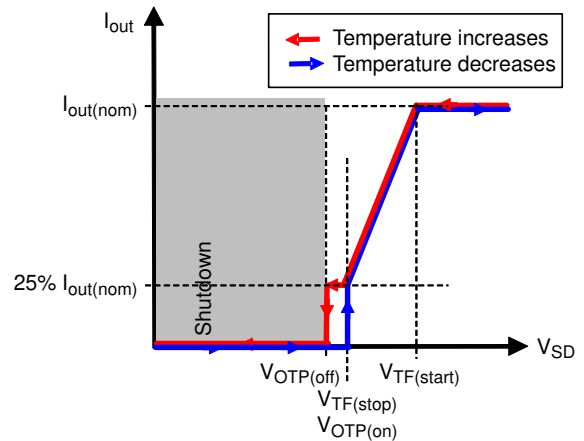


Figure 57. Output Current Reduction vs. SD Pin Voltage for NCL30082D

NCL30082

At startup, when V_{CC} reaches $V_{CC(on)}$, the controller is not allowed to start pulsing for at least $180\ \mu\text{s}$ in order to allow the SD pin voltage to reach its nominal value if a

filtering capacitor is connected to the SD pin. This is to avoid flickering of the LED light in case of over temperature.

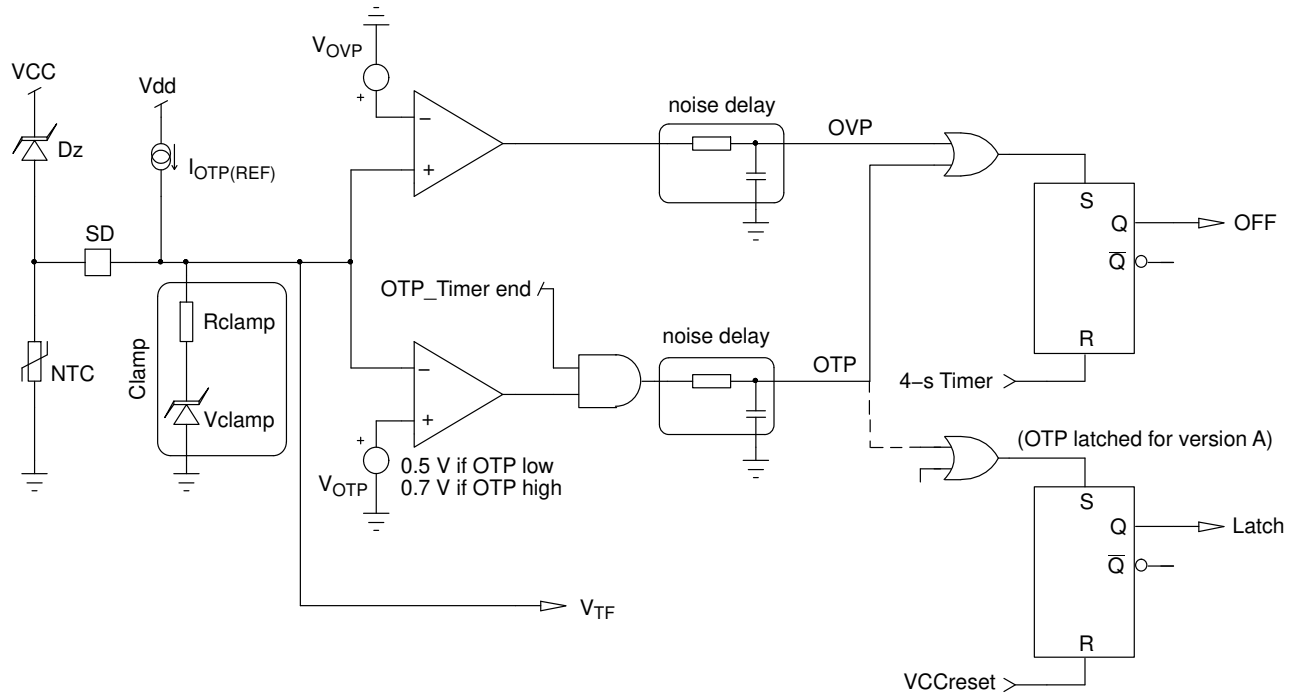


Figure 58. Thermal Fold-back and OVP/OTP Circuitry

In the case of excess voltage, the Zener diode starts to conduct and inject current into the internal clamp resistor R_{clamp} thus causing the pin SD voltage to increase. When

this voltage reaches the OVP threshold (2.5 V typ.), the controller shuts-down and waits for at least 4 seconds before restarting switching.

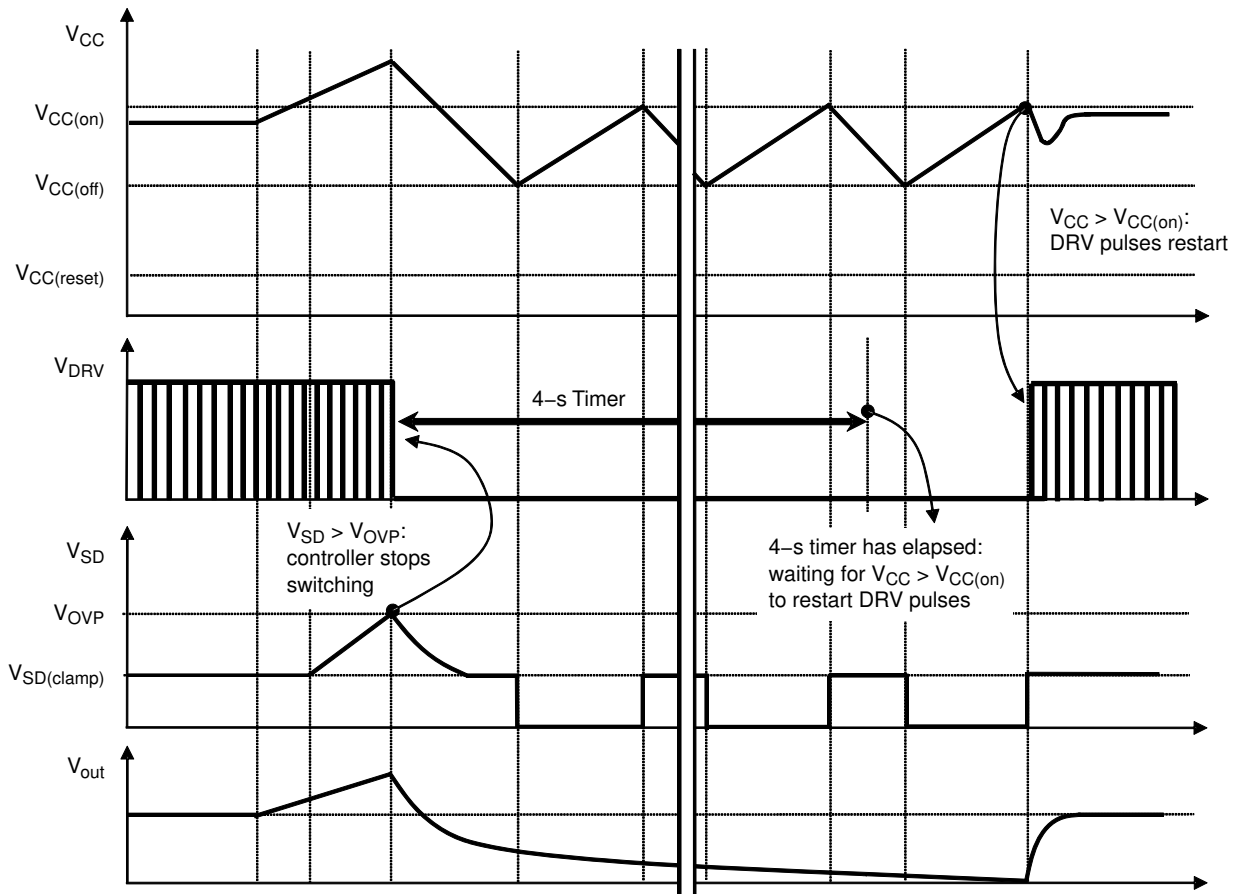


Figure 59. OVP with SD Pin Chronograms

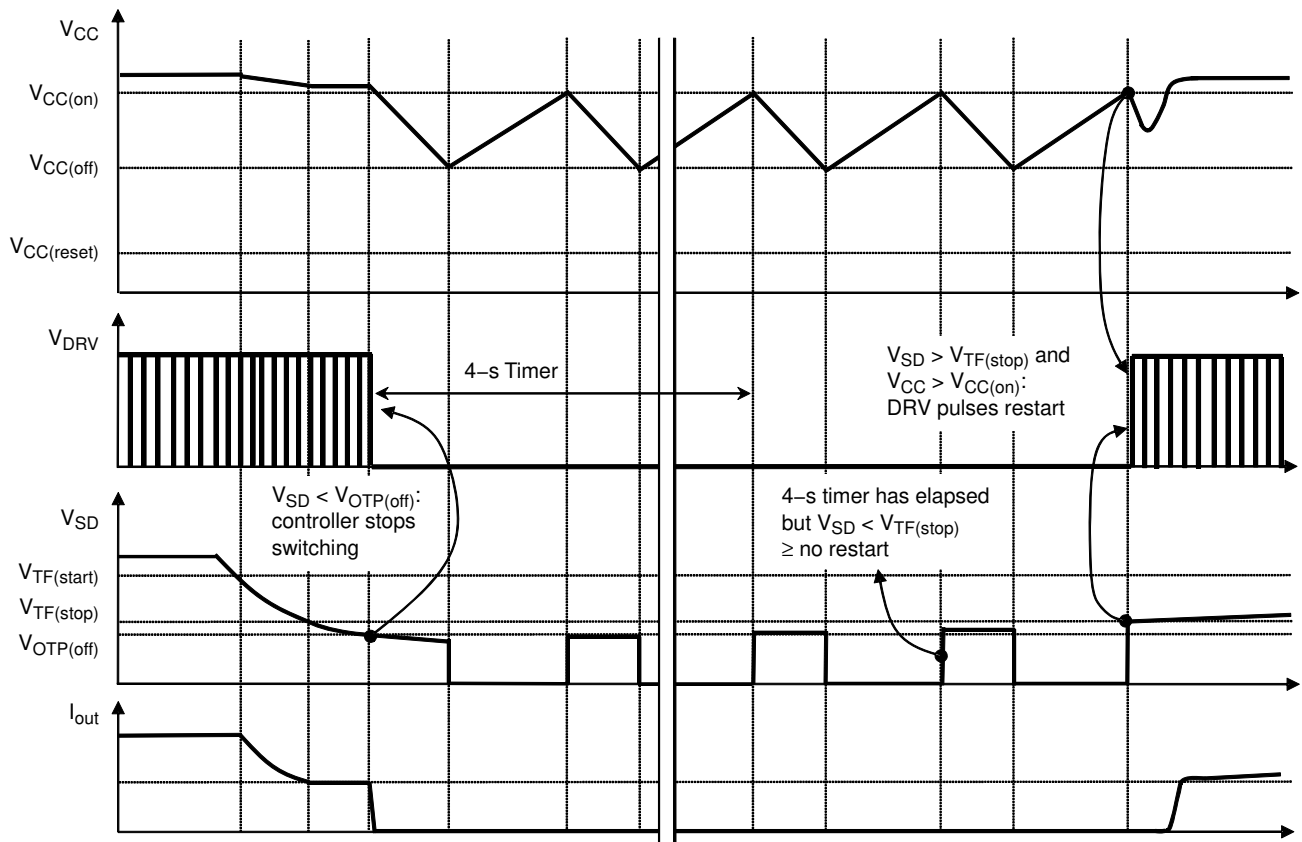


Figure 60. Thermal Fold-back / OTP Chronograms

PWM or Linear Dimming Detection

The pin DIM allows implementing either linear dimming or PWM dimming of the LED light.

If the power supply designer apply an analog signal varying from $V_{DIM(EN)}$ to V_{DIM100} to the DIM pin, the output current will increase or decrease proportionally to the voltage applied. For $V_{DIM} = V_{DIM100}$, the power supply delivers the maximum output current.

If a voltage lower than $V_{DIM(EN)}$ is applied to the DIM pin, the DRV pulses are disabled. Thus, for PWM dimming, a PWM signal with a low state value $< V_{DIM(EN)}$ and a high state value $> V_{DIM100}$ should be applied.

The DIM pin is pulled up internally by a small current source. Thus, if the pin is left open, the controller is able to start.

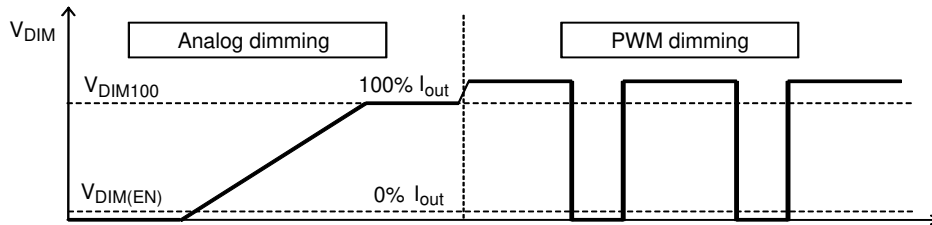


Figure 61. Pin DIM Chronograms

Note:

- If a PWM voltage with a high state value $< V_{DIM100}$ is applied to the DIM pin, the product will still be in PWM dimming mode, but the reference voltage will be decreased according to V_{DIM} . This allows increased dynamic range on the dimming control pin.
- **Thermal Foldback and dimming:** if the IC is in a dimming state and the thermal foldback (TF) is activated, the output current is further reduced to a value equal to $\text{Dimming} * \text{TF}$.

V_{CC} Over Voltage Protection (Open LED Protection)

If no output load is connected to the LED power supply, the controller must be able to safely limit the output voltage excursion.

In the NCL30082, when the V_{CC} voltage reaches the V_{CC(OVP)} threshold, the controller stops the DRV pulses and the 4-s timer starts counting. The IC re-start pulsing after the 4-s timer has elapsed and when V_{CC} ≥ V_{CC(on)}.

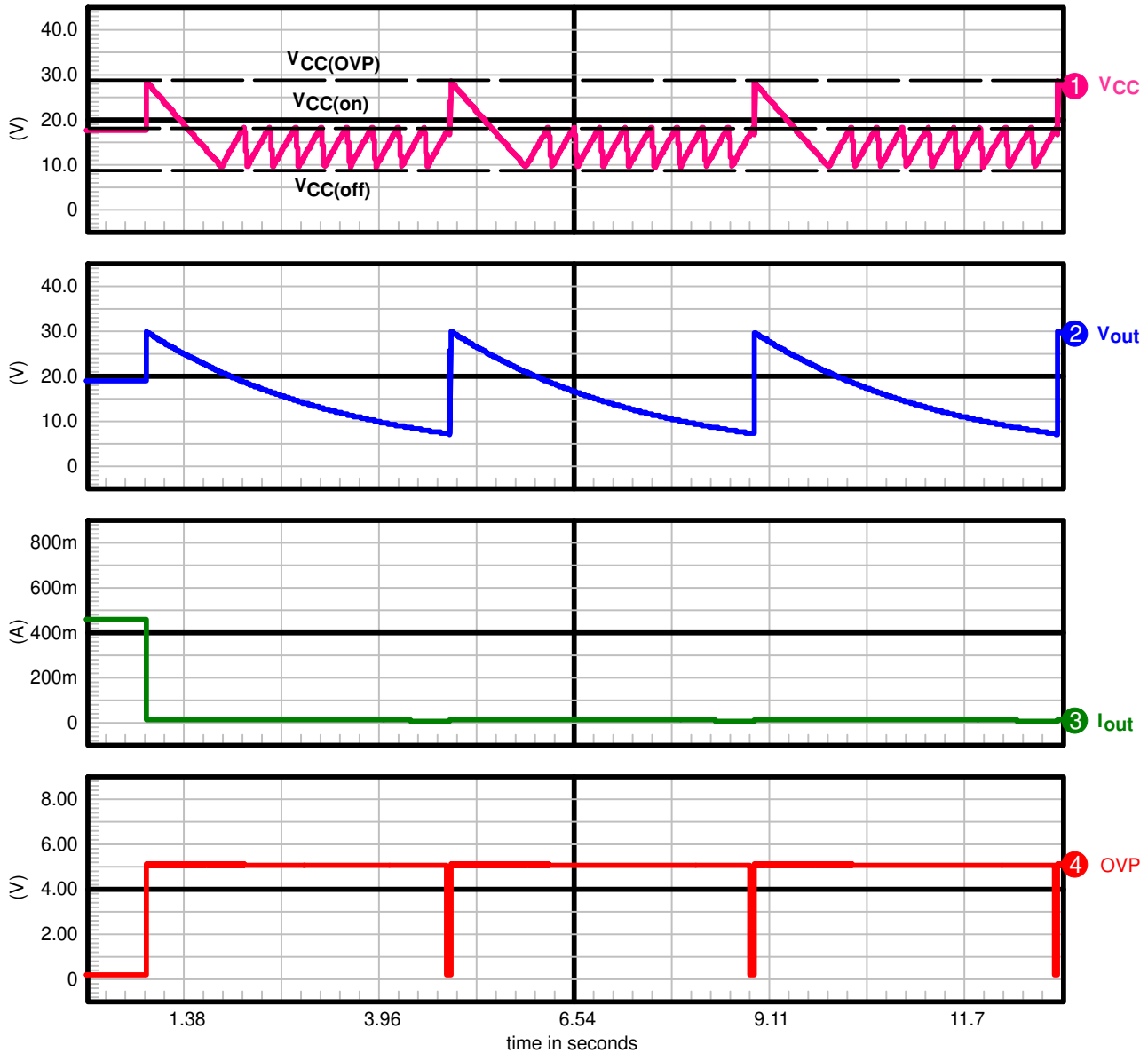


Figure 62. Open LED Protection Chronograms

Valley Lockout

Quasi-square wave resonant systems have a wide switching frequency excursion. The switching frequency increases when the output load decreases or when the input voltage increases. The switching frequency of such systems must be limited.

The NCL30082 changes the valley as the input voltage increases and as the output current set-point is varied (dimming and thermal fold-back). This limits the switching frequency excursion. Once a valley is selected, the controller stays locked in the valley until the input voltage

or the output current set-point varies significantly. This avoids valley jumping and the inherent noise caused by this phenomenon.

The input voltage is sensed by the VIN pin (line range detection in Figure 63). The internal logic selects the operating valley according to VIN pin voltage, SD pin voltage and DIM pin voltage.

By default, when the output current is not dimmed, the controller operates in the first valley at low line and in the second valley at high line.