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NCN6000

Compact Smart Card Interface IC

The NCN6000 is an integrated circuit dedicated to the smart card interface applications. The device handles any type of smart card through a simple and flexible microcontroller interface. On top of that, due to the built-in chip select pin, several couplers can be connected in parallel. The device is particularly suited for low cost, low power applications, with high extended battery life coming from extremely low quiescent current.

Features

- 100% Compatible with ISO7816-3 and EMV Standard
- Wide Battery Supply Voltage Range: $2.7 \leq V_{bat} \leq 6.0$ V
- Programmable CRD_VCC Supply to Cope with either 3.0 V or 5.0 V Card Operation
- Built-in DC-DC Converter Generates the CRD_VCC Supply with a Single External Low Cost Inductor only, providing a High Efficiency Power Conversion
- Full Control of the Power Up/Down Sequence Yields High Signal Integrity on both the Card I/O and the Signal Lines
- Programmable Card Clock Generator
- Built-in Chip Select Logic allows Parallel Coupling Operation
- ESD Protection on Card Pins (8.0 kV, Human Body Model)
- Fault Monitoring includes $V_{bat_{low}}$ and $V_{cc_{low}}$, providing Logic Feedback to External CPU
- Card Detection Programmable to Handle Positive or Negative Going Input
- Built-in Programmable CRD_CLK Stop Function Handles both High or Low State
- These are Pb-Free Devices**

Typical Application

- E-Commerce Interface
- ATM Smart Card
- Pay TV System

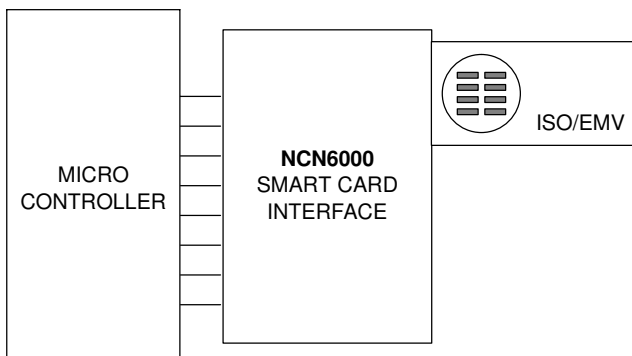


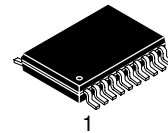
Figure 1. Simplified Application

**For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

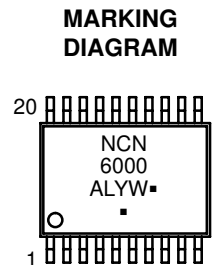


ON Semiconductor®

<http://onsemi.com>



TSSOP-20
DTB SUFFIX
CASE 948E



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS

| | | | | |
|-----------------|----|---|----|--------------|
| A0 | 1 | ○ | 20 | V_{bat} |
| A1 | 2 | | 19 | L_{out_H} |
| PGM | 3 | | 18 | L_{out_L} |
| PWR_ON | 4 | | 17 | PWR_GND |
| STATUS | 5 | | 16 | GROUND |
| \overline{CS} | 6 | | 15 | CRD_VCC |
| RESET | 7 | | 14 | CRD_IO |
| I/O | 8 | | 13 | CRD_CLK |
| INT | 9 | | 12 | CRD_RST |
| CLOCK_IN | 10 | | 11 | CRD_DET |

(Top View)

ORDERING INFORMATION

| Device | Package | Shipping† |
|---------------|-----------|------------------|
| NCN6000DTB | TSSOP-20* | 75 Units / Rail |
| NCN6000DTBG | TSSOP-20* | 75 Units / Rail |
| NCN6000DTBR2 | TSSOP-20* | 2500/Tape & Reel |
| NCN6000DTBR2G | TSSOP-20* | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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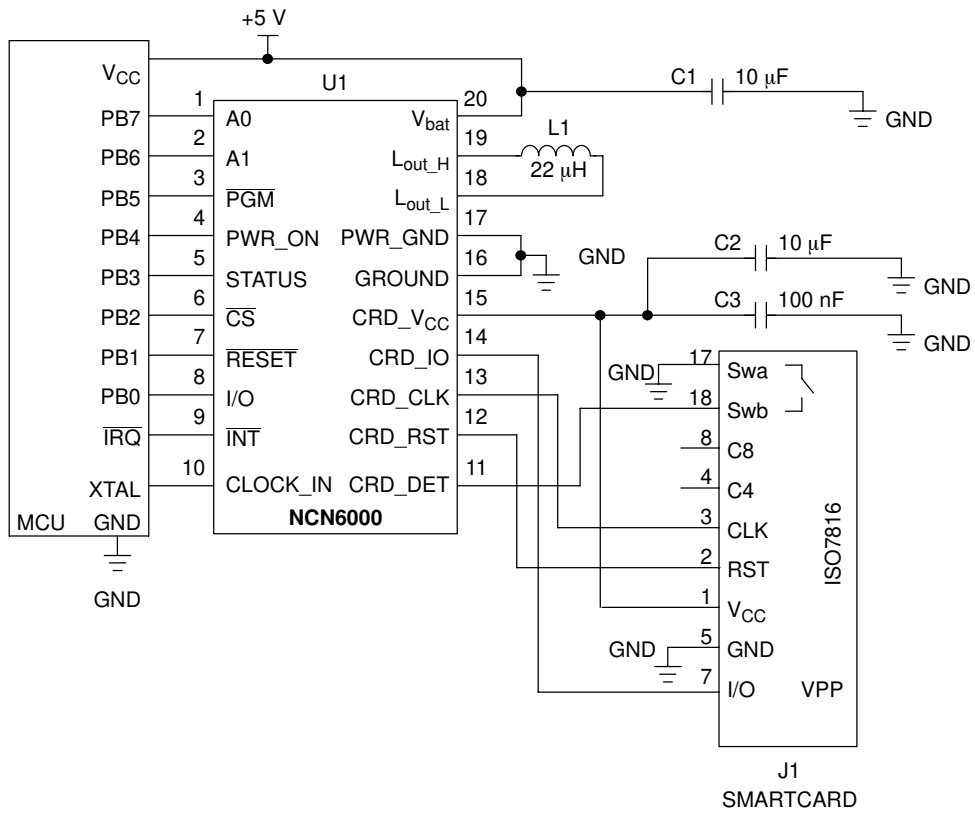


Figure 2. Typical Application

NCN6000

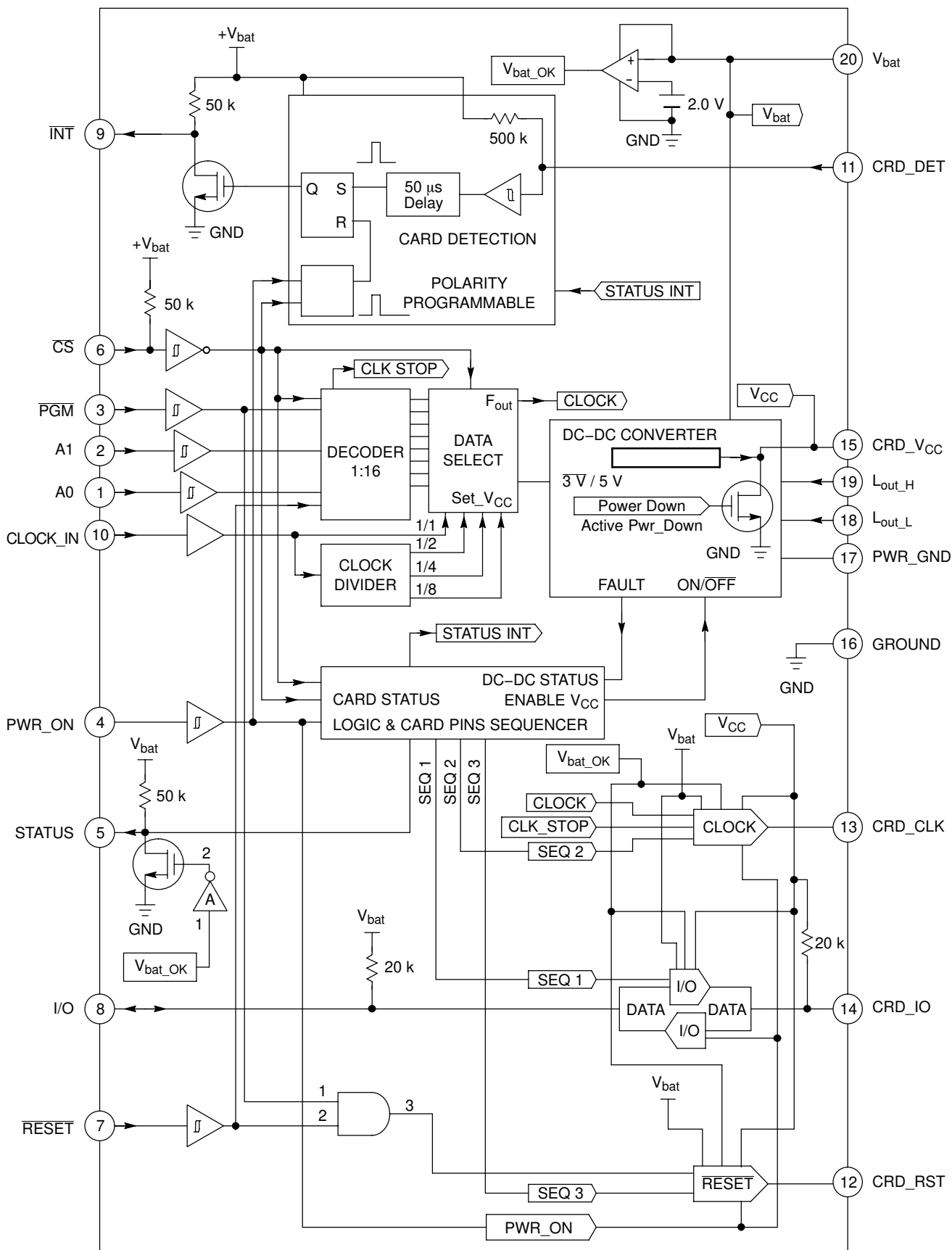


Figure 3. Block Diagram

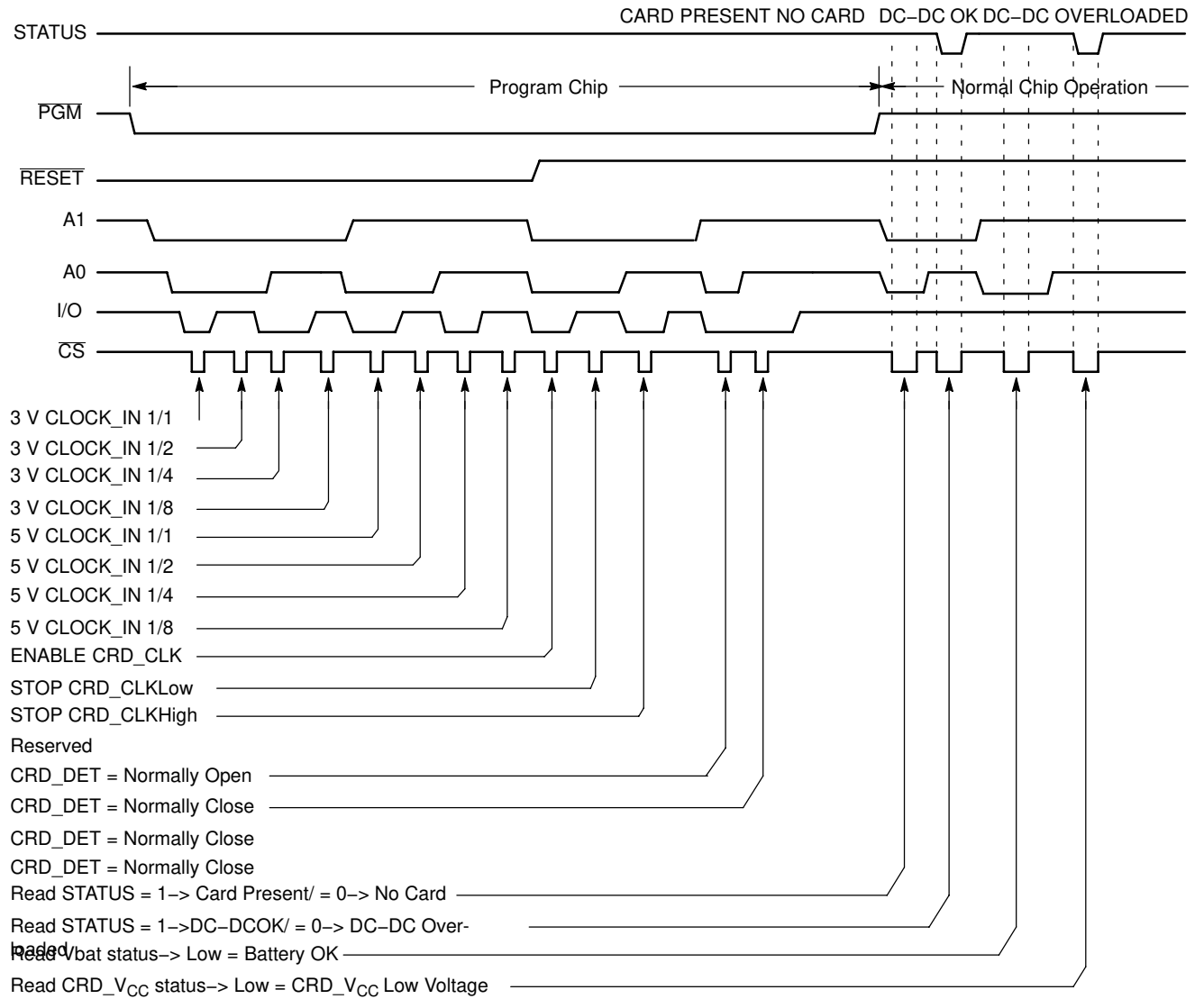


Figure 4. Programming and Normal Operation Basic Timing

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The programming can be achieved with the card powered ON or OFF. The identification of the interrupt is carried out by polling the STATUS pin, the Vbat voltage and the DC-DC results being provided on the same pin as depicted

by the table in Figure 4. During the programming mode, the PGM pin can be released to High since the mode is internally latched by the Negative going transition presents on the Chip Select pin.

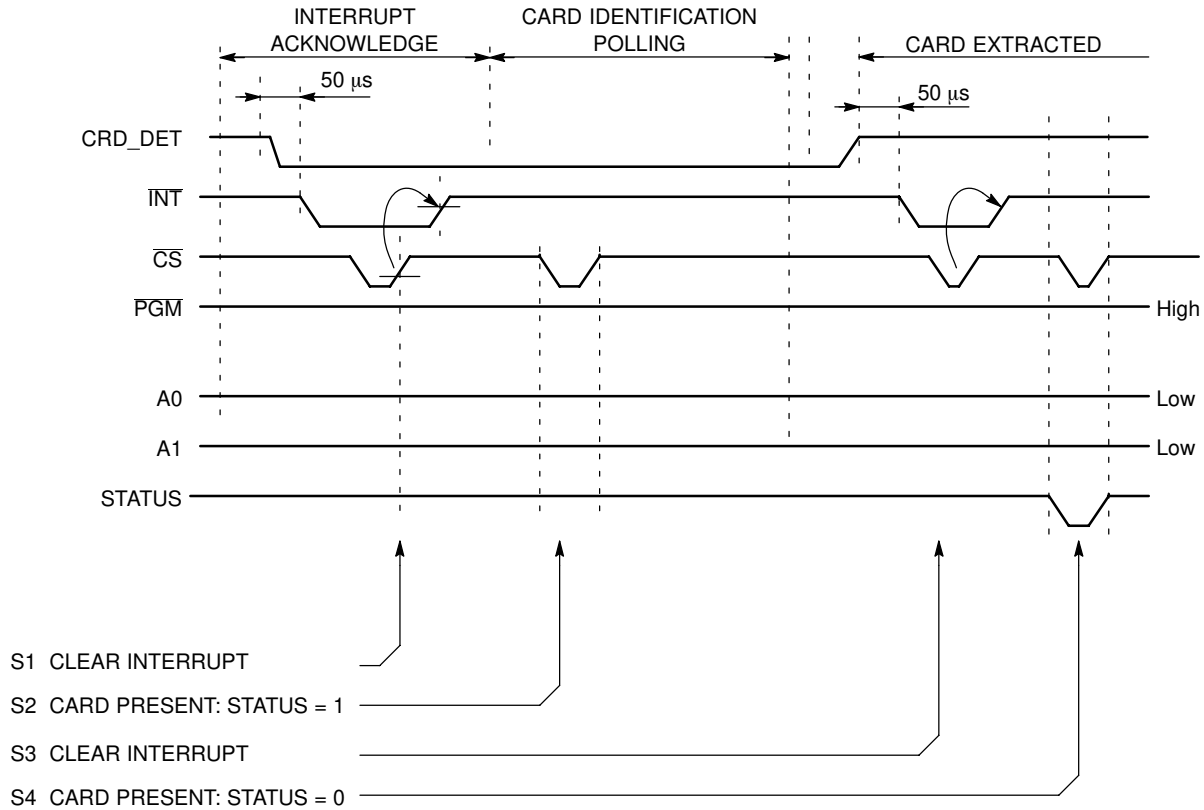


Figure 5. Interrupt Servicing and Card Polling

When a card is either inserted or extracted, the CRD_DET pin signal is debounced internally prior to pull the INT pin to Low. The built-in logic circuit automatically accommodates positive or negative input signal slope, on both insertion and extraction state, depending upon the polarity defined during the initialization sequence. The default condition is Normally Open switch, negative going card detection. The external CPU shall acknowledge the request by forcing CS = L which, in turn, releases the INT pin to High upon positive going of Chip Select (Table 4). Polling the STATUS pin as depicted in Table 3 identifies the active card. If a card is present, the STATUS returns High,

otherwise a Low is presented pin 5. The 50 µs digital filter is activated during both Insertion and Extraction of the card. The MPU shall clear the INT line when the card has been extracted, making the interrupt function available for other purposes. However, neither the NCN6000 operation nor the smart card I/O line or commands are affected by the state of the INT pin.

On the other hand, clearing the INT and reading the STATUS register can be performed by a single read by the MPU: states S1 and S2 can be combined in a single instruction, the same for S3 and S4.

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ABBREVIATIONS

| | |
|------------------|---|
| Lout_H | DC–DC External Inductor |
| Lout_L | DC–DC External Inductor |
| Cout | Output Capacitor |
| VCC | Card Power Supply Input |
| Icc | Current at CRD_VCC Pin |
| Class A | 5.0 V Smart Card |
| Class B | 3.0 V Smart Card |
| \overline{CS} | Chip Select (from MPU) |
| Z | High Impedance Logic State (according to ISO7816) |
| CRD_VCC | Interface IC Card Power Supply Output |
| CRD_CLK | Interface IC Card Clock Output |
| CRD_RST | Interface IC Card Reset Output |
| CRD_IO | Interface IC Card I/O Signal Line |
| CRD_DET | Interface IC Card Detection |
| ATR | Answer to Reset |
| \overline{PGM} | Select Programming or Normal Operation |
| \overline{INT} | Interrupt (to MPU) |
| tr | Rise Time |
| tf | Fall Time |
| td | Delay Time |
| ts | Storage Time |

PIN FUNCTIONS AND DESCRIPTION

| Pin | Name | Type | Description |
|-----|--------------------|--------------------|---|
| 1 | A0 | INPUT | This pin is combined with A1, \overline{PGM} , \overline{RESET} and I/O to program the chip mode of operation and to read the data provided by STATUS. (Figures 4 and 5 and Tables 2 and 3) |
| 2 | A1 | INPUT | This pin is combined with A0, \overline{PGM} , \overline{RESET} and I/O to program the chip mode of operation and to read the data provided by STATUS. (Figures 4 and 5 and Tables 2 and 3) |
| 3 | \overline{PGM} | INPUT | This pin is combined with A0, A1, \overline{RESET} and I/O to program the chip mode of operation and to read the data provided by STATUS. (Figures 4 and 5 and Tables 2 and 3) |
| 4 | PWR_ON | INPUT Pull Down | This pin validates the operation of the internal DC–DC converter: $\overline{CS} = L + PWR_ON =$ Negative going: DC–DC is OFF $\overline{CS} = L + PWR_ON =$ Positive going: DC–DC is ON Note: The PWR_ON bit must be combined with a Low state \overline{CS} signal to activate the function. (Table 2) |
| 5 | STATUS | OUTPUT | This pin provides logic state related to the card and NCN6000 status. According to the A0, A1 and \overline{PGM} logic state, this pin carries either the Card present status or the Vbat or the DC–DC operation state. When $\overline{PGM} = L$, STATUS is not affected, see Table 2. |
| 6 | \overline{CS} | INPUT Pull Up | This pin provides the NCN6000 chip select function. The PWR_ON, \overline{RESET} , I/O, A0, A1 and \overline{PGM} signals are disabled when $\overline{CS} = H$. When $\overline{PGM} = L$ and $\overline{CS} = L$, the device jumps to the programming mode (Figure 4 and Tables 1, 2 and 3). The Chip Select pin must be a unique physical address when more than one card are controlled by a single MPU. The data presented by the MPU are latched upon positive going edge of the Chip Select pin. |
| 7 | \overline{RESET} | INPUT Pull Down | This pin provides two modes of operation depending upon the logic state of \overline{PGM} pin 3: $\overline{PGM} = 1$: The signal present at this pin is translated to pin 12 (card reset signal) when $\overline{CS} = L$ and PWR_ON = H. It is latched when $\overline{CS} = H$. $\overline{PGM} = 0$: The signal present on this pin is used as a logic input to program the internal functions (Figure 5 and Tables 2 and 3). |

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PIN FUNCTIONS AND DESCRIPTION (continued)

| Pin | Name | Type | Description |
|-----|----------|-------------------------------|---|
| 8 | I/O | Input/Output Pull Up | This pin is connected to an external microcontroller interface. A bidirectional level translator adapts the serial I/O signal between the smart card and the microcontroller. The level translator is enabled when $\overline{CS} = L$. The signal present on this pin is latched when $\overline{CS} = H$. This pin is also used in programming mode (Tables 1, 2 and 3, Figures 4 and 5). |
| 9 | INT | OUTPUT Pull Down | This pin is activated LOW when a card has been inserted and detected by the interface or when the NCN6000 reports Vbat or CRD_VCC status (See Table 6). The signal is reset to a logic 1 on the rising edge of either \overline{CS} or PWR_ON. The Collector open mode makes possible the wired AND/OR external logic. When two or more interfaces share the INT function with a single microcontroller, the software must poll the STATUS pin to identify the origin of the interrupt (Figure 5). |
| 10 | CLOCK_IN | CLOCK INPUT High Impedance | This pin can be connected to either the microcontroller master clock, or to any clock signal, to drive the external smart cards. The signal is fed to internal clock selector circuit and translated to the CRD_CLK pin at either the same frequency, or divided by 2 or 4 or 8, depending upon the programming mode (Tables 1, 2 and 3). Care must be observed, at PCB level, to minimize the pick-up noise coming from the CLOCK_IN line. It is recommended to put a shield, built with a 10 mil copper track, around this line and terminated to the GND. |
| 11 | CRD_DET | INPUT | The signal coming from the external card connector is used to detect the presence of the card. A built-in pull up low current source makes this pin active LOW or HIGH, assuming one side of the external switch is connected to ground. At Vbat start up, the default condition is Normally Open switch, negative going insertion detection. The Normally Closed switch, positive going insertion detection, can be defined by programming the NCN6000 accordingly. In this case, the polarity must be set up during the first cycles of the system initialization, otherwise an already inserted card will not be detected by the chip. |
| 12 | CRD_RST | OUTPUT | This pin is connected to the RESET pin of the card connector. A level translator adapts the RESET signal from the microcontroller to the external card. The output current is internally limited to 15 mA. The CRD_RST is validated when PWR_ON = H and PGM = H and hard wired to Ground when the card is deactivated. |
| 13 | CRD_CLK | OUTPUT | This pin is connected to the CLK pin of the card connector. The CRD_CLK signal comes from the clock selector circuit output. Combining A0, A1, PGM and I/O, as depicted in Table 3 and Figure 3, programs the clock selection. This signal can be forced into a standby mode with CRD_CLK either High or Low, depending upon the mode defined by the programming sequence (Tables 1, 2 and 3 and Figure 4). Care must be observed, at PCB level, to minimize the pick-up noise coming from the CRD_CLK line. It is recommended to put a shield, built with a 10mil copper track, around this line and terminated to the GND. |
| 14 | CRD_IO | I/O | This pin handles the connection to the serial I/O pin of the card connector. A bidirectional level translator adapts the serial I/O signal between the card and the microcontroller. The CRD_IO pin current is internally limited to 15 mA. A built-in register holds the previous state presents on the I/O input pin. |
| 15 | CRD_VCC | POWER | This pin provides the power to the external card. It is the logic level "1" for CRD_IO, CRD_RST and CRD_CLK signals. The energy stored by the DC-DC external inductor Lout must be smoothed by a 10 μ F capacitor, associated with a 100 nF ceramic in parallel, connected across CRD_VCC and GND. In the event of a CRD_VCC U_{VLOW} voltage, the NCN6000 detects the situation and feedback the information in the STATUS bit. The device does not take any further action, particularly the DC-DC converter is neither stopped nor reprogrammed by the NCN6000. It is up to the external MPU to handle the situation. However, when the CRD_VCC is overloaded, the NCN6000 shut off the DC-DC converter, pulls the INT pin Low and reports the fault in the STATUS register. |
| 16 | GROUND | SIGNAL | The logic and low level analog signals shall be connected to this ground pin. This pin must be externally connected to the PWR_GND pin 17. The designer must make sure no high current transients are shared with the low signal currents flowing into this pin. |
| 17 | PWR_GND | POWER | This pin is the Power Ground associated with the built-in DC-DC converter and must be connected to the system ground together with GROUND pin 11. Using good quality ground plane is recommended to avoid spikes on the logic signal lines. |
| 18 | Lout_L | POWER | The High Side of the external inductor is connected between this pin and Lout_H to provide the DC-DC function. The built-in MOS devices provide the switching function together with the CRD_VCC voltage rectification. |

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PIN FUNCTIONS AND DESCRIPTION (continued)

| Pin | Name | Type | Description |
|-----|--------|-------|---|
| 19 | Lout_H | POWER | The High Side of the external inductor is connected between this pin and Lout_L to provide the DC-DC function. The current flowing into this inductor is limited by a sense resistor internally connected from Vbat/pin 20 and pin 19. Typically, Lout = 22 μ H, with ESR < 2.0 Ω , for a nominal 55 mA output load. |
| 20 | Vbat | POWER | This pin is connected to the supply voltage and monitored by the NCN6000. The operation is inhibited when Vbat is below the minimum 2.70 V value, followed by a PWR_DOWN sequence and a Low STATUS state. |

MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
|--|----------------------|--|------------|
| Battery Supply Voltage | Vbat | 7.0 | V |
| Battery Supply Current (Note 2) | Ibat | 300 | mA |
| Power Supply Voltage | Vcc | 6.0 | V |
| Power Supply Current | Icc | ± 100 | mA |
| Digital Input Pins | Vin | $-0.5 \text{ V} < V_{in} < V_{bat} + 0.5 \text{ V}$, but < 7.0 V | V |
| Digital Input Pins | Iin | ± 5.0 | mA |
| Digital Output Pins | Vout | $-0.5 \text{ V} < V_{in} < V_{bat} + 0.5 \text{ V}$, but < 7.0 V | V |
| Digital Output Pins | Iout | ± 10 | mA |
| Card Interface Pins | Vcard | $-0.5 \text{ V} < V_{card} < \text{CRD_VCC} + 0.5 \text{ V}$ | V |
| Card Interface Pins, except CRD_CLK | Icard | ± 15 | mA |
| Inductor Current | ILout | 300 | mA |
| ESD Capability (Note 3) Standard Pins Card Interface Pins and CRD_DET | VESD | 2.0 8.0 | kV |
| TSSOP-20 Package Power Dissipation @ Tamb = +85°C Thermal Resistance Junction to Air (R θ ja) | PDS R θ ja | 320 125 | mW °C/W |
| Operating Ambient Temperature Range | TA | -25 to +85 | °C |
| Operating Junction Temperature Range | TJ | -25 to +125 | °C |
| Maximum Junction Temperature (Note 4) | TJmax | +150 | °C |
| Storage Temperature Range | Tsg | -65 to +150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = +25°C.
2. This current represents the maximum peak current the pin can sustain, not the NCN6000 consumption (see I_{batop}).
3. Human Body Model, R = 1500 Ω , C = 100 pF.
4. Absolute Maximum Rating beyond which damage to the device may occur.

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POWER SUPPLY SECTION (–25°C to +85°C ambient temperature, unless otherwise noted.)

| Rating | Symbol | Pin | Min | Typ | Max | Unit |
|---|---|-----|----------------------------------|-------------------------|-------------------------------|--------------------|
| Power Supply | Vbat | 20 | 2.7 | – | 6.0 | V |
| Standby Supply Current Conditions: PWR_ON = L, STATUS = H, CLOCK_IN = H, CS = H. All other logic inputs and outputs are open: Vbat = 3.0 V Vbat = 5.0 V | Ibat _{sb} | 20 | – – | 3.0 – | 8.0 15 | μA |
| DC Operating Current (Figure 19) PWR_ON = H, CLOCK_IN = 0, CS = H, all CRD pins unloaded @ Vbat = 6.0 V, CRD_VCC = 5.0 V @ Vbat = 3.6 V, CRD_VCC = 5.0 V | Ibat _{op} | 20 | – – | 7.0 2.0 | – 5.0 | mA |
| Vbat Undervoltage Detection _{High} Vbat Undervoltage Detection _{Low} Vbat Undervoltage Detection _{Hysteresis} | Vbat _{LH} Vbat _{LL} Vbat _{HY} | 20 | 2.1 2.0 – | – – 100 | 2.7 2.6 – | V V mV |
| Output Card Supply Voltage @ I _{cc} = 55 mA @ 2.70 V ≤ Vbat ≤ 6.0 V CRD_VCC = 3.0 V CRD_VCC = 5.0 V @ Vbat _{LL} < Vbat < 2.70 V CRD_VCC = 5.0 V | V _{cc} V _{C3H} V _{C5H} V _{C5H} | 15 | 2.75 4.75 4.50 | – – – | 3.25 5.25 – | V V |
| Output Card Supply Peak Current @ V _{cc} = 5.0 V @ CRD_VCC = 5.0 V @ CRD_VCC = 3.0 V @ Vbat = 3.6 V, CRD_VCC = 5.0 V, Tamb < 65°C | I _{ccp} | 15 | 55 55 65 | – – – | – – – | mA |
| Output Current Limit Time Out | tdoff | 15 | – | 4.0 | – | ms |
| Output Over Current Limit | I _{ccov} | 15 | – | – | 100 | mA |
| Output Dynamic Peak Current @ CRD_VCC = 3.0 V or 5.0 V, Cout = 10 μF Ceramic XR7, Pulse Width 400 ns (Notes 5 and 6) | I _{ccd} | 15 | 100 | – | – | mA |
| Battery Start-Up Current @ CRD_VCC = 3.0 V, –25°C ≤ TA ≤ +85°C @ CRD_VCC = 5.0 V, –25°C ≤ TA ≤ +85°C | I _{ccst} | 20 | – – | 140 300 | – – | mA |
| Output Card Supply Voltage Ripple @ I _{out} = 22 μH, Cout 1 = 10 μF, Cout 2 = 100 nF, Vbat = 3.6 V I _{out} = 55 mA CRD_VCC = 5.0 V (Note 5) CRD_VCC = 3.0V | V _{ccrip} | 15 | – – | – – | 50 50 | mV |
| Output Card Supply Turn On Time @ I _{out} = 22 μF, Cout1 = 10 μF, Cout2 = 100 nF, Vbat = 2.7 V, CRD_VCC = 5.0 V | V _{ccTON} | 15 | – | – | 2.0 | ms |
| Output Card Supply Shut Off Time @ Cout1 = 10 μF, Ceramic, Vbat = 2.7 V, CRD_VCC = 5.0 V, V _{ccOFF} < 0.4 V | V _{ccTOFF} | 15 | – | – | 250 | μs |
| DC–DC Converter Operating Frequency | F _{sw} | 18 | – | 600 | – | kHz |
| Power Switch Drain/Source Resistor | R _{ONS} | 18 | – | 1.9 | 2.2 | Ω |
| Output Rectifier ON Resistor | R _{OND} | 15 | – | 2.8 | 3.4 | Ω |

5. Ceramic X7R, SMD types capacitors are mandatory to achieve the CRD_VCC specifications. When electrolytic capacitor is used, the external filter must include a 100 nF, max 50 mΩ ESR capacitor in parallel, to reduce both the high frequency noise and ripple to a minimum. Depending upon the PCB layout, it might be necessary is to use two 6.8 μF/10 V/ceramic/X7R//SMD1206 in parallel, yielding an improved CRD_VCC ripple over the temperature range.

6. According to ISO7816–3, paragraph 4.3.2.

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DIGITAL PARAMETERS SECTION @ 2.70 V ≤ Vbat ≤ 6.0 V, NORMAL OPERATING MODE (–25°C to +85°C ambient temperature, unless otherwise noted.) Note: Digital inputs undershoot < –0.30 V to ground, Digital inputs overshoot < 0.30 V to Vbat

| Rating | Symbol | Pin | Min | Typ | Max | Unit |
|--|--------------------------------------|-------------------------------|--------------|--------|-------------|------|
| Input Asynchronous Clock Duty Cycle = 50% @ Vbat = 3.0V over the temperature range | F _{CLKIN} | 10 | – | – | 40 | MHz |
| Clock Rise Time Clock Fall Time | F _{tr} F _{tf} | 10 | – – | – – | 5.0 5.0 | ns |
| I/O Data Transfer Switching Time, Both Directions (I/O and CRD_IO), @ Cout = 30 pF I/O Rise Time* (Note 7) I/O Fall Time | T _{RIO} T _{FIO} | 8, 14 | – | – | 0.8 0.8 | μs |
| Input/Output Data Transfer Time, Both Directions @ 50% CRD_VCC, L to H and H to L | T _{TIO} | 8, 14 | – | – | 150 | ns |
| Minimum PWR_ON Low Level Logic State Time to Power Down the DC–DC Converter | T _{WON} | 4 | 2.0 | – | – | μs |
| CRD_VCC Power Up/Down Sequence Interval | T _{DSEQ} | | – | 0.5 | 2.0 | μs |
| STATUS Pull Up Resistance | R _{STA} | 5 | 20 | 50 | 80 | kΩ |
| Chip Select \overline{CS} Pull Up Resistance | R _{CSPU} | 6 | 20 | 50 | 80 | kΩ |
| Interrupt INT Pull Up Resistance | R _{INTPU} | 9 | 20 | 50 | 80 | kΩ |
| Positive Going Input High Voltage Threshold (A0, A1, PGM, PWR_ON, \overline{CS} , RESET, CRD_DET) | V _{IH} | 1, 2, 3, 4, 6, 7, 11 | 0.70 * Vbat | – | Vbat | V |
| Negative Going Input High Voltage Threshold (A0, A1, PGM, PWR_ON, \overline{CS} , RESET, CRD_DET) | V _{IL} | 1, 2, 3, 4, 6, 7, 11 | 0 | – | 0.30 * Vbat | V |
| Output High Voltage STATUS, INT @ I _{OH} = –10 μA | V _{OH} | 5, 9 | Vbat – 1.0 V | – | – | V |
| Output High Voltage STATUS, INT @ I _{OH} = 200 μA | V _{OL} | 5, 9 | – | – | 0.40 | V |

7. Since a 20 kΩ pull up resistor is provided by the NCN6000, the external MPU can use an Open Drain connection.

DIGITAL PARAMETERS SECTION @ 2.70 V ≤ Vbat ≤ 6.0 V, CHIP PROGRAMMING MODE (–25°C to +85°C ambient temperature, unless otherwise noted.)

| Rating | Symbol | Pin | Min | Typ | Max | Unit |
|---|-------------------|------------------------|-----|-----|-----|------|
| A0, A1, \overline{PGM} , PWR_ON, \overline{RESET} and I/O Data Set Up Time | T _{SMOD} | 1, 2, 3, 4, 7, 8 | 2.0 | – | – | μs |
| A0, A1, \overline{PGM} , PWR_ON, \overline{RESET} and I/O Data Set Up Time | T _{HMOD} | 1, 2, 3, 4, 7, 8 | 2.0 | – | – | μs |
| Chip Select \overline{CS} Low State Pulse Width | T _{WCS} | 6 | 2.0 | – | – | μs |

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SMART CARD SECTION (–25°C to +85°C ambient temperature, unless otherwise noted.)

| Rating | Symbol | Pin | Min | Typ | Max | Unit |
|--|--|--------|--|--------------------------------|---|--|
| CRD_RST @ CRD_VCC = +5.0 V Output RESET V _{OH} @ I _{crd_rst} = –20 μA Output RESET V _{OL} @ I _{crd_rst} = 200 μA Output RESET Rise Time @ C _{out} = 30 pF Output RESET Fall Time @ C _{out} = 30 pF CRD_RST @ V _{cc} = +3.0 V Output RESET V _{OH} @ I _{crd_rst} = –20 μA Output RESET V _{OL} @ I _{crd_rst} = 200 μA Output RESET Rise Time @ C _{out} = 30 pF Output RESET Fall Time @ C _{out} = 30 pF | V _{OH} V _{OL} t _R t _F V _{OH} V _{OL} t _R t _F | 12 | CRD_VCC – 0.9 0 | – | CRD_VCC 0.4 100 100 | V V ns ns V V ns ns |
| CRD_CLK @ CRD_VCC = +3.0 V or +5.0 V CRD_VCC = +5.0 V Output Frequency (See Note 8) Output Duty Cycle @ DC Fin = 50% ± 1% Output CRD_CLK Rise Time @ C _{out} = 30 pF Output CRD_CLK Fall Time @ C _{out} = 30 pF Output V _{OH} @ I _{crd_clk} = –20 μA Output V _{OL} @ I _{crd_clk} = 100 μA CRD_VCC = +3.0 V Output Frequency (See Note 8) Output Duty Cycle @ DC Fin = 50% ± 1% Output CRD_CLK Rise Time @ C _{out} = 30 pF Output CRD_CLK Fall Time @ C _{out} = 30 pF Output V _{OH} @ I _{crd_clk} = –20 μA @ C _{out} = 30 pF Output V _{OL} @ I _{crd_clk} = 100 μA @ C _{out} = 30 pF | F _{CRDCLK} F _{CRDDC} t _R t _F V _{OH} V _{OL} F _{CRDCLK} F _{CRDDC} t _R t _F V _{OH} V _{OL} | 13 | 45 3.15 0 40 1.85 0 | – | 5.0 55 18 18 CRD_VCC +0.5 5.0 60 18 18 CRD_VCC 0.7 | MHz % ns ns V V MHz % ns ns V V |
| CRD_I/O @ CRD_VCC = +5.0 V CRD_I/O Data Transfer Frequency CRD_I/O Rise Time @ C _{out} = 30 pF CRD_I/O Fall Time @ C _{out} = 30 pF Output V _{OH} @ I _{crd_i/o} = –20 μA Output V _{OL} @ I _{crd_i/o} = 500 μA, V _{IL} = 0 V CRD_I/O @ CRD_VCC = +3.0 V CRD_I/O Data Transfer Frequency CRD_I/O Rise Time @ C _{out} = 30 pF CRD_I/O Fall Time @ C _{out} = 30 pF Output V _{OH} @ I _{crd_i/o} = –20 μA Output V _{OL} @ I _{crd_i/o} = 500 μA, V _{IL} = 0 V | F _{IO} T _{RIO} T _{FIO} V _{OH} V _{OL} F _{IO} T _{RIO} T _{FIO} V _{OH} V _{OL} | 14 | CRD_VCC – 0.9 0 | 315 315 | 0.8 0.8 CRD_VCC 0.4 0.8 0.8 CRD_VCC 0.4 | kHz μs μs V V kHz μs μs V V |
| CRD_IO Pull Up Resistor @ PWR_ON = H | R _{CRDPU} | 14 | 14 | 20 | 26 | kΩ |
| Card Detection Debouncing Delay: Card Insertion Card Extraction | T _{CRDIN} T _{CRDOFF} | 11 | 50 50 | – | 150 150 | μs μs |
| Card Insertion or Extraction Positive Going Input High Voltage | V _{IHDET} | 11 | 0.70 * V _{bat} | – | V _{bat} | V |
| Card Insertion or Extraction Negative Going Input Low Voltage | V _{ILDET} | 11 | 0 | – | 0.30 * V _{bat} | V |
| Card Detection Bias Pull Up Current @ V _{bat} = 5.0 V | I _{DET} | 11 | – | 10 | – | μA |
| Output Peak Max Current Under Card Static Operation Mode @ V _{cc} = 3.0 V or V _{cc} = 5.0 V | I _{crd_iorst} | 12, 14 | – | – | 15 | mA |
| Output Peak Max Current Under Card Static Operation Mode @ V _{cc} = 3.0 V or V _{cc} = 5.0 V | I _{crd_clk} | 13 | – | – | 70 | mA |

8. The CRD_CLK clock can operate up to 20 MHz, but the rise and fall time are not guaranteed to be fully within the ISO7816 specification over the temperature range. Typically, t_r and t_f are 12 ns @ CRD_CLK = 10 MHz.

NCN6000

Programming and Status Functions

The NCN6000 features a programming interface and a status interface. Figure 4 illustrates the programming mode.

Table 1. Programming and Status Functions Pinout Logic

| Pins | Name | CRD_VCC Prg. 3.0 V/5.0 V | CLOCK_IN Divide Ratio | CRD_DET | CLOCK STOP AND START | Poll Card Status | DC-DC Status | Vbat Status | CRD_VCC Status |
|------|-----------------|-----------------------------|--------------------------|-------------------------|-------------------------|---------------------|-----------------|----------------|-------------------|
| 5 | STATUS | Not Affected | Not Affected | Not Affected | Not Affected | READ | READ | READ | READ |
| 6 | \overline{CS} | Latch On Rising Edge | Latch On Rising Edge | Latch On Rising Edge | Latch On Rising Edge | 0 | 0 | 0 | 0 |
| 3 | PGM | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | A0 | 0/1 | 0/1 | 0/1 | 0/1 | 0 | 1 | 0 | 1 |
| 2 | A1 | 0/1 | 0/1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 7 | RESET | 0 | 0 | 1 | 1 | Z | Z | Z | Z |
| 8 | I/O (in) | 0/1 | 0/1 | 0/1 | 0/1 | Z | Z | Z | Z |

The \overline{PGM} signal, pin 3, controls the mode of operation (chip programming or smart card transaction) and must be set up accordingly prior to pull Chip Select (pin 6) Low.

Table 2. Status Pin Logic Output

| Name | \overline{CS} | PGM | A1 | A0 | Status Logic Level |
|------------------|-----------------|-----|----|----|--|
| None | H | X | X | X | No Chip Access |
| None | L | L | X | X | Programming Mode, No Read Available |
| CARD PRESENT | L | H | L | L | Low: No Card Inserted High: Card inserted |
| DC-DC | L | H | L | H | Low: DC-DC Over Range High: DC-DC Operates Normally |
| Vbat | L | H | H | L | Low: Vbat Within Range High: Vbat Below Minimum range |
| CRD_VCC Overload | L | H | H | H | Low: CRD_VCC Voltage Below Minimum Range High: CRD_VCC in Range |

Card VCC, Card CLOCK and Card Detection Polarity Programming

The CRD_VCC and CLOCK_IN programming options allows matching the system frequency with the card clock frequency, and to select 3.0 V or 5.0 V CRD_VCC supply. The CRD_DET programming option allows the usage of either Normally Open or Normally Close detection switch. Table 3 highlights the A0, A1, PGM and I/O logic states for the possible options. **The default power up reset condition**

is state 1: asynchronous clock, ratio 1/1, CRD_CLK active, CRD_DET = Normally Open, CRD_VCC = 3.0 V. All states are latched for each output variable in programming mode at the positive going slope of Chip Select [\overline{CS}] signal. It is the system designer’s responsibility to set up the options needed to match the chip with the peripherals. In particular, when using Normally Close switch, the CRD_DET polarity must be defined during the first cycles of the initialization.

Table 3. Card VCC, Card Clock and Card Detection Polarity Truth Table

| HEXA | \overline{CS} | PWR_ON | PGM | \overline{RESET} | A1 | A0 | I/O | CRD_VCC | CRD_CLK | CRD_DET | STATUS |
|------|-----------------|--------|-----|--------------------|----|----|-----|---------|--------------|--------------------------|--------------|
| \$00 | L | – | L | L | L | L | L | 3.0 V | CLOCK_IN 1/1 | – | H (Note 13) |
| \$01 | L | – | L | L | L | L | H | 3.0 V | CLOCK_IN 1/2 | – | H (Note 13) |
| \$02 | L | – | L | L | L | H | L | 3.0 V | CLOCK_IN 1/4 | – | H (Note 13) |
| \$03 | L | – | L | L | L | H | H | 3.0 V | CLOCK_IN 1/8 | – | H (Note 13) |
| \$04 | L | – | L | L | H | L | L | 5.0 V | CLOCK_IN 1/1 | – | H (Note 13) |
| \$05 | L | – | L | L | H | L | H | 5.0 V | CLOCK_IN 1/2 | – | H (Note 13) |
| \$06 | L | – | L | L | H | H | L | 5.0 V | CLOCK_IN 1/4 | – | H (Note 13) |
| \$07 | L | – | L | L | H | H | H | 5.0 V | CLOCK_IN 1/8 | – | H (Note 13) |
| \$08 | L | – | L | H | L | L | L | – | START | – | H (Note 13) |
| \$09 | L | – | L | H | L | L | H | – | STOP Low | – | H (Note 13) |
| \$0A | L | – | L | H | L | H | L | – | STOP High | – | H (Note 13) |
| \$0B | L | – | L | H | L | H | H | – | Reserve | – | H (Note 13) |
| \$0C | L | – | L | H | H | L | L | – | – | Normally Open (Note 12) | H (Note 13) |
| \$0D | L | – | L | H | H | L | H | – | – | Normally Close (Note 12) | H (Note 13) |
| \$0E | L | – | L | H | H | H | L | – | – | Normally Close (Note 12) | H (Note 13) |
| \$0F | L | – | L | H | H | H | H | – | – | Normally Close Note 12) | H (Note 13) |
| \$10 | L | – | H | Z | L | L | Z | – | – | – | Card Present |
| \$12 | L | 1 | H | Z | L | H | Z | – | – | – | DC–DC status |
| \$14 | L | – | H | Z | H | L | Z | – | – | – | Vbat |
| \$16 | L | 1 | H | Z | H | H | Z | – | – | – | CRD_VCC |

- 9. The programmed conditions are latched upon the Chip Select (\overline{CS} , pin 6) positive going transient.
- 10. Card clock integrity is guaranteed no spikes whatever be the frequency switching.
- 11. The STATUS register is not affected when the NCN6000 operates in any of the programming functions.
- 12. The CRD_VCC and CRD_CLK are not affected when the NCN6000 operates outside their respective decoded logic address.
- 13. The High Level on STATUS in registers \$00 to \$0F, inclusive, having being implemented to reduce current consumption but have no other meanings.
- 14. At turn on, the NCN6000 is initialized with CRD_VCC = 3.0V, CLOCK_IN Ratio = 1/1, CRD_CLK = START, CRD_DET = Normally Open.

DC-DC Converter and Card Detector Status

The NCN6000 status can be polled when $\overline{CS} = L$. Please consult Figures 4 and 5 for a description of input and output signals. The status message is described in Table 4.

Note: in order to cope with a start up under low battery condition, the Vbat OK message uses a negative logic as depicted here below.

Table 4. Card and DC-DC Status Output

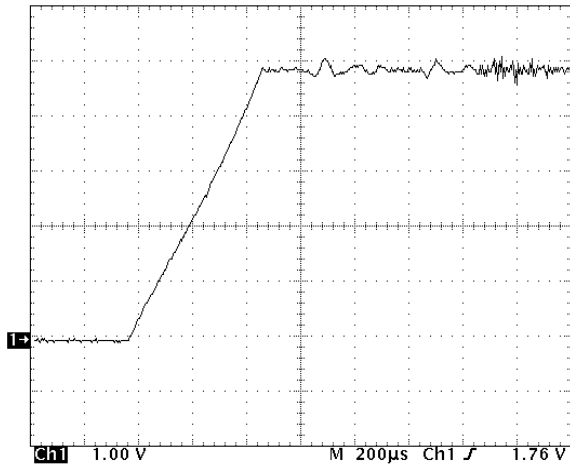
| PGM | A1 | A0 | STATUS | Message |
|------|----|----|--------|----------------------------|
| HIGH | L | L | LOW | No Card |
| HIGH | L | L | HIGH | Card Present |
| HIGH | L | H | LOW | DC-DC Converter Overloaded |
| HIGH | L | H | HIGH | DC-DC Converter OK |
| HIGH | H | L | LOW | Vbat OK |
| HIGH | H | L | HIGH | Vbat Undervoltage |
| HIGH | H | H | HIGH | CRD_VCC OK |
| HIGH | H | H | LOW | CRD_VCC Undervoltage |

The STATUS pin provides a feedback related to the detection of the card, the state of the DC-DC converter, the Vbat undervoltage and CRD_VCC undervoltage situations. When $\overline{PGM} = H$, the STATUS pin returns a High if a card is detected present, a Low being asserted if there is no card inserted. In any case, the external card is not automatically powered up. When the external MPU asserts $PWR_ON = H$, together with $\overline{CS} = L$, the CRD_VCC supply is provided to the card and the state of the DC-DC converter, the Vbat and the CRD_VCC can be polled through the STATUS pin.

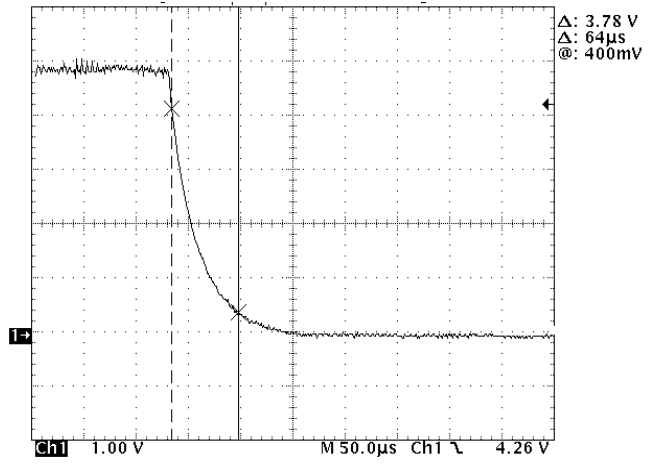
Card Power Supply Timing

At power up, the CRD_VCC power supply rise time depends upon the current capability of the DC-DC converter associated with the external inductor L1 and the reservoir capacitor connected across CRD_VCC and GROUND.

On the other hand, at turn off, the CRD_VCC fall time depends upon the external reservoir capacitor and the peak current absorbed by the internal CMOS transistor built across CRD_VCC and GROUND. These behaviors are depicted in Figure 6. Since these parameters have finite values, depending upon the external constraints, the designer must take care of these limits if the t_{ON} or the t_{OFF} provided by the data sheets does not meet his requirements.



Typical CRD_VCC Rise Time @ Cout = 10 µF, V = 5.0 V



Typical CRD_VCC Fall Time @ Cout = 10 µF, V = 5.0 V

Figure 6. Card Power Supply Turn ON and OFF Timing

Basic Operating Modes Flow Chart

The NCN6000 brings all the functions necessary to handle data communication between a host computer and the smart card. The built-in Chip Select pin provides a simple way to share the same MPU bus with several card interface. On top of that, the logic control are derived from specific pins, avoiding the risk of mixing up the operation when the interface is controlled by a low end microcontroller.

During the transaction operation, the external MPU takes care of whatever is necessary to be data on the single

bidirectional I/O line. Leaving aside the DC-DC control and associated failures, the NCN6000 does not take any further responsibility in the data transaction.

When the chip operates in the programming mode, the NCN6000 provide a flexible access to set up the CRD_VCC voltage, the CRD_CLK and the CRD_DET smart card signals.

The external microcontroller takes care of the smart card transaction and shall handle the interface accordingly.

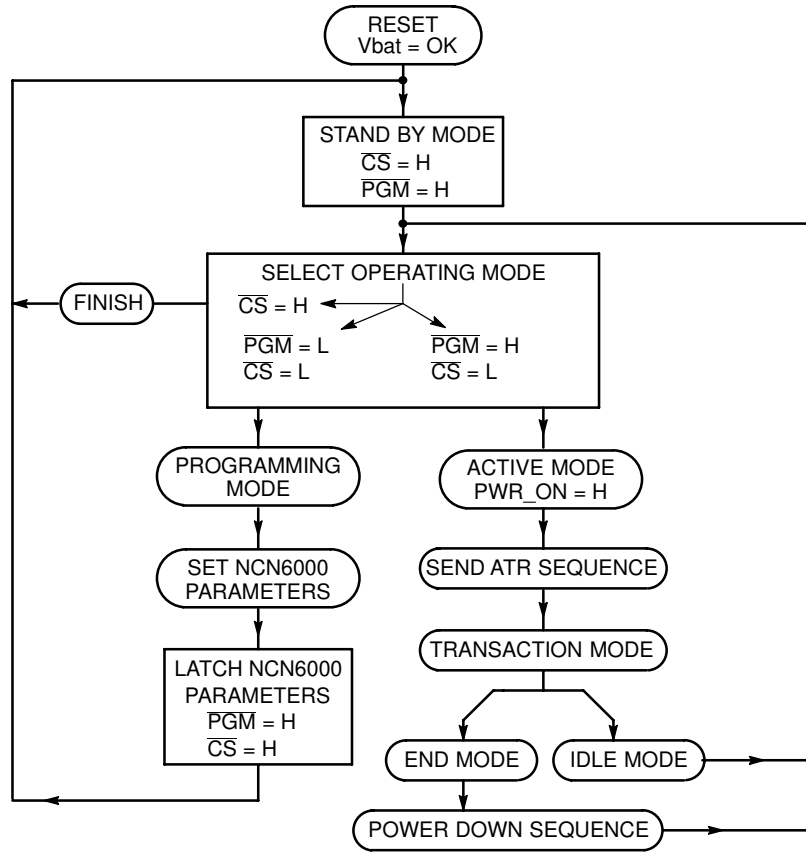


Figure 7. Operating Modes Flow Chart

Standby Mode

The Standby Mode allows the NCN6000 to detect a card insertion, keeping the power consumption at a minimum. The power supply CRD_VCC is not applied to the card, until the external controllers set PWR_ON = H with CS = L.

When a card is inserted, the internal logic filters the signal present pin 11, then asserts the INT pin to Low if the pulse applied to CRD_DET is longer than 150 μs. The external MPU shall run whatever is necessary to handle the card.

The INT is cleared (return to High) when a positive going transition is asserted to either the CS or to the PWR_ON signal logically combined with Chip Select = Low.

Standby Mode

Logic Conditions:

CS = H
 PWR_ON = H
 A0 = Z
 A1 = Z
 PGM = Z
 I/O = Z
 RESET = Z

Card Output:

CRD_VCC = 0 V
 CRD_CLK = L
 CRD_RST = L
 CRD_IO = L

Programming Mode

The programming mode allows the configuration of the card power supply, card clock and Card Detection input logic polarity. These signals (CRD_VCC, CRD_CLK and CRD_DET) are described in the pin description paragraph associated with Tables 1 and 3 and Figures 4 and 8.

Programming Mode Logic Conditions:

CS = L
 PWR_ON = L
 A0 = H/L
 A1 = H/L
 PGM = L
 I/O = L/H
 RESET = L/H

Card Output:

CRD_VCC = 0 V
 CRD_CLK = L
 CRD_RST = L
 CRD_IO = H/L depending upon the previous I/O pin logic state

The I/O and RESET pins are not connected to the smart card and become logic inputs to control the NCN6000 programming sequence. The programmed values are latched upon transition of CS from Low to High, PGM being Low during the transition.

When a programming mode is validated by a Chip Select negative going transient, the mode is latched and PGM can be released to High. This latch is automatically reset when CS returns to High.

The logic input signals can be set simultaneously, or one bit a time (using either a STAA or a BSET function), the key point being the minimum delay between the shorter bit and the Chip Select pulse. The programmed value is latched into the NCN6000 register on the CS positive going edge.

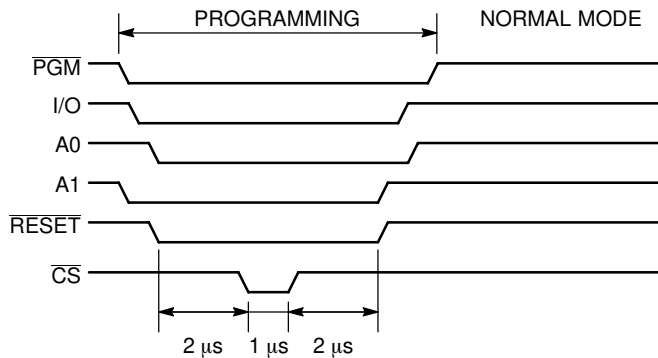


Figure 8. Minimum Programming Timings

Active Mode

In the active mode, the NCN6000 is selected by the external MPU and the STATUS pin can be polled to get the status of either the DC-DC converter or the presence of the card (inserted or not valid). The power is not connected to the card: CRD_VCC = 0 V.

Active Mode Logic Conditions:

CS = L
 PWR_ON = L
 A0 = L
 A1 = L
 PGM = H
 I/O = Z
 RESET = Z
 STATUS = L/H is Card Inserted?

Card Output:

CRD_VCC = 0 V
 CRD_CLK = L
 CRD_RST = L
 CRD_IO = H/L depending upon the previous I/O pin logic state

The Chip Select pulse [CS] will automatically clear the previously asserted INT signal upon the positive going transition.

If a card is present, the MPU shall activate the DC-DC converter by asserting PWR_ON = H. The NCN6000 will automatically run a power up sequence when the CRD_VCC reaches the undervoltage level (either VC5H or VC3H, depending upon the CRD_VCC voltage supply programmed). The CRD_IO, CRD_RST and CRD_CLK pins are validated, according to the ISO7816-3 sequence. The interface is now in transaction mode and the system is ready for data exchange through the I/O and RESET lines. At any time, the microcontroller can change the CRD_CLK frequency and mode, or the CRD_VCC value as determined by the card being in use.

Transaction Mode

During the transaction mode, the NCN6000 maintains power supply and clock signal to the card. All the signal levels related with the card are translated as necessary to cope with the MPU and the card.

The DC-DC converter status and the Vbat state can be monitored on the STATUS by using the A0 and A1 logic inputs as depicted in Tables 3 and 4.

Transaction Mode Logic Conditions:

\overline{CS} = L
 PWR_ON = H
 A0 = H
 A1 = H
 PGM = H
 I/O = DATA TRANSFER
 RESET = H/L
 STATUS = L/H DC-DC status: Fail/Pass?

Card Output:

CRD_VCC = 3.0 or 5.0 V
 CRD_CLK = CLOCK
 CRD_RST = H/L
 CRD_IO = DATA TRANSFER

To make sure the data are not polluted by power losses, it is recommended to check the state of CRD_VCC before launching a new data transaction. Since $\overline{CS} = L$, this is achieved by forcing bits A0 and A1 according to Table 4, and reading the STATUS pin 5.

Idle Mode

The idle mode is used when a card is powered up (CRD_VCC = Vcc), without communication on going.

Idle Mode

Logic Conditions:

\overline{CS} = L
 PWR_ON = H
 A0 = H
 A1 = H
 PGM = H
 I/O = Z
 RESET = H
 STATUS = L/H according to the internal register results

Card Output:

CRD_VCC = 3.0 or 5.0 V
 CRD_CLK = CLOCK active or L or H
 CRD_RST = H
 CRD_IO = Z

In addition, the CRD_CLK signal can be stopped, as depicted in Tables 3 and 4, to minimize the current consumption of the external smart card, leaving CRD_VCC active.

Power Down Operation

The power down mode can be initiated by either the external MPU (pulling PWR_ON = L) or by one of the internal error condition (CRD_VCC overload or Vbat Low). The communication session is terminated immediately, according to the ISO7816-3 sequence. On the other hand, the MPU can run the Standby mode by forced $\overline{CS} = H$.

When the card is extracted, the interface shall detect the operation and run the Power Shut Off of the card as described by the ISO/CEI 7816-3 sequence depicted here after:

ISO7816-3 sequence:

- ⇒ Force RST to Low
- ⇒ Force CLK to Low, unless it is already in this state
- ⇒ Force CRD_IO to Low
- ⇒ Shut Off the CRD_VCC supply

Since the internal digital filter is activated for any card insertion or extraction, the physical power sequence will be activated 150 μs maximum after the card has been extracted. Of course, such a delay does not exist when the MPU launch the power down intentionally.

The time delay between each negative going signal is 500 ns typical (Figure 10).

NCN6000

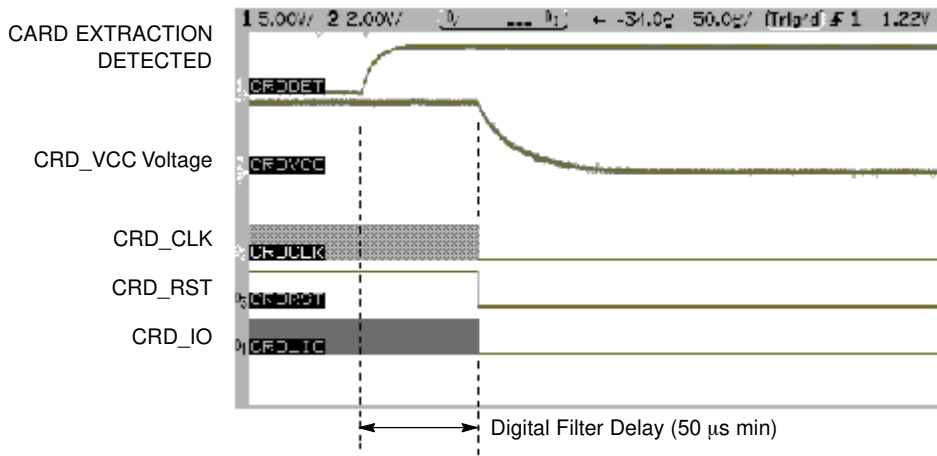


Figure 9. Typical Power Down Sequence in the NCN6000 Interface

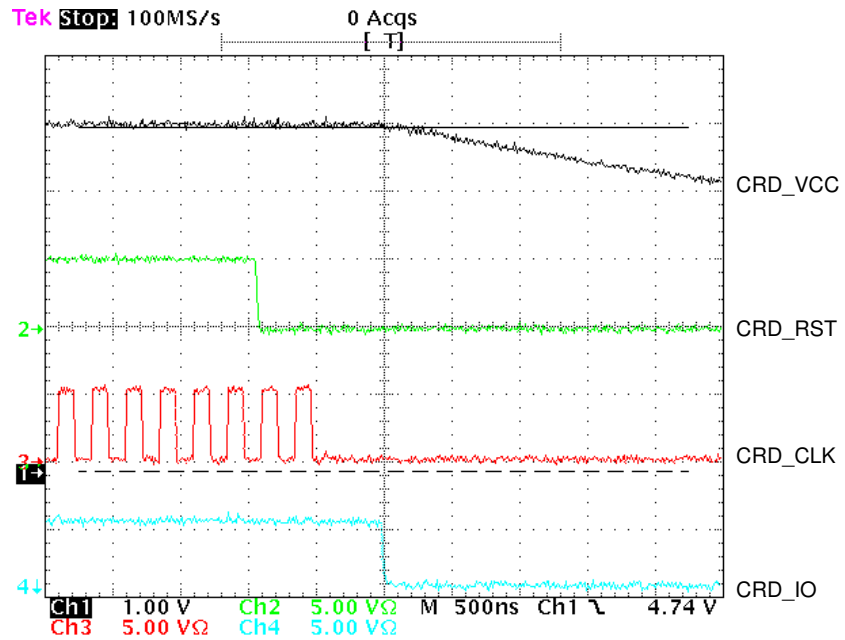


Figure 10. Power Down Sequence Details

Card Detection

The card detector circuit provides a 500 kΩ pull up resistor to bias the CRD_DET pin, yielding a logic High when the pin is left open (assuming a NO switch). The internal logic associated with pin 11 provides an automatic selection of the slope card detection, depending upon the polarity set by the external MPU. At start up, the CRD_DET is preset to cope with Normally Open switch. When a Normally Close switch is used in the card socket, it is mandatory to program the NCN6000 chip during the initialization sequence, otherwise the system will not start if a card was previously inserted. Table 3 gives the programming code for such a function. The next lines provide a typical assembler source to handle this CRD_DET Normally Close polarity:

```
Smart EQU $20 ; NCN6000 Physical CS Address
LDX #$1000 ; Offset
LDAA #$09 ; I/O = H, A0 = A1 = L, RESET = H
STAA smart, X ; Set CRD_DET = Normally Closed
Switch
```

The CRD_DET polarity can be updated at any time, during the Program Mode sequence (PGM = L), but, generally speaking, is useless since the switch does not change during the usage of the considered module. On the other hand, the card detection switch shall be connected across pin 11 and ground, for any polarity selected.

The transition presents pin 11, whatever be the polarity, is filtered out by the internal digital filter circuit, avoiding false interrupt. In addition to the minimum internal 50 μs timing, the MPU shall provide an additional delay to cope with the mechanical stabilization of the card interface (typically 3 ms), prior to valid the CRD_VCC supply.

When a card is inserted, the detector circuit asserts \overline{INT} = Low as depicted before. When the NCN6000 detects a card extraction, the power down sequence is activated, regardless of the PWR_ON state, and the \overline{INT} pin is asserted Low. It is up to the external MPU to clear this interrupt by forcing a chip select pulse as depicted in Figure 5.

The 75 μs delay represent the digital filter built-in the NCN6000 chip being used for the characterization. Any pulse shorter than this delay does not generate an interrupt. However, to guarantee an interrupt will be generated, the CRD_DET signal must be longer than 150 μs as defined by the specification.

The Chip Select pulse is generated by the external microcontroller, the minimum pulse width being 2 μs to make sure the card is detected.

The oscillogram, Figure 11, depicts the behavior for a Normally Open switch, the delay existing between the interrupt negative going state and the \overline{CS} being Low comes from the particular software latency existing in this particular MPU.

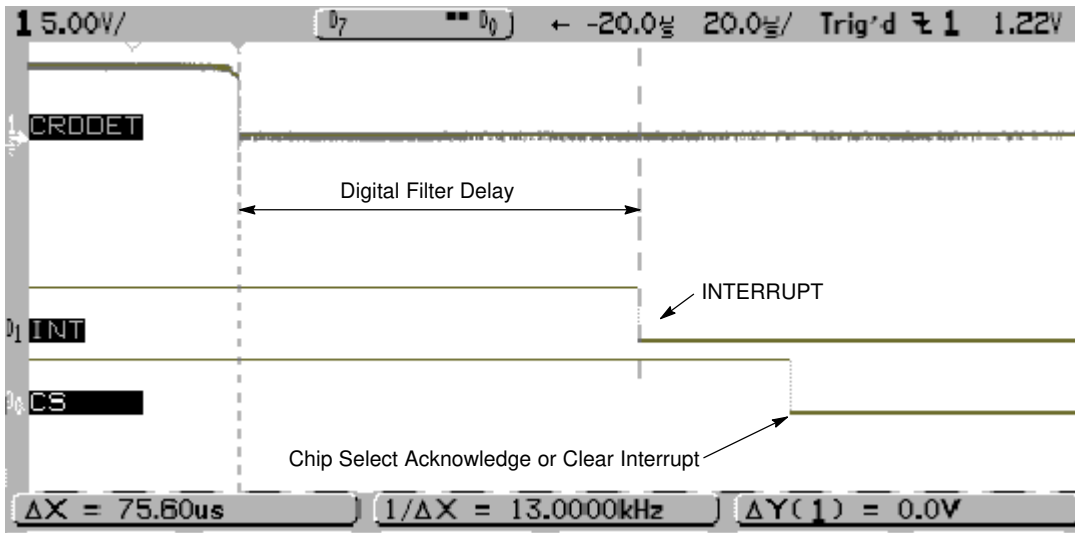


Figure 11. Card Insertion Detection and Interrupt Signals

NCN6000

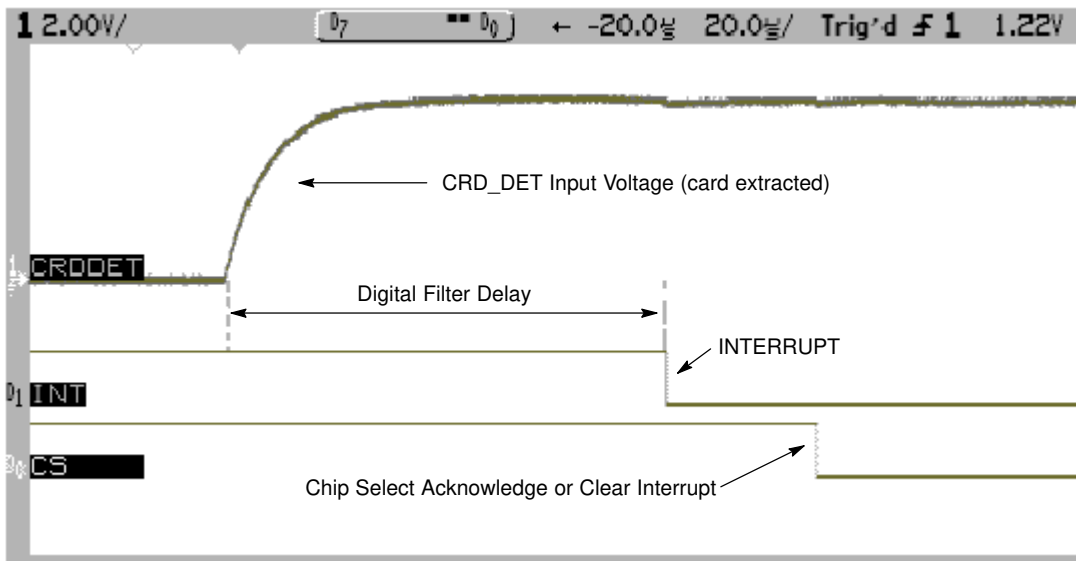


Figure 12. Card Extraction Detection and Interrupt Signals

When the card is extracted, the CRD_DET signal generates an interrupt, assuming the positive pulse width is longer than the digital filter. The oscillogram, Figure 12, depicts the behavior for a Normally Open switch.

Note: since the internal pull up resistor is relatively high (500 kΩ typical), one must use a 10 MΩ input impedance probe to read this signal.

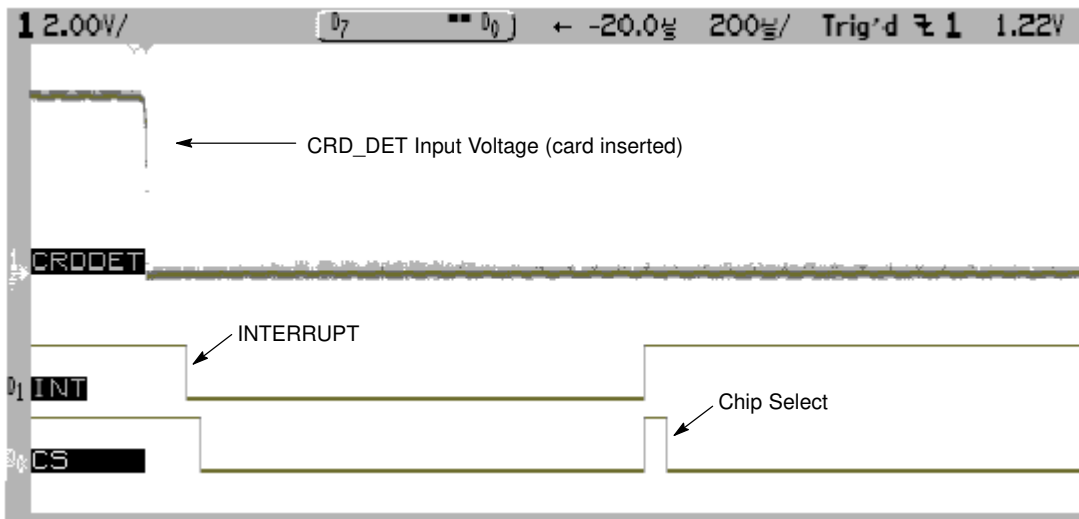


Figure 13. Interrupt Acknowledgement During a Card Insertion Detection Sequence

The interrupt signal, provided pin 9, is cleared by a positive going Chip Select signal as depicted by the oscillogram, Figure 13. The \overline{CS} pulse width is irrelevant, as long as it is larger than 2.0 µs, to activate a different sequence. Leaving the interrupt signal Low has no influence

on the internal behavior of the NCN6000, but will be automatically cleared when the DC-DC will be activated by the MPU ($\overline{CS}=L$, PWR_ON = Positive High transition)

Power Management

The purpose of the power management is to activate the circuit functions needed to run a given mode of operation, yielding a minimum current consumption on the Vbat supply. In the Standby mode (PWR_ON = L), the power management provides energy to the card detection circuit only. All the card interface pins are forced to ground potential.

In the event of a power up request coming from the external MPU (PWR_ON = H, CS = L), the power manager starts the DC-DC converter.

When the CRD_VCC voltage reaches the programmed value (3.0 V or 5.0 V), the circuit activates the card signals according to the following sequence:

- CRD_VCC
- ⇒CRD_IO
- ⇒CRD_CLK
- ⇒CRD_RST

The logic level of the data lines are asserted High or Low, depending upon the state forced by the external MPU, when the start up sequence is completed. Under no situation the NCN6000 shall launch automatically a smart card ATR sequence. Assuming PWR_ON = H, the CRD_VCC voltage

is maintained whatever be the logic level presents on Chip Select, pin 6.

At the end of the transaction, asserted by the MPU (PWR_ON = L, CS = L), or under a card extraction, the ISO7816-3 power down sequence takes place:

- CRD_RST
- ⇒CRD_CLK
- ⇒CRD_IO
- ⇒CRD_VCC

When CS = H, the bi-directional I/O line (pins 8 and 15) is forced into the High impedance mode to avoid signal collision with any data coming from the external MPU.

The CRD_VCC voltage is controlled by means of CS and PWR_ON logic signal as depicted in Figure 14. The PWR_ON logic level define the CRD_VCC voltage status, the amplitude being the one pre programmed into the chip.

In order to avoid uncontrolled command applied to the smart card, the NCN6000 internal logic circuit, together with the Vbat monitoring, clamps the card outputs until the CRD_VCC voltage reaches the minimum value. During the CRD_VCC slope, all the card outputs are kept Low and no spikes can be write to the smart card. The oscillogram on the right hand side is a magnification of the curves given on the opposite side.

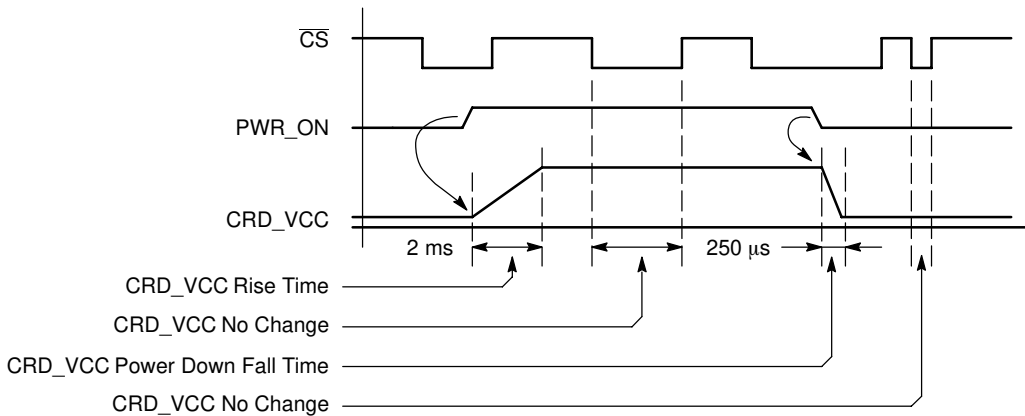


Figure 14. Card Power Supply Control

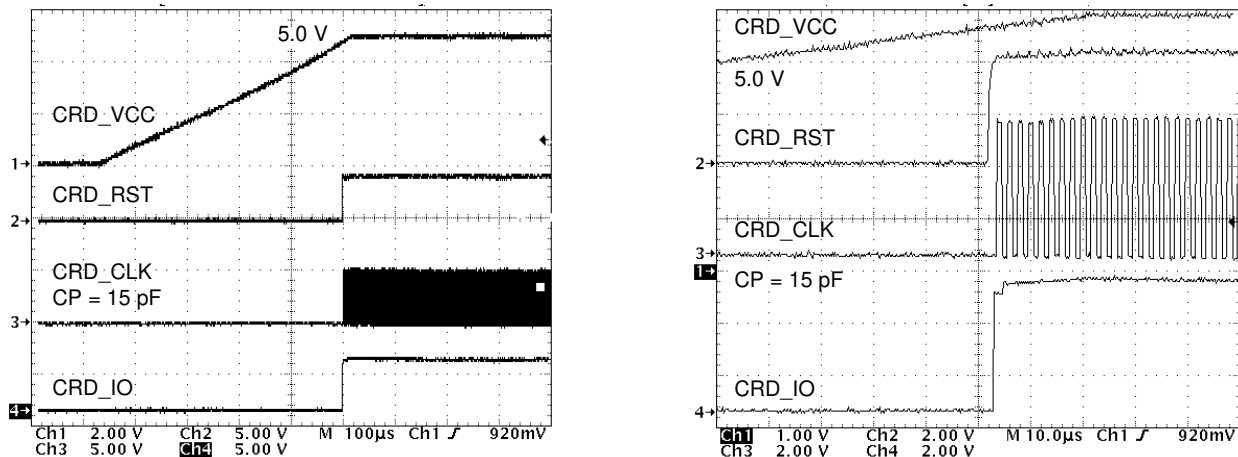


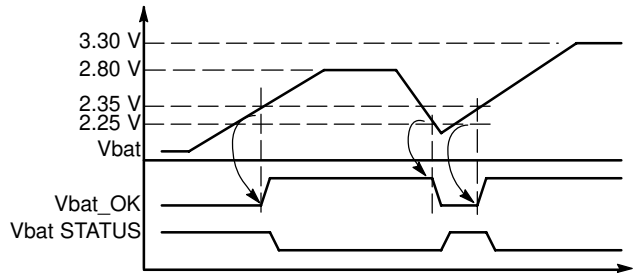
Figure 15. Smart Card Signals Sequence at Power On

Vbat Supply Voltage Monitoring

The built-in comparator, associated with the band gap reference, continuously monitors the +Vbat input. During the start up, all the NCN6000 functions are deactivated and no data transfer can take place. When the +Vbat voltage rises above 2.35 V (typical), the chip is activated and all the functions becomes available. The typical behavior is provided here after Figure 16. At this point, the internal Power On Reset signal is activated (not accessible externally) and all the logic signals are forced into the states as defined by Table 3.

If the +Vbat voltage drops below 2.25 V (typical) during the operation, the NCN6000 generate a Power Down sequence and is forced in a no operation mode. The built-in 100 mV (typical) hysteresis avoids unstable operation when the battery voltage slowly varies around the 2.30 V.

On the other hand, the microcontroller can read the STATUS signal, pin 5, to control the state of the battery prior to launch either a NCN6000 programming or an ATR sequence (Table 4).



Note: Drawing is not to scale and voltages are typical. See specifications data for details.

Figure 16. Typical Vbat Monitoring

DC-DC Converter Operation

The built-in DC-DC converter is based on a modified boost structure to cover the full battery and card operating voltage range. The built-in battery voltage monitor provides an automatic system to accommodate the mode of operation whatever be the Vbat and CRD_VCC voltages. Comparator U3/ Figure 17 tracks the two voltages and set up the operating mode accordingly.

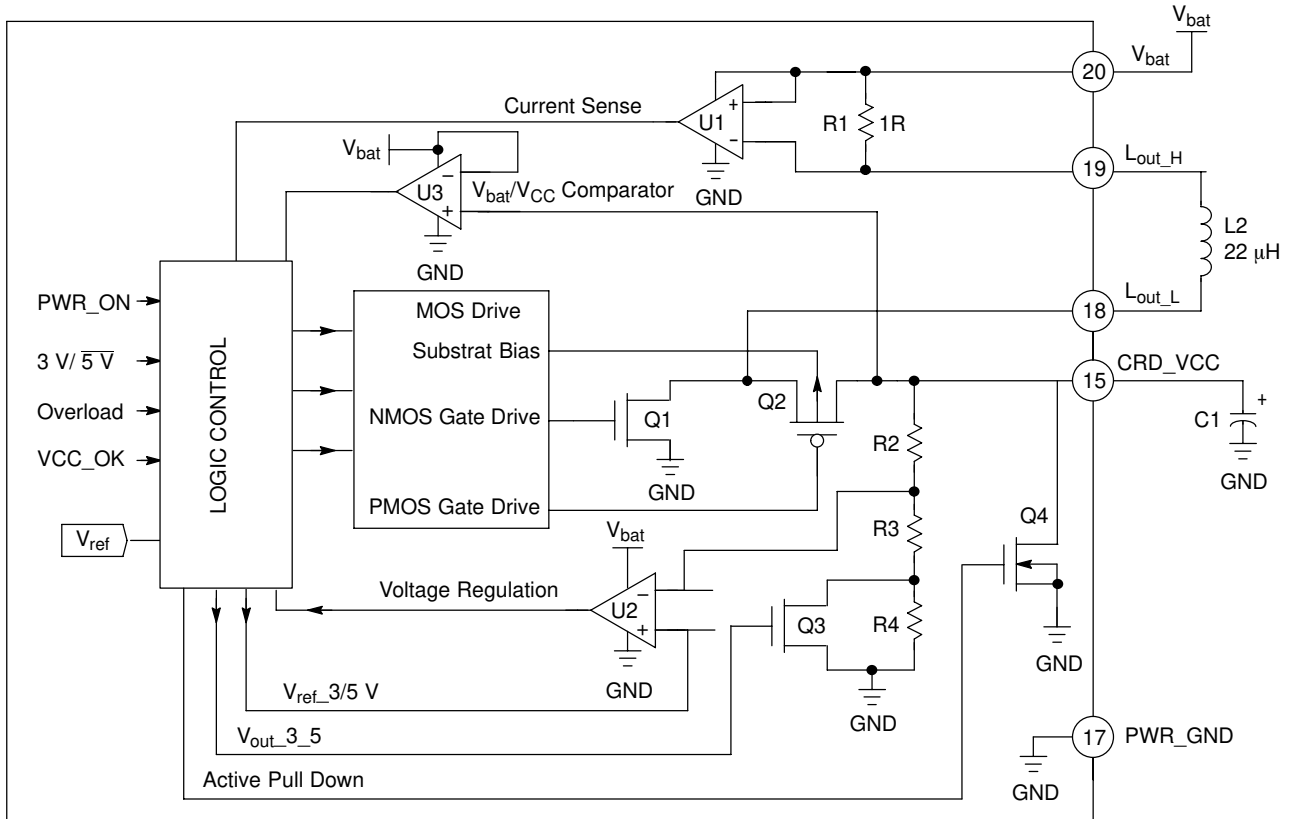


Figure 17. Basic DC-DC Structure

When the input voltage V_{bat} is lower than the programmed CRD_VCC , the system operates under the boost mode, providing the voltage regulation and current limit to the smart card. In this mode, the external inductor, typically $22\ \mu H$, stores the energy to drive the $+5.0\ V$ card supply from the external low voltage battery. The

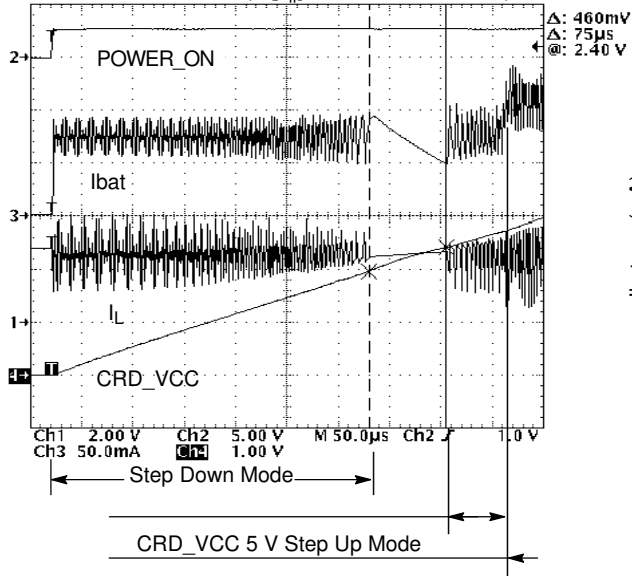


Figure 18. DC-DC Operating Modes

When the input voltage V_{bat} is higher than the programmed CRD_VCC , the system operates under a step down mode, yielding the voltage regulation and current limit identical to the boost mode. In this case, the built-in structure turns Off Q1 and inverts the Q2 substrate bias to control the current flowing to the load. These operations are fully automatic and transparent for the end user.

The High and Low limits of the current flowing into the external inductor L1 are sensed by the operational amplifier U1 associated with the internal shunt R1. Since this shunt resistor is located on the hot side of the inductor, the device reads both the charge and discharge of the inductor, providing a clean operation of the converter.

In order to optimize the DC-DC power conversion efficiency, it is recommended to use external inductor with $R < 2.0\ \Omega$.

The output capacitor C1 stores the energy coming from the converter and smooths the CRD_VCC voltage applied to the external card. At this point, care must be observed, beside the micro farad value, to select the right type of capacitor. According to the capacitor's manufacturers, the internal ESR can range from a low $10\ m\Omega$ to more than $3.0\ \Omega$, thus yielding high losses during the DC-DC operation, depending upon the technology used to build the capacitor.

oscilloscope, Figure 18, depicts the DC-DC behavior under these two modes of operation.

Beside the DC-DC converter, NMOS Q4 provides a low impedance to ground during the Power Down sequence, yielding the $250\ \mu s$ maximum switch time depicted in the data sheet.

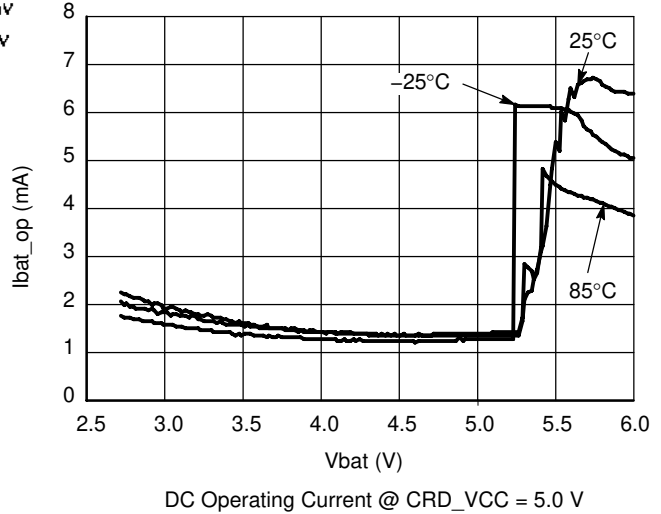


Figure 19. Typical DC Operating Current

The standard electrolytic capacitors have the low cost advantage for a relative high micro farad value, but have poor tolerance, high leakage current and high ESR.

The tantalum type brings much lower leakage current together with high capacity value per volume, but cost can be an issue and ESR is rarely better than $500\ m\Omega$.

The new ceramic type have a very low leakage together with ESR in the $50\ m\Omega$ range, but value above $10\ \mu F$ are relatively rare. Moreover, depending upon the low cost ceramic material used to build these capacitors, the thermal coefficient can be very bad, as depicted in Figure 20. The X7R type is highly recommended to achieve low voltage ripple.

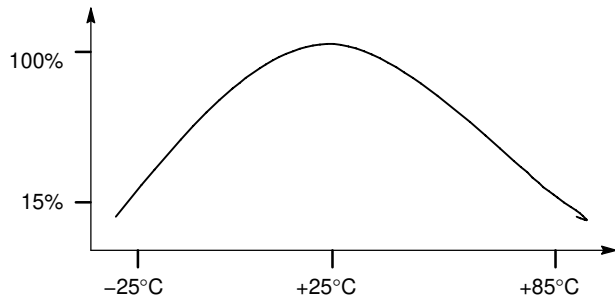


Figure 20. Typical Y7R Ceramic Type Value as a Function of the Temperature.

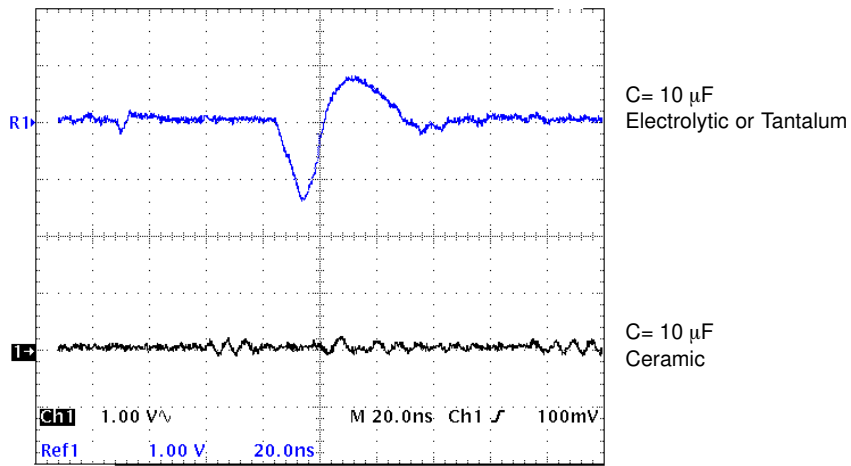
NCN6000

Based on the experiments carried out during the NCN6000 characterization, the best compromise, at time of printing this document, is to use two 6.8 $\mu\text{F}/10\text{ V}/\text{Ceramic}/\text{X7R}$ capacitor in parallel to achieve the CRD_VCC filtering. The ESR will not extend 50 m Ω over the temperature range and the combination of standard parts provide an acceptable -20% to $+20\%$ tolerance,

together with a low cost. Obviously, the capacitor must be SMD type to achieve the extremely low ESR and ESL necessary for this application. Figure 21 illustrates the CRD_VCC ripple observed in the NCN6000 demo board depending upon the type of capacitor used to filter the output voltage.

Table 5. Ceramic/Electrolytic Capacitors Comparison

| Manufacturers | Type/Series | Format | Max Value | Tolerance | Typ. Z @ 500 kHz |
|---------------|-----------------------|--------|-------------------------------|---------------|------------------|
| MURATA | CERAMIC/GRM225 | 0805 | 10 $\mu\text{F}/6.3\text{ V}$ | $+80\%/-20\%$ | 30 m Ω |
| VISHAY | Tantalum/594C/593C | | 10 $\mu\text{F}/16\text{ V}$ | | 450 m Ω |
| VISHAY | Electrolytic/94SV | | 10 $\mu\text{F}/10\text{ V}$ | $-20\%/+20\%$ | 400 m Ω |
| | Electrolytic Low Cost | | 10 $\mu\text{F}/10\text{ V}$ | $-35\%/+50\%$ | 2.0 Ω |



Top Trace = Electrolytic or Tantalum 10 μF
 Bottom Trace = X7R 10 μF ceramic
 The high ripple pulse across CRD_VCC is the consequence of the large ESR of the electrolytic capacitor.

Figure 21. CRD_VCC Ripple as a Function of the Capacitor Technology

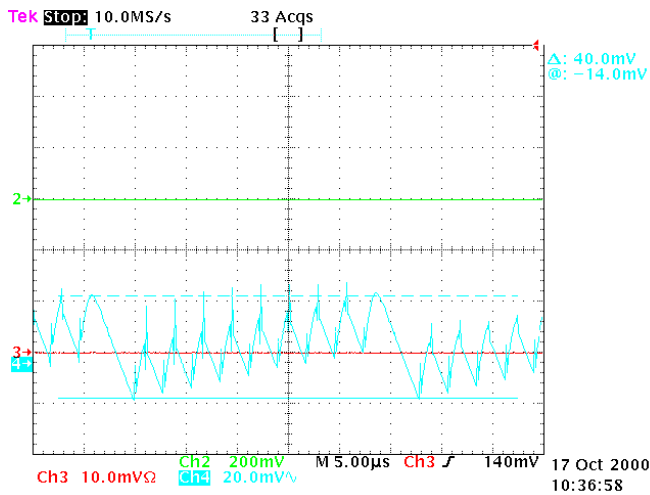


Figure 22. External Capacitor Current Charge and CRD_VCC Voltage Ripple.

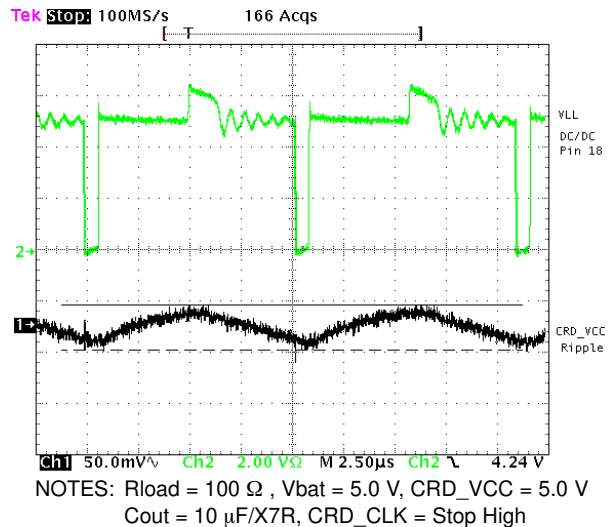


Figure 23. CRD_VCC Voltage Ripple

Clock Divider

The main purpose of the built-in clock generator is threefold:

1. Adapts the voltage level shifter to cope with the different voltages that might exist between the MPU and the Smart Card.
2. Provides a frequency division to adapt the Smart Card operating frequency from the external clock source.
3. Controls the clock state according to the smart card specification.

In addition, the NCN6000 adjusts the signal coming from the microprocessor to get the Duty Cycle window as defined by the ISO7816-3 specification.

The logic input pins A0, A1, $\overline{\text{PGM}}$, I/O and $\overline{\text{RESET}}$ fulfill the programming functions when both $\overline{\text{PGM}}$ and $\overline{\text{CS}}$ are

Low. The clock input stage (CLOCK_IN) can handle a 40 MHz frequency maximum, the divider being capable to provide a 1:8 ratio. Of course, the ratio must be defined by the engineer to cope with the Smart Card considered in a given application and, in any case, the output clock [CRD_CLK] shall be limited to 20 MHz maximum signal. In order to maximize the CLOCK_IN bandwidth, this pin has no Schmitt trigger input. The simple associated CMOS has a $V_{\text{bat}}/2$ threshold level. In order to minimize the dI/dt and dV/dV developed in the CRD_CLK line, the peak current as been internally limited to 30 mA peak (typical @ $\text{CRD_VCC} = 5.0 \text{ V}$), hence limited the rise and fall time to 10 ns typical. Consequently, the NCN6000 fulfills the ISO7816 specification up to 10 MHz maximum, but can be used up to 20 MHz when the final application operates in a limited ambient temperature range.

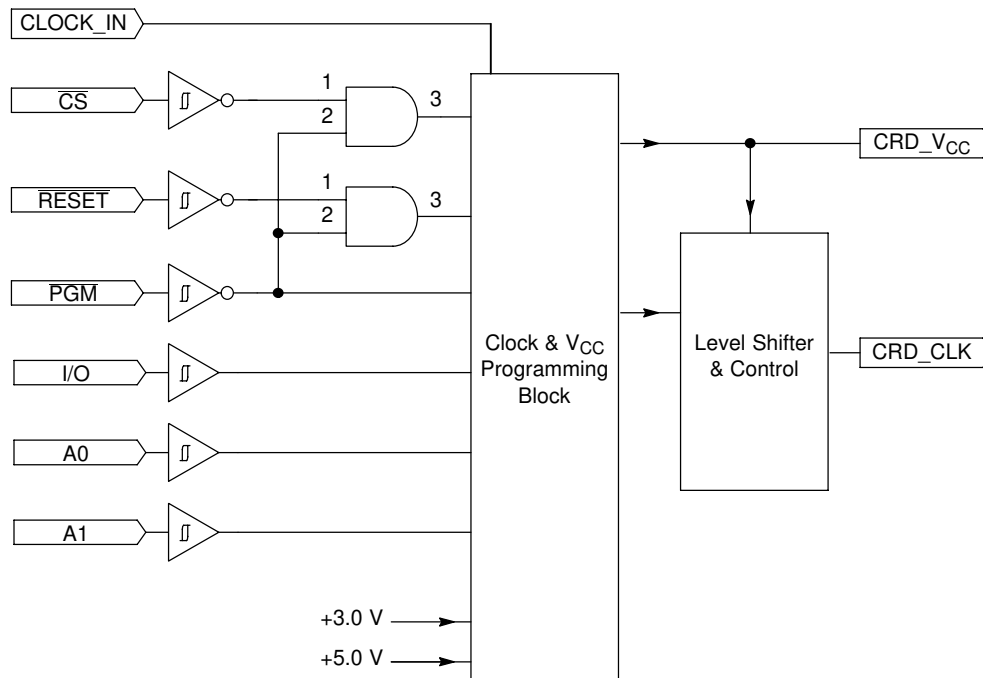


Figure 24. Simplified Frequency Divider and Programming Functions

In order to avoid any duty cycle out of the frequency smart card ISO7816-3 specification, the divider is synchronized by the last flip flop, thus yielding a constant 50% duty cycle, whatever be the divider ratio. Consequently, the output

CRD_CLK frequency division can be delayed by eight CLOCK_IN pulses and the microcontroller software must take this delay into account prior to launch a new data transaction.