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# NCP1060, NCP1063

## High-Voltage Switcher for Low Power Offline SMPS

The NCP106X products integrate a fixed frequency current mode controller with a 700 V MOSFET. Available in a PDIP-7, SOIC-10 or SOIC-16 package, the NCP106X offer a high level of integration, including soft-start, frequency-jittering, short-circuit protection, skip-cycle, adjustable peak current set point, ramp compensation, and a Dynamic Self-Supply (eliminating the need for an auxiliary winding).

Unlike other monolithic solutions, the NCP106X is quiet by nature: during nominal load operation, the part switches at one of the available frequencies (60 kHz or 100 kHz). When the output power demand diminishes, the IC automatically enters frequency foldback mode and provides excellent efficiency at light loads. When the power demand reduces further, it enters into a skip mode to reduce the standby consumption down to a no load condition.

Protection features include: a timer to detect an overload or a short-circuit event, Overvoltage Protection with auto-recovery and AC input line voltage detection (A version).

The ON proprietary integrated Over Power Protection (OPP) lets you harness the maximum delivered power without affecting your standby performance simply via external resistors.

For improved standby performance, the connection of an auxiliary winding stops the DSS operation and helps to reduce input power consumption below 50 mW at high line.

NCP106x can be seamlessly used both in non-isolated and in isolated topologies.

### Features

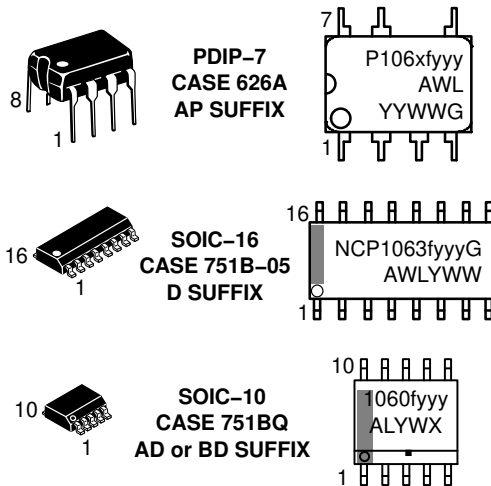
- Built-in 700 V MOSFET with  $R_{DS(on)}$  of 34  $\Omega$  (NCP1060) and 11.4  $\Omega$  (NCP1063)
- Large Creepage Distance Between High-voltage Pins
- Current-Mode Fixed Frequency Operation – 60 kHz or 100 kHz (130 kHz on demand)
- Adjustable Peak Current: see below table
- Fixed Ramp Compensation
- Direct Feedback Connection for Non-isolated Converter
- Internal and Adjustable Over Power Protection (OPP) Circuit
- Skip-Cycle Operation at Low Peak Currents Only
- Dynamic Self-Supply: No Need for an Auxiliary Winding
- Internal 4 ms Soft-Start
- Auto-Recovery Output Short Circuit Protection with Timer-Based Detection
- Auto-Recovery Overvoltage Protection with Auxiliary Winding Operation
- Frequency Jittering for Better EMI Signature
- No Load Input Consumption < 50 mW



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### MARKING DIAGRAMS



x = Power Switch Circuit On-state Resistance  
(0 = 34  $\Omega$ , 3 = 11.4  $\Omega$ )  
f = Brown In (A = Yes, B = No)  
yyy = Oscillator Frequency  
(060 = 60 kHz, 100 = 100 kHz)  
A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G or ■ = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 28 of this data sheet.

- Frequency Foldback to Improve Efficiency at Light Load
- These are Pb-Free Devices

### Typical Applications

- Auxiliary / Standby Isolated and Non-isolated Power Supplies
- Power Meter SMPS
- Wide Vin Low Power Industrial SMPS

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## PRODUCT INFORMATION & INDICATIVE MAXIMUM OUTPUT POWER

Product	R <sub>DS(on)</sub>	I <sub>PK(0)</sub>	230 Vac ± 15%		85 – 265 Vac	
			Adapter	Open Frame	Adapter	Open Frame
NCP1060 60 kHz	34 Ω	300 mA	3.3 W	8.3 W	1.9 W	4.7 W
NCP1063 100 kHz	11.4 Ω	780 mA	6.2 W	15.5 W	3.3 W	7.8 W

NOTE: Informative values only, with T<sub>amb</sub> = 25°C, T<sub>case</sub> = 100°C, PDIP-7 package, Self supply via Auxiliary winding and circuit mounted on minimum copper area as recommended.

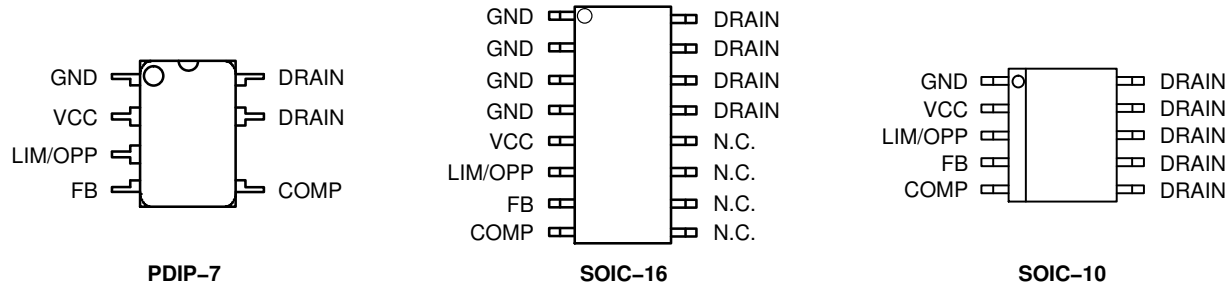


Figure 1. Pin Connections

Table 1. PIN FUNCTION DESCRIPTION

Pin No			Pin Name	Function	Pin Description
PDIP 7	SOIC 10	SOIC 16			
1	1	1-4	GND	The IC Ground	
2	2	5	V <sub>CC</sub>	Powers the internal circuitry	This pin is connected to an external capacitor. The V <sub>DD</sub> includes an auto-recovery over voltage protection.
3	3	6	LIM/OPP	I <sub>peak</sub> set / Over power limitation	The current drawn from the pin decreases I <sub>peak</sub> of the primary winding. If resistive divider from the auxiliary winding is connected to this pin it sets the OPP compensation level (it diminishes the peak current.)
4	4	7	FB	Feedback signal input	This is the inverting input of the trans conductance error amplifier. It is normally connected to the switching power supply output through a resistor divider.
5	5	8	Comp	Compensation	The error amplifier output is available on this pin. The network connected between this pin and ground adjusts the regulation loop bandwidth. Also, by connecting an opto-coupler to this pin, the peak current set point is adjusted accordingly to the output power demand.
6		9-12			This un-connected pin ensures adequate creepage distance
7,8	6-10	13-16	Drain	Drain connection	The internal drain MOSFET connection

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**Table 2. TYPICAL APPLICATIONS**

	<ul style="list-style-type: none"> <li>• If the output voltage is above 9.0 V typ. between <math>V_{CC(ON)}</math> level and <math>V_{OVP}</math> level – VCC supplied from output via D2</li> <li>• R2 limits maximal output power</li> <li>• Direct feedback, resistive divider formed by R3, R4 sets output voltage</li> </ul>
	<ul style="list-style-type: none"> <li>• VCC supplied from DSS</li> <li>• Output voltage is below 9.0 V typ.</li> <li>• LIM/OPP pin floating – no limit output power</li> <li>• Optocoupler feedback</li> </ul>
<b>Typical Non-isolated Application – Buck Converter</b>	
	<ul style="list-style-type: none"> <li>• If the output voltage is above 9.0 V typ. between <math>V_{CC(ON)}</math> level and <math>V_{OVP}</math> level – VCC supplied from output via D2</li> <li>• R2 limits maximal output power</li> <li>• Direct feedback, resistive divider formed by R3, R4 sets output voltage</li> </ul>
	<ul style="list-style-type: none"> <li>• VCC supplied from DSS</li> <li>• Output voltage is below 9.0 V typ.</li> <li>• LIM/OPP pin floating – no limit output power</li> <li>• Direct feedback, resistive divider formed by R2, R3 sets output voltage</li> </ul>
<b>Typical Non-isolated Application – Buck-Boost Converter</b>	

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**Table 2. TYPICAL APPLICATIONS**

	<ul style="list-style-type: none"> <li>• VCC supplied from DSS</li> <li>• Output voltage is below 9.0 V typ.</li> <li>• LIM/OPP pin floating – no limit output power</li> <li>• Resistive divider formed by R2, R3 sets output voltage</li> </ul>
	<ul style="list-style-type: none"> <li>• If the output voltage is above 9.0 V typ. between V<sub>CC(ON)</sub> level and V<sub>OVP</sub> level – VCC supplied from output via D4</li> <li>• LIM/OPP pin floating – no limit output power</li> <li>• Resistive divider formed by R2, R3 sets output voltage</li> </ul>
<p><b>Typical Non-isolated Application – Flyback Converter</b></p>	
	<ul style="list-style-type: none"> <li>• VCC supplied from auxiliary winding</li> <li>• Resistive divider formed by R2, R3 sets output power limit and over power protection</li> <li>• Optocoupler feedback, resistive divider formed by R6, R7 sets output voltage</li> </ul>
<p><b>Typical Isolated Application – Flyback Converter</b></p>	

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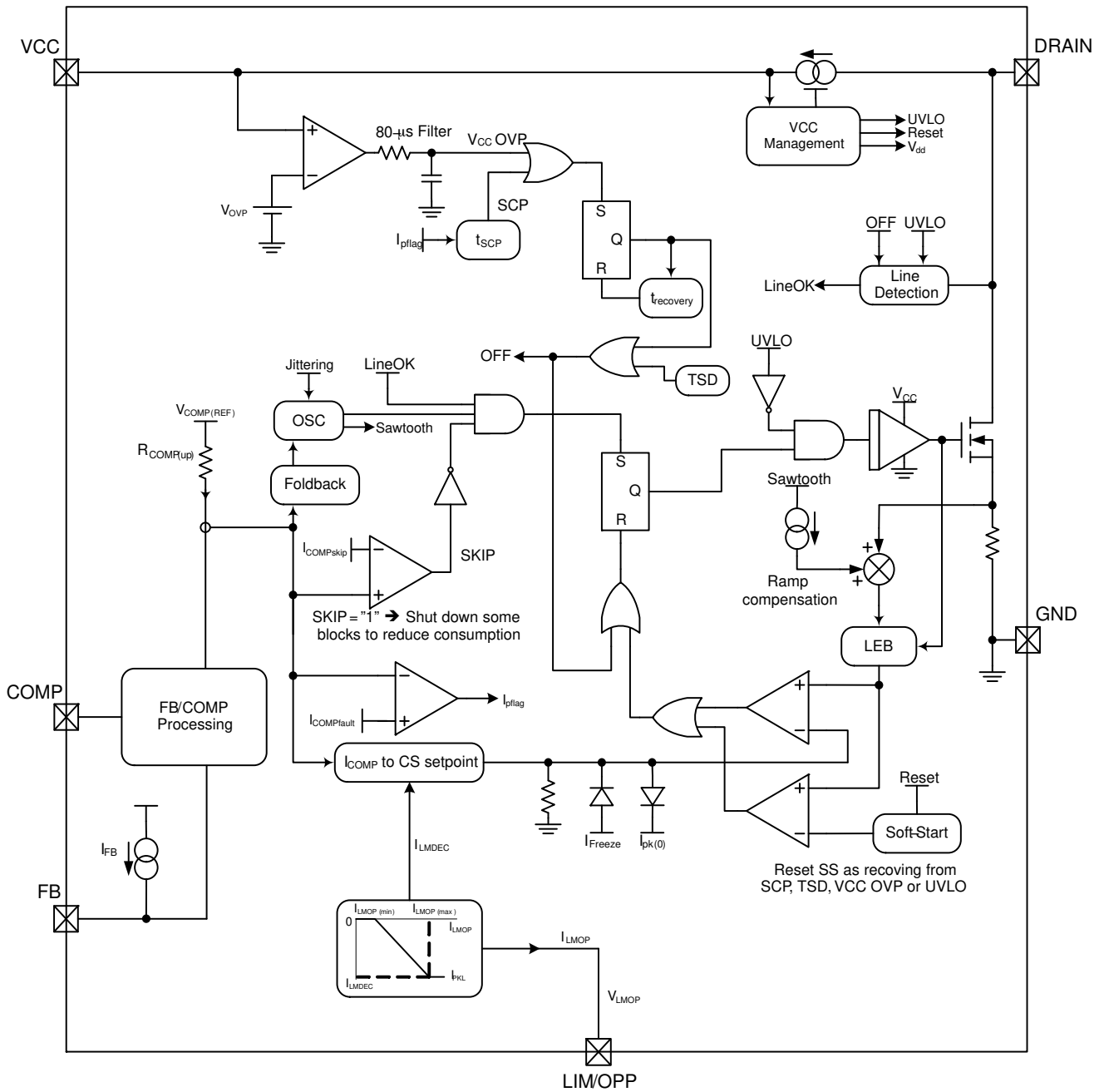


Figure 2. Simplified Internal Circuit Architecture

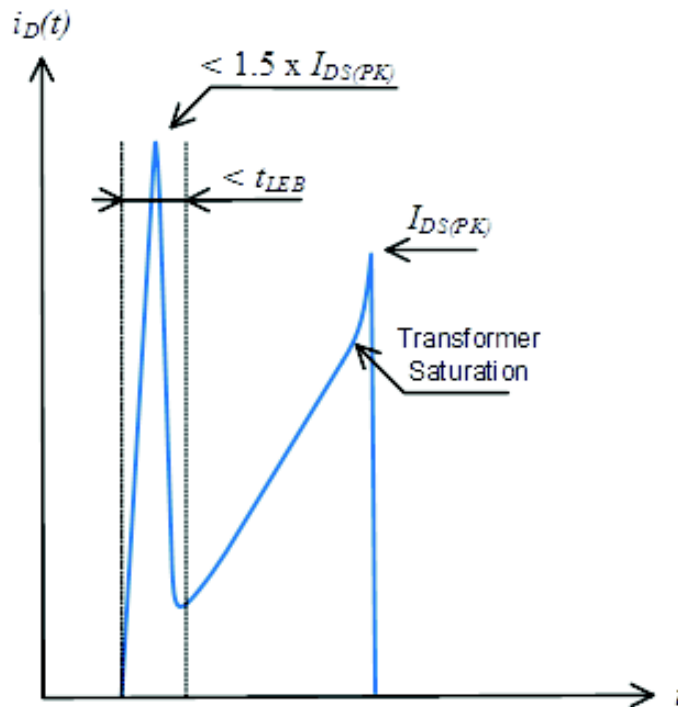
# NCP1060, NCP1063

**Table 3. MAXIMUM RATING TABLE** (All voltages related to GND terminal)

Rating	Symbol	Value	Unit
Power supply voltage, $V_{CC}$ pin, continuous voltage	$V_{CC}$	-0.3 to 20	V
Voltage on all pins, except Drain and $V_{CC}$ pin	$V_{inmax}$	-0.3 to 10	V
Drain voltage	$BV_{dss}$	-0.3 to 700	V
Maximum Current into $V_{CC}$ pin	$I_{CC}$	10	mA
Drain Current Peak during Transformer Saturation ( $T_J = 150^\circ\text{C}$ , Note 2): NCP1060 NCP1063	$I_{DS(PK)}$	300 850	mA
Drain Current Peak during Transformer Saturation ( $T_J = 125^\circ\text{C}$ , Note 2): NCP1060 NCP1063		335 950	
Drain Current Peak during Transformer Saturation ( $T_J = 25^\circ\text{C}$ , Note 2): NCP1060 NCP1063		520 1500	
Thermal Resistance Junction-to-Air – PDIP7 with 200 mm <sup>2</sup> of 35- $\mu$ copper area	$R_{\theta JA}$	115	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Air – SOIC10 with 200 mm <sup>2</sup> of 35- $\mu$ copper area	$R_{\theta JA}$	132	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Air – SOIC16 with 200 mm <sup>2</sup> of 35- $\mu$ copper area	$R_{\theta JA}$	104	$^\circ\text{C}/\text{W}$
Junction Temperature Range	$T_J$	-40 to +150	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-60 to +150	$^\circ\text{C}$
Human Body Model ESD Capability (All pins except HV pin) per JEDEC JESD22-A114F	HBM	2	kV
Charged-Device Model ESD Capability per JEDEC JESD22-C101E	CDM	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.
2. Maximum drain current  $I_{DS(PK)}$  is obtained when the transformer saturates. It should not be mixed with short pulses that can be seen at turn on. Figure 3 below provides spike limits the device can tolerate.



**Figure 3. Spike Limits**

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**Table 4. ELECTRICAL CHARACTERISTICS**

(For typical values  $T_J = 25^\circ\text{C}$ , for min/max values  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 14\text{ V}$  unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
<b>SUPPLY SECTION AND <math>V_{CC}</math> MANAGEMENT</b>						
$V_{CC(\text{on})}$	$V_{CC}$ increasing level at which the switcher starts operation	2 (5)	8.4	9.0	9.5	V
$V_{CC(\text{min})}$	$V_{CC}$ decreasing level at which the HV current source restarts	2 (5)	7.0	7.5	7.8	V
$V_{CC(\text{off})}$	$V_{CC}$ decreasing level at which the switcher stops operation (UVLO)	2 (5)	6.7	7.0	7.2	V
$I_{CC1}$	Internal IC consumption, NCP1060 switching at 60 kHz, LIM/OPP = 0 A Internal IC consumption, NCP1060 switching at 100 kHz, LIM/OPP = 0 A Internal IC consumption, NCP1063 switching at 60 kHz, LIM/OPP = 0 A Internal IC consumption, NCP1063 switching at 100 kHz, LIM/OPP = 0 A	2 (5)	–	0.92 0.97 0.99 1.07	–	mA
$I_{CC\text{skip}}$	Internal IC consumption, COMP is 0 V (No switching on MOSFET)	2 (5)	–	340	–	$\mu\text{A}$

**POWER SWITCH CIRCUIT**

$R_{DS(\text{on})}$	Power Switch Circuit on–state resistance NCP1060 ( $I_d = 50\text{ mA}$ ) $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ NCP1063 ( $I_d = 50\text{ mA}$ ) $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$	7, 8 (6–10) (13–16)	– – – –	34 65 11.4 22	41 72 14.0 24	$\Omega$
$BV_{DSS}$	Power Switch Circuit & Startup breakdown voltage ( $I_{D(\text{off})} = 120\text{ }\mu\text{A}$ , $T_J = 25^\circ\text{C}$ )	7, 8 (6–10) (13–16)	700	–	–	V
$I_{DSS(\text{off})}$	Power Switch & Startup breakdown voltage off–state leakage current $T_J = 125^\circ\text{C}$ ( $V_{ds} = 700\text{ V}$ )	7, 8 (6–10) (13–16)	–	84	–	$\mu\text{A}$
$t_r$ $t_f$	Switching characteristics ( $R_L = 50\text{ }\Omega$ , $V_{DS}$ set for $I_{\text{drain}} = 0.7 \times I_{\text{lim}}$ ) Turn–on time (90% – 10%) Turn–off time (10% – 90%)	7, 8 (6–10) (13–16)	– –	20 10	– –	ns
$t_{\text{on}(\text{min})}$	Minimum on time NCP1060 NCP1063	7, 8 (6–10) (13–16)	– –	200 230	– –	ns

**INTERNAL START–UP CURRENT SOURCE**

$I_{\text{start}1}$	High–voltage current source, $V_{CC} = V_{CC(\text{on})} - 200\text{ mV}$	7, 8 (6–10) (13–16)	5	8	12	mA
$I_{\text{start}2}$	High–voltage current source, $V_{CC} = 0\text{ V}$	7, 8 (6–10) (13–16)	–	0.5	–	mA
$V_{CC\text{TH}}$	$V_{CC}$ Transient level for $I_{\text{start}1}$ to $I_{\text{start}2}$ toggling point	2 (5)	–	1.4	–	V
$V_{\text{start}(\text{min})}$	Minimum startup voltage, $V_{CC} = 0\text{ V}$	7, 8 (6–10) (13–16)	–	–	21	V

**CURRENT COMPARATOR**

$I_{\text{PK}}$	Maximum internal current setpoint at 50% duty cycle FB = 2 V, LIM/OPP = 0 $\mu\text{A}$ , $T_J = 25^\circ\text{C}$ NCP1060 NCP1063	– –	– –	250 650	– –	mA
$I_{\text{PK}(0)}$	Maximum internal current setpoint at beginning of switching cycle FB = 2 V, LIM/OPP pin open $T_J = 25^\circ\text{C}$ NCP1060 NCP1063	– –	268 702	300 780	332 858	mA

- The final switch current is:  $I_{\text{PK}(0)} / (V_{\text{in}}/L_P + S_a) \times V_{\text{in}}/L_P + V_{\text{in}}/L_P \times t_{\text{prop}}$ , with  $S_a$  the built–in slope compensation,  $V_{\text{in}}$  the input voltage,  $L_P$  the primary inductor in a flyback, and  $t_{\text{prop}}$  the propagation delay.
- Oscillator frequency is measured with disabled jittering.



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**Table 4. ELECTRICAL CHARACTERISTICS**

(For typical values  $T_J = 25^\circ\text{C}$ , for min/max values  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 14\text{ V}$  unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
<b>CURRENT COMPARATOR</b>						
$I_{PKSW}$	Final switch current with a primary slope of 200 mA/ $\mu\text{s}$ , $F_{SW} = 60\text{ kHz}$ (Note 3), LIM/OPP pin open NCP1060 NCP1063	– –	– –	330 740	– –	mA
$I_{PKSW}$	Final switch current with a primary slope of 200 mA/ $\mu\text{s}$ , $F_{SW} = 100\text{ kHz}$ (Note 3), LIM/OPP pin open NCP1060 NCP1063	– –	– –	320 710	– –	mA
$I_{LMDEC}$	Maximum internal current setpoint at beginning of switching cycle $FB = 2\text{ V}$ , LIM/OPP = $-285\ \mu\text{A}$ , $T_J = 25^\circ\text{C}$ NCP1060 NCP1063	– –	– –	128 312	– –	mA
$t_{SS}$	Soft-start duration (guaranteed by design)	–	–	4	–	ms
$t_{prop}$	Propagation delay from current detection to drain OFF state	–	–	70	–	ns
$t_{LEB}$	Leading Edge Blanking Duration NCP1060 NCP1063	– –	– –	130 160	– –	ns

### INTERNAL OSCILLATOR

$f_{OSC}$	Oscillation frequency, 60 kHz version, $T_J = 25^\circ\text{C}$ (Note 4)	–	54	60	66	kHz
$f_{OSC}$	Oscillation frequency, 100 kHz version, $T_J = 25^\circ\text{C}$ (Note 4)	–	90	100	110	kHz
$f_{jitter}$	Frequency jittering in percentage of $f_{OSC}$	–	–	$\pm 6$	–	%
$f_{swing}$	Jittering swing frequency	–	–	300	–	Hz
$D_{max}$	Maximum duty-cycle	–	62	66	72	%

### ERROR AMPLIFIER SECTION

$V_{REF}$	Voltage Feedback Input ( $V_{COMP} = 2.5\text{ V}$ )	4 (7)	3.2	3.3	3.4	V
$I_{FB}$	Input Bias Current ( $V_{FB} = 3.3\text{ V}$ )	4 (7)	–	1	–	$\mu\text{A}$
$G_M$	Transconductance	5 (8)	–	2	–	mS
$I_{OTAlim}$	OTA maximum current capability ( $V_{FB} > V_{OTAen}$ )	5 (8)	–	$\pm 150$	–	$\mu\text{A}$
$V_{OTAen}$	FB voltage to disable OTA	4 (7)	0.7	1.3	1.7	V

### COMPENSATION SECTION

$I_{COMPfault}$	COMP current for which Fault is detected	5 (8)	–	–40	–	$\mu\text{A}$
$I_{COMP100\%}$	COMP current for which internal current set-point is 100% ( $I_{PK(0)}$ )	5 (8)	–	–44	–	$\mu\text{A}$
$I_{COMPfreeze}$	COMP current for which internal current setpoint is: $I_{Freeze1}$ or 2 (NCP1060/3)	5 (8)	–	–80	–	$\mu\text{A}$
$V_{COMP(REF)}$	Equivalent pull-up voltage in linear regulation range (Guaranteed by design)	5 (8)	–	2.7	–	V
$R_{COMP(up)}$	Equivalent feedback resistor in linear regulation range (Guaranteed by design)	5 (8)	–	17.7	–	k $\Omega$
$V_{LMOP}$	Voltage on LIM/OPP pin @ $I_{LMOP} = -35\ \mu\text{A}$ Voltage on LIM/OPP pin @ $I_{LMOP} = -250\ \mu\text{A}$ , $T_J = 25^\circ\text{C}$	3 (6)	1.40 1.28	1.50 1.35	1.60 1.42	V
$I_{LMOP}$	Maximum current from LIM/OPP pin	3 (6)	–	–330	–420	$\mu\text{A}$
$I_{LMOP(min)}$	Current at which LIM/OPP starts to decrease $I_{PEAK}$	3 (6)	–20	–26	–32	$\mu\text{A}$
$I_{LMOP(max)}$	Current at which LIM/OPP stops to decrease $I_{PEAK}$	3 (6)	–	–285	–	$\mu\text{A}$
$I_{LMOP(neg)}$	Negative Active Clamp Voltage ( $I_{LMOP} = -2.5\text{ mA}$ )	3 (6)	–	–0.7	–	V

- The final switch current is:  $I_{PK(0)} / (V_{in}/L_P + S_a) \times V_{in}/L_P + V_{in}/L_P \times t_{prop}$ , with  $S_a$  the built-in slope compensation,  $V_{in}$  the input voltage,  $L_P$  the primary inductor in a flyback, and  $t_{prop}$  the propagation delay.
- Oscillator frequency is measured with disabled jittering.

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**Table 4. ELECTRICAL CHARACTERISTICS**

(For typical values  $T_J = 25^\circ\text{C}$ , for min/max values  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 14\text{ V}$  unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
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**COMPENSATION SECTION**

$I_{LMOP(pos)}$	Positive Active Clamp (Guaranteed by design)	3 (6)		2.5		mA
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**FREQUENCY FOLDBACK & SKIP**

$I_{COMPfold}$	Start of frequency foldback COMP pin current level	5 (8)	–	–68	–	$\mu\text{A}$
$I_{COMPfold(end)}$	End of frequency foldback COMP pin current level, $f_{sw} = f_{min}$	5 (8)	–	–100	–	$\mu\text{A}$
$f_{min}$	The frequency below which skip-cycle occurs	–	21	25	29	kHz
$I_{COMPskip}$	The COMP pin current level to enter skip mode	5 (8)	–	–120	–	$\mu\text{A}$
$I_{Freeze1}$	Internal minimum current setpoint ( $I_{COMP} = I_{COMPFreeze}$ ) in NCP1060		–	110	–	mA
$I_{Freeze2}$	Internal minimum current setpoint ( $I_{COMP} = I_{COMPFreeze}$ ) in NCP1063		–	270	–	mA

**RAMP COMPENSATION**

$S_{a(60)}$	The internal ramp compensation @ 60 kHz: NCP1060 NCP1063	– –	– –	8.4 15.6	– –	mA/ $\mu\text{s}$
$S_{a(100)}$	The internal ramp compensation @ 100 kHz: NCP1060 NCP1063	– –	– –	14 26	– –	mA/ $\mu\text{s}$

**PROTECTIONS**

$t_{SCP}$	Fault validation further to error flag assertion	–	35	48	–	ms
$t_{recovery}$	OFF phase in fault mode	–	–	400	–	ms
$V_{OVP}$	$V_{CC}$ voltage at which the switcher stops pulsing	2 (5)	17.0	18.0	18.8	V
$t_{OVP}$	The filter of $V_{CC}$ OVP comparator	–	–	80	–	$\mu\text{s}$
$V_{HV(EN)}$	The drain pin voltage above which allows MOSFET operate, which is detected after TSD, UVLO, SCP, or $V_{CC}$ OVP mode. (A version only)	7.8 (6–10) (13–16)	67	87	110	V

**TEMPERATURE MANAGEMENT**

TSD	Temperature shutdown (Guaranteed by design)	–	150	163	–	$^\circ\text{C}$
TSD <sub>hyst</sub>	Hysteresis in shutdown (Guaranteed by design)	–	–	20	–	$^\circ\text{C}$

- The final switch current is:  $I_{PK(0)} / (V_{in}/L_P + S_a) \times V_{in}/L_P + V_{in}/L_P \times t_{prop}$ , with  $S_a$  the built-in slope compensation,  $V_{in}$  the input voltage,  $L_P$  the primary inductor in a flyback, and  $t_{prop}$  the propagation delay.
- Oscillator frequency is measured with disabled jittering.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# NCP1060, NCP1063

## TYPICAL CHARACTERISTICS

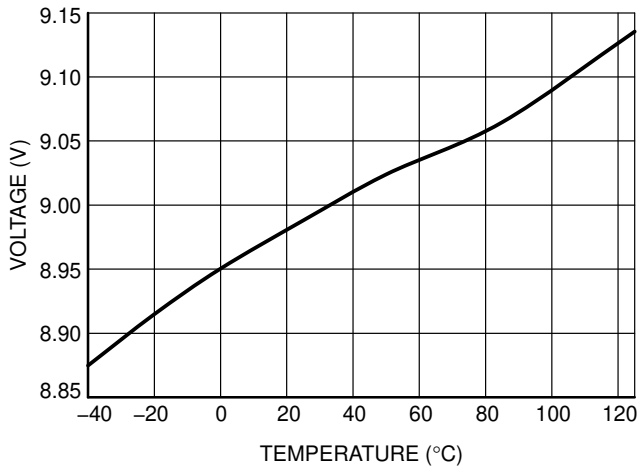


Figure 4.  $V_{CC(on)}$  vs. Temperature

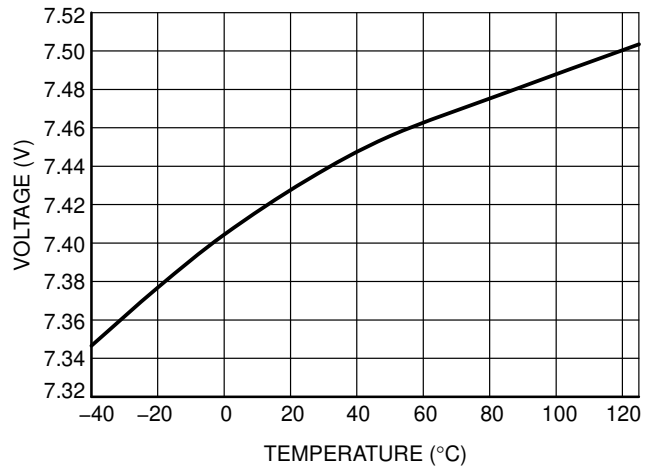


Figure 5.  $V_{CC(min)}$  vs. Temperature

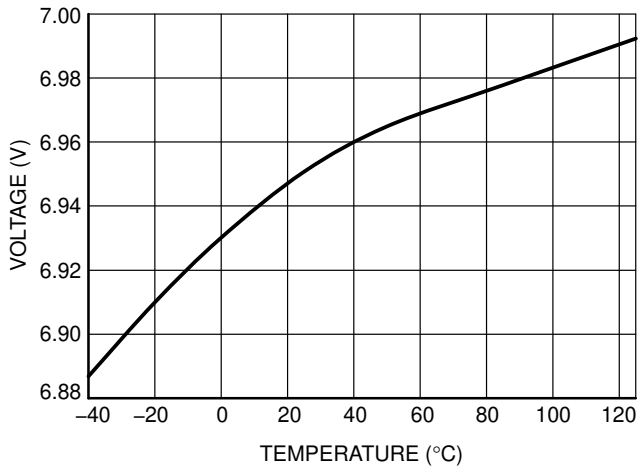


Figure 6.  $V_{CC(off)}$  vs. Temperature

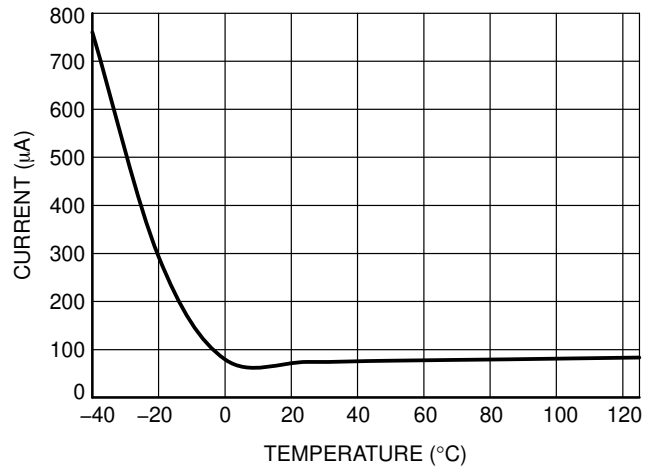


Figure 7.  $I_{DSS(off)}$  vs. Temperature

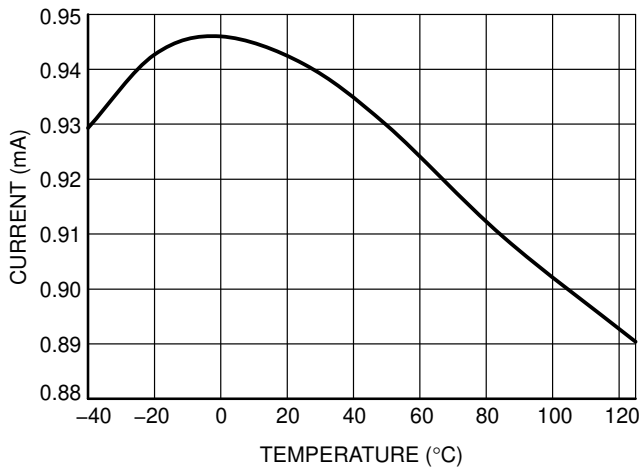


Figure 8.  $I_{CC1}$  60 kHz vs. Temperature

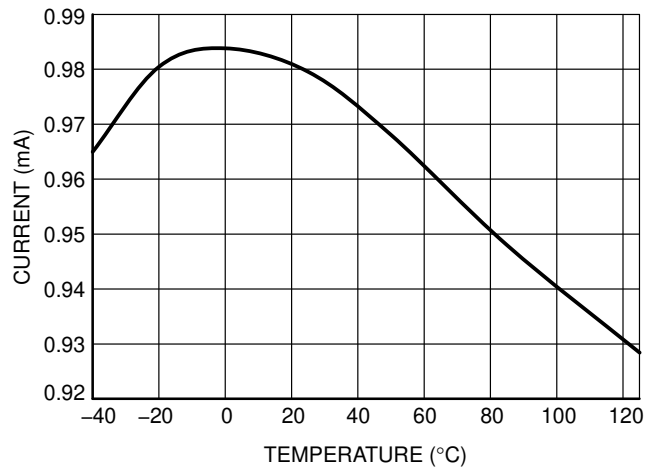


Figure 9.  $I_{CC1}$  100 kHz vs. Temperature

# NCP1060, NCP1063

## TYPICAL CHARACTERISTICS

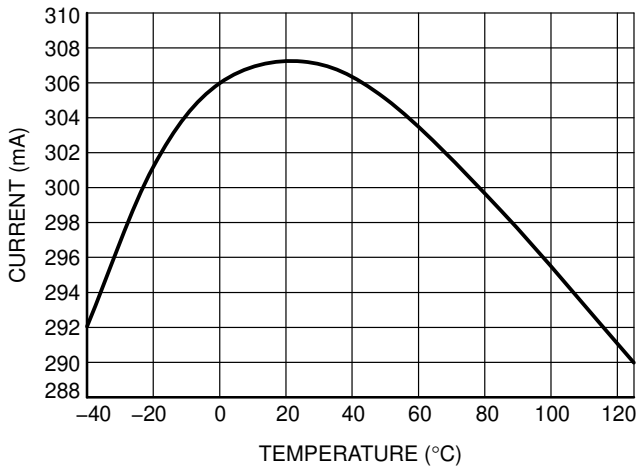


Figure 10.  $I_{PK(0)1060}$  vs. Temperature

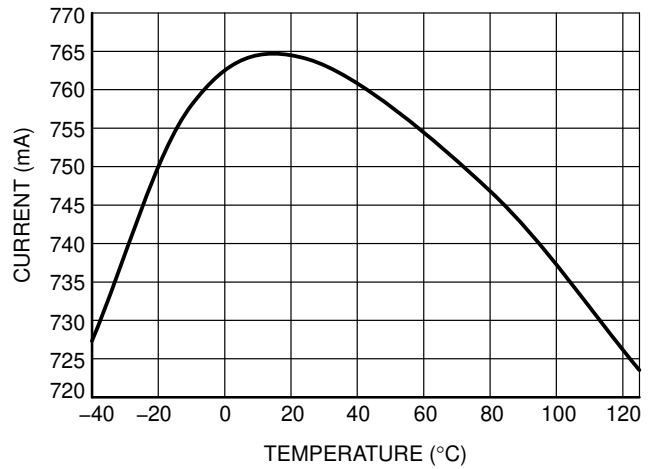


Figure 11.  $I_{PK(0)1063}$  vs. Temperature

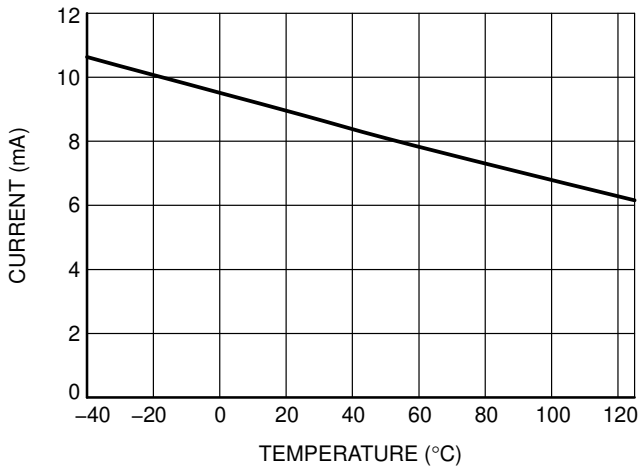


Figure 12.  $I_{start1}$  vs. Temperature

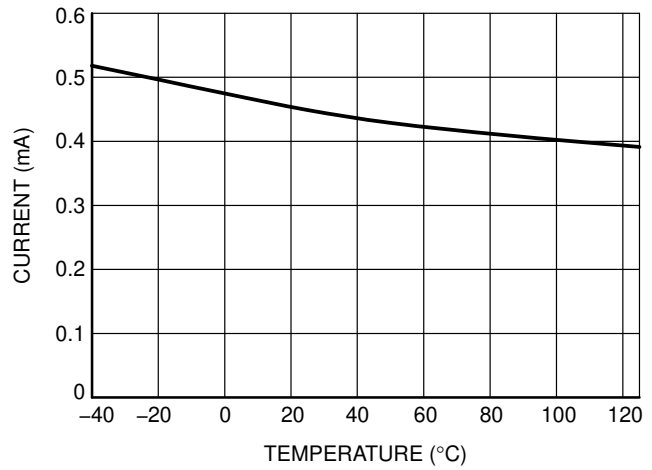


Figure 13.  $I_{start2}$  vs. Temperature

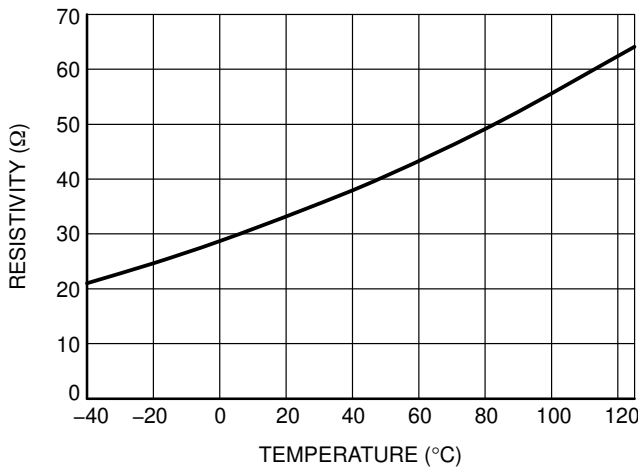


Figure 14.  $R_{DS(on)1060}$  vs. Temperature

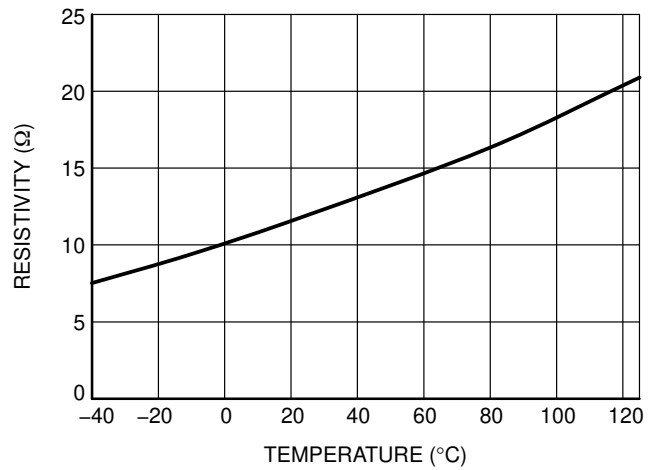


Figure 15.  $R_{DS(on)1063}$  vs. Temperature

# NCP1060, NCP1063

## TYPICAL CHARACTERISTICS

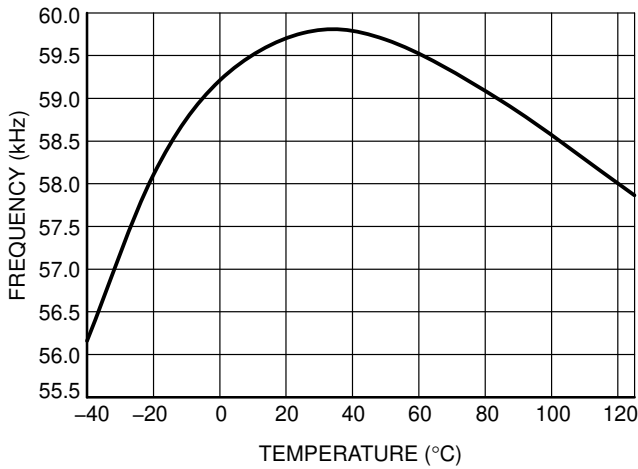


Figure 16.  $f_{OSC60}$  vs. Temperature

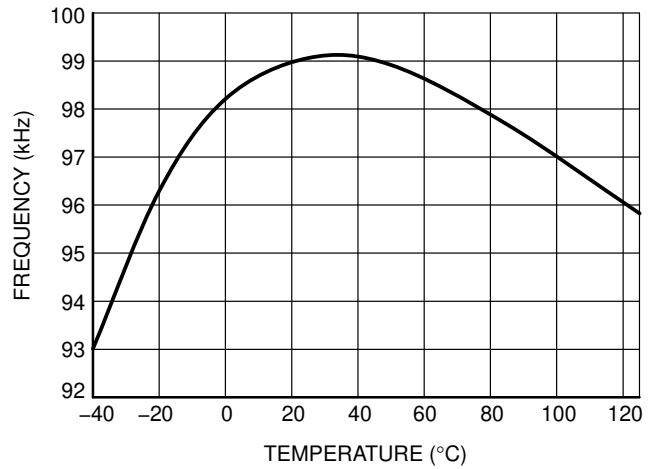


Figure 17.  $f_{OSC100}$  vs. Temperature

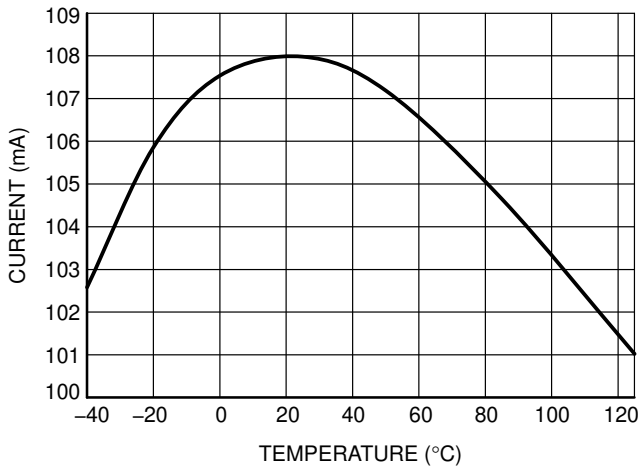


Figure 18.  $I_{freeze1060}$  vs. Temperature

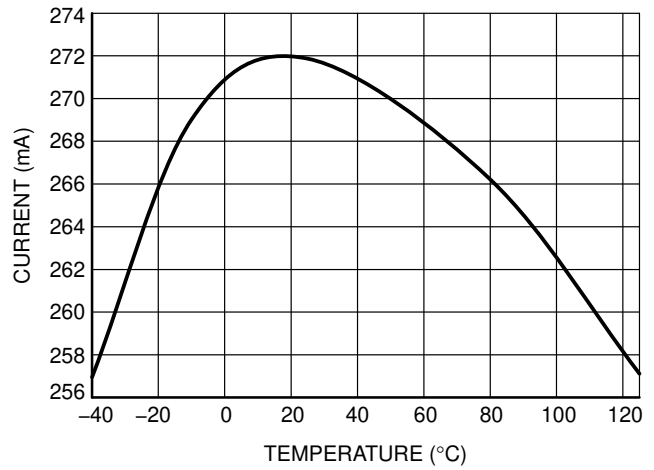


Figure 19.  $I_{freeze1063}$  vs. Temperature

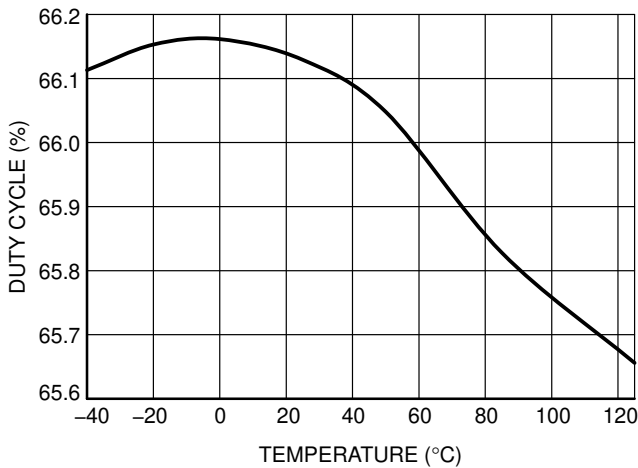


Figure 20.  $D_{(max)}$  vs. Temperature

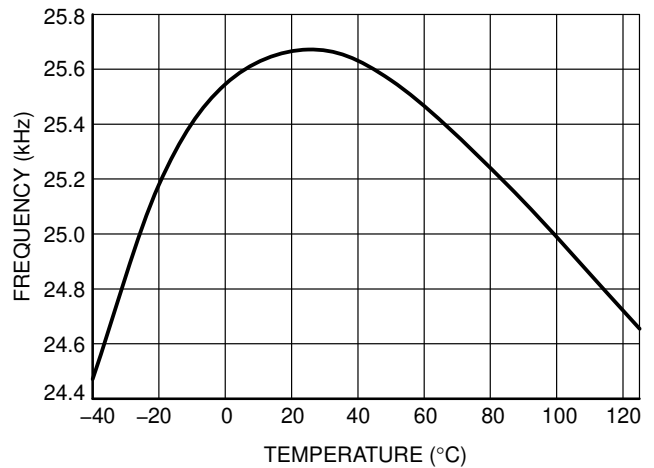


Figure 21.  $f_{min}$  vs. Temperature

# NCP1060, NCP1063

## TYPICAL CHARACTERISTICS

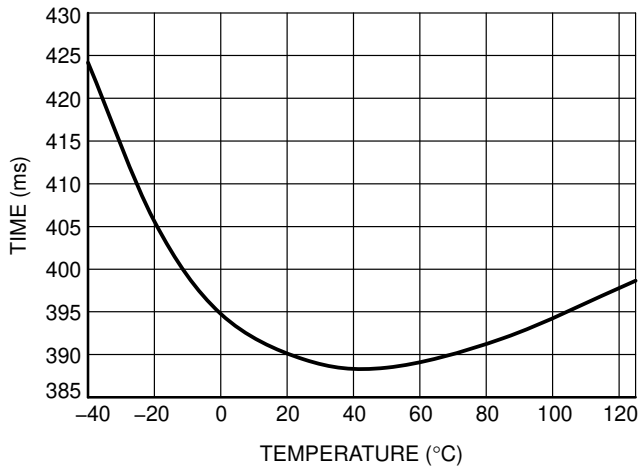


Figure 22.  $t_{\text{recovery}}$  vs. Temperature

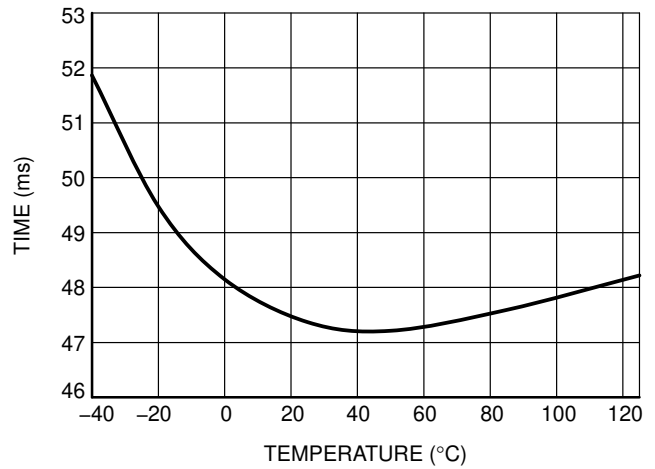


Figure 23.  $t_{\text{SCP}}$  vs. Temperature

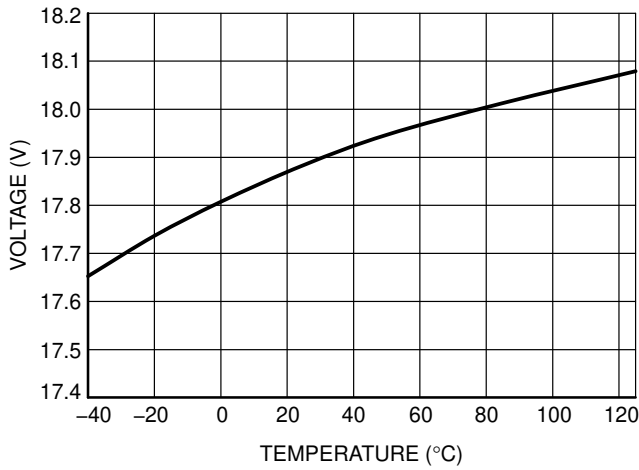


Figure 24.  $V_{\text{OVP}}$  vs. Temperature

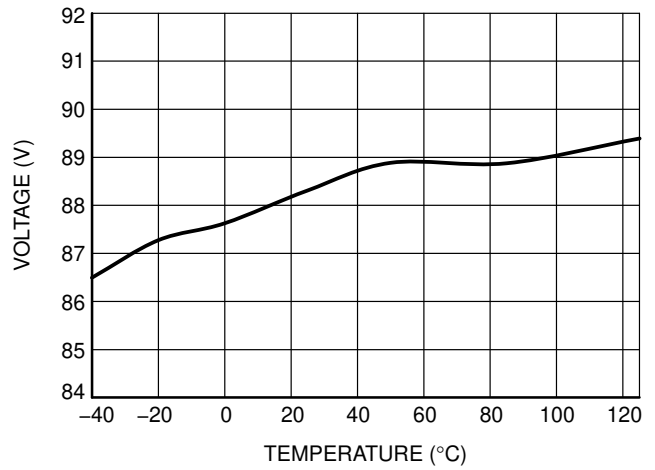


Figure 25.  $V_{\text{HV(EN)}}$  vs. Temperature

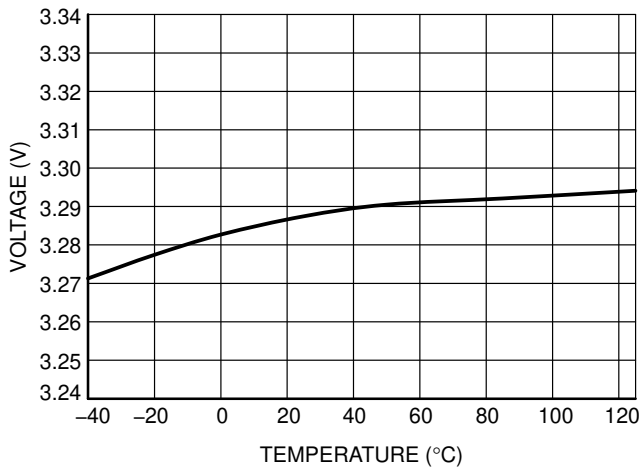


Figure 26.  $V_{\text{REF}}$  vs. Temperature

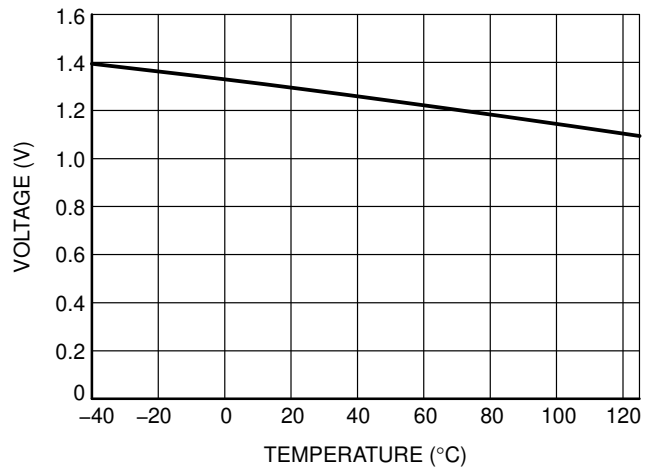


Figure 27.  $V_{\text{OTAen}}$  vs. Temperature

# NCP1060, NCP1063

## TYPICAL CHARACTERISTICS

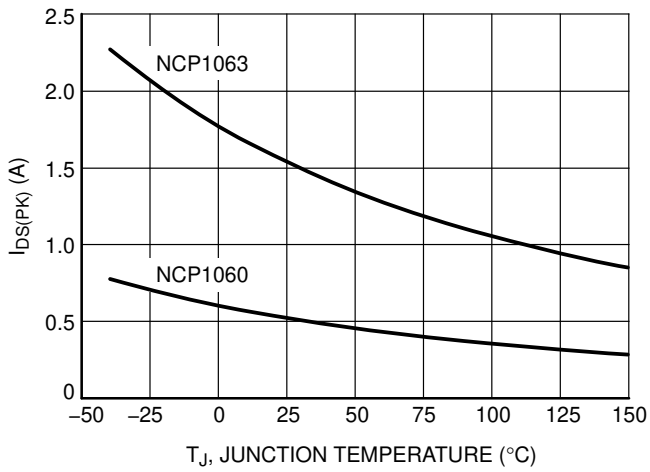


Figure 28. Drain Current Peak during Transformer Saturation vs. Junction Temperature

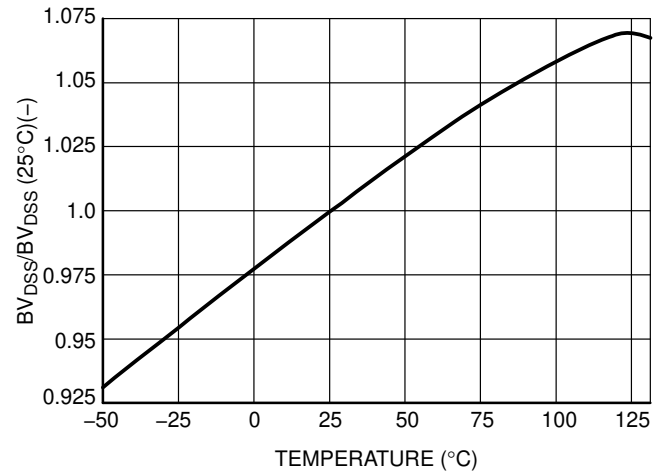


Figure 29. Breakdown Voltage vs. Temperature

## Application Information

### Introduction

The NCP106X offers a complete current-mode control solution. The component integrates everything needed to build a rugged and cost effective Switch-Mode Power Supply (SMPS) featuring low standby power. The Quick Selection Table, Table 5, details the differences between references, mainly peak current setpoints,  $R_{DS(on)}$  value and operating frequency.

- **Current-mode operation:** the controller uses current-mode control architecture.
- **700 V – Power MOSFET:** Due to ON Semiconductor Very High Voltage Integrated Circuit technology, the circuit hosts a high-voltage power MOSFET featuring a  $34\ \Omega$  or  $11.4\ \Omega$   $R_{DS(on)}$  –  $T_j = 25^\circ\text{C}$ . This value lets the designer build a power supply up to 7.8 W or 15.5 W operated on universal mains. An internal current source delivers the startup current, necessary to crank the power supply.
- **Dynamic Self-Supply:** Due to the internal high voltage current source, this device could be used in the application without the auxiliary winding to provide supply voltage.
- **Short circuit protection:** by permanently monitoring the COMP line activity, the IC is able to detect the presence of a short-circuit, immediately reducing the output power for a total system protection. A  $t_{SCP}$  timer is started as soon as the COMP current is below threshold,  $I_{COMPfault}$ , which indicates the maximum peak current. If at the end of this timer the fault is still present, then the device enters a safe, auto-recovery burst mode, affected by a fixed timer recurrence,  $t_{recovery}$ . Once the short has disappeared, the controller resumes and goes back to normal operation.
- **Built-in VCC Over Voltage Protection:** when the auxiliary winding is used to bias the  $V_{CC}$  pin (no DSS), an internal comparator is connected to  $V_{CC}$  pin. In case the voltage on the pin exceeds a level of  $V_{OVP}$  (18 V typically), the controller immediately stops switching and waits a full timer period ( $t_{recovery}$ ) before attempting to restart. If the fault is gone, the controller resumes operation. If the fault is still there, e.g. a broken opto-coupler, the controller protects the load through a safe burst mode.
- **Line detection:** An internal comparator monitors the drain voltage as recovering from one of the following situations:
  - ◆ Short Circuit Protection,
  - ◆  $V_{CC}$  OVP is confirmed,
  - ◆ UVLO,
  - ◆ TSD
- If the drain voltage is lower than the internal threshold ( $V_{HV(EN)}$ ), the internal power switch is inhibited. This avoids operating at too low ac input. This is also called brown-in function in some fields. For applications not using standard AC mains (24 Vdc industrial bus for instance), the B version doesn't incorporate this line detection and let the device start as soon as voltage supply reaches  $V_{start(min)}$ .
- **Frequency jittering:** an internal low-frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis. To improve the EMI signature at low power levels, the jittering remains active in frequency foldback mode.
- **Soft-Start:** a 4 ms soft-start ensures a smooth startup sequence, reducing output overshoots.
- **Frequency foldback capability:** a continuous flow of pulses is not compatible with no-load/light-load standby power requirements. To excel in this domain, the controller observes the COMP pin current information and when it reaches a level of  $I_{COMPfold}$ , the oscillator then starts to reduce its switching frequency as the feedback current continues to increase (the power demand continues to reduce). It can go down to 25 kHz (typical) reached for a feedback level of  $I_{COMPfold(end)}$  (100  $\mu\text{A}$  roughly). At this point, if the power continues to drop, the controller enters classical skip-cycle mode.
- **Skip:** if SMPS naturally exhibits a good efficiency at nominal load, it begins to be less efficient when the output power demand diminishes. By skipping un-needed switching cycles, the NCP106X drastically reduces the power wasted during light load conditions.
- **Ipeak set:** If current in range 26  $\mu\text{A}$  and 285  $\mu\text{A}$  is drawn from the pin, the peak current is proportionally reduced down to 40% of its original value. This feature enables to designer to set up the peak current to the value which is ideal for the application.

By routing a portion of the negative voltage present during the on-time on the auxiliary winding to the LIM/OPP pin, the user has a simple and non-dissipative means to alter the maximum peak current setpoint as the bulk voltage increases.





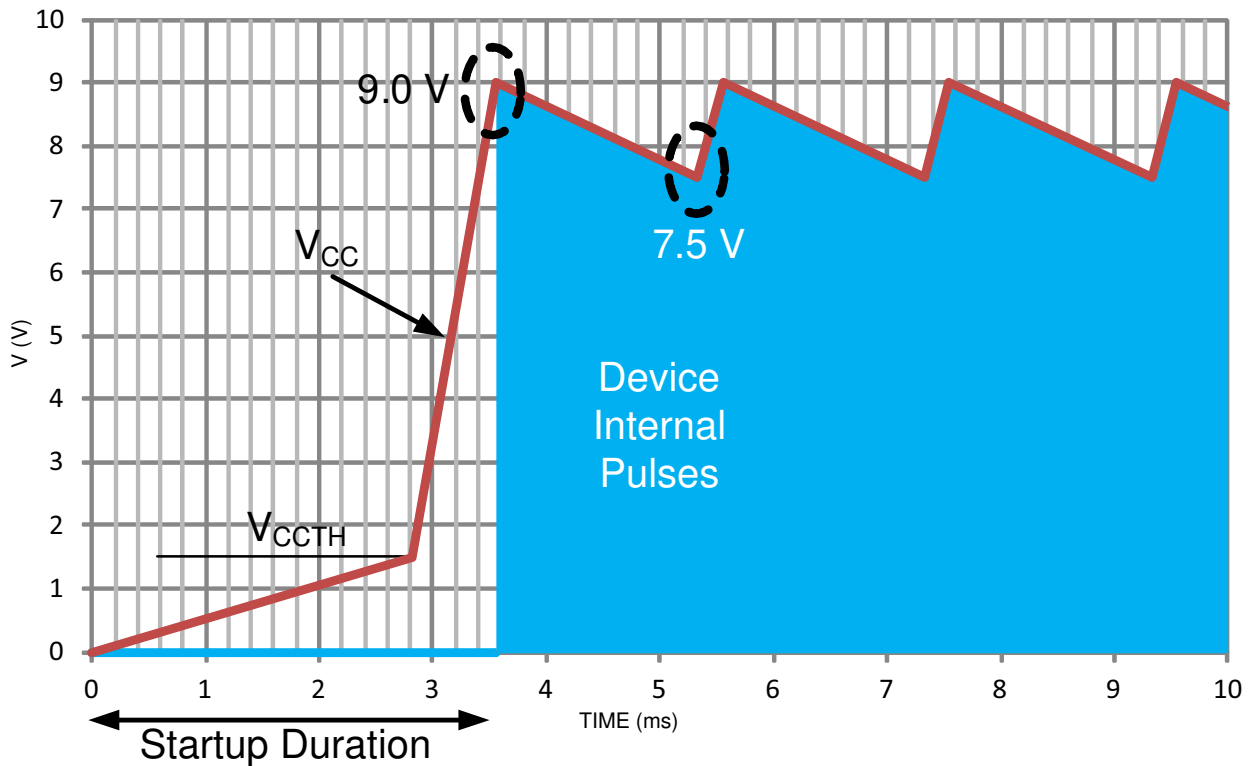


Figure 31. The Charge/Discharge Cycle Over a 1 µF V<sub>CC</sub> Capacitor

As one can see, even if there is auxiliary winding to provide energy for V<sub>CC</sub>, it happens that the device is still biased by DSS during start-up time or some fault mode when the voltage on auxiliary winding is not ready yet. The V<sub>CC</sub> capacitor shall be dimensioned to avoid V<sub>CC</sub> crosses V<sub>CC(off)</sub> level, which stops operation. The ΔV between V<sub>CC(min)</sub> and V<sub>CC(off)</sub> is 0.5 V. There is no current source to charge V<sub>CC</sub> capacitor when driver is on, i.e. drain voltage is close to zero. Hence the V<sub>CC</sub> capacitor can be calculated using

$$C_{VCC} \geq \frac{I_{CC1} \cdot D_{max}}{f_{OSC} \cdot \Delta V} \quad (\text{eq. 1})$$

Take the 60 kHz device as an example. C<sub>VCC</sub> should be above

$$\frac{0.8 \text{ m} \cdot 72\%}{54 \text{ kHz} \cdot 0.5} = 21 \text{ nF.}$$

A margin that covers the temperature drift and the voltage drop due to switching inside FET should be considered, and thus a capacitor above 0.1 µF is appropriate.

The V<sub>CC</sub> capacitor has only a supply role and its value does not impact other parameters such as fault duration or the frequency sweep period for instance. As one can see on Figure 30, an internal OVP comparator, protects the switcher against lethal V<sub>CC</sub> runaways. This situation can occur if the feedback loop optocoupler fails, for instance, and you would like to protect the converter against an over voltage event. In that case, the over voltage protection (OVP) circuit and immediately stops the output pulses for

t<sub>recovery</sub> duration (400 ms typically). Then a new start-up attempt takes place to check whether the fault has disappeared or not. The OVP paragraph gives more design details on this particular section.

#### Fault Condition – Short-circuit on V<sub>CC</sub>

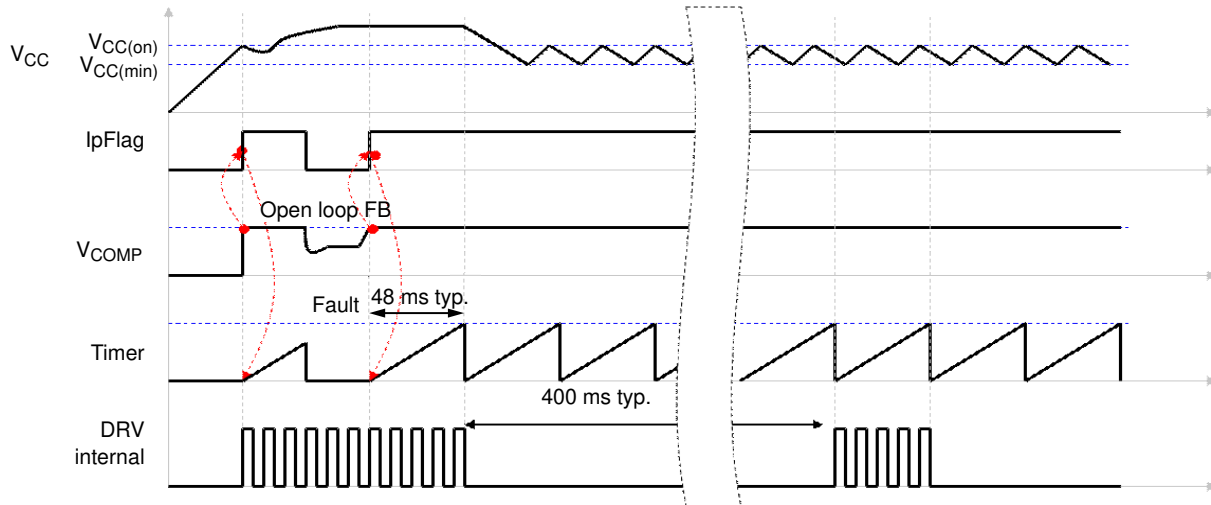
In some fault situations, a short-circuit can purposely occur between V<sub>CC</sub> and GND. In high line conditions (V<sub>HV</sub> = 370 V<sub>DC</sub>) the current delivered by the startup device will seriously increase the junction temperature. For instance, since I<sub>start1</sub> equals 5 mA (the min corresponds to the highest T<sub>j</sub>), the device would dissipate 370 x 5 m = 1.85 W. To avoid this situation, the controller includes a novel circuitry made of two startup levels, I<sub>start1</sub> and I<sub>start2</sub>. At power-up, as long as V<sub>CC</sub> is below a 1.4 V level, the source delivers I<sub>start2</sub> (around 500 µA typical), then, when V<sub>CC</sub> reaches 1.4 V, the source smoothly transitions to I<sub>start1</sub> and delivers its nominal value. As a result, in case of short-circuit between V<sub>CC</sub> and GND, the power dissipation will drop to 370 x 500 µ = 185 mW. Figure 31 portrays this particular behavior.

The first startup period is calculated by the formula C x V = I x t, which implies a 1 µ x 1.4 / 500 µ = 2.8 ms startup time for the first sequence. The second sequence is obtained by toggling the source to 8 mA with a delta V of V<sub>CC(on)</sub> – V<sub>CCTH</sub> = 9.0 – 1.4 = 7.6 V, which finally leads to a second startup time of 1 µ x 7.6 / 8 m = 0.95 ms. The total startup time becomes 2.8 m + 0.95 m = 3.75 ms. Please note that this calculation is approximated by the presence of the knee in the vicinity of the transition.

**Fault Condition – Output Short-circuit**

As soon as  $V_{CC}$  reaches  $V_{CC(on)}$ , drive pulses are internally enabled. If everything is correct, the auxiliary winding increases the voltage on the  $V_{CC}$  pin as the output voltage rises. During the start-sequence, the controller smoothly ramps up the peak drain current to maximum setting, i.e.  $I_{PK}$ , which is reached after a typical period of 4 ms. When the output voltage is not regulated, the current coming through COMP pin is below  $I_{COMPfault}$  level (40  $\mu$ A typically), which is not only during the startup period but also anytime an overload occurs, an internal error flag is

asserted,  $I_{pflag}$ , indicating that the system has reached its maximum current limit set point. The assertion of this flag triggers a fault counter  $t_{SCP}$  (48 ms typically). If at counter completion,  $I_{pflag}$  remains asserted, all driving pulses are stopped and the part stays off in  $t_{recovery}$  duration (about 400 ms). A new attempt to re-start occurs and will last 48 ms providing the fault is still present. If the fault still affects the output, a safe burst mode is entered, affected by a low duty-cycle operation (11%). When the fault disappears, the power supply quickly resumes operation. Figure 32 depicts this particular mode:



**Figure 32. In case of short-circuit or overload, the NCP106X protects itself and the power supply via a low frequency burst mode. The  $V_{CC}$  is maintained by the current source and self-supplies the controller.**

**Auto-recovery Over Voltage Protection**

The particular NCP106X arrangement offers a simple way to prevent output voltage runaway when the optocoupler fails. As Figure 33 shows, a comparator monitors the  $V_{CC}$  pin. If the auxiliary pushes too much voltage into the  $C_{VCC}$  capacitor, then the controller considers an OVP situation and stops the internal drivers. When an OVP occurs, all switching pulses are permanently disabled. After  $t_{recovery}$  delay, it resumes the internal drivers. If the failure symptom still exists, e.g. feedback opto-coupler fails, the device keeps the auto-recovery OVP mode. It is recommended insertion of a resistor ( $R_{limit}$ ) between the auxiliary dc level and the  $V_{CC}$  pin to protect the

IC against high voltage spikes, which can damage the IC, and to filter out the  $V_{CC}$  line to avoid undesired OVP activation.  $R_{limit}$  should be carefully selected to avoid triggering the OVP as we discussed, but also to avoid disturbing the  $V_{CC}$  in low / light load conditions.

Self-supplying controllers in extremely low standby applications often puzzles the designer. Actually, if a SMPS operated at nominal load can deliver an auxiliary voltage of an arbitrary 16 V ( $V_{nom}$ ), this voltage can drop below 10 V ( $V_{stby}$ ) when entering standby. This is because the recurrence of the switching pulses expands so much that the low frequency re-fueling rate of the  $V_{CC}$  capacitor is not enough to keep a proper auxiliary voltage.

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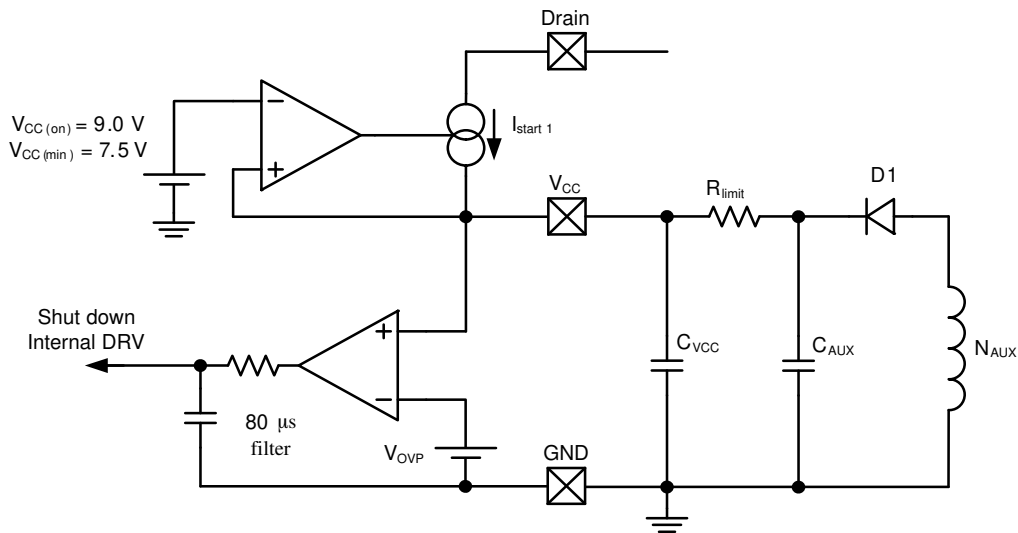


Figure 33. A more detailed view of the NCP106X offers better insight on how to properly wire an auxiliary winding

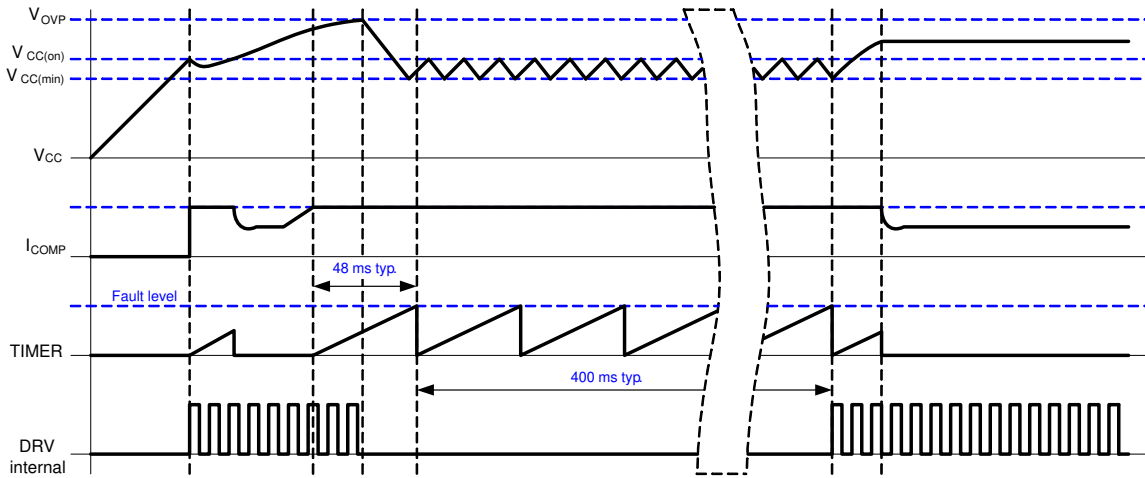


Figure 34. describes the main signal variations when the part operates in auto-recovery OVP:

### Soft-start

The NCP106X features a 4 ms soft-start which reduces the power-on stress but also contributes to lower the output overshoot. Figure 35 shows a typical operating waveform.

The NCP106X features a novel patented structure which offers a better soft-start ramp, almost ignoring the start-up pedestal inherent to traditional current-mode supplies.

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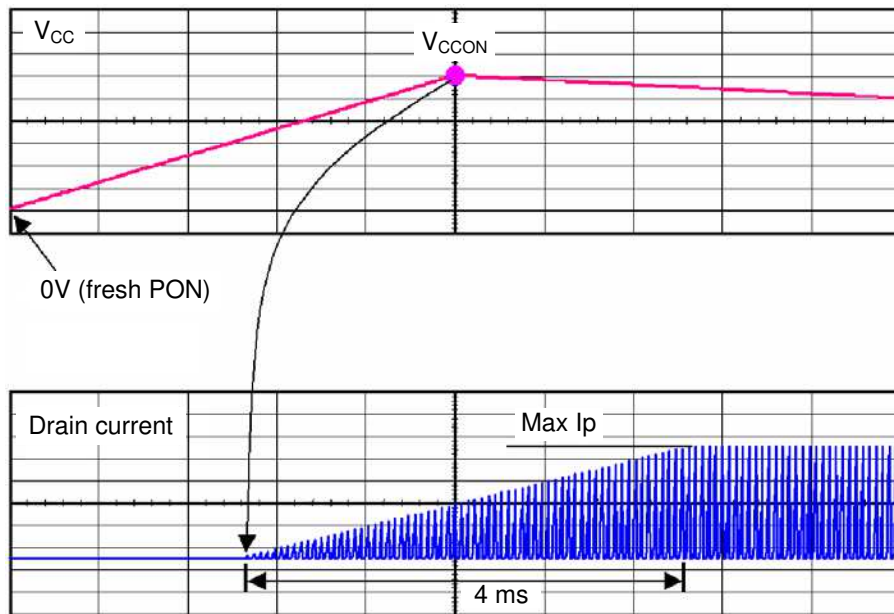


Figure 35. The 4 ms Soft-start Sequence

### Jittering

Frequency jittering is a method used to soften the EMI signature by spreading the energy in the vicinity of the main switching component. The NCP106X offers a  $\pm 6\%$  deviation of the nominal switching frequency. The sweep

sawtooth is internally generated and modulates the clock up and down with a fixed frequency of 300 Hz. Figure 36 shows the relationship between the jitter ramp and the frequency deviation. It is not possible to externally disable the jitter.

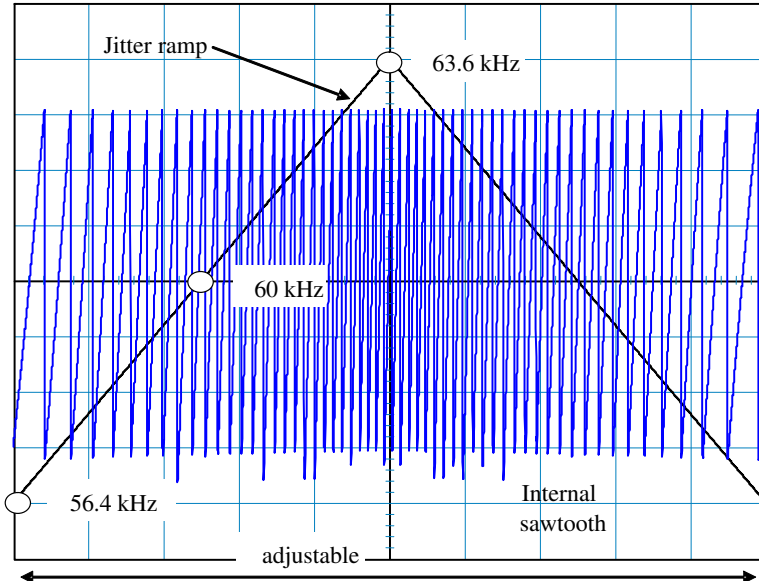


Figure 36. Modulation Effects on the Clock Signal by the Jittering Sawtooth

### Line Detection (for A version only)

An internal comparator monitors the drain voltage as recovering from one of the following situations:

- Short Circuit Protection,
- V<sub>CC</sub> OVP is confirmed,

- UVLO
- TSD

If the drain voltage is lower than the internal threshold V<sub>HV(EN)</sub> (87 Vdc typically), the internal power switch is inhibited. This avoids operating at too low ac input.

# NCP1060, NCP1063

## Frequency Foldback

The reduction of no-load standby power associated with the need for improving the efficiency, requires to change the traditional fixed-frequency type of operation. This device implements a switching frequency foldback when the COMP current passes above a certain level,  $I_{COMPfold}$ , set around 68  $\mu A$ . At this point, the oscillator enters frequency foldback and reduces its switching frequency.

The internal peak current set-point is following the COMP current information until its level reaches  $I_{Freeze}$ .

Below this value, the peak current setpoint is frozen to 30% of the  $I_{PK(0)}$ . The only way to further reduce the transmitted power is to diminish the operating frequency down to  $F_{min}$  (25 kHz typically). This value is reached at a COMP current level of  $I_{COMPfold(end)}$  (100  $\mu A$  typically). Below this point, if the output power continues to decrease, the part enters skip cycle for the best noise-free performance in no-load conditions. Figure 37 and Figure 38 depict the adopted scheme for the part.

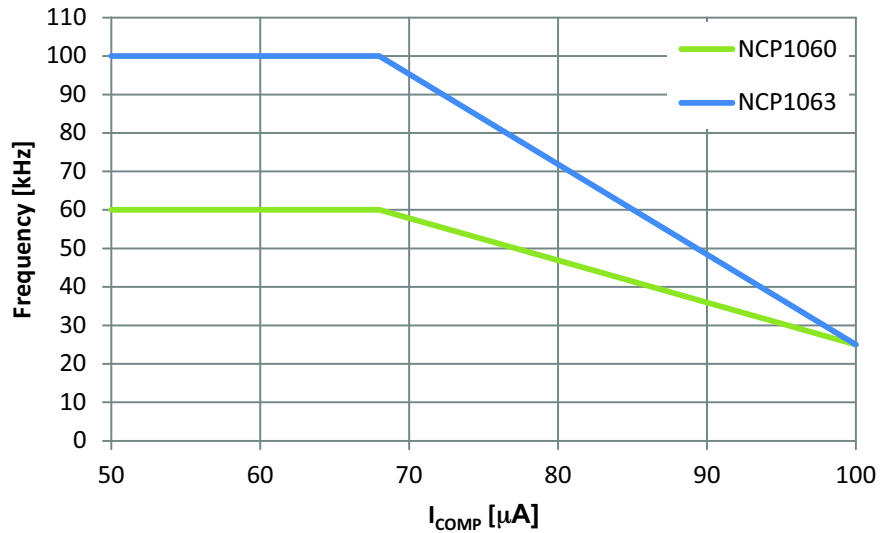


Figure 37. By observing the current on the COMP pin, the controller reduces its switching frequency for an improved performance at light load.

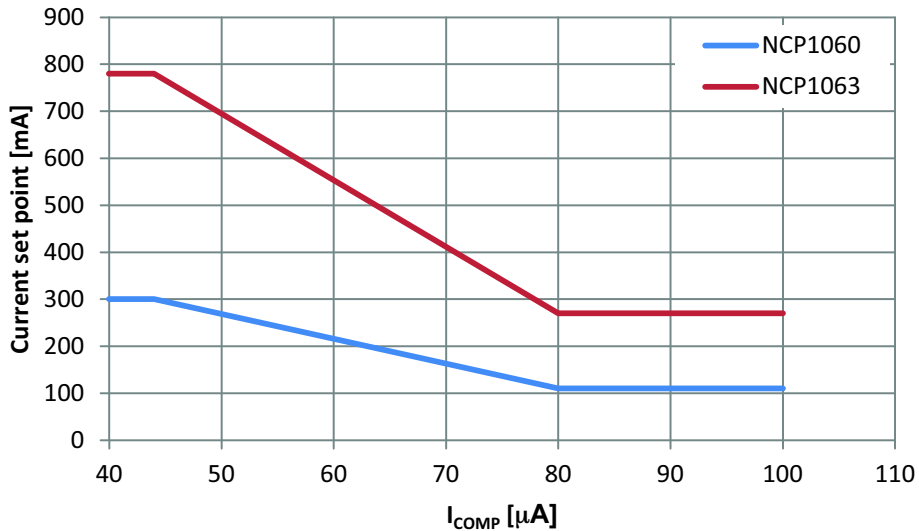


Figure 38.  $I_{pk}$  set-point is frozen at lower power demand.

## NCP1060, NCP1063

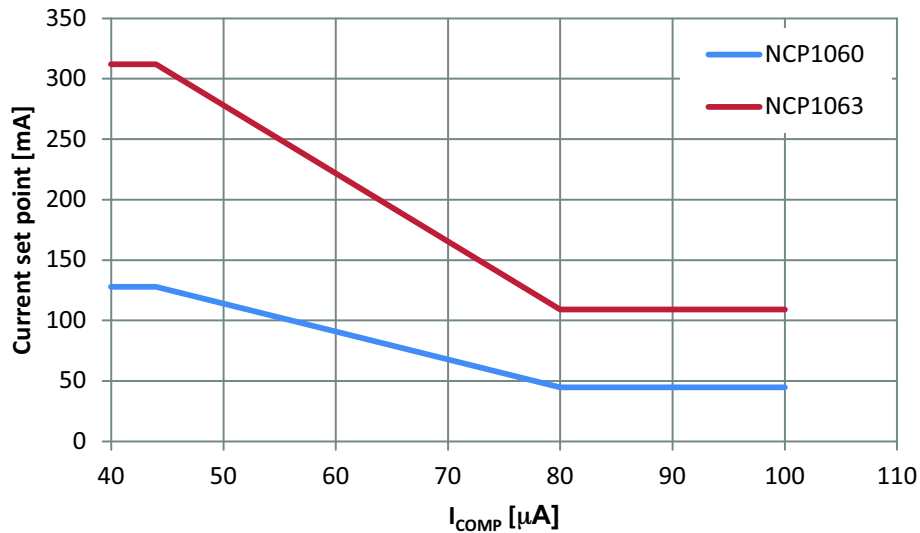


Figure 39. I<sub>pk</sub> set-point is frozen at lower power demand ( $I_{LMOP} \geq 285 \mu A$ )

### Feedback and Skip

Figure 40 depicts the relationship between COMP pin voltage and current. The COMP pin operates linearly as the absolute value of COMP current ( $I_{COMP}$ ) is above  $40 \mu A$ . In

this linear operating range, the dynamic resistance is  $17.7 k\Omega$  typically ( $R_{COMP(up)}$ ) and the effective pull up voltage is  $2.7 V$  typically ( $V_{COMP(REF)}$ ). When  $I_{COMP}$  is decreases, the COMP voltage will increase to  $3.2 V$ .

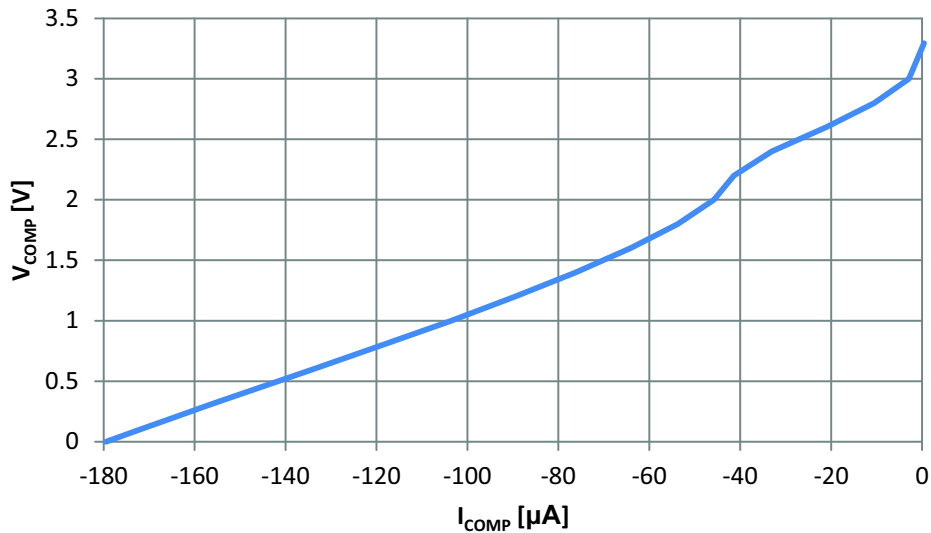


Figure 40. COMP Pin Voltage vs. Current

Figure 41 depicts the skip mode block diagram. When the COMP current information reaches  $I_{COMPskip}$ , the internal clock setting the flip-flop is blanked and the internal consumption of the controller is decreased. The hysteresis of

internal skip comparator is minimized to lower the ripple of the auxiliary voltage for  $V_{CC}$  pin and  $V_{OUT}$  of power supply during skip mode. It eases the design of  $V_{CC}$  over load range.

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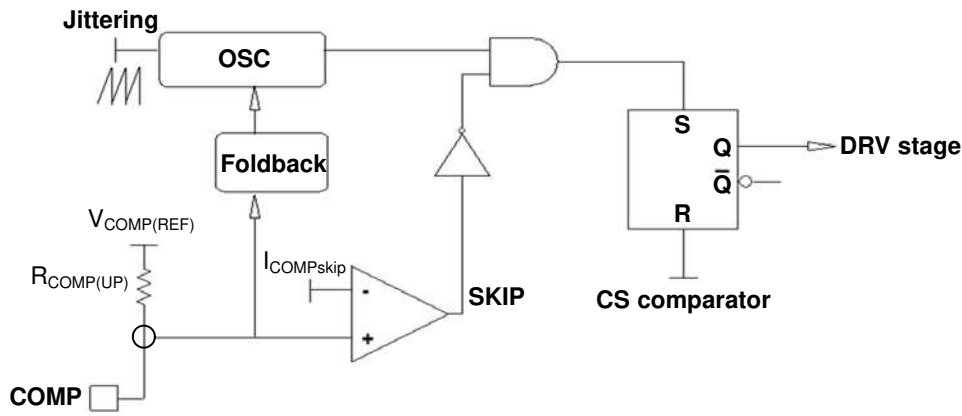


Figure 41. Skip Cycle Schematic

### Limit and OPP Function

The function makes the integrated circuit more flexible. The current drawn out of LIM/OPP pin defines the current set point.

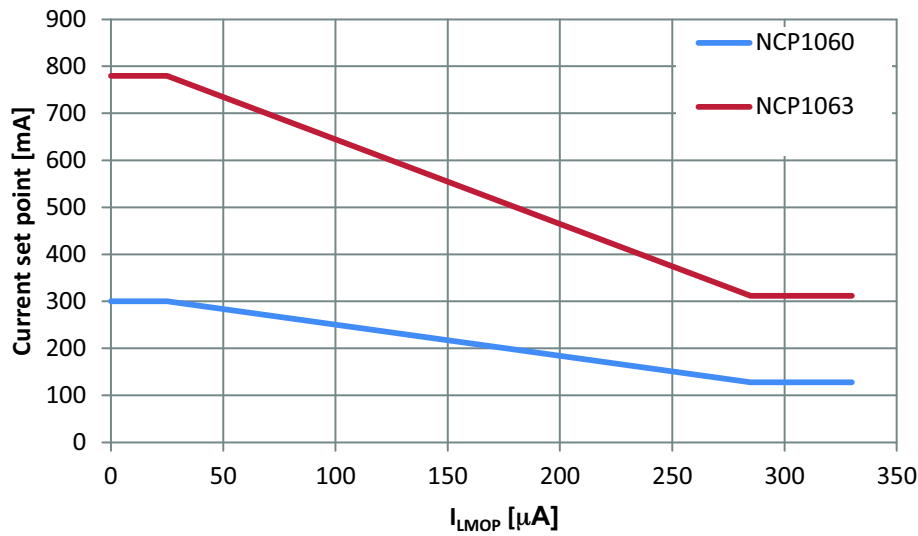


Figure 42. Ipk set-point dependence on  $I_{LMOP}$  current

There are several known ways to implement Over Power Protection (OPP), all suffering from particular problems. These problems range from the added consumption burden on the converter or the skip-cycle disturbance brought by the current-sense offset. A way to reduce the power capability at high line is to capitalize on the negative voltage swing present on the auxiliary diode anode. During the power switch on-time, this point dips to  $-NV_{in}$ , N being the turns ratio between the primary winding and the auxiliary winding. The negative plateau on auxiliary winding will have an amplitude dependant on the input voltage. Resistors

$R_{OPPU}$  and  $R_{OPPL}$  (Figure 43) define current drawn from LIM/OPP and the negative voltage on auxiliary winding. The negative voltage is tied up with bulk voltage, so the higher the bulk voltage is, the deeper is the negative voltage on auxiliary winding, the higher current is drawn from LIM/OPP pin and the lower the peak current is. During the internal MOSFET off period, voltage on auxiliary winding is positive, but the IC ignores the LIM/OPP current. The positive LIM/OPP current has no influence on proper IC function.





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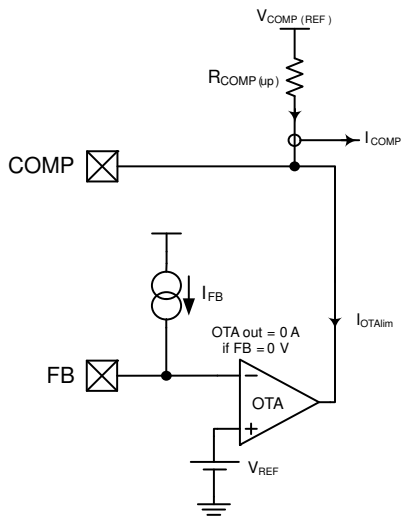


Figure 45. FB Pin Connection

### Design Procedure

The design of an SMPS around a monolithic device does not differ from that of a standard circuit using a controller and a MOSFET. However, one needs to be aware of certain characteristics specific of monolithic devices. Let us follow the steps:

$V_{in \text{ min}} = 90 \text{ Vac}$  or  $127 \text{ Vdc}$  once rectified, assuming a low bulk ripple

$V_{in \text{ max}} = 265 \text{ Vac}$  or  $375 \text{ Vdc}$

$V_{out} = 12 \text{ V}$

$P_{out} = 5 \text{ W}$

Operating mode is CCM

$\eta = 0.8$

1. The lateral MOSFET body-diode shall never be forward biased, either during start-up (because of a large leakage inductance) or in normal operation as shown in Figure 46. This condition sets the maximum voltage that can be reflected during toff. As a result, the Flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you thus must adopt a turn ratio which adheres to the following equation:

$$N \cdot (V_{out} + V_f) < V_{in, \text{min}} \quad (\text{eq. 2})$$

2. In our case, since we operate from a  $127 \text{ V DC}$  rail while delivering  $12 \text{ V}$ , we can select a reflected voltage of  $120 \text{ V dc}$  maximum. Therefore, the turn ratio  $N_p:N_s$  must be smaller than

$$\frac{V_{\text{reflect}}}{V_{out} + V_f} = \frac{120}{12 + 0.5} = 9.6 \text{ or } N_p : N_s < 9.6.$$

Here we choose  $N = 8$  in this case. We will see later on how it affects the calculation.

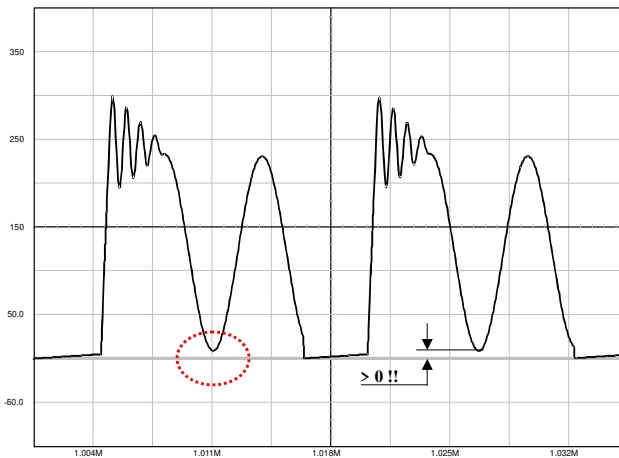


Figure 46. The Drain-Source Wave Shall Always be Positive