



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



NCP1075A/B, NCP1076A/B, NCP1077A/B, NCP1079A/B

Enhanced Off-line Switcher for Robust and Highly Efficient Power Supplies

The NCP107xu products integrate a fixed frequency current mode controller with a 700 V MOSFET. Available in a two different pin-out of the very common PDIP-7 package, the NCP107xu offers a high level of integration, including soft-start, frequency-jittering, short-circuit protection, skip-cycle, a maximum peak current set-point, ramp compensation, and a dynamic self-supply (DSS, eliminating the need for an auxiliary winding).

Unlike other monolithic solutions, the NCP107xu is quiet by nature: during nominal load operation, the part switches at one of the available frequencies (65 or 100 kHz). When the output power demand diminishes, the IC automatically enters frequency foldback mode and provides excellent efficiency at light loads. When the power demand reduces further, it enters into a skip mode to reduce the standby consumption down to a no load condition.

Protection features include: a timer to detect an overload or a short-circuit event, Over-voltage Protection with auto-recovery. Ac input line voltage detection prevents lethal runaway in low input voltage conditions (Brown-out) as well as too high an input line (Ac line Over-voltage Protection). This also allows an Over-power Protection to compensate all internal delays in high input voltage conditions and optimize the maximum output current capability.

For improved standby performance, the connection of an auxiliary winding stops the DSS operation and helps to reduce input power consumption below 50 mW at high line.

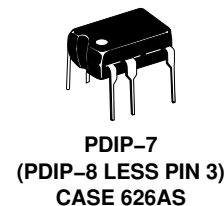
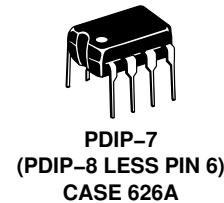
Features

- Built-in 700 V MOSFET with $R_{DS(ON)}$ of 13.5 Ω (NCP1075u), 4.8 Ω (NCP1076u/77u) and 2.9 Ω (NCP1079u)
- Large Creepage Distance Between High Voltage Pins
- Current-mode Fixed Frequency Operation – 65 / 100 kHz
- Various Options for Maximum Peak Current: see below table
- Fixed Slope Compensation
- Skip-cycle Operation at Low Peak Currents Only
- Dynamic Self-supply: No Need for an Auxiliary Winding
- Internal 10 ms Soft-start
- Auto-recovery Output Short-circuit Protection with Timer-based Detection
- Auto-recovery Over-voltage Protection with Auxiliary Winding Operation

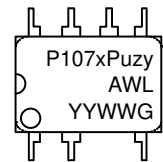
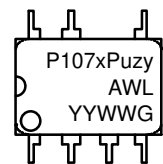


ON Semiconductor®

www.onsemi.com



MARKING DIAGRAMS



| | |
|-------|---------------------------------------|
| x | = Power Version (5, 6, 7, 9) |
| u | = Pin Connections (A, B) |
| z | = Internal Options (upon demand) |
| y | = Oscillator Frequency 65, 100 (A, B) |
| A | = Assembly Location |
| WL | = Wafer Lot |
| Y, YY | = Year |
| W, WW | = Work Week |
| G | = Pb-Free Package |

ORDERING INFORMATION

See detailed ordering and shipping information on page 30 of this data sheet.

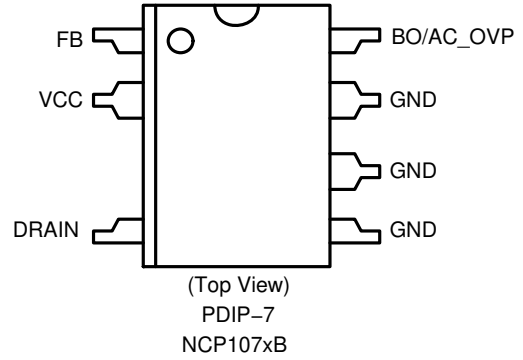
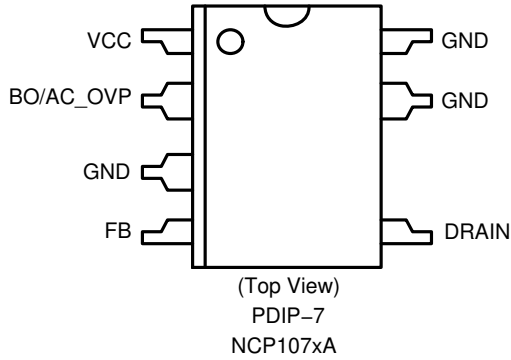
- Adjustable Brown-out Protection and OVP
- 2nd Leading Edge Blanking – Current Protection
- Over Power Protection
- Frequency Jittering for Better EMI Signature
- No Load Input Consumption < 50 mW
- Frequency Foldback to Improve Efficiency at Light Load
- These are Pb-free Devices

Typical Applications

- Auxiliary / Standby Isolated Power Supplies
- Major Home Appliances Power Supplies
- Power Meter SMPS
- Wide Input Industrial SMPS

NCP1075A/B, NCP1076A/B, NCP1077A/B, NCP1079A/B

PIN CONNECTIONS



PIN FUNCTION DESCRIPTION

| Pin No | | Pin Name | Function | Pin Description |
|-----------|-----------|-----------|---|---|
| PDIP 7 v1 | PDIP 7 v2 | | | |
| 1 | 2 | VCC | IC supply pin | This pin is connected to an external capacitor. The V_{CC} management includes an auto-recovery over-voltage protection. |
| 2 | 8 | BO/AC_OVP | Brown-out / Ac Line Over-voltage protection | Detects both input voltage conditions (Brown-out) and too high an input voltage (Ac line OVP). Do not leave this pin floating – if this pin is not used it should be directly connected do GND. |
| 3 | 5 | GND | The IC Ground | |
| 4 | 1 | FB | Feedback signal input | By connecting an opto-coupler to this pin, the peak current set-point is adjusted accordingly to the output power demand. |
| 5 | 4 | DRAIN | Drain connection | The internal drain MOSFET connection |
| 6 | 3 | NC | | This un-connected pin ensures adequate creep-age distance |
| 7 | 6 | GND | The IC Ground | |
| 8 | 7 | GND | The IC Ground | |

PRODUCTS INFOS & INDICATIVE MAXIMUM OUTPUT POWER

| Product | $R_{DS(ON)}$ | I_{PK} | 230 Vrms $\pm 15\%$ | | 85–265 Vrms | |
|---------------------|---------------|----------|---------------------|------------|-------------|------------|
| | | | Adapter | Open Frame | Adapter | Open Frame |
| NCP1075u | 13.5 Ω | 400 mA | 8.5 W | 14 W | 6 W | 10 W |
| NCP1076u / NCP1077u | 4.8 Ω | 800 mA | 19 W | 31 W | 14 W | 23 W |
| NCP1079u | 2.9 Ω | 1050 mA | 25 W | 41 W | 18 W | 30 W |

NOTE: Informative values only, with $T_{amb} = 25^{\circ}\text{C}$, $T_{case} = 100^{\circ}\text{C}$, PDIP-7 package, Self-supply via Auxiliary winding and circuit mounted on minimum copper area as recommended.

QUICK SELECTION TABLE

| Device | Frequency [kHz] | $R_{DS(ON)}$ [Ω] | I_{PK} [mA] | Package type |
|----------|-----------------|---------------------------|---------------|---------------------|
| NCP1075u | 65, 100 | 13.5 | 400 | PDIP-7 (Pb-Free) |
| NCP1076u | 65, 100 | 4.8 | 650 | |
| NCP1077u | 65, 100 | 4.8 | 800 | |
| NCP1079u | 65, 100 | 2.9 | 1050 | |

NCP1075A/B, NCP1076A/B, NCP1077A/B, NCP1079A/B

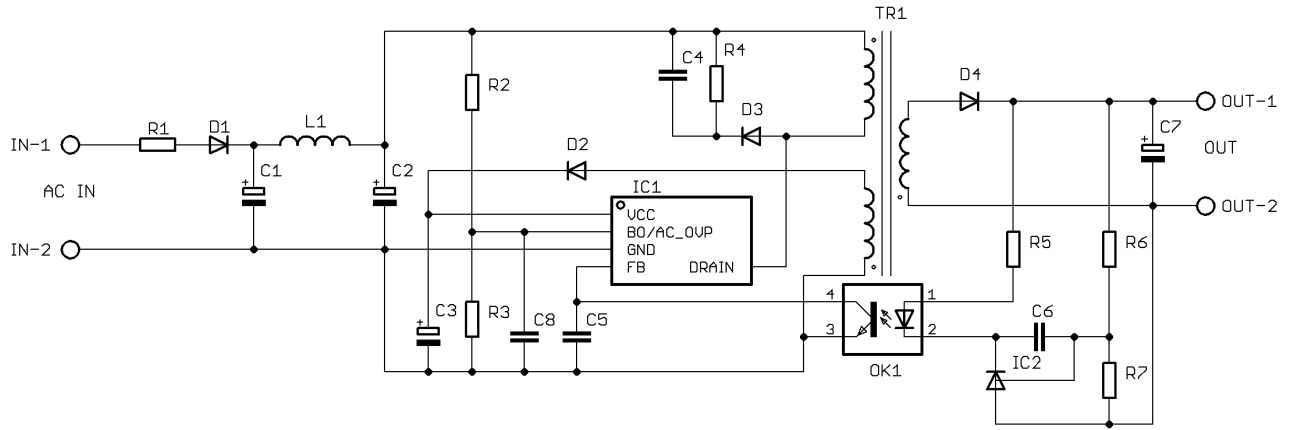


Figure 1. Typical Isolated Application (Flyback Converter), Enable Brown-out, Ac Line OVP and OPP Functions

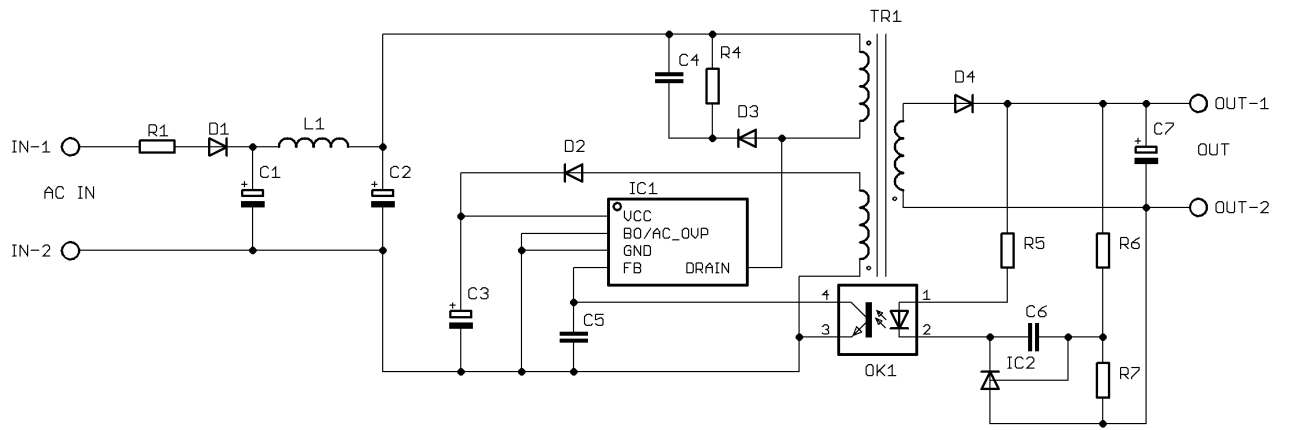


Figure 2. Typical Isolated Application (Flyback Converter), Disabled Brown-out Function – Against Line Detection

NCP1075A/B, NCP1076A/B, NCP1077A/B, NCP1079A/B

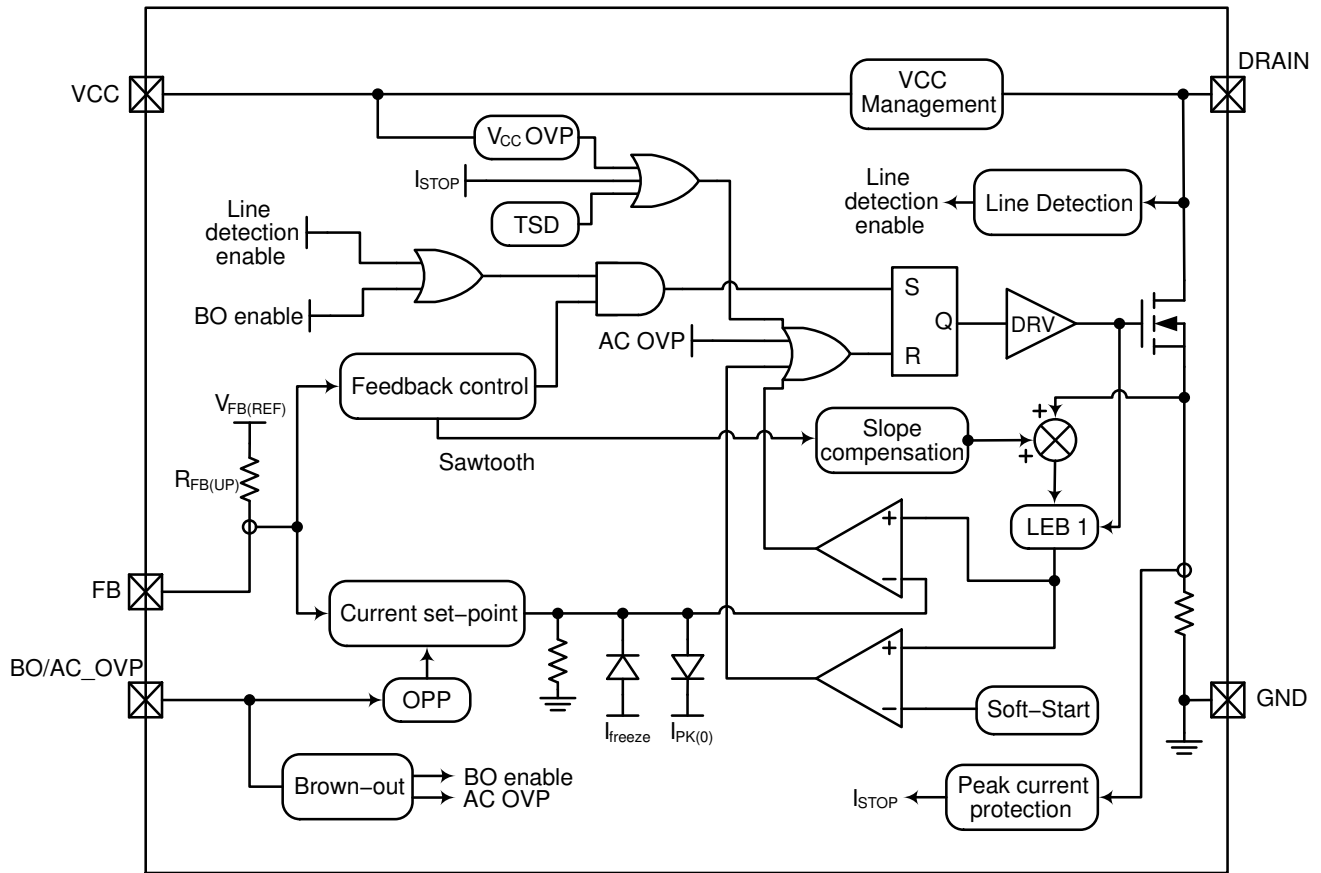


Figure 3. Simplified Internal Circuit Architecture

NCP1075A/B, NCP1076A/B, NCP1077A/B, NCP1079A/B

MAXIMUM RATINGS TABLE (All voltages related to GND terminal)

| Rating | Symbol | Value | Unit | |
|--|---------------|-------------------|-------------|---------------|
| Power supply voltage, VCC pin, continuous voltage | V_{CC} | -0.3 to 20 | V | |
| Voltage on all pins, except DRAIN and VCC pin | V_{inmax} | -0.3 to 10 | V | |
| DRAIN voltage | BV_{DSS} | -0.3 to 700 | V | |
| Maximum Current into VCC pin | I_{CC} | 15 | mA | |
| Drain Current Peak during Transformer Saturation ($T_J = 150^{\circ}C$): NCP1075u NCP1076u/77u NCP1079u | $I_{DS(PK)}$ | 0.9 2.2 3.6 | A | |
| Drain Current Peak during Transformer Saturation ($T_J = 25^{\circ}C$): NCP1075u NCP1076u/77u NCP1079u | | 1.5 3.9 6.4 | | |
| Thermal Resistance Junction-to-Air – PDIP7 | 0.36 Sq. Inch | $R_{\theta J-A}$ | 77 | $^{\circ}C/W$ |
| | 1.0 Sq. Inch | | 68 | |
| Maximum Junction Temperature | T_{JMAX} | 150 | $^{\circ}C$ | |
| Storage Temperature Range | | -60 to +150 | $^{\circ}C$ | |
| Human Body Model ESD Capability (All pins except HV pin) per JEDEC JESD22-A114F | HBM | 2 | kV | |
| Human Body Model ESD Capability (Drain pin) per JEDEC JESD22-A114F | HBM | 1 | kV | |
| Charged-Device Model ESD Capability per JEDEC JESD22-C101E | CDM | 1 | kV | |
| Machine Model ESD Capability per JEDEC JESD22-A115-A | MM | 200 | V | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.
2. Maximum drain current $I_{DS(PK)}$ is obtained when the transformer saturates. It should not be mixed with short pulses that can be seen at turn on. Figure 4 below provides spike limits the device can tolerate.

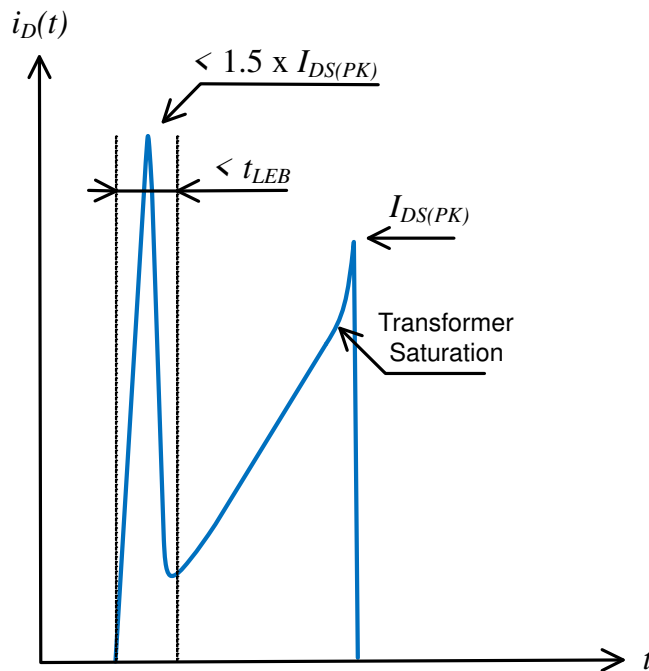


Figure 4. Spike Limits

NCP1075A/B, NCP1076A/B, NCP1077A/B, NCP1079A/B

ELECTRICAL CHARACTERISTICS

(For typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 12\text{ V}$ unless otherwise noted)

| Symbol | Rating | Pin | Min | Typ | Max | Unit |
|--------|--------|-----|-----|-----|-----|------|
|--------|--------|-----|-----|-----|-----|------|

SUPPLY SECTION AND VCC MANAGEMENT

| | | | | | | |
|-----------------|--|-------|-----|----------------------|-----|---------------|
| $V_{CC(ON)}$ | V_{CC} increasing level at which the switcher starts operation | 1 (2) | 8.0 | 8.4 | 8.9 | V |
| $V_{CC(MIN)}$ | V_{CC} decreasing level at which the HV current source restarts | 1 (2) | 6.5 | 6.9 | 7.3 | V |
| $V_{CC(OFF)}$ | V_{CC} decreasing level at which the switcher stops operation (UVLO) | 1 (2) | 6.1 | 6.5 | 6.9 | V |
| $V_{CC(reset)}$ | V_{CC} voltage at which the internal latch is reset (Guaranteed by design) | 1 (2) | | 4 | | V |
| I_{CC1} | Internal IC consumption, MOSFET switching ($f_{SW} = 65\text{ kHz}$) NCP1075u NCP1076u/77u NCP1079u | 1 (2) | - | 1.10 1.26 1.40 | - | mA |
| $I_{CC(skip)}$ | Internal IC consumption, V_{FB} is 0 V (No switching on MOSFET) | 1 (2) | - | 400 | - | μA |

POWER SWITCH CIRCUIT

| | | | | | | |
|----------------|--|-------|----------------------------|--|---|---------------|
| $R_{DS(ON)}$ | Power Switch Circuit on-state resistance ($I_{DRAIN} = 50\text{ mA}$) NCP1075u $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ NCP1076u/77u $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ NCP1079u $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ | 5 (4) | - - - - - - | 13.5 26.0 4.8 9.3 2.9 5.3 | 16.8 31.6 6.8 11.6 3.9 7.5 | Ω |
| BV_{DSS} | Power Switch Circuit & Start-up breakdown voltage ($I_{DRAIN(OFF)} = 120\text{ }\mu\text{A}$, $T_J = 25^\circ\text{C}$) | 5 (4) | 700 | - | - | V |
| $I_{DSS(OFF)}$ | Power Switch & Start-up breakdown voltage off-state leakage current $T_J = 125^\circ\text{C}$ ($V_{DS} = 700\text{ V}$) | 5 (4) | - | 85 | - | μA |
| t_R t_F | Switching characteristics ($R_L = 50\text{ }\Omega$, V_{DS} set for $I_{DRAIN} = 0.7 \times I_{lim}$) Turn-on time (90% - 10%) Turn-off time (10% - 90%) | 5 (4) | - - | 20 10 | - - | ns |

INTERNAL START-UP CURRENT SOURCE

| | | | | | | |
|---------------|--|-------|-----|-----|------|----|
| I_{start1} | High-voltage current source, $V_{CC} = V_{CC(ON)} - 200\text{ mV}$ | 5 (4) | 4.0 | 9.0 | 12.0 | mA |
| I_{start2} | High-voltage current source, $V_{CC} = 0\text{ V}$ | 5 (4) | - | 0.5 | - | mA |
| $V_{HV(MIN)}$ | Minimum start-up voltage, $V_{CC} = 0\text{ V}$ | 5 (4) | - | 21 | - | V |
| $V_{CC(TH)}$ | V_{CC} Transient level for I_{start1} to I_{start2} toggling point | 1 (2) | - | 1.6 | - | V |

CURRENT COMPARATOR

| | | | | | | |
|-------------|---|------------------|---------------------------|---------------------------|----------------------------|----|
| I_{PK} | Maximum internal current set-point at 50% duty-cycle FB pin open, $T_J = 25^\circ\text{C}$ NCP1075u NCP1076u NCP1077u NCP1079u | - - - - | - - - - | 400 650 800 1050 | - - - - | mA |
| $I_{PK(0)}$ | Maximum internal current set-point at beginning of switching cycle FB pin open, BO/AC_OVP pin voltage $\leq 0.8\text{ V}$, $T_J = 25^\circ\text{C}$ NCP1075u NCP1076u NCP1077u NCP1079u | - - - - | 420 690 850 1110 | 470 765 940 1230 | 520 840 1030 1350 | mA |

- The final switch current is: $I_{PK(0)} / (V_{in}/L_P + S_a) \times V_{in}/L_P + V_{in}/L_P \times t_{prop}$, with S_a the built-in slope compensation, V_{in} the input voltage, L_P the primary inductor in a flyback, and t_{prop} the propagation delay.
- Oscillator frequency is measured with disabled jittering.

NCP1075A/B, NCP1076A/B, NCP1077A/B, NCP1079A/B

ELECTRICAL CHARACTERISTICS

(For typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 12\text{ V}$ unless otherwise noted)

| Symbol | Rating | Pin | Min | Typ | Max | Unit |
|---------------------------|---|-----|-----|---------------------------|-----|------|
| CURRENT COMPARATOR | | | | | | |
| $I_{PKSW(65)}$ | Final switch current with a primary slope of 200 mA/ μs , $f_{SW} = 65\text{ kHz}$ (Note 3) NCP1075u NCP1076u NCP1077u NCP1079u | - | - | 450 710 860 1100 | - | mA |
| $I_{PKSW(100)}$ | Final switch current with a primary slope of 200 mA/ μs , $f_{SW} = 100\text{ kHz}$ (Note 3) NCP1075u NCP1076u NCP1077u NCP1079u | - | - | 440 685 825 1040 | - | mA |
| $I_{PK(OPP)}$ | Maximum internal current set-point at beginning of switching cycle FB pin open, BO/AC_OVP pin voltage = 2.65 V, $T_J = 25^\circ\text{C}$ NCP1075u NCP1076u NCP1077u NCP1079u | - | - | 375 610 750 985 | - | mA |
| t_{SS} | Soft-start duration (Guaranteed by design) | - | - | 10 | - | ms |
| t_{prop} | Propagation delay from current detection to drain OFF state | - | - | 100 | - | ns |
| t_{LEB1} | Leading Edge Blanking Duration 1 | - | - | 300 | - | ns |
| t_{LEB2} | Leading Edge Blanking Duration 2 | - | - | 100 | - | ns |

INTERNAL OSCILLATOR

| | | | | | | |
|----------------|---|---|----|---------|-----|-----|
| $f_{OSC(65)}$ | Oscillation frequency, 65 kHz version, $T_J = 25^\circ\text{C}$ (Note 4) | - | 59 | 65 | 71 | kHz |
| $f_{OSC(100)}$ | Oscillation frequency, 100 kHz version, $T_J = 25^\circ\text{C}$ (Note 4) | - | 90 | 100 | 110 | kHz |
| f_{jitter} | Frequency jittering in percentage of f_{OSC} | - | - | ± 6 | - | % |
| f_{swing} | Jittering modulation frequency | - | - | 300 | - | Hz |
| D_{MAX} | Maximum duty-cycle | - | 64 | 68 | 72 | % |

FEEDBACK SECTION

| | | | | | | |
|------------------|---|-------|---|------|---|---------------|
| $I_{FB(fault)}$ | FB current for which Fault is detected | 4 (1) | - | -35 | - | μA |
| $I_{FB100\%}$ | FB current for which internal current set-point is 100% ($I_{PK(0)}$) | 4 (1) | - | -44 | - | μA |
| $I_{FB(freeze)}$ | FB current for which internal current set-point is I_{freeze} | 4 (1) | - | -90 | - | μA |
| $V_{FB(REF)}$ | Equivalent pull-up voltage in linear regulation range (Guaranteed by design) | 4 (1) | - | 3.3 | - | V |
| $R_{FB(UP)}$ | Equivalent feedback resistor in linear regulation range (Guaranteed by design) | 4 (1) | - | 19.5 | - | k Ω |

FREQUENCY FOLDBACK & SKIP

| | | | | | | |
|-------------------|--|-------|----|--------------------------|----|---------------|
| I_{FBfold} | Start of frequency foldback FB pin current level | 4 (1) | - | -68 | - | μA |
| $I_{FBfold(END)}$ | End of frequency foldback FB pin current level, $f_{SW} = f_{MIN}$ | 4 (1) | - | -100 | - | μA |
| f_{MIN} | The frequency below which skip-cycle occurs, $T_J = 25^\circ\text{C}$ (Note 4) | - | 23 | 27 | 31 | kHz |
| $I_{FB(skip)}$ | The FB pin current level to enter skip mode | 4 (1) | - | -120 | - | μA |
| I_{freeze} | Internal minimum current set-point ($I_{FB} = I_{FB(freeze)}$) NCP1075u NCP1076u NCP1077u NCP1079u | - | - | 165 270 330 430 | - | mA |

- The final switch current is: $I_{PK(0)} / (V_{in}/L_P + S_a) \times V_{in}/L_P + V_{in}/L_P \times t_{prop}$, with S_a the built-in slope compensation, V_{in} the input voltage, L_P the primary inductor in a flyback, and t_{prop} the propagation delay.
- Oscillator frequency is measured with disabled jittering.

NCP1075A/B, NCP1076A/B, NCP1077A/B, NCP1079A/B

ELECTRICAL CHARACTERISTICS

(For typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 12\text{ V}$ unless otherwise noted)

| Symbol | Rating | Pin | Min | Typ | Max | Unit |
|---------------------------|--|-----|-----|-----|-----|-------------------|
| SLOPE COMPENSATION | | | | | | |
| $S_{a(65)}$ | The internal slope compensation @ 65 kHz: | | | | | mA/ μs |
| | NCP1075u | - | - | 9 | - | |
| | NCP1076u | - | - | 15 | - | |
| | NCP1077u | - | - | 18 | - | |
| $S_{a(100)}$ | The internal slope compensation @ 100 kHz: | | | | | mA/ μs |
| | NCP1075u | - | - | 14 | - | |
| | NCP1076u | - | - | 23 | - | |
| | NCP1077u | - | - | 28 | - | |
| | NCP1079u | - | - | 36 | - | |

PROTECTIONS

| | | | | | | |
|-----------------|---|-------|------|------|------|---------------|
| t_{SCP} | Fault validation further to error flag assertion | - | 35 | 48 | - | ms |
| $t_{recovery}$ | OFF phase in fault mode | - | - | 420 | - | ms |
| V_{OVP} | V_{CC} voltage at which the switcher stops pulsing | 1 (5) | 17.0 | 18.0 | 18.8 | V |
| t_{OVP} | The filter of V_{CC} OVP comparator | - | - | 80 | - | μs |
| $V_{BO(EN)}$ | Brown-out level detection | 2 (8) | - | 50 | - | mV |
| $V_{BO(ON)}$ | Brown-out level, the switcher starts pulsing, OPP starts to decrease I_{PK} | 2 (8) | 0.72 | 0.80 | 0.88 | V |
| $V_{BO(HYST)}$ | Brown-out hysteresis (Guaranteed by design) | 2 (8) | - | 100 | - | mV |
| $V_{ACOV(ON)}$ | OVP level when the switcher stops pulsing | 2 (8) | 2.6 | 2.9 | 3.2 | V |
| $V_{ACOV(OFF)}$ | OVP level when the switcher starts pulsing | 2 (8) | 2.3 | 2.6 | 2.9 | V |
| $t_{BOfilter}$ | V_{BO} filter | - | - | 20 | - | μs |
| t_{BO} | Brown-out timer | - | - | 50 | - | ms |
| $V_{HV(EN)}$ | The drain pin voltage above which the MOSFET operates. Checked after one of the following events: TSD, UVLO, SCP, or V_{CC} OVP mode, BO/AC_OVP pin = 0 V | 5 (4) | 72 | 91 | 110 | V |
| $I_{PK(150)}$ | High current protection, percent of max limit I_{PK} (Guaranteed by design) | - | - | 150 | - | % |

TEMPERATURE MANAGEMENT

| | | | | | | |
|---------|---|---|-----|----|---|------------------|
| TSD | Temperature shutdown (Guaranteed by design) | - | 150 | - | - | $^\circ\text{C}$ |
| TSDHYST | Hysteresis in shutdown (Guaranteed by design) | - | - | 20 | - | $^\circ\text{C}$ |

3. The final switch current is: $I_{PK(0)} / (V_{in}/L_P + S_a) \times V_{in}/L_P + V_{in}/L_P \times t_{prop}$, with S_a the built-in slope compensation, V_{in} the input voltage, L_P the primary inductor in a flyback, and t_{prop} the propagation delay.

4. Oscillator frequency is measured with disabled jittering.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

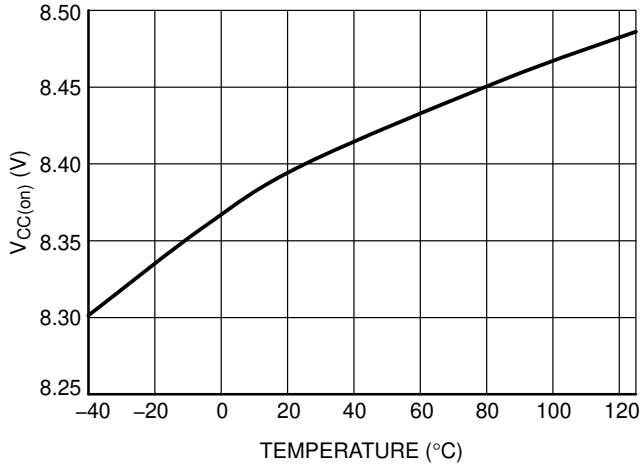


Figure 5. $V_{CC(on)}$ vs. Temperature

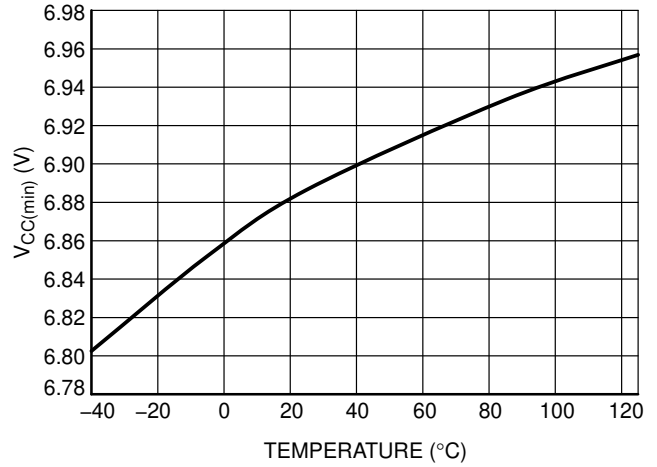


Figure 6. $V_{CC(min)}$ vs. Temperature

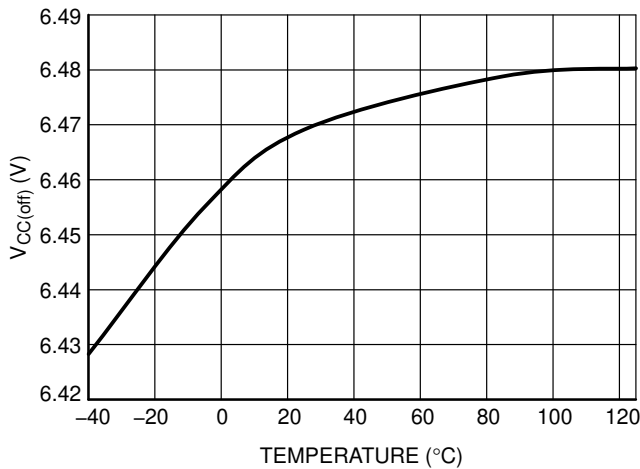


Figure 7. $V_{CC(off)}$ vs. Temperature

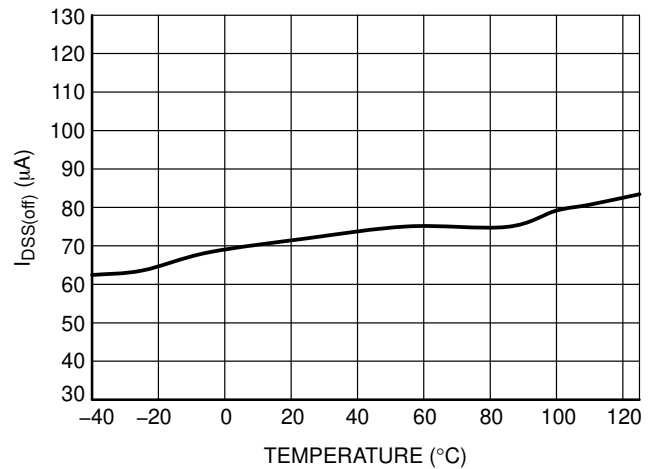


Figure 8. $I_{DSS(off)}$ vs. Temperature

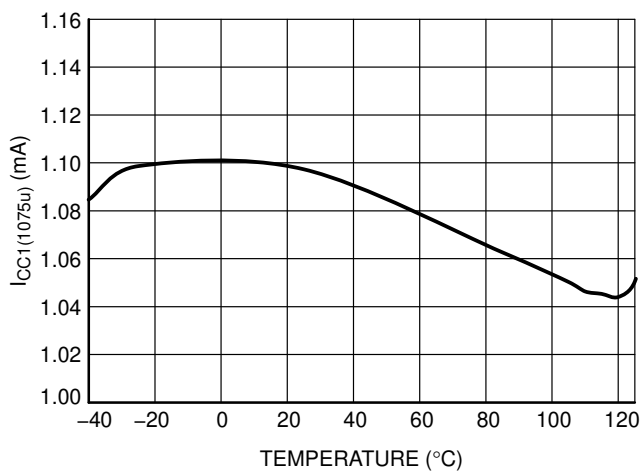


Figure 9. $I_{CC1(1075u)}$ vs. Temperature

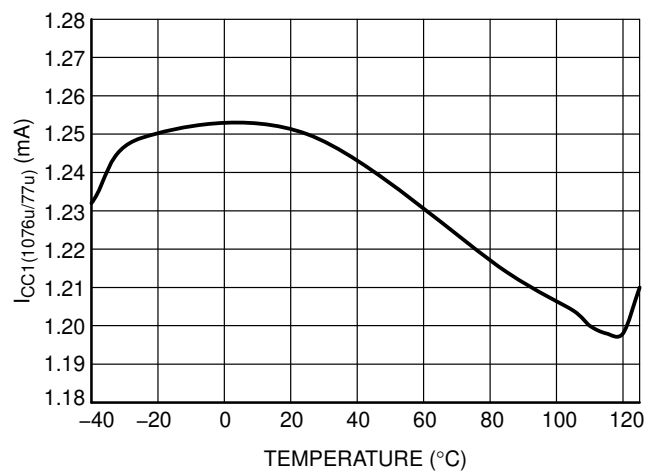


Figure 10. $I_{CC1(1076u/77u)}$ vs. Temperature

TYPICAL CHARACTERISTICS

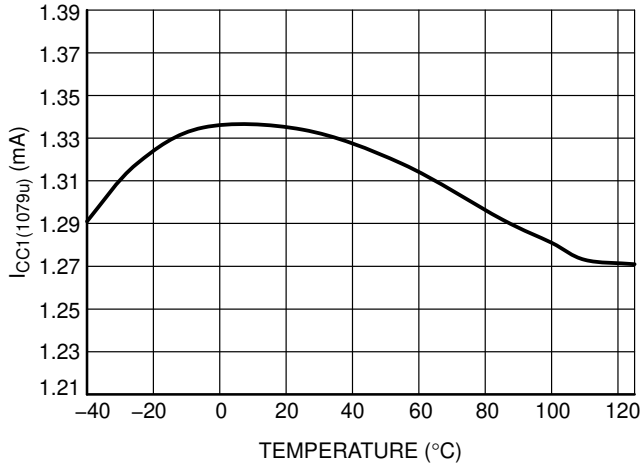


Figure 11. I_{CC1}(1079u) vs. Temperature

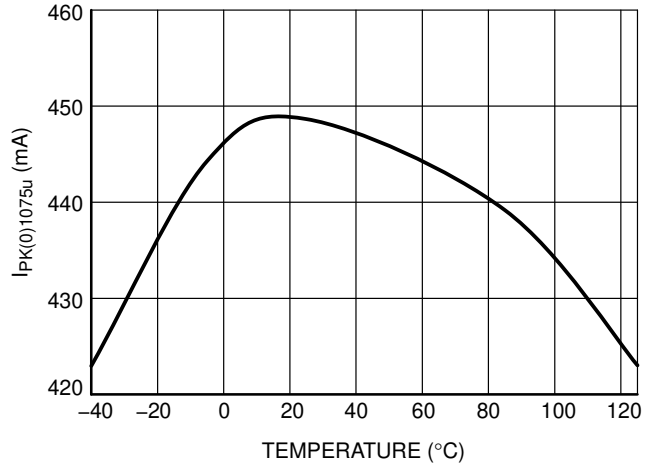


Figure 12. I_{PK}(0)1075u vs. Temperature

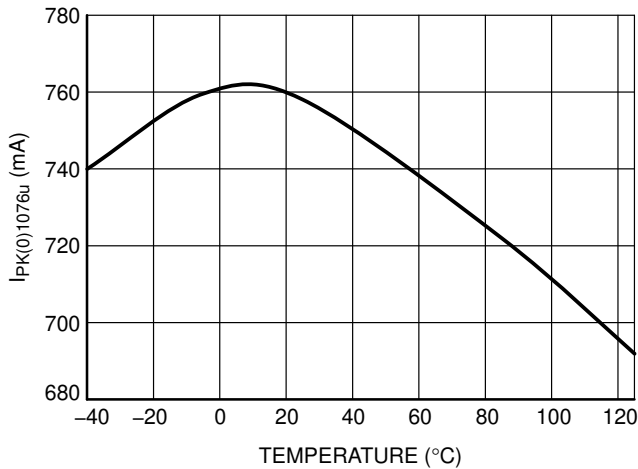


Figure 13. I_{PK}(0)1076u vs. Temperature

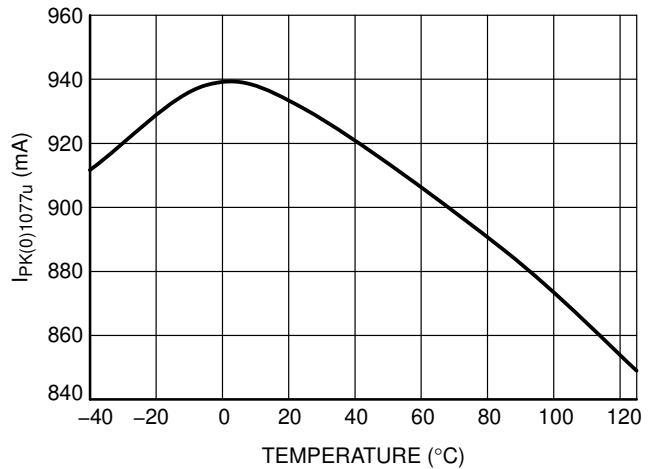


Figure 14. I_{PK}(0)1077u vs. Temperature

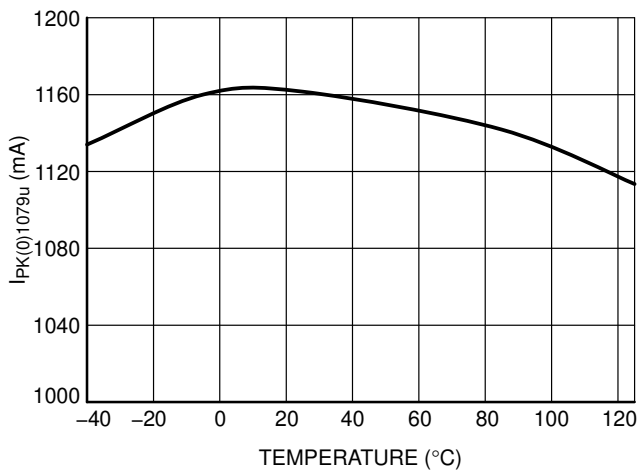


Figure 15. I_{PK}(0)1079u vs. Temperature

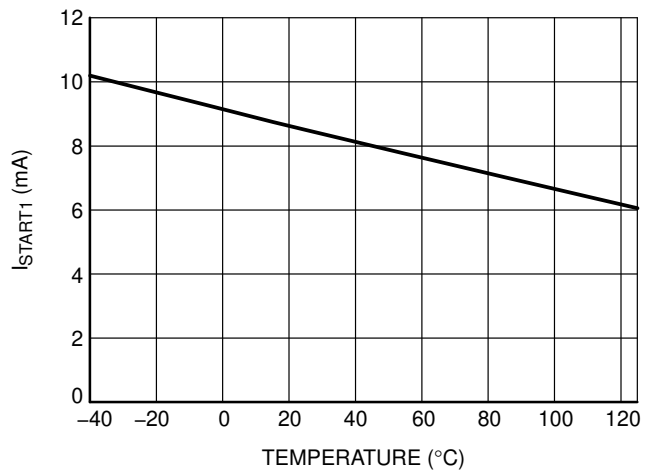


Figure 16. I_{START1} vs. Temperature

TYPICAL CHARACTERISTICS

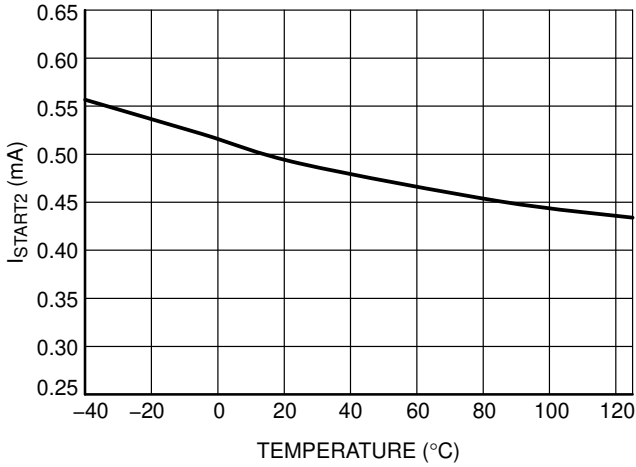


Figure 17. I_{START2} vs. Temperature

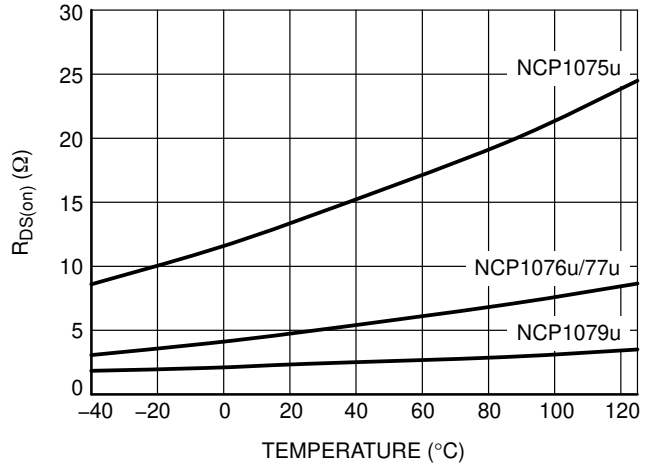


Figure 18. R_{DS(on)} vs. Temperature

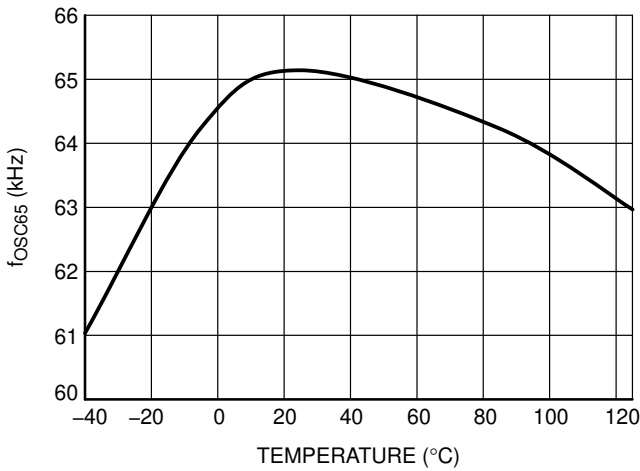


Figure 19. f_{OSC65} vs. Temperature

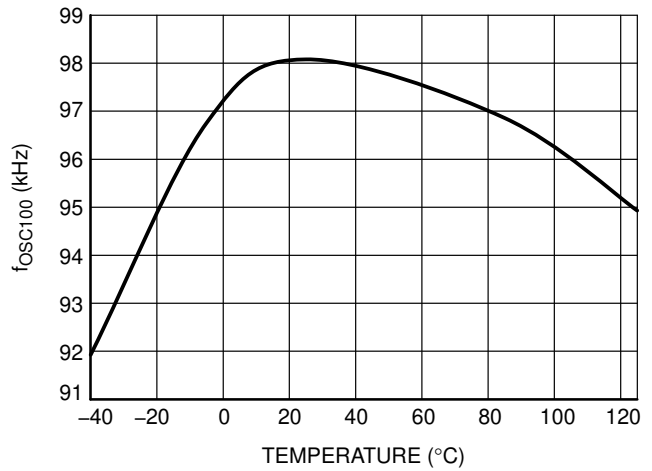


Figure 20. f_{OSC100} vs. Temperature

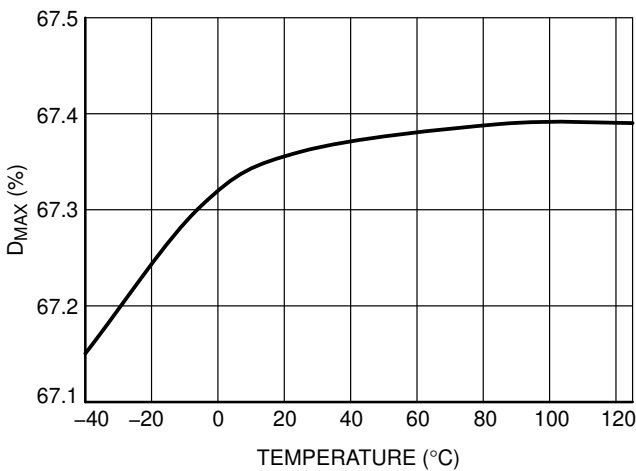


Figure 21. D_{MAX} vs. Temperature

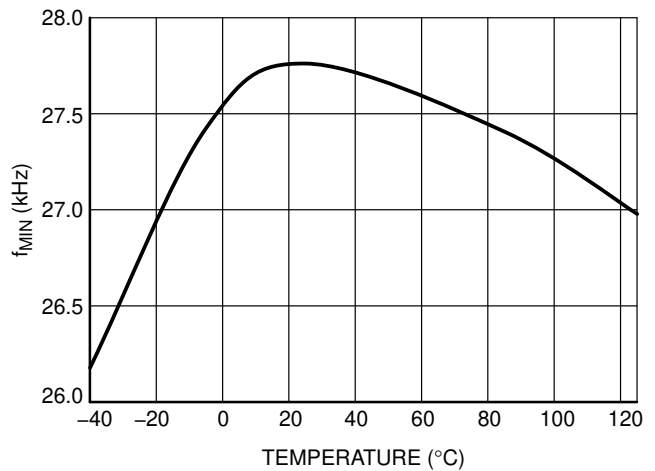


Figure 22. f_{MIN} vs. Temperature

TYPICAL CHARACTERISTICS

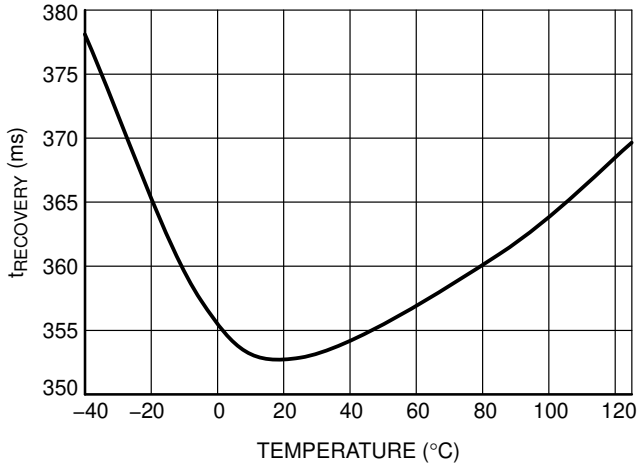


Figure 23. $t_{RECOVERY}$ vs. Temperature

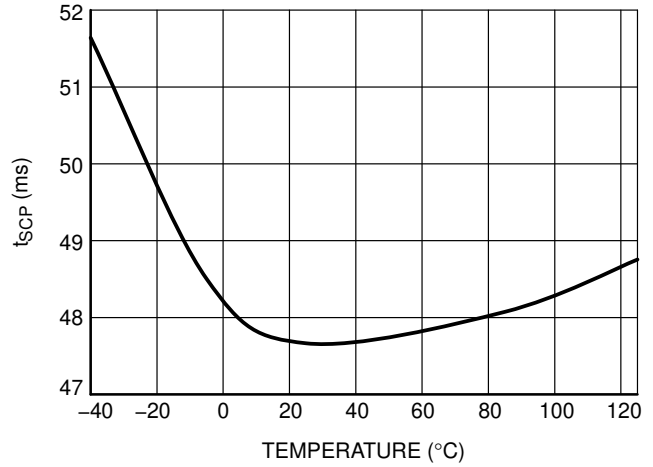


Figure 24. t_{SCP} vs. Temperature

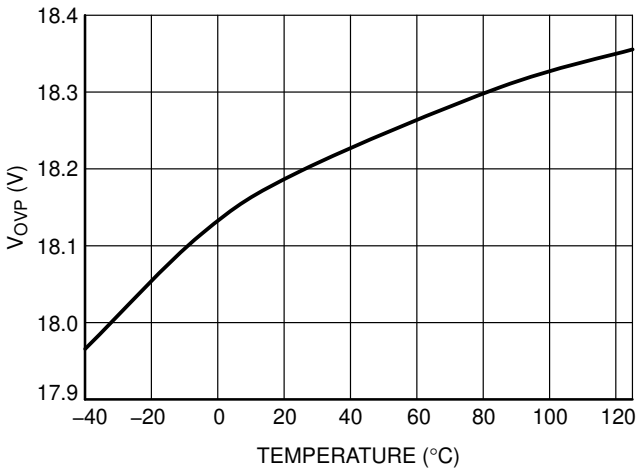


Figure 25. V_{OVP} vs. Temperature

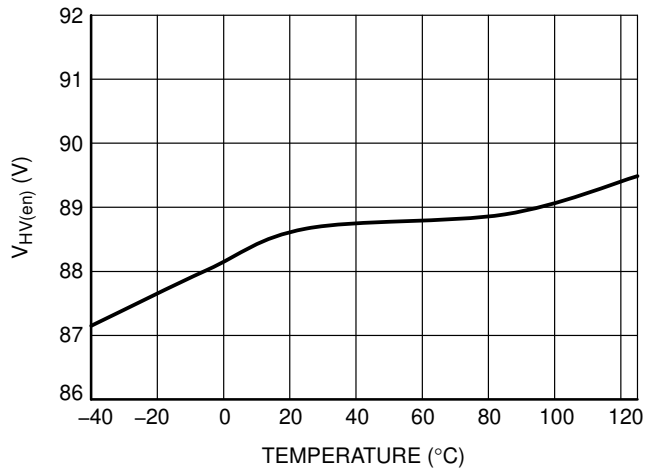


Figure 26. $V_{HV(en)}$ vs. Temperature

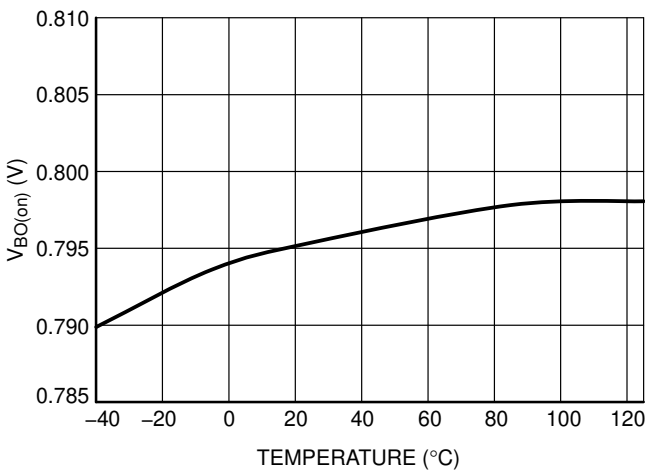


Figure 27. $V_{BO(on)}$ vs. Temperature

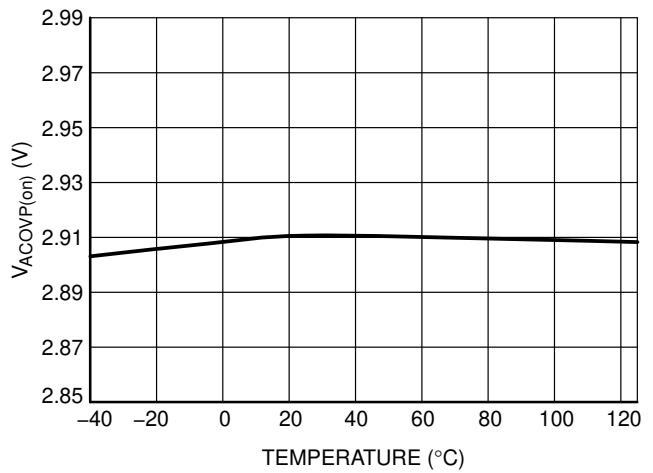


Figure 28. $V_{ACOV P(on)}$ vs. Temperature

TYPICAL CHARACTERISTICS

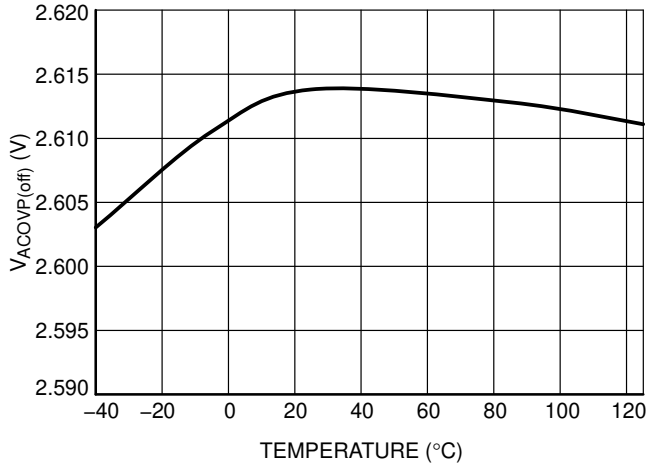


Figure 29. $V_{ACOVP(off)}$ vs. Temperature

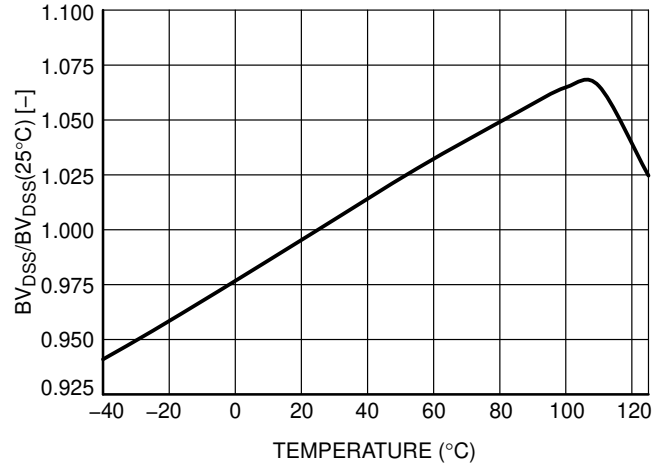


Figure 30. $BV_{DSS}/BV_{DSS}(25^{\circ}C)$ vs. Temperature

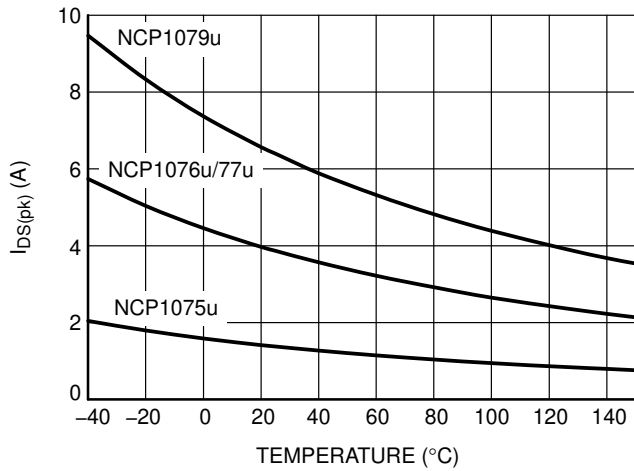


Figure 31. Drain Current Peak during Transformer Saturation vs. Junction Temperature

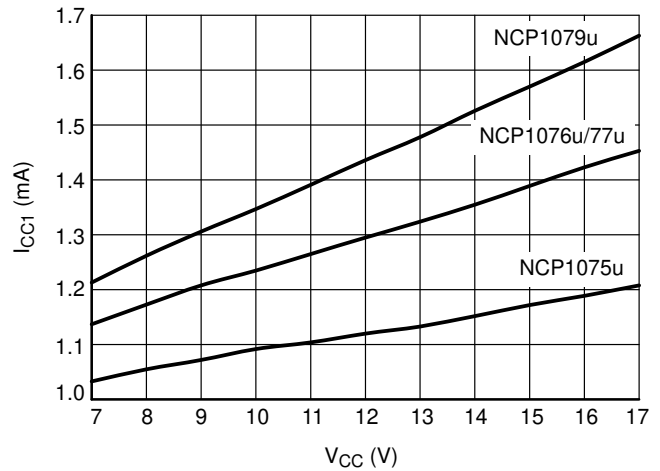


Figure 32. I_{CC1} vs. V_{CC}

APPLICATION INFORMATION

Introduction

Thanks to ON Semiconductor Very High Voltage Integrated Circuit technology, the circuit hosts a high-voltage power MOSFET featuring a 13.5/4.8/2.9 Ω $R_{DS(ON)} - T_J = 25^\circ\text{C}$. An internal current source delivers the start-up current, necessary to crank the power supply.

- **Current-mode operation:** The controller uses current-mode control architecture.
- **700 V Power MOSFET:** Thanks to ON Semiconductor Very High Voltage Integrated Circuit technology, the circuit hosts a high-voltage power MOSFET featuring a 4.8 and 2.9 Ω $R_{DS(ON)} - T_J = 25^\circ\text{C}$. This value lets the designer build a power supply up to 28 W operated on universal mains. An internal current source delivers the start-up current, necessary to crank the power supply.
- **Dynamic Self-Supply:** This device could be used in an application without an auxiliary winding to provide supply voltage via an internal high-voltage current source.
- **Short-circuit protection:** By permanently monitoring the feedback line activity, the IC is able to detect the presence of a short-circuit, immediately reducing the output power for a total system protection. A t_{SCP} timer is started as soon as the feedback current is below threshold, $I_{FB(fault)}$, which indicates a maximum peak current condition. If at the end of this timer the fault is still present, then the device enters a safe, auto-recovery burst mode, affected by a fixed timer recurrence, $t_{recovery}$. Once the short has disappeared, the controller resumes and goes back to normal operation.
- **Built-in VCC Over-Voltage Protection:** When the auxiliary winding is used to bias the VCC pin (no DSS), an internal comparator is connected to VCC pin. In case the voltage on the pin exceeds the V_{OVP} level (18 V typically), the controller immediately stops switching and awaits a full timer period ($t_{recovery}$) before attempting to re-start. If the fault is gone, the controller resumes operation. If the fault is still there, e.g. in the case of a broken opto-coupler, the controller protects the load through a safe burst mode.
- **Line detection:** An internal comparator monitors the drain voltage. If the drain voltage is lower than the internal threshold ($V_{HV(EN)}$), the internal power switch

is inhibited. This avoids operating at too low an ac input. Line detection is active, when BO/AC_OVP pin is grounded.

- **Brown-out detection and AC line Over-Voltage Protection:** The BO/AC_OVP input monitors bulk voltage level via resistive divider and thus assures that the application is working only for designed bulk voltage. When BO/AC_OVP pin is connected to ground, Line detection is inhibited.
- **Internal OPP:** An internal function using the bulk voltage to program the maximum current reduction for a given input voltage. Internal OPP is active when BO/AC_OVP pin is connected via resistive divider to the bulk voltage.
- **2nd LEB:** Second level of current protection. If peak current is 150% max peak current limit, then the controller stops switching after three pulses and waits for an auto-recovery period ($t_{recovery}$) before attempting to re-start.
- **Frequency jittering:** An internal low-frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis. To improve the EMI signature at low power levels, the jittering remains active in frequency foldback mode.
- **Soft-Start:** A 10 ms soft-start ensures a smooth start-up sequence, reducing output overshoots.
- **Frequency foldback capability:** A continuous flow of pulses is not compatible with no-load/light-load standby power requirements. To excel in this domain, the controller observes the feedback current information and when it reaches a level of I_{FBfold} , the oscillator then starts to reduce its switching frequency as the feedback current continues to increase (the power demand continues to reduce). It can go down to 27 kHz (typical) reached for a feedback level of $I_{FBfold(END)}$ (100 μA roughly). At this point, if the power continues to drop, the controller enters classical skip-cycle mode.
- **Skip:** If SMPS naturally exhibits a good efficiency at nominal load, they begin to be less efficient when the output power demand diminishes. By skipping un-needed switching cycles, the NCP107xu drastically reduces the power wasted during light load conditions.

Start-up Sequence

When the power supply is first powered from the mains outlet, the internal current source (typically 9.2 mA) is biased and charges up the V_{CC} capacitor from the drain pin. Once the voltage on this V_{CC} capacitor reaches the $V_{CC(ON)}$ level (typically 8.4 V), the current source turns off and pulses are delivered by the output stage: the circuit is awake and activates the power MOSFET if the bulk voltage is above $V_{HV(EN)}$ level (Brown-in protection) or voltage on BO/AC_OVP pin is above $V_{BO(ON)}$ level (Brown-out protection). Figure 33 details the simplified internal circuitry.

Being loaded by the circuit consumption, the voltage on the V_{CC} capacitor goes down. When V_{CC} is below $V_{CC(MIN)}$ level (7 V typically), it activates the internal current source to bring V_{CC} toward $V_{CC(ON)}$ level and stops again: a cycle takes place whose low frequency depends on the V_{CC} capacitor and the IC consumption. A 1.5 V ripple takes place on the V_{CC} pin whose average value equals $(V_{CC(ON)} + V_{CC(MIN)})/2$. Figure 34 portrays a typical operation of the DSS.

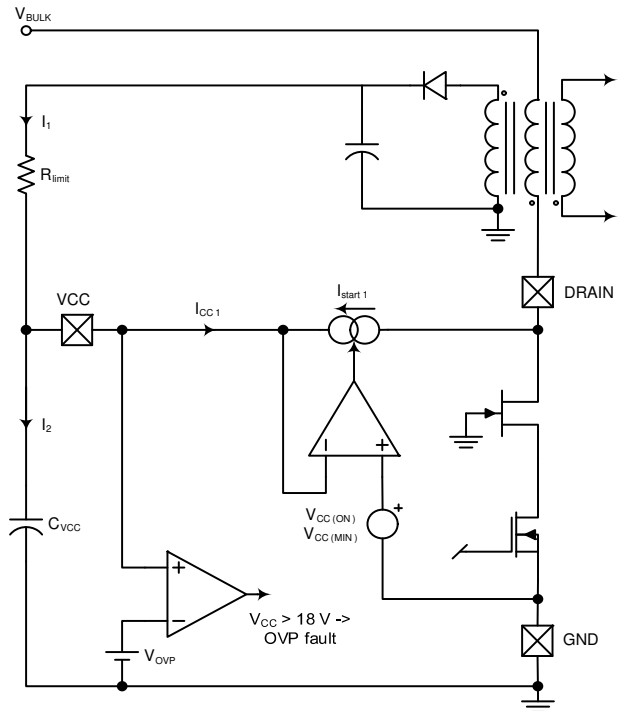


Figure 33. The Internal Arrangement of the Start-up Circuitry

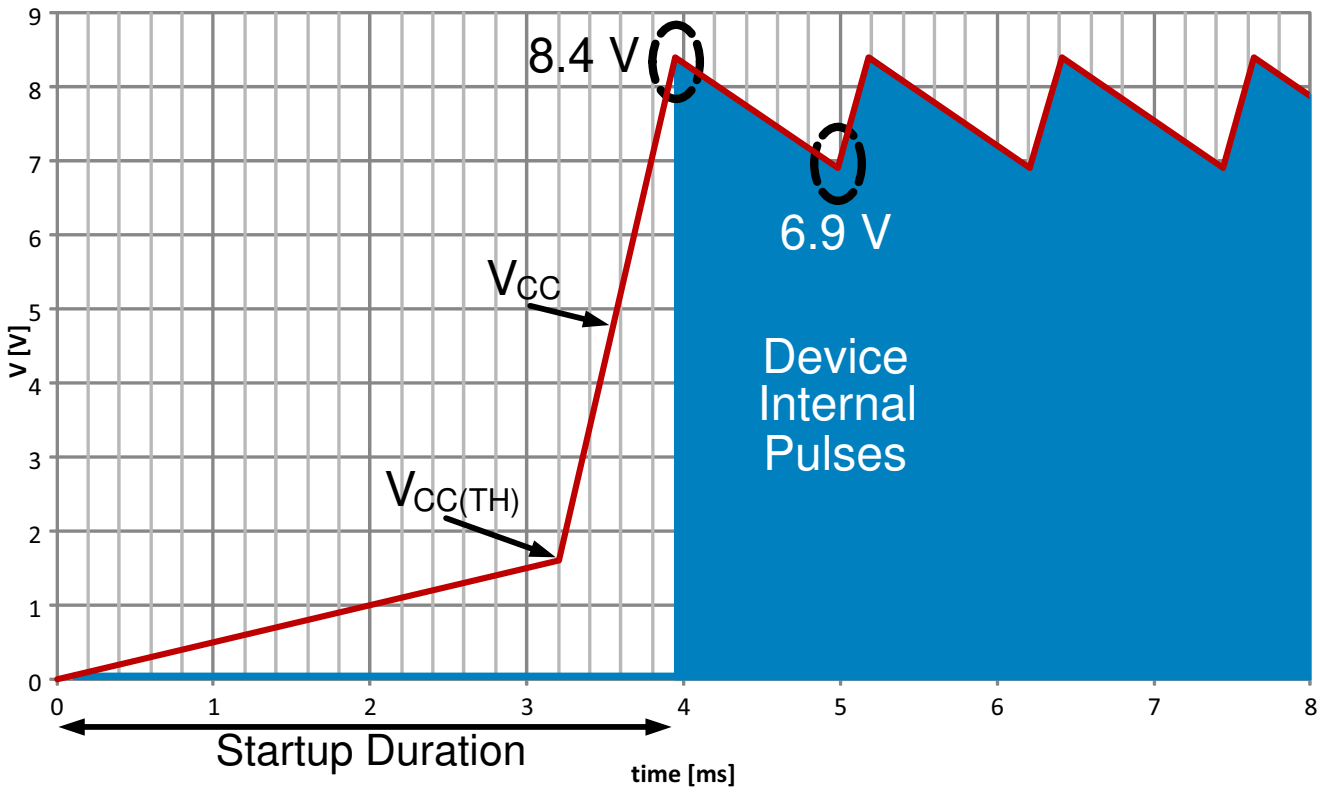


Figure 34. The Charge / Discharge Cycle Over a 1 μ F V_{CC} Capacitor

As one can see, even if there is auxiliary winding to provide energy for V_{CC} , it happens that the device is still biased by DSS during start-up time or some fault mode when the voltage on auxiliary winding is not ready yet. The V_{CC} capacitor shall be dimensioned to avoid V_{CC} crosses $V_{CC(OFF)}$ level, which stops operation. The ΔV between $V_{CC(MIN)}$ and $V_{CC(OFF)}$ is 0.5 V. There is no current source to charge V_{CC} capacitor when driver is on, i.e. drain voltage is close to zero. Hence the V_{CC} capacitor can be calculated using

$$C_{VCC} \geq \frac{I_{CC1} \cdot D_{MAX}}{f_{OSC} \cdot \Delta V} \quad (\text{eq. 1})$$

Take the 65 kHz device as an example. C_{VCC} should be above

$$C_{VCC} = \frac{1.45 \cdot 10^{-3} \cdot 0.73}{59 \cdot 10^3 \cdot 0.5} = 36 \text{ nF}$$

A margin that covers the temperature drift and the voltage drop due to switching inside FET should be considered, and thus a capacitor above 0.1 μF is appropriate.

The V_{CC} capacitor has only a supply role and its value does not impact other parameters such as fault duration or the frequency sweep period for instance. As one can see on Figure 33, an internal OVP comparator protects the switcher against lethal V_{CC} runaways. This situation can occur if the feedback loop opto-coupler fails, for instance, and you would like to protect the converter against an over-voltage event. In that case, the over-voltage protection (OVP) circuit immediately stops the output pulses for $t_{recovery}$ duration (420 ms typically). Then a new start-up attempt takes place to check whether the fault has disappeared or not. The OVP paragraph gives more design details on this particular section.

Fault Condition – Short-circuit on VCC

In some fault situations, a short-circuit can purposely occur between V_{CC} and GND. In high line conditions ($V_{HV} = 370 \text{ V dc}$) the current delivered by the start-up device will seriously increase the junction temperature. For instance, since I_{start1} equals 4.9 mA (the min corresponds to the highest T_J), the device would dissipate $370 \times 4.9 \times 10^{-3} = 1.81 \text{ W}$. To avoid this situation, the

controller includes a novel circuitry made of two start-up levels, I_{start1} and I_{start2} . At power-up, as long as V_{CC} is below a 1.6 V level, the source delivers I_{start2} (around 500 μA typical), then, when V_{CC} reaches 1.6 V, the source smoothly transitions to I_{start1} and delivers its nominal value. As a result, in case of short-circuit between V_{CC} and GND, the power dissipation will drop to $370 \times 500 \times 10^{-6} = 185 \text{ mW}$. Figure 34 portrays this particular behavior.

The first start-up period is calculated by the formula $C \times V = I \times t$, which implies a $1 \times 10^{-6} \times 1.6 / (500 \times 10^{-6}) = 3.2 \text{ ms}$ start-up time for the first sequence. The second sequence is obtained by toggling the source to 8.9 mA with a ΔV of $V_{CC(ON)} - V_{CC(TH)} = 8.4 \text{ V} - 1.6 \text{ V} = 6.8 \text{ V}$, which finally leads to a second start-up time of $1 \times 10^{-6} \times 6.8 / (8.9 \times 10^{-3}) = 0.76 \text{ ms}$. The total start-up time becomes $3.2 \text{ ms} + 0.76 \text{ ms} = 3.96 \text{ ms}$. Please note that this calculation is approximated by the presence of the knee in the vicinity of the transition.

Fault Condition – Output Short-circuit

As soon as V_{CC} reaches $V_{CC(ON)}$, drive pulses are internally enabled. If everything is correct, the auxiliary winding increases the voltage on the V_{CC} pin as the output voltage rises. During the start-sequence, the controller smoothly ramps up the peak drain current to maximum setting, i.e. I_{PK} , which is reached after a typical period of 10 ms. When the output voltage is not regulated, the current coming through FB pin is below $I_{FBfault}$ level (35 μA typically), which is not only during the start-up period but also anytime an overload occurs, an internal error flag is asserted, I_{pFlag} , indicating that the system has reached its maximum current limit set-point. The assertion of this flag triggers a fault counter t_{SCP} (48 ms typically). If at counter completion, I_{pFlag} remains asserted, all driving pulses are stopped and the part stays off in $t_{recovery}$ duration (about 420 ms). A new attempt to re-start occurs and will last 48 ms providing the fault is still present. If the fault still affects the output, a safe burst mode is entered, affected by a low duty-cycle operation (11%). When the fault disappears, the power supply quickly resumes operation. Figure 35 depicts this particular mode:

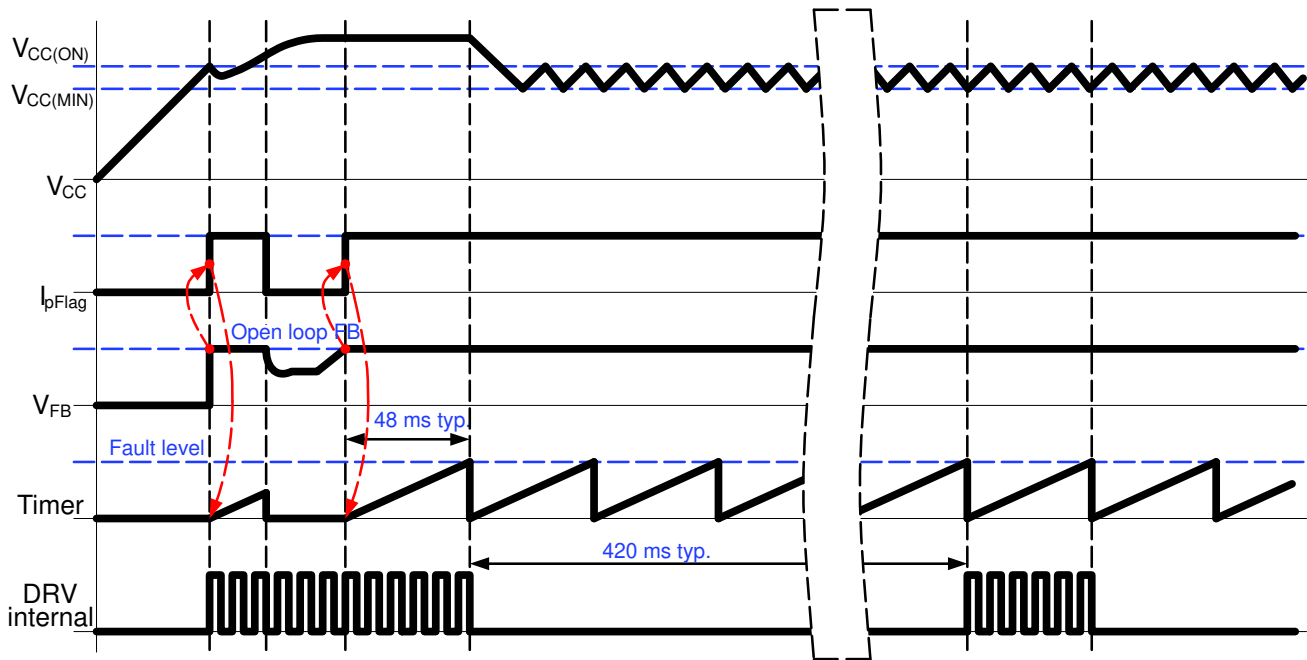


Figure 35. In Case of Short-circuit or Overload, the NCP107xu Protects Itself and the Power Supply Via a Low Frequency Burst Mode. The V_{CC} is Maintained by the Current Source and Self-supplies the Controller.

Auto-recovery Over-voltage Protection

The particular NCP107xu arrangement offers a simple way to prevent output voltage runaway when the opto-coupler fails. As Figure 36 shows, a comparator monitors the VCC pin. If the auxiliary winding delivers too much voltage to the C_{VCC} capacitor, then the controller considers an OVP situation and stops the internal drivers. When an OVP occurs, all switching pulses are permanently disabled. After $t_{recovery}$ delay, the circuit resumes operations. If the failure symptom still exists, e.g. feedback opto-coupler fails, the device keeps the auto-recovery OVP mode. We recommend the insertion of a resistor (R_{limit}) between the auxiliary dc level and the VCC pin to protect the IC against high voltage spikes, which can damage the IC. It

is also recommended to filter out the VCC line to avoid undesired OVP activations. R_{limit} should be carefully selected to suppress false-triggers of the OVP as we discussed, but also to avoid disturbing the V_{CC} in low / light load conditions.

Self-supplying controllers in extremely low-standby applications often puzzles the designer. Actually, if a SMPS operated at nominal load can deliver an auxiliary voltage of an arbitrary 16 V (V_{nom}), this voltage can drop below 10 V (V_{stby}) when entering standby. This is because the recurrence of the switching pulses expands so much that the low frequency re-fueling rate of the V_{CC} capacitor is not enough to keep a proper auxiliary voltage.

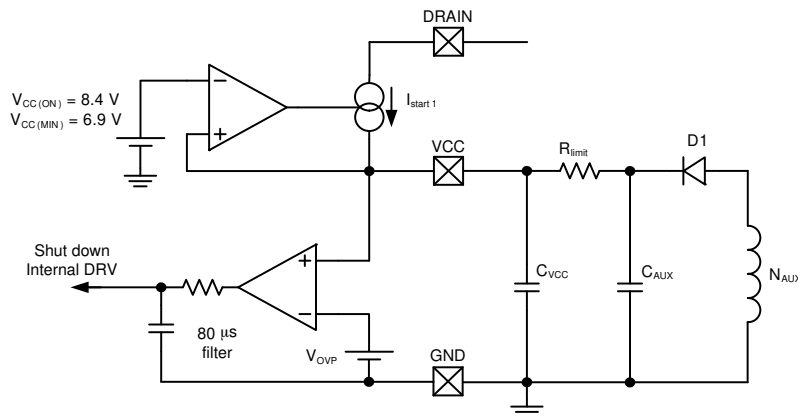


Figure 36. A More Detailed View of the NCP107xu Offers Better Insight on How to Properly Wire an Auxiliary Winding

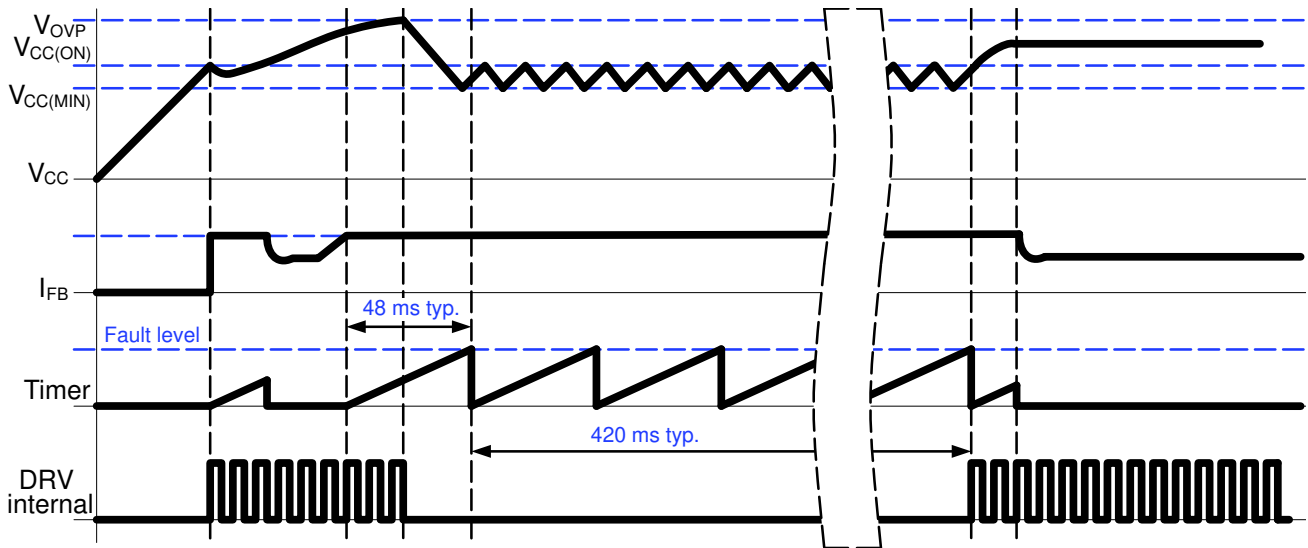


Figure 37. Describes the Main Signal Variations When the Part Operates in Auto-recovery OVP

Soft-start

The NCP107xu features a 10 ms soft-start which reduces the power-on stress but also contributes to lower the output overshoot. Soft-start is running every time when IC starts switching. It means a first start, a new start after OVP, TSD,

Brown-out, etc. Figure 38 shows a typical operating waveform. The NCP107xu features a novel patented structure which offers a better soft-start ramp, almost ignoring the start-up pedestal inherent to traditional current-mode supplies:

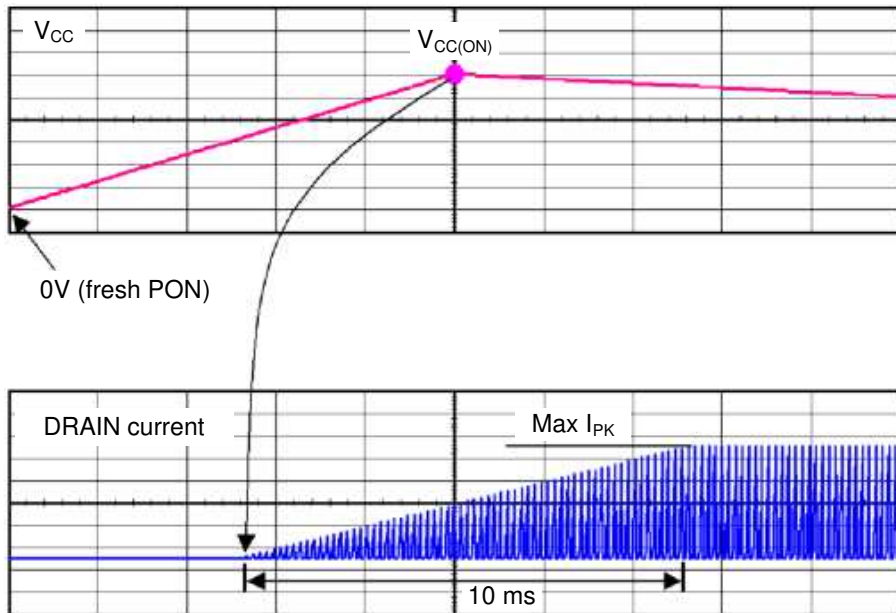


Figure 38. The 10 ms Soft-start Sequence

Jittering

Frequency jittering is a method used to soften the EMI signature by spreading the energy in the vicinity of the main switching component. The NCP107xu offers a $\pm 6\%$ deviation of the nominal switching frequency. The sweeping

sawtooth is internally generated and modulates the clock up and down with a fixed frequency of 300 Hz. Figure 39 shows the relationship between the jitter ramp and the frequency deviation. It is not possible to externally disable the jitter.

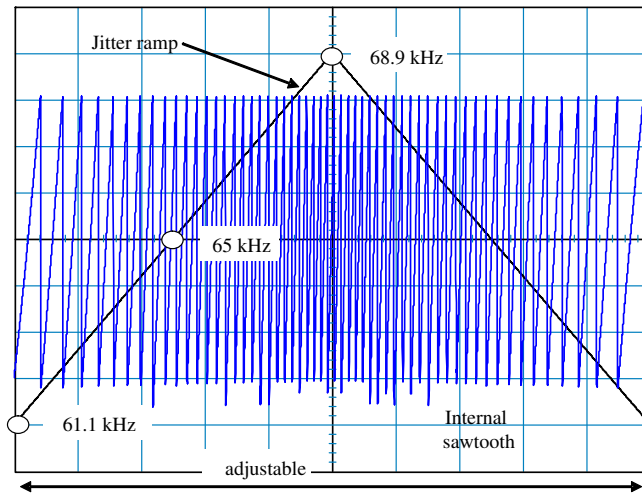


Figure 39. Modulation Effects on the Clock Signal by the Jittering Sawtooth

Line Detection

When BO/AC_OVP pin is grounded (voltage on this pin is below $V_{BO(EN)}$) Figure 2, then an internal comparator monitors the drain voltage as recovering from one of the following situations:

- Short-Circuit Protection,
- V_{CC} OVP is Confirmed,
- UVLO
- TSD

If the drain voltage is lower than the internal threshold $V_{HV(EN)}$ (91 V dc typically), the internal power switch is inhibited. This avoids operating at too low ac input.

Brown-out Function, Ac Line Over-voltage Protection

The Brown-out circuitry offers a way to protect the application from operation under too low an input voltage. Below a given level, the controller blocks the output pulses, above it, it authorizes them. The internal circuitry, depicted by Figure 40, offers a way to observe the high-voltage (HV) rail.

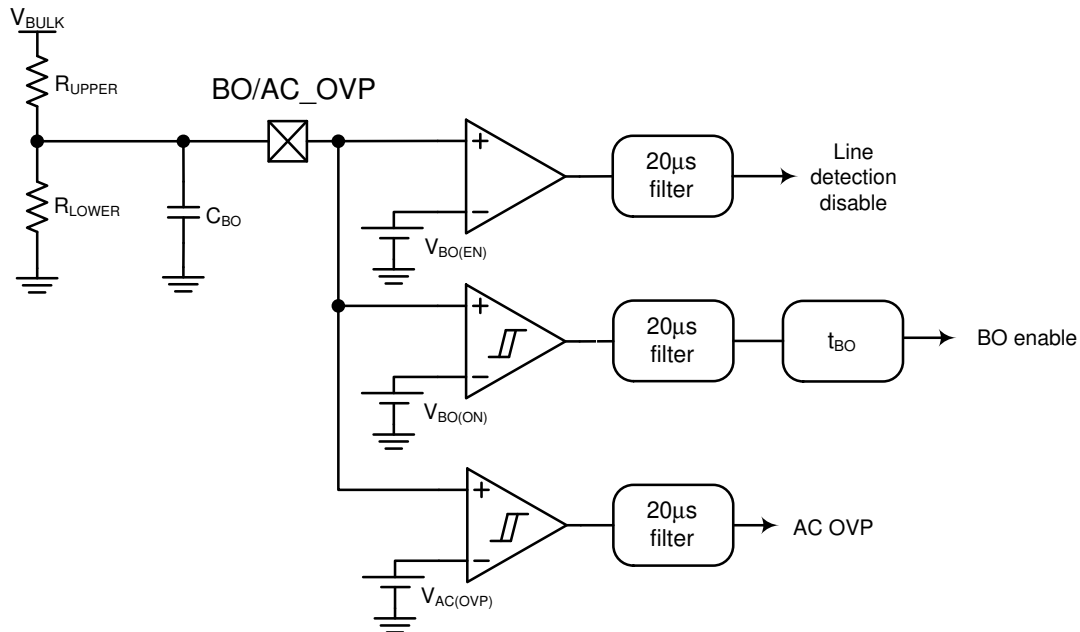


Figure 40. The Internal Brown-out Configuration

NCP1075A/B, NCP1076A/B, NCP1077A/B, NCP1079A/B

A resistive divider made of R_{UPPER} and R_{LOWER} , brings a portion of the HV rail on BO/AC_OVP pin. Below the $V_{BO(EN)} = 50\text{ mV}$ is the Brown-out function disabled, over the $V_{BO(EN)}$ Brown-out function is enable and against Line detection is inhibited. If voltage on BO/AC_OVP pin is

higher than $V_{BO(ON)}$, switcher starts pulsing. If voltage falls down under $V_{BO(OFF)}$ – level $V_{BO(ON)}$ minus $V_{BO(HYST)}$, the switcher waits 50 ms and then stops pulsing, depicted by Figure 41. Bulk voltage at which IC starts switching is set by resistive divider.

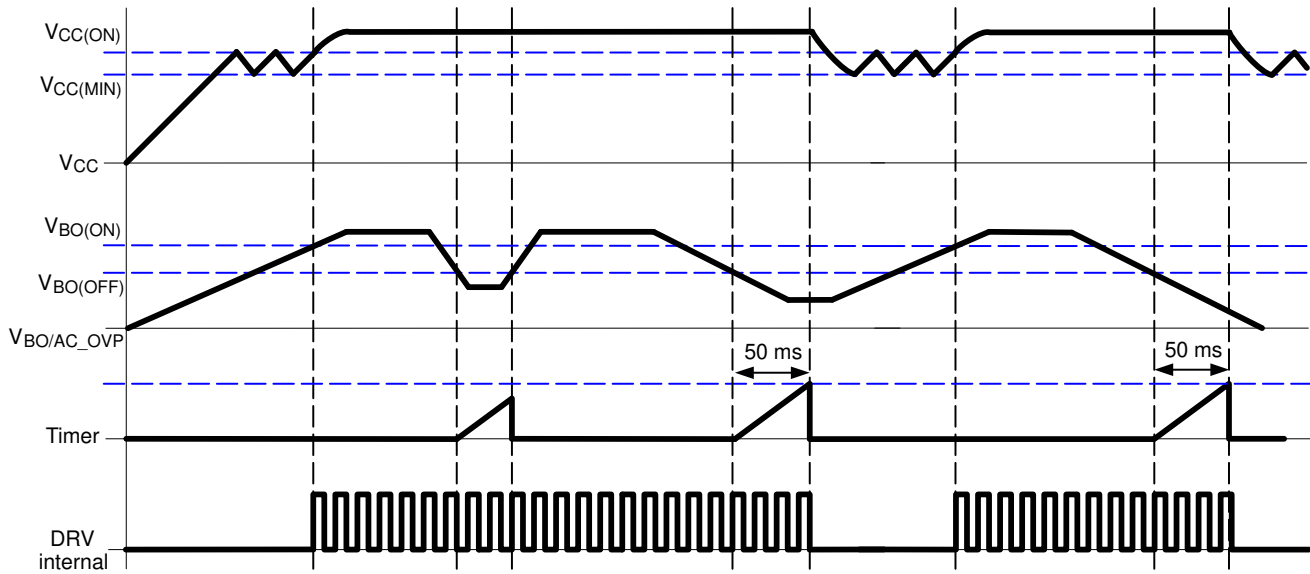


Figure 41. Brown-out Input Functionality with 50 ms Timer

NCP1075A/B, NCP1076A/B, NCP1077A/B, NCP1079A/B

The IC also includes over-voltage protection. If the voltage on BO/AC_OVP pin exceed $V_{ACOVP(ON)}$, the switcher immediately stops pulsing until the voltage on BO/AC_OVP pin drops under $V_{ACOVP(OFF)}$, depicted by Figure 42.

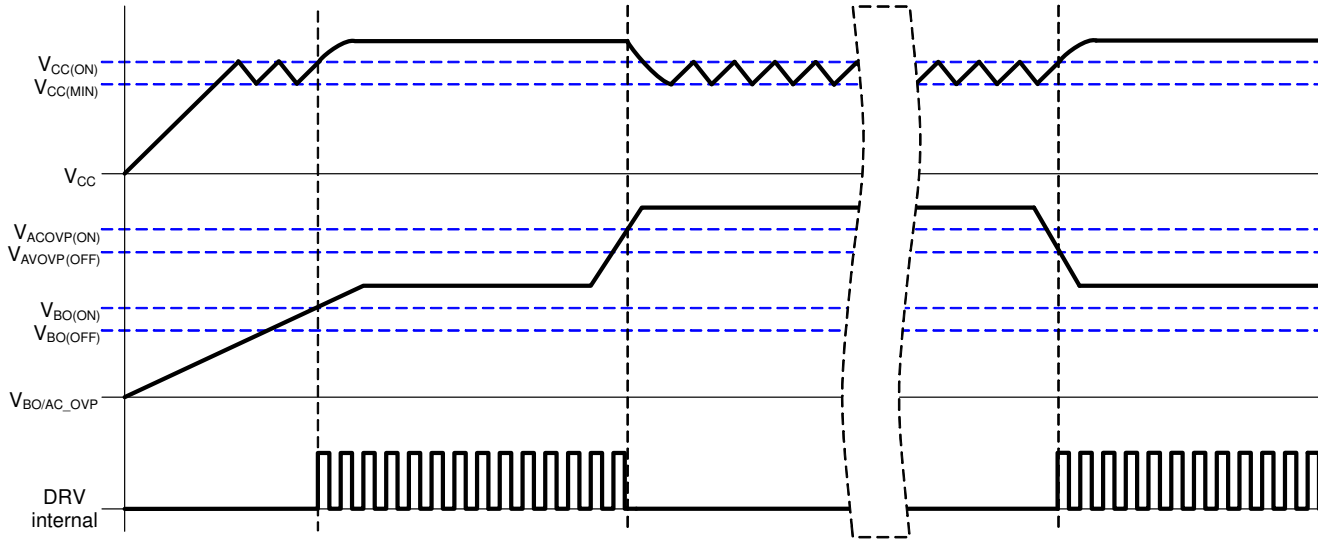


Figure 42. Brown-out Input Functionality with Ac Line OVP Function

Calculation of the resistive divider:

$$\frac{R_{LOWER}}{R_{UPPER}} = \frac{V_{BO(ON)}}{V_{BULK} - V_{BO(ON)}} \quad (\text{eq. 2})$$

If we decide to start pulsing at $V_{BULK(ON)} = 113 \text{ V dc}$ (80 V rms at ac mains):

$$\frac{R_{LOWER}}{R_{UPPER}} = \frac{V_{BO(ON)}}{V_{BULK(ON)} - V_{BO(ON)}} = \frac{0.8}{113 - 0.8} \approx 7.1 \text{ m}$$

We choose $R_{LOWER} = 100 \text{ k}\Omega$

$$R_{UPPER} = \frac{100 \cdot 10^3}{7.1 \cdot 10^{-3}} = 14 \text{ M}\Omega$$

Then power losses on resistive divider for worst case ($V_{BULK} = 409 \text{ V dc}$)

$$P = U \cdot I = \frac{U^2}{R} = \frac{U^2}{R_{UPPER} + R_{LOWER}} = \frac{409^2}{14 \cdot 10^6 + 100 \cdot 10^3} = 12 \text{ mW} \quad (\text{eq. 3})$$

For $V_{BULK(ON)} = 113 \text{ V dc}$ will be over-voltage protection (voltage when the switcher stops pulsing):

$$V_{BULK(OVP)} = V_{ACOVP(ON)} \cdot \frac{R_{LOWER} + R_{UPPER}}{R_{LOWER}} = V_{ACOVP(ON)} \cdot \frac{V_{BULK(ON)}}{V_{BO(ON)}} = 29 \cdot \frac{113}{0.8} = 409 \text{ Vdc} = 290 \text{ Vrms} \quad (\text{eq. 4})$$

NCP1075A/B, NCP1076A/B, NCP1077A/B, NCP1079A/B

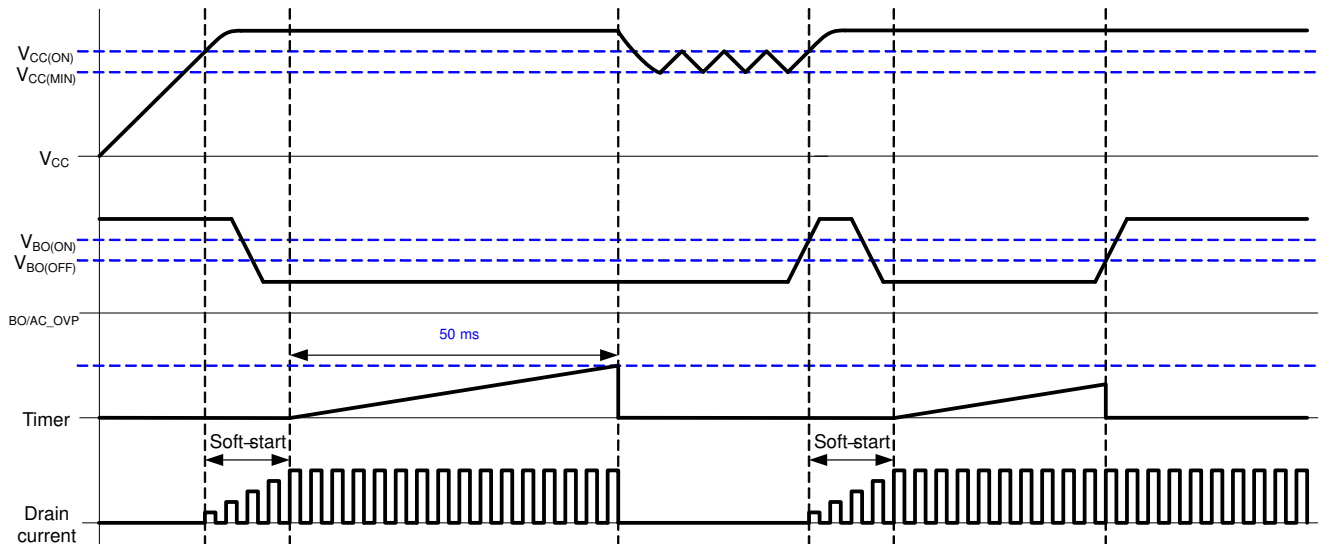


Figure 43. Brown-out Functionality in Soft-start

If voltage on VCC pin is higher than $V_{CC(ON)}$ and voltage on BO/AC_OVP pin is higher than $V_{BO(ON)}$ then IC starts pulsing, drain current is increasing for 10 ms (Soft-start). Brown-out is inhibited during Soft-start, when Soft-start ended, Brown-out checked if is voltage on BO/AC_OVP pin higher than $V_{BO(OFF)}$. If the voltage is lower, timer count 50 ms and if the voltage don't increase over $V_{BO(OFF)}$ then IC stops switching as one can see on Figure 43.

Frequency Foldback

The reduction of no-load standby power associated with the need for improving the efficiency, requires to change the traditional fixed-frequency type of operation. This device implements a switching frequency foldback when the feedback current passes above a certain level, I_{FBfold} , set

around $68 \mu A$. At this point, the oscillator enters frequency foldback and reduces its switching frequency.

The internal peak current set-point is following the feedback current information until its level reaches the minimal freezing level point of I_{freeze} . Below this value, the peak current set-point is frozen to 30% of the $I_{PK(0)}$. The only way to further reduce the transmitted power is to diminish the operating frequency down to f_{MIN} (27 kHz typically). This value is reached at a feedback current level of $I_{FBfold(END)}$ ($100 \mu A$ typically). Below this point, if the output power continues to decrease, the part enters skip cycle for the best noise-free performance in no-load conditions. Figures 44 and 45 depict the adopted scheme for the part.

NCP1075A/B, NCP1076A/B, NCP1077A/B, NCP1079A/B

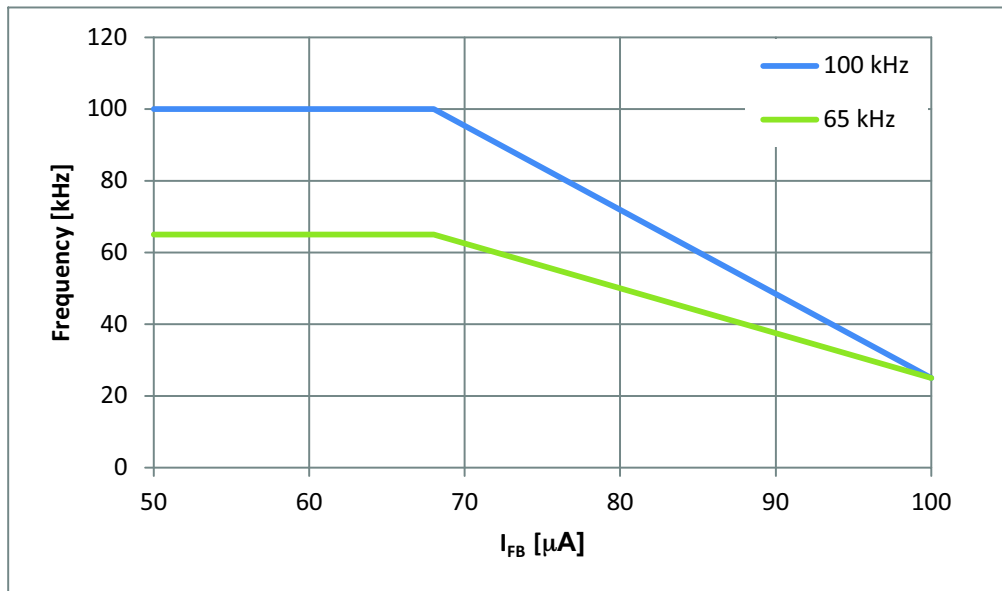


Figure 44. By Observing the Current on the FB pin, the Controller Reduces its Switching Frequency for an Improved Performance at Light Load

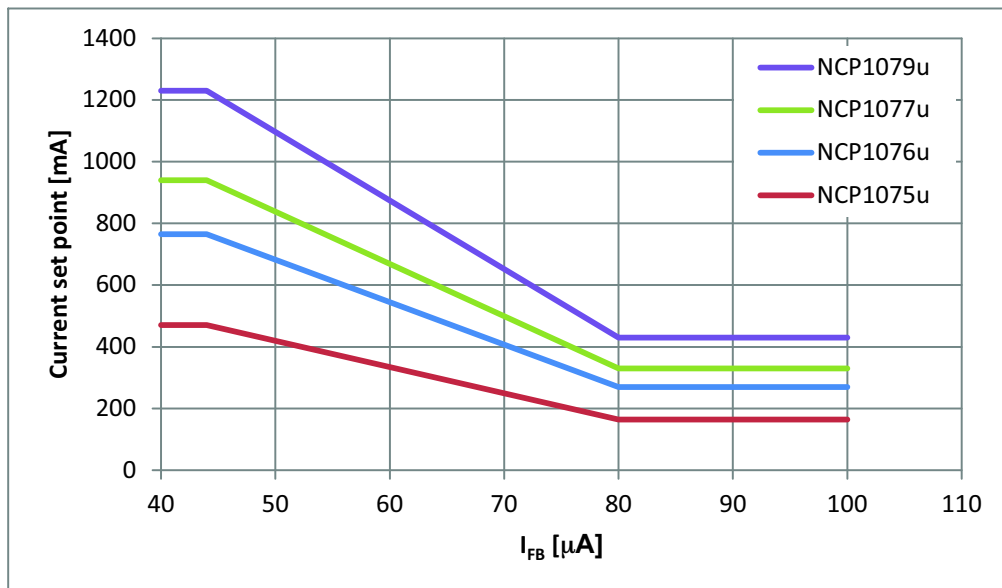


Figure 45. I_{PK} Set-point is Frozen at Lower Power Demand

Feedback and Skip

The FB pin operates linearly as the absolute value of feedback current (I_{FB}) is above $40 \mu A$. In this linear operating range, the dynamic resistance is $19.5 k\Omega$ typically

($R_{FB(UP)}$) and the effective pull up voltage is $3.3 V$ typically ($V_{FB(REF)}$). When I_{FB} is decreased, the FB voltage will increase to $3.3 V$.

NCP1075A/B, NCP1076A/B, NCP1077A/B, NCP1079A/B

Figure 46 depicts the skip mode block diagram. When the FB current information reaches $I_{FB(skip)}$, the internal clock to set the flip-flop is blanked and the internal consumption of the controller is decreased. The hysteresis of internal skip

comparator is minimized to lower the ripple of the auxiliary voltage for V_{CC} pin and V_{OUT} of power supply during skip mode. It eases the design of V_{CC} overload range.

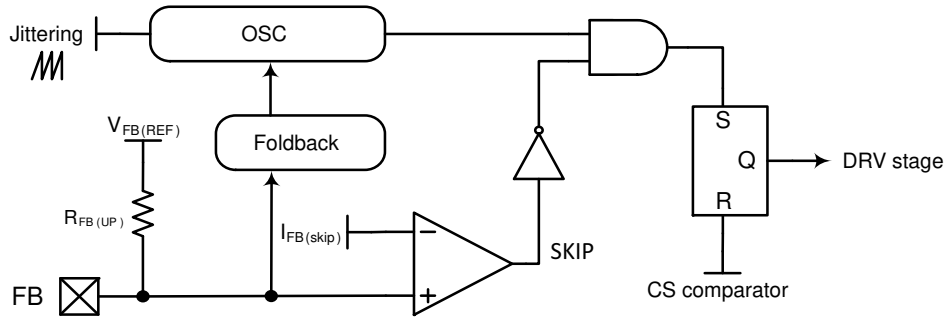


Figure 46. Skip Cycle Schematic

Over-power Protection

This function lets you limit the maximum dc output current regardless of the operating input voltage. For a correct operation, the BO/AC_OVP pin must be connected via a resistive divider to observe the bulk voltage.

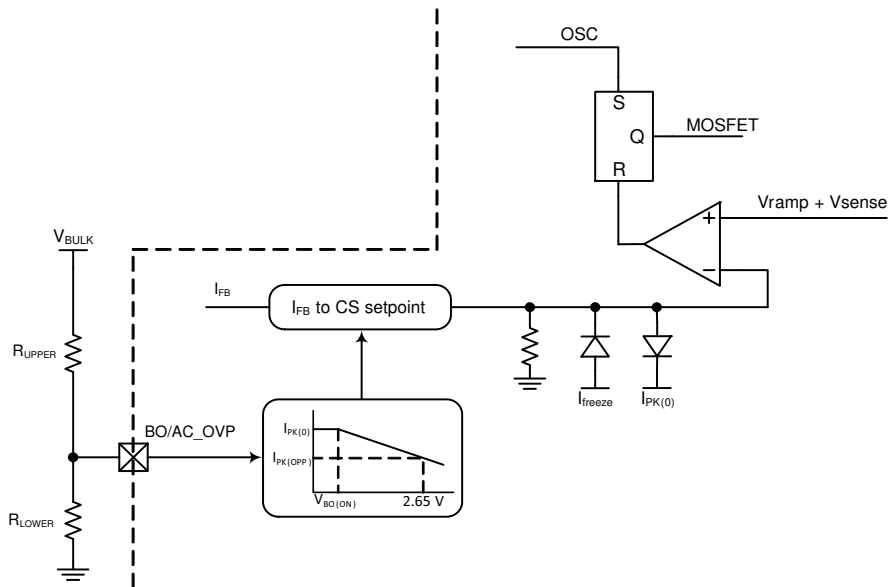


Figure 47. The OPP Circuitry Affects the Maximum Peak Current Set-point in Relationship to the Input Voltage.

NCP1075A/B, NCP1076A/B, NCP1077A/B, NCP1079A/B

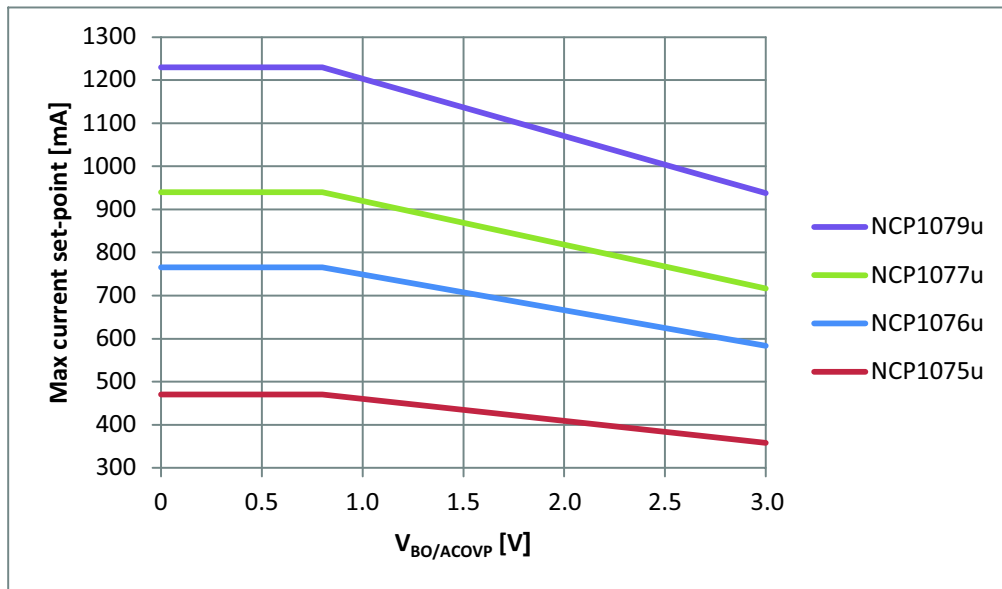


Figure 48. Current Set-point Dependence on BO/AC_OVP Pin Voltage

There are several known ways to implement Over-power Protection (OPP), all suffering from particular problems. These problems range from the added consumption burden on the converter or the skip-cycle disturbance brought by the current-sense offset. In this case is added consumption due to resistive divider (Equation 2).

Maximum peak current is reduced internally according to bulk voltage. When $V_{BO(OPP)}$ is maximum, the peak current set-point is reduced by 10%. Bulk voltage at which will be maximum current peak reduced by 20% (10% in NCP1075u):

$$V_{BULK(OPP)} = V_{BO(OPP)} \cdot \frac{V_{BULK(ON)}}{V_{BO(ON)}} = V_{BO(OPP)} \cdot \frac{R_{LOWER} + R_{UPPER}}{R_{LOWER}} = 2.65 \cdot \frac{100 \cdot 10^3 + 14 \cdot 10^6}{100 \cdot 10^3} = 375 \text{ Vdc} = 265 \text{ Vrms} \quad (\text{eq. 5})$$