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NCP1239

Low-Standby High Performance PWM Controller

Housed in SO−16 the NCP1239 represents a major leap toward ultra−compact Switch Mode Power Supplies specifically tailored for medium to high power off−line applications, e.g. notebook adapters. The NCP1239 offers everything needed to build a rugged and efficient power supply, including a dedicated event management to drive a Power Factor Correction (PFC) front−end circuitry. The circuit disables the front−end PFC stage while still in fault or standby conditions by interrupting the PFC controller powering for improved no−load consumption figures. As soon as normal operating mode recovers, the NCP1239 feeds back the PFC that wakes−up.

When power demand is low, the IC automatically enters the so−called skip−cycle mode and provides excellent efficiency at light loads. Because this occurs at a user adjustable low peak current, no acoustic noise takes place.

Features

- Current−Mode Operation with Internal Ramp Compensation
- Internal High−Voltage Current Source for loss−less Startup
- Adjustable Skip−Cycle Capability
- Selectable Soft−Start Period
- Internal Frequency Dithering for Improved EMI Signature
- Go−to−Standby Signal for PFC Front−Stage
- Large V_{CC} Operation from 12.2 V to 36 V
- 500 mV Overcurrent Limit
- 500 mA/−800 mA Peak Current Capability
- 5 V/10 mA Pinned−out Reference Voltage
- Adjustable Switching Frequency up to 250 kHz.
- Overload Protection Independent of the Auxiliary V_{CC}
- Adjustable Over Power Compensation (NCP1239F)
- Programmable Maximum Duty Cycle (NCP1239V)
- Pb−Free Packages are Available*

Typical Applications

- High Power AC/DC Adapters for Notebooks etc.
- Offline Battery Chargers
- Telecom and PC Power Supplies
- Flyback Applications (NCP1239F) and Forward Applications (NCP1239V)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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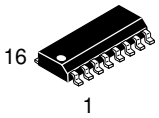
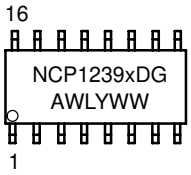


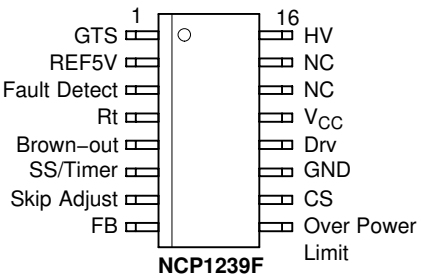
SO−16
FD or VD SUFFIX
CASE 751B

MARKING DIAGRAM

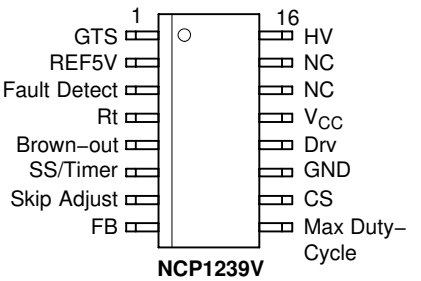


NCP1239xD	= Device Code
x	= F or V
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



NCP1239F



NCP1239V

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

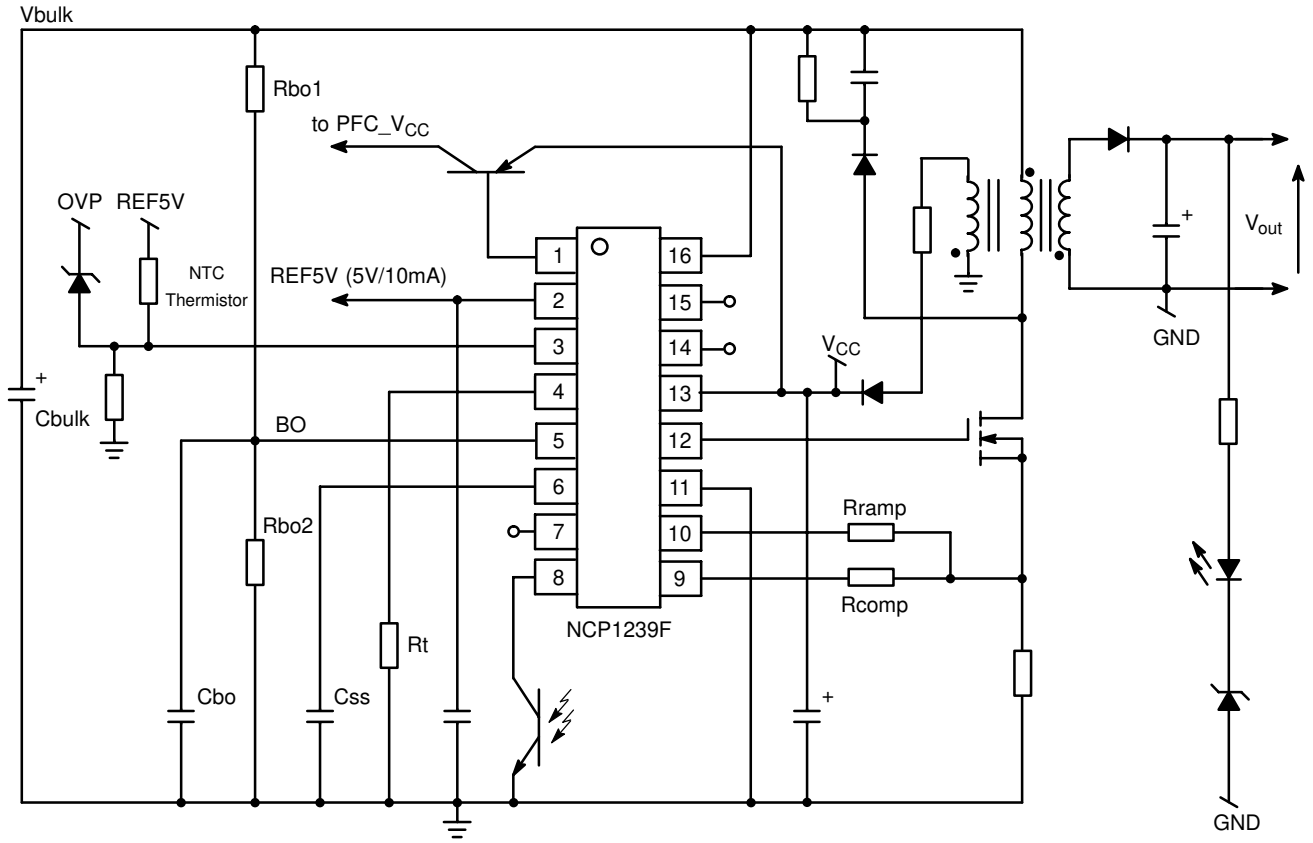


Figure 1. NCP1239F Typical Application Example

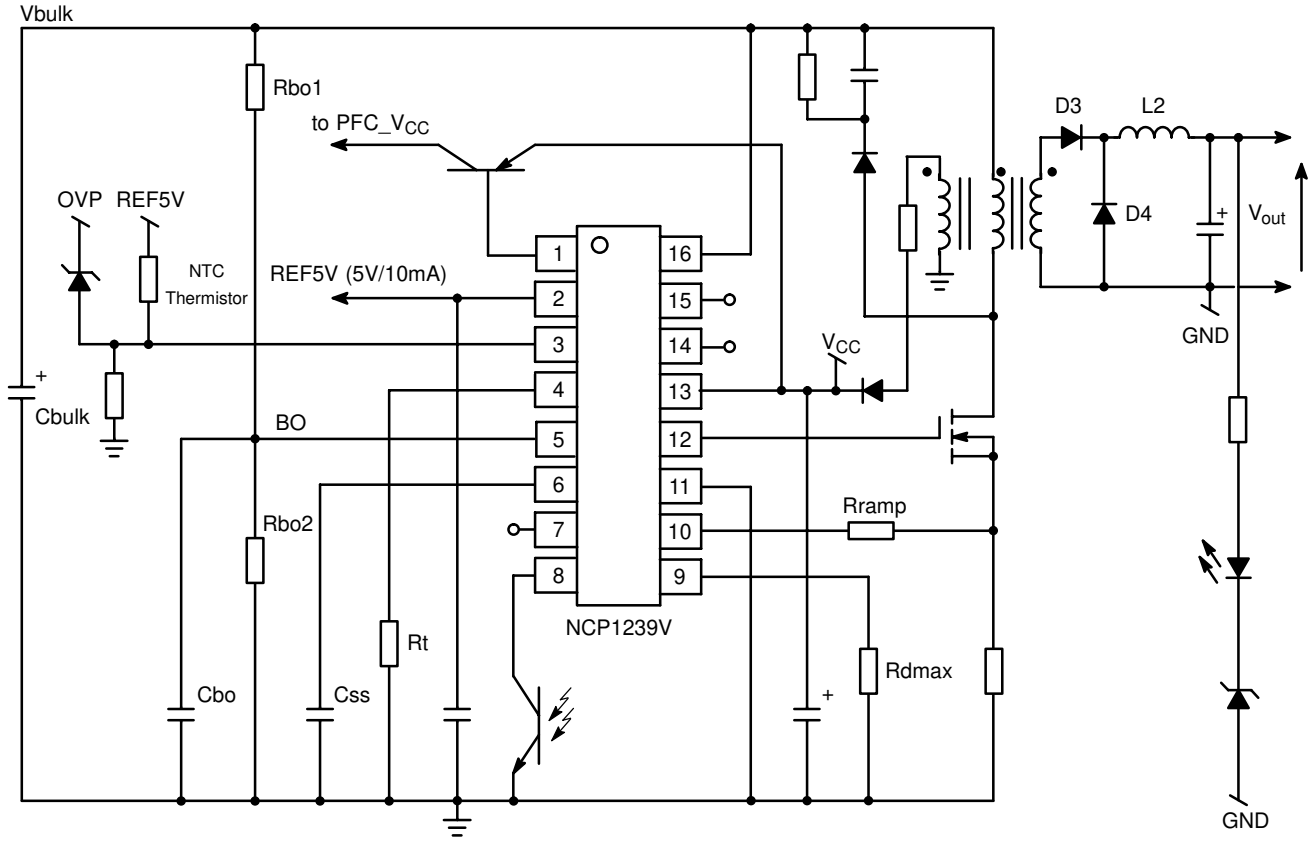


Figure 2. NCP1239V Typical Application Example

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	36	V
Pins 1 to 10 (except Vref Pin) Maximum Voltage		–0.3, +10	V
Maximum Voltage on Pin 16 (HV)		500	V
Thermal Resistance, Junction–to–Air, SOIC Version	$R_{\theta JA}$	145	°C/W
Maximum Junction Temperature	TJ_{MAX}	150	°C
Storage Temperature Range		–60 to +150	°C
ESD Capability, HBM Model (All Pins except HV)		2	kV
ESD Capability Machine Model (All Pins except V_{CC}) Machine Model (V_{CC} Pin)		200 160	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = 0°C to +125°C, V_{pin16} = 48 V, V_{CC} = 20 V unless otherwise noted.)

Symbol	Rating	Pin	Min	Typ	Max	Unit
Supply Section						
V_{CCON}	Turn–on Threshold Level, V_{CC} Going up	13	15.5	16.4	17.5	V
V_{CCOFF}	Minimum Operating Voltage after Turn–on	13	10.5	11.2	12.2	V
HYST1	Difference (V_{CCON} – V_{CCOFF})	13	4.5	5.1	–	V
$V_{CCLATCH}$	V_{CC} Decreasing Level at which the Latch–off Phase ends	13	6.5	6.9	7.2	V
$V_{CCRESET}$	V_{CC} Level at which the Internal Logic gets reset	13	–	4.0	–	V
I_{CC1}	Internal IC Consumption, no output load on Pin 12 (@I_{Rt} = 20 μA) NCP1239F NCP1239V	13	 – –	 2.1 2.6	 3.0 4.0	mA
I_{CC2a}	Internal IC Consumption, 1 nF output load on Pin 12 NCP1239F (65 kHz) NCP1239V (118 kHz)	13	 – –	 3.1 4.2	 3.8 6.5	mA
I_{CC2b}	Internal IC Consumption, 1 nF output load on Pin 12 NCP1239F (100 kHz) NCP1239V (182 kHz)	13	 – –	 3.9 5.5	 5.0 8.5	mA
I_{CC2c}	Internal IC Consumption, 1 nF output load on Pin 12 NCP1239F (130 kHz) NCP1239V (236 kHz)	13	 – –	 4.6 6.7	 5.9 9.6	mA
I_{CC3}	Internal IC Consumption, latchoff phase (NCP1239F and NCP1239V)	13	–	 0.40	 0.75	mA
Internal Startup Current Source						
I_{C1_hv}	High–Voltage Current Source (sunk by Pin 16), V_{CC} = 10 V	16	2.0	4.0	5.3	mA
I_{C1_VCC}	Startup Charge Current flowing out of the V_{CC} Pin, V_{CC}=10 V	13	1.8	3.6	4.5	mA
I_{C2}	High–Voltage Current Source, V_{CC} = 0	16	–	4.2	–	mA
5 V Reference Voltage (REF5V)						
REF5V	Reference Voltage @ No load on Pin 2 @ I_{pin2} = 5 mA	2	 4.7 4.6	 5.0 4.9	 5.2 5.1	V
Iref	Current Capability	2	5.0	10	–	mA

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = 0°C to +125°C, V_{pin16} = 48 V, V_{CC} = 20 V unless otherwise noted.)

Symbol	Rating	Pin	Min	Typ	Max	Unit
Drive Output						
Vcl	Output Voltage Positive Clamp	12	11.5	13.6	16	V
T_{rise}	Output Voltage Rise−Time @ CL = 1 nF, 10−90% of output signal	12	–	40	–	ns
T_{fall}	Output Voltage Fall−Time @ CL = 1 nF, 10−90% of output signal	12	–	25	–	ns
V_{source}	High State Voltage Drop @ I_{pin12} = 3 mA and V_{CC} = 12 V	12	–	2.5	3.3	V
I_{source}	Source Current Capability (@ V_{pin12} = 0 V)	12	–	500	–	mA
R_{OL}	Sink Resistance @ V_{pin12} =1 V	12	–	3.8	7.5	Ω
I_{sink}	Sink Current Capability (@ V_{pin12} = 10 V)	12	–	800	–	mA
Oscillator						
fsw	Recommended Switching Frequency Range	12	25	–	250	kHz
Vosc	Pin 4 Voltage @ Rt = 100 kΩ	4	–	1.6	–	V
Kosc	Product (Switching Frequency times the Rt Pin 4 resistance) (Note 1) @ 65 kHz and 130 kHz (NCP1239F) @ 118 kHz and 236 kHz (NCP1239V)		 6050 11000	 6500 11800	 6950 12600	kHz*kΩ
Δfsw	Internal Modulation Swing, in percentage of fsw		–	±3.5	–	%
Dmax	Maximum Duty−Cycle		75.5	80.0	83.0	%
Current Limitation						
I_{Limit}	Maximum Internal Set−Point	10	0.84	0.90	0.95	V
T_{DEL_CS}	Propagation Delay from V_{pin10} > I_{Limit} to gate turned off (Pin 12 loaded by 1 nF)	10	–	130	220	ns
$T_{LEB-65kHz}$	Leading Edge Blanking Duration (Pins 9 and 10) @ 65 kHz (NCP1239F)	9, 10	–	420	–	ns
$T_{LEB-130kHz}$	Leading Edge Blanking Duration (Pins 9 and 10) @ 130 kHz (NCP1239F)	9, 10	–	230	–	ns
$T_{LEB-118kHz}$	Leading Edge Blanking Duration (Pin 10) @ 118 kHz (NCP1239V)	10	–	320	–	ns
$T_{LEB-236kHz}$	Leading Edge Blanking Duration (Pin 10) @ 236 kHz (NCP1239V)	10	–	170	–	ns
Over Power Limit (NCP1239F)						
I_{ocp}	Internal Current Source of the Over Power Limit Pin @ 1 V on Pin 5 and V_{pin9} = 0.5 V @ 2 V on Pin 5 and V_{pin9} = 0.5 V	9	 60 120	 80 160	 100 185	μA
V_{opl}	Over Power Limitation Threshold @ T_J = 25°C @ T_J = 0°C to 125°C	9	 0.48 0.47	 0.50 0.50	 0.52 0.52	V
T_{DEL_OCP}	Propagation Delay from V_{pin9} > V_{opl} to gate turned off (Pin 12 loaded by 1 nF)	9	–	130	220	ns
Maximum Duty−Cycle (Dmax) Control (NCP1239V)						
I_{Dmax}	Pin 9 Current Source @ V_{pin9} = 1.0 V and V_{pin9} = 2.0 V	9	46	55	63	μA
D_{max}	Maximum Duty Cycle @ 118 kHz and V_{pin9} = 1.0 V	9	20	24	29	%
K_{Dmax}	Dmax Coefficient @ 118 kHz and V_{pin9} = 1.0 V (Note 2)	9	1.10	1.30	1.53	%/kΩ

1. The nominal switching frequency fsw equals: fsw = K_{OSC}/Rt. The implemented jittering makes the switching frequency continuously vary around this nominal value (±3.5% variation).
2. K_{Dmax} is the proportionality coefficient that links the maximum duty−cycle to the Pin 9 resistor: Dmax = K_{Dmax}*R_{pin9}. K_{Dmax} is defined in the “Maximum Duty−Cycle Limitation” section of the operating description.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = 0°C to +125°C, V_{pin16} = 48 V, V_{CC} = 20 V unless otherwise noted.)

Symbol	Rating	Pin	Min	Typ	Max	Unit
Soft−Start and Timer						
I_{ch}	Soft−Start or Jittering charge current @ V_{pin6} = 2.4 V	6	60	95	110	μA
I_{disch}	Jittering Discharge Current @ V_{pin6} = 2.4 V	6	77	107	137	μA
V_{jitter}	Jittering Saw−Tooth Lower Threshold	6	1.67	1.80	1.89	V
$V_{jitter}H$	Jittering Saw−Tooth Upper Threshold	6	2.85	3.00	3.20	V
$V_{timer}L$	Timer Peak Threshold	6	4.0	4.3	4.6	V
I_{timerC}	Timer Charge Current @ V_{pin6} = 3.5 V and Pin 8 open	6	3.9	5.2	6.4	μA
I_{timerD}	Timer Discharge Current @ V_{pin6} = 3.5 V and Pin 8 open	6	–	400	–	μA
Feedback Section						
Rup	Internal Pullup Resistor	8	–	20	–	kΩ
Ifb	Source Current @ V_{pin8} = 0.5 V	8	–	200	–	μA
Iratio	Pin 8 to current Setpoint division ratio	–	–	3.0	–	–
Internal Ramp Compensation						
R_{ramp}	Internal Resistor	10	–	32	–	kΩ
V_{ramp}	Internal Saw−Tooth Amplitude	10	–	3.2	–	V
Skipping Mode and Standby Management						
Rgts	Pin 1 output impedance in standby state (Pin 8 grounded, V_{pin6} > 4.5 V) @ V_{CC} = 12.5 V	1	4.0	8.0	18	kΩ
Igts	Sink Current Source in Normal Mode @ V_{pin8} = 2 V, Pin 7 open @ V_{CC} – V_{pin1}=0.7 V	1	0.6	1.0	–	mA
FB−skip	Default Feedback Level for Skip−Cycle Operation and Standby Detection	7	380	430	480	mV
FB_stby−out	Default Feedback Level to Leave Standby	7	650	740	810	mV
$V_{stby-out}/V_{skip}$	Ratio leave standby Setpoint to skip−cycle Setpoint		1.5	1.7	1.9	–
R_{pin7}	Internal Pin 7 Impedance	7	–	110	–	kΩ
	Pin 7 to Skipping Setpoint ratio		–	3.0	–	–
Brown−Out Detection						
BO_{thH}	Brown−Out Detection Upper Threshold	5	0.45	0.50	0.55	V
BO_{thL}	Brown−Out Detection Low Threshold	5	0.20	0.24	0.28	V
BO_{hyst}	Brown−Out Hysteresis	5	0.20	0.26	0.30	V
Protections						
TSD	Thermal Shutdown: Thermal Shutdown Threshold Hysteresis			 140 30		°C
Vfault	Fault Detection Threshold	3	2.2	2.4	2.6	V

ORDERING INFORMATION

Device	Package	Shipping†
NCP1239FDR2	SOIC−16	2500 / Tape & Reel
NCP1239FDR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
NCP1239VDR2	SOIC−16	2500 / Tape & Reel
NCP1239VDR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Pin Description
1	GTS	Shuts the PFC down in standby	The standby detection block changes Pin 1 state in accordance to the mode (standby or normal mode). Pin1 is designed to drive an external pnp transistor that connects or disconnects the NCP1239's V_{CC} to the PFC's.
2	REF5V	A 5V reference voltage	This pin helps to internally bias the controller but can also be used to power surrounding logic gates for any purposes. The typical output current is 10 mA. This voltage source is disabled during the circuit startup and latched−off phases. A 100 nF filtering capacitor must be placed between Pin 2 and ground.
3	Fault Detect	Enables to permanently shutdown the part	If the Pin 3 voltage exceeds 2.4 V, the circuit is permanently shut down. This pin can be used to monitor the voltage across a thermistor in order to protect the application from excessive heating and/or to detect an overvoltage condition.
4	Rt	Timing resistor	Pin 4 resistor allows a precise frequency programming. The circuit is optimized to operate between 50 kHz and 150 kHz (NCP1239F) and between 100 kHz and 250 kHz (NCP1239V).
5	Brown−Out	Brown−Out	This pin receives a portion of the bulk capacitor to authorize operation above a certain level of mains only. It also serves to elaborate an offset voltage on Pin 9 used for Over Power Compensation.
6	SS/Timer	Performs soft−start and fault timeout	During Power on and fault conditions, the capacitor connected to this pin ensures a soft−start period. When a fault is detected, this pin is internally brought high by a current source. If 4.3 V are reached, the fault is confirmed and the circuit enters an auto−recovery burst mode, otherwise the pin goes back to a lower value and oscillates to perform frequency jittering.
7	Skip Adjust	Adjust skip level	By adjusting the skip−cycle level, it is possible to fight against noisy transformers and modify the standby detection thresholds. Keep Pin 7 open to operate with the default levels (skip threshold setpoint: 140 mV, normal mode recovery setpoint: 250 mV).
8	FB	Feedback signal	An opto−coupler collector pulls this pin low to regulate
9	Over Power Limit (NCP1239F)	Enables a precise peak current clamp and then an accurate Over Power Detection	This pin delivers a current proportional to V_{pin5}, an image of the high voltage rail. Inserting a resistor between Pin 9 and the current sense resistor, an offset proportional to the input voltage is built. Such offset compensates the circuit and power switch propagation delays for an accurate power limitation in the whole input voltage range.
9	Max Duty−Cycle (NCP1239V)	Enables to precisely clamp the maximum duty−cycle.	This terminal sources a constant current. Connect a resistor between Pin 9 and Ground to select the maximum duty−cycle.
10	CS	The current sense input	This pin receives the primary current information via a sense element. By inserting a resistor in series with this pin, it becomes possible to introduce ramp compensation.
11	Ground	The IC ground	–
12	Drv	Drives the MOSFET	By offering up to +500 mA/−800 mA peak, this pin lets you drive large Qg MOSFET's. It is clamped to 16 V maximum not to exceed the maximum gate−source voltage of most power MOSFET's.
13	V_{CC}	Supplies the controller	This pin accepts up to 36 V from an auxiliary winding.
14	NC	–	Creepage distance.
15	NC	–	Creepage distance.
16	HV	The high−voltage startup	This pin connects to the bulk capacitor to generate the startup current.

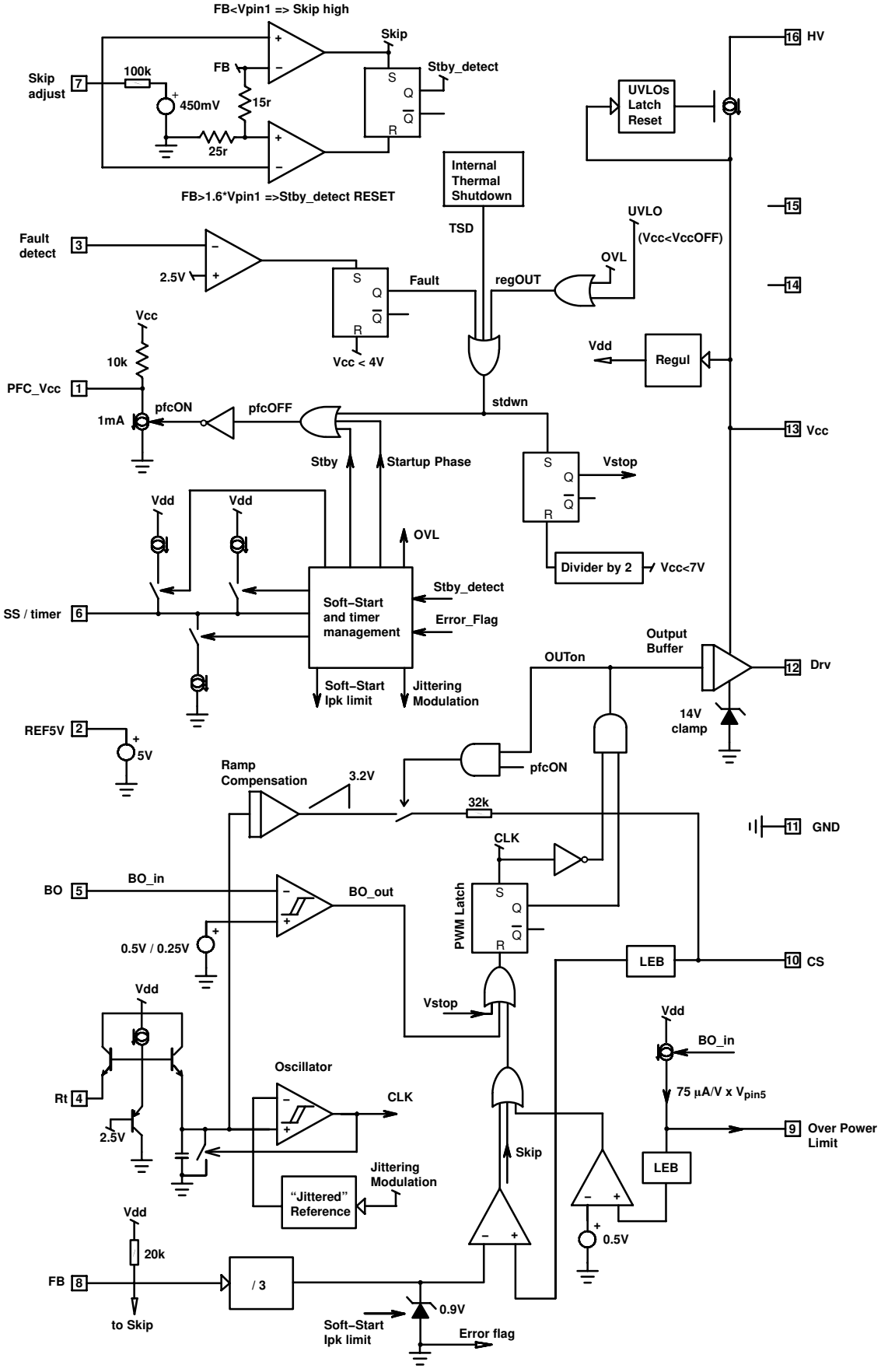


Figure 3. NCP1239F Internal Circuit Architecture

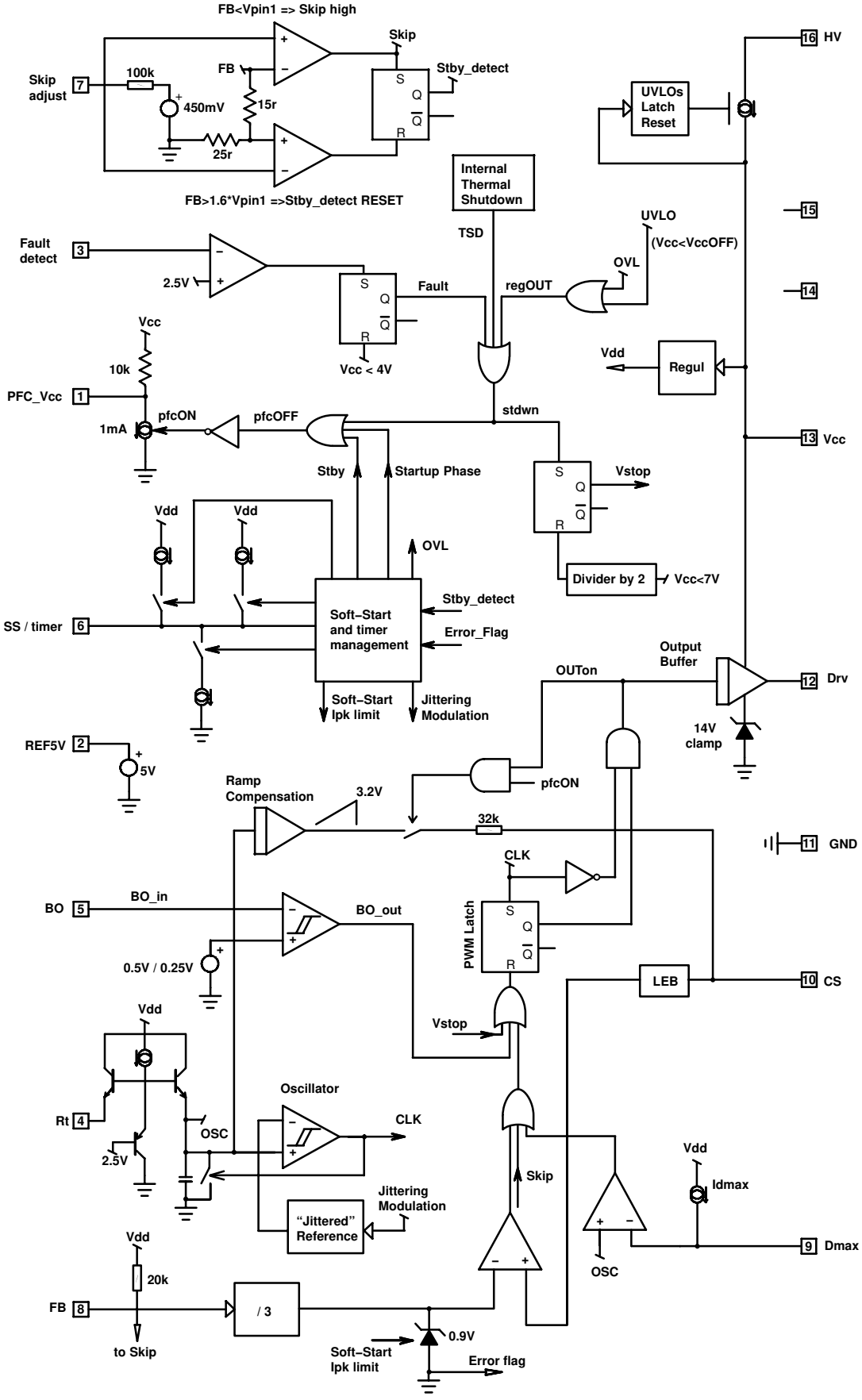


Figure 4. NCP1239V Internal Circuit Architecture

TYPICAL PERFORMANCE CHARACTERISTICS

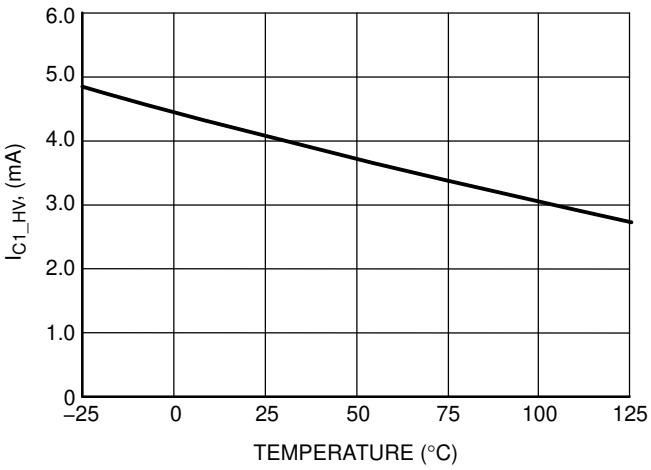


Figure 5. High Voltage Current Source vs. Temperature @ V_{CC} = 10 V

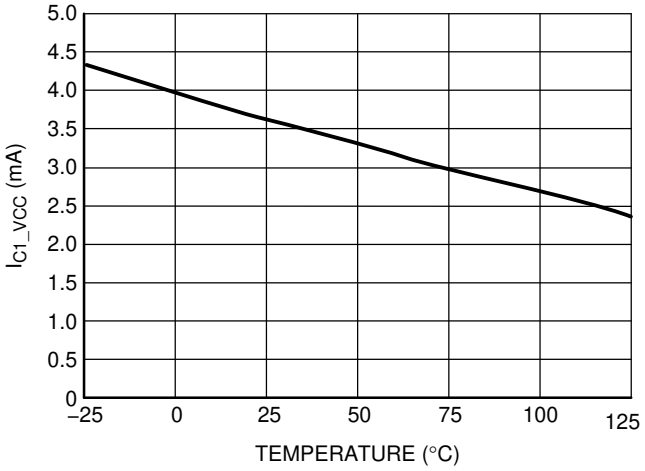


Figure 6. Startup Current Sourced by V_{CC} Pin vs. Temperature @ V_{CC} = 10 V

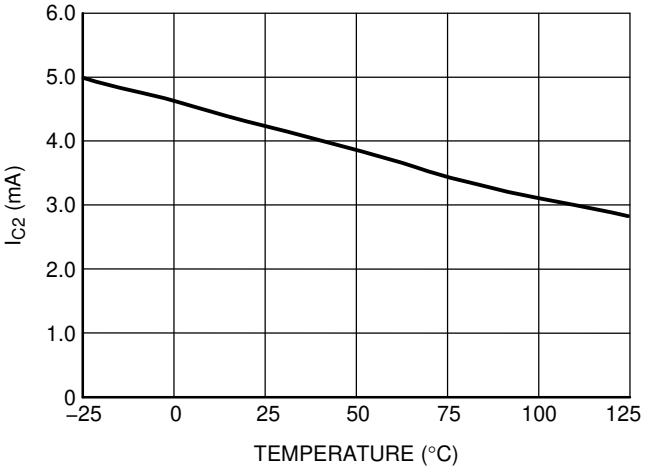


Figure 7. High Voltage Current Source vs. Temperature @ V_{CC} = 0 V

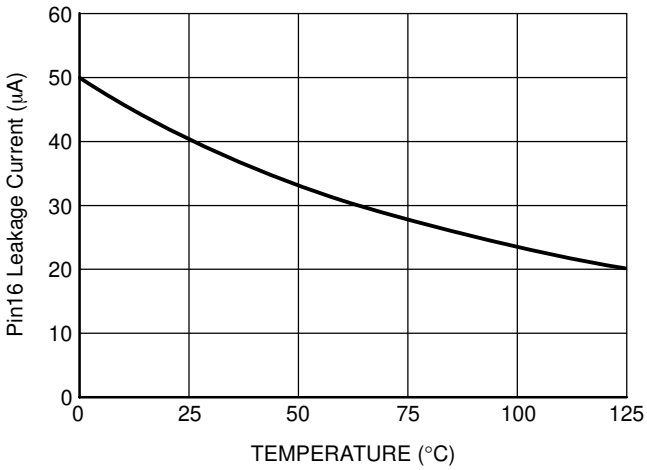


Figure 8. High Voltage Pin Leakage Current vs. Temperature

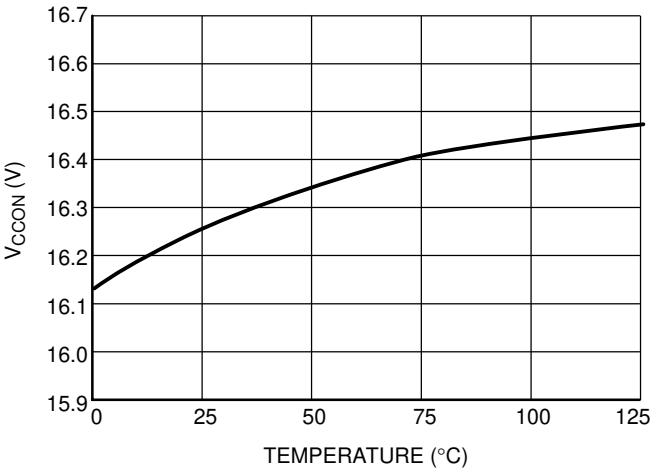


Figure 9. V_{CC} Startup Threshold vs. Temperature

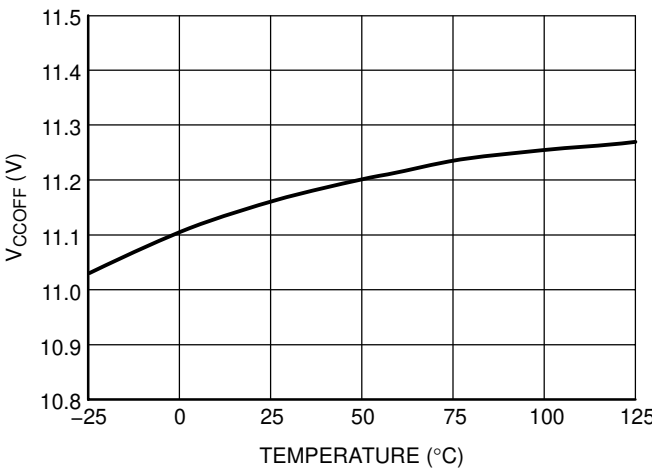


Figure 10. V_{CC} Turn–Off Threshold vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

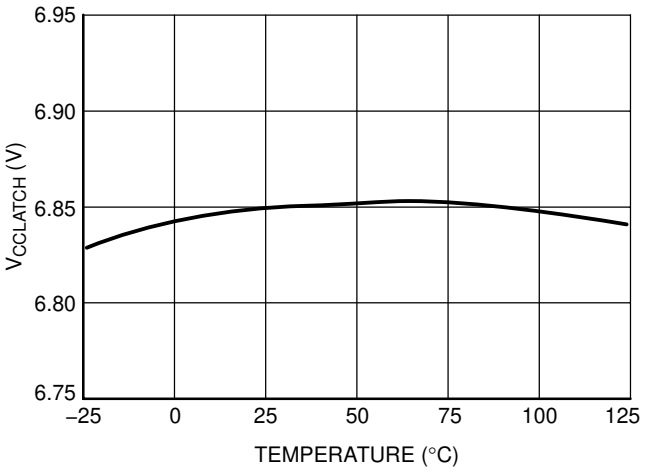


Figure 11. V_{CC} Latched–Off vs. Temperature

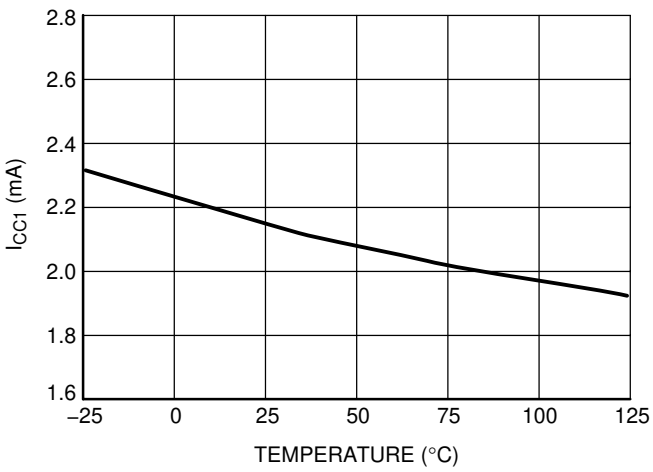


Figure 12. No Load Circuit Consumption vs. Temperature

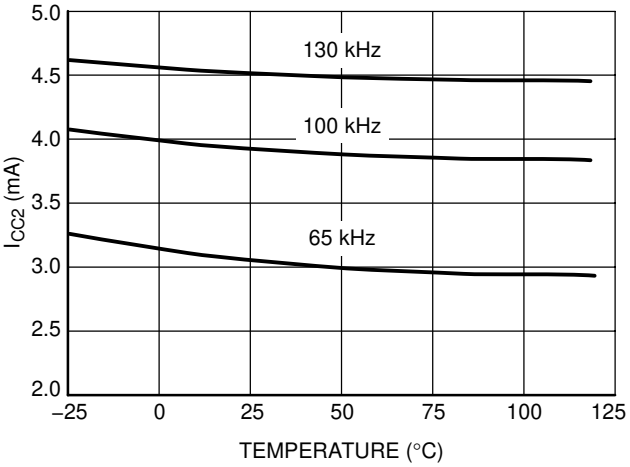


Figure 13. NCP1239F Circuit Consumption (1 nF on driver Pin 12) vs. Temperature

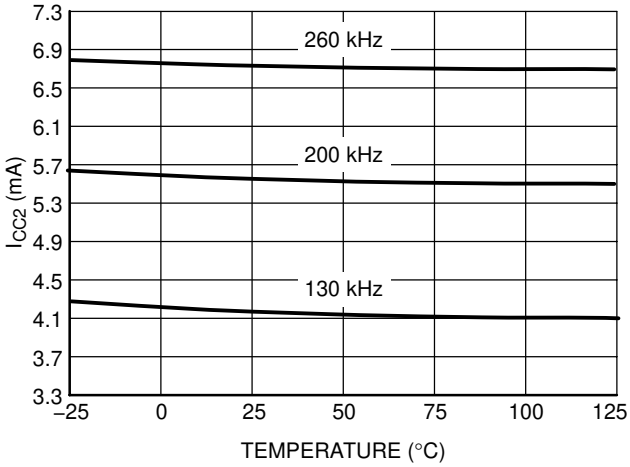


Figure 14. NCP1239V Circuit Consumption (1 nF on driver Pin 12) vs. Temperature

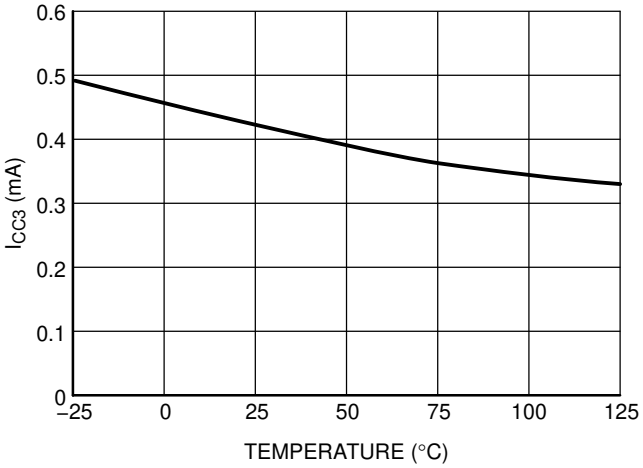


Figure 15. Latched–Off Mode Consumption vs. Temperature

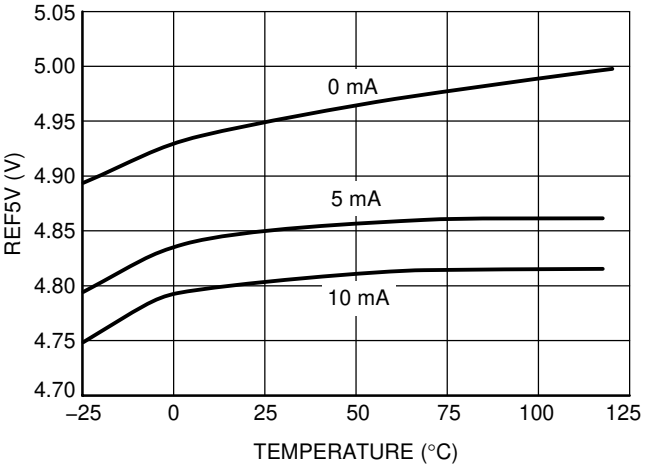


Figure 16. REF5V Voltage Source vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

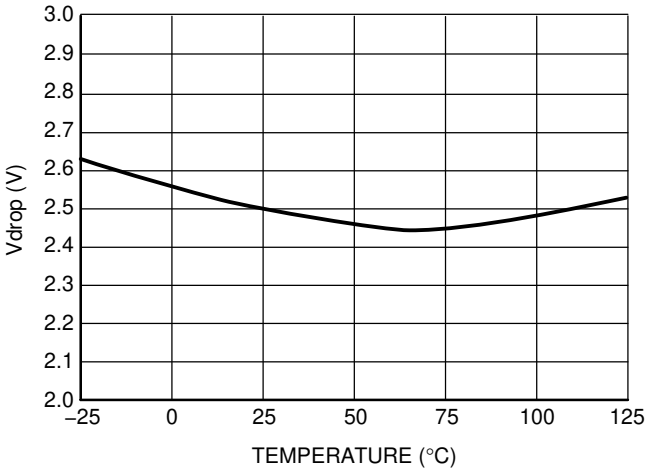


Figure 17. Driver High State Voltage Drop vs. Temperature

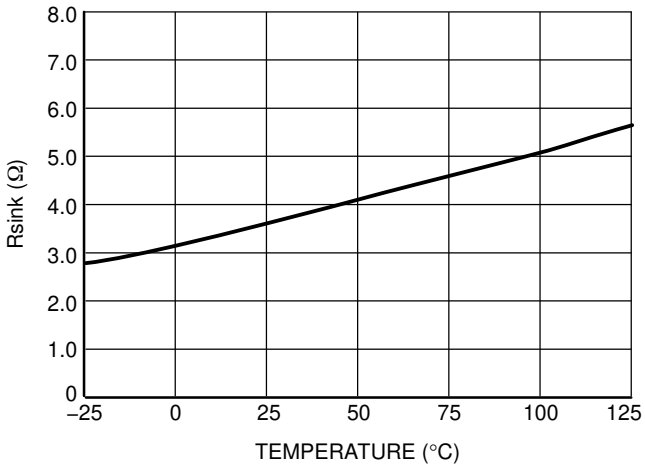


Figure 18. Driver Sink Resistance vs. Temperature

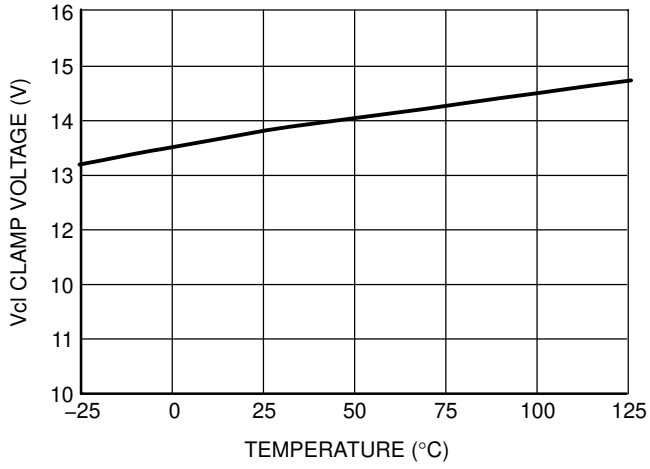


Figure 19. Driver Voltage Clamp vs. Temperature

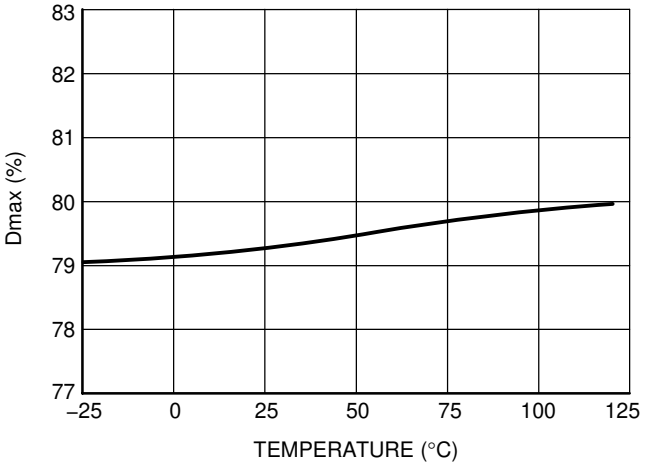


Figure 20. Maximum Duty Cycle vs. Temperature (NCP1239F)

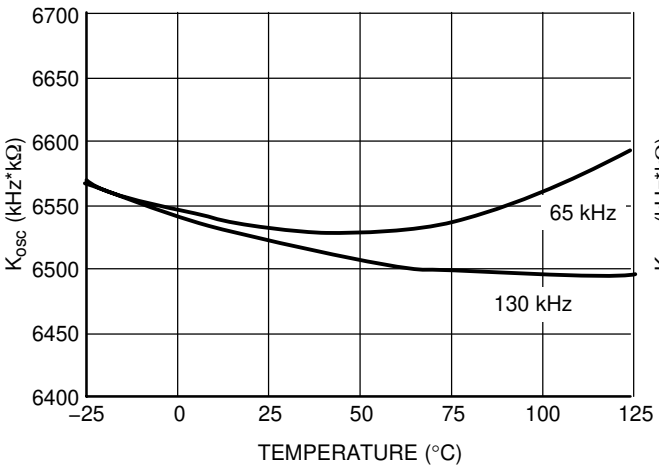


Figure 21. Oscillator K_{osc} Parameter vs. Temperature (K_{osc} = fsw * R_{pin4}) (NCP1239F)

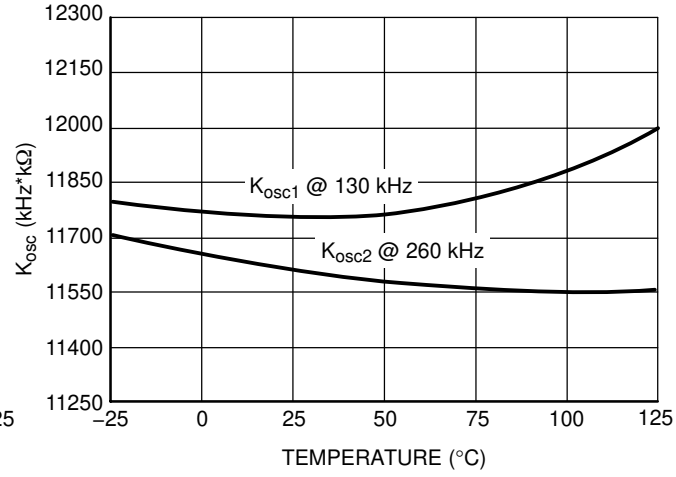


Figure 22. Oscillator K_{osc} Parameter vs. Temperature (K_{osc} = fsw * R_{pin4}) (NCP1239V)

TYPICAL PERFORMANCE CHARACTERISTICS

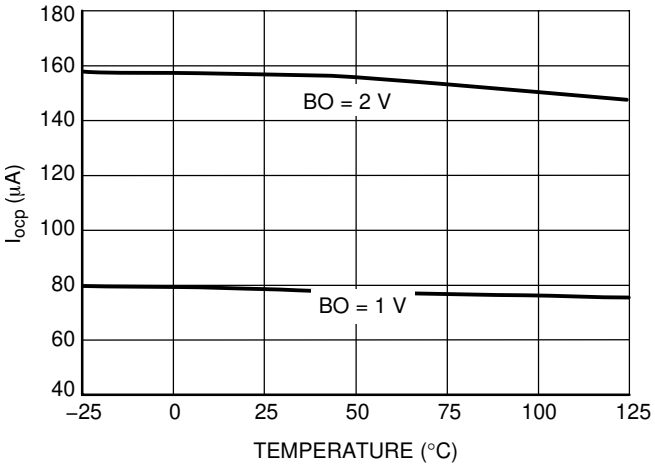


Figure 23. Pin 9 Current vs. Temperature (@ V_{pin9} = 0.5 V) (NCP1239F)

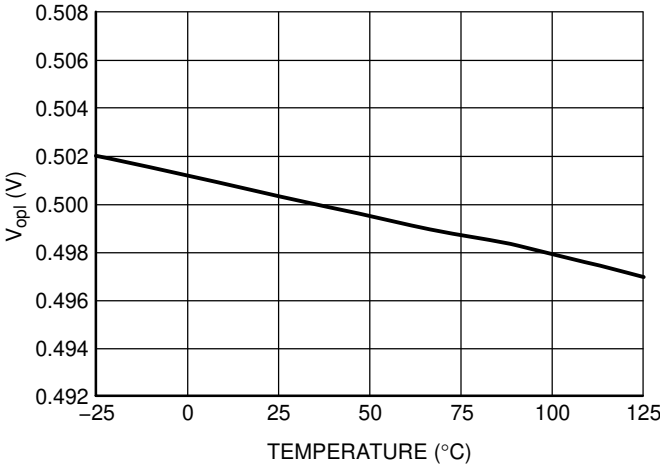


Figure 24. Over Power Limitation Threshold vs. Temperature (NCP1239F)

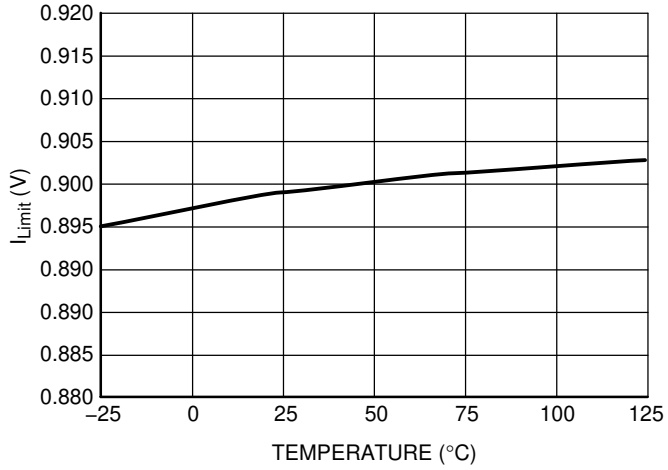


Figure 25. Maximum Current Setpoint vs. Temperature

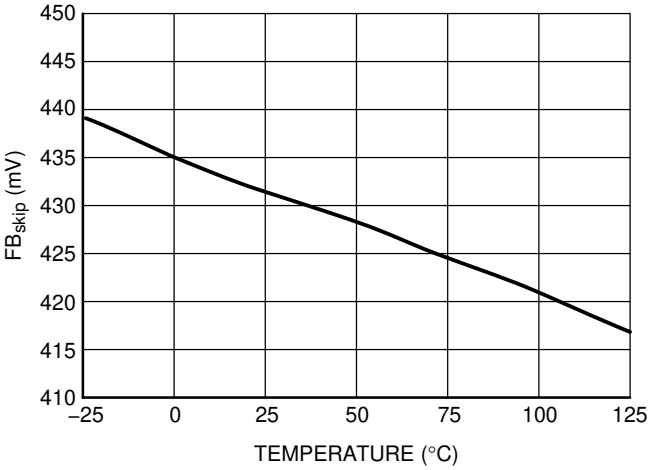


Figure 26. Default Feedback Threshold for Standby Detection vs. Temperature

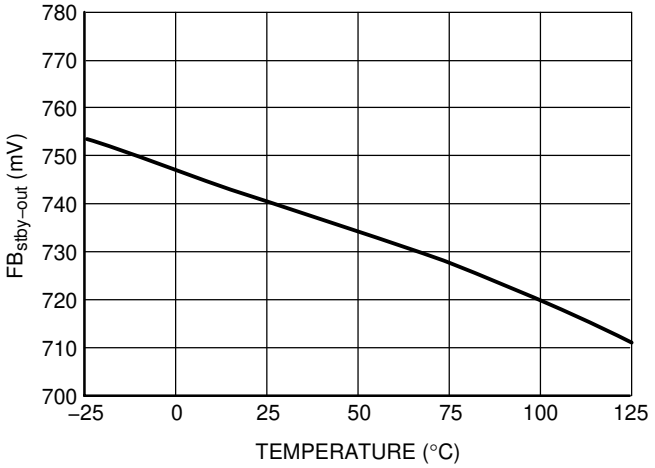


Figure 27. Default Feedback Level for Normal Operation Recovery

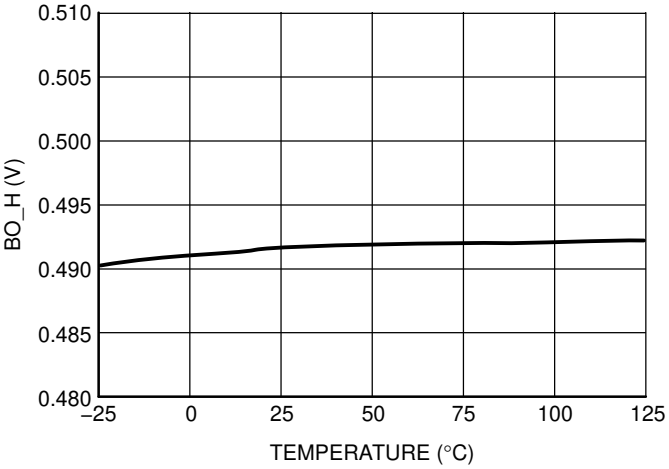


Figure 28. Brown–Out Upper Threshold vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

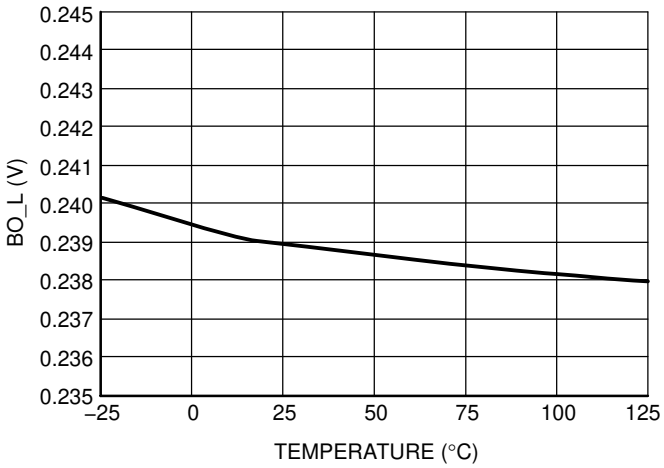


Figure 29. Brown–Out Low Threshold vs. Temperature

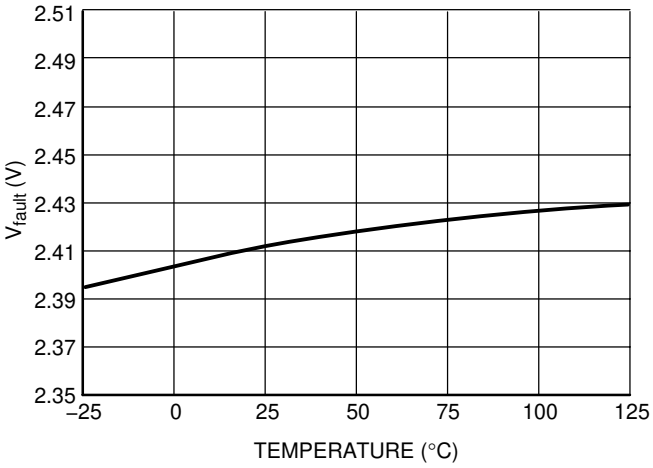


Figure 30. Fault Detect Threshold vs. Temperature

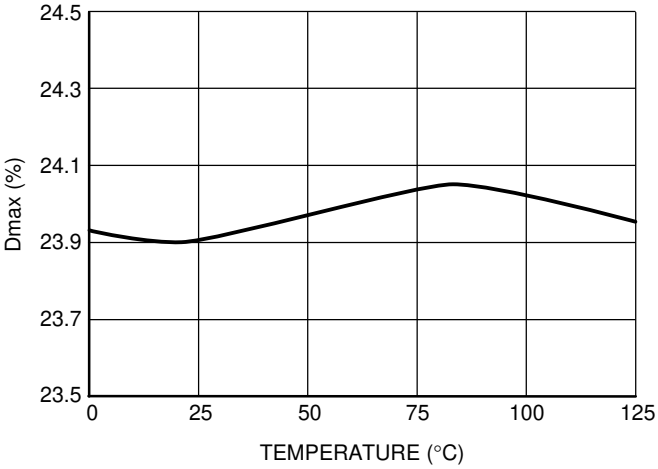


Figure 31. Maximum Duty–Cycle vs. Temperature @ V_{pin9} = 1 V (NCP1239V)

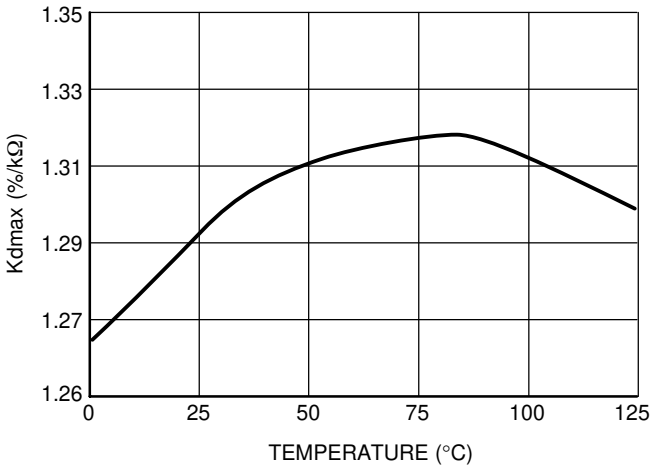
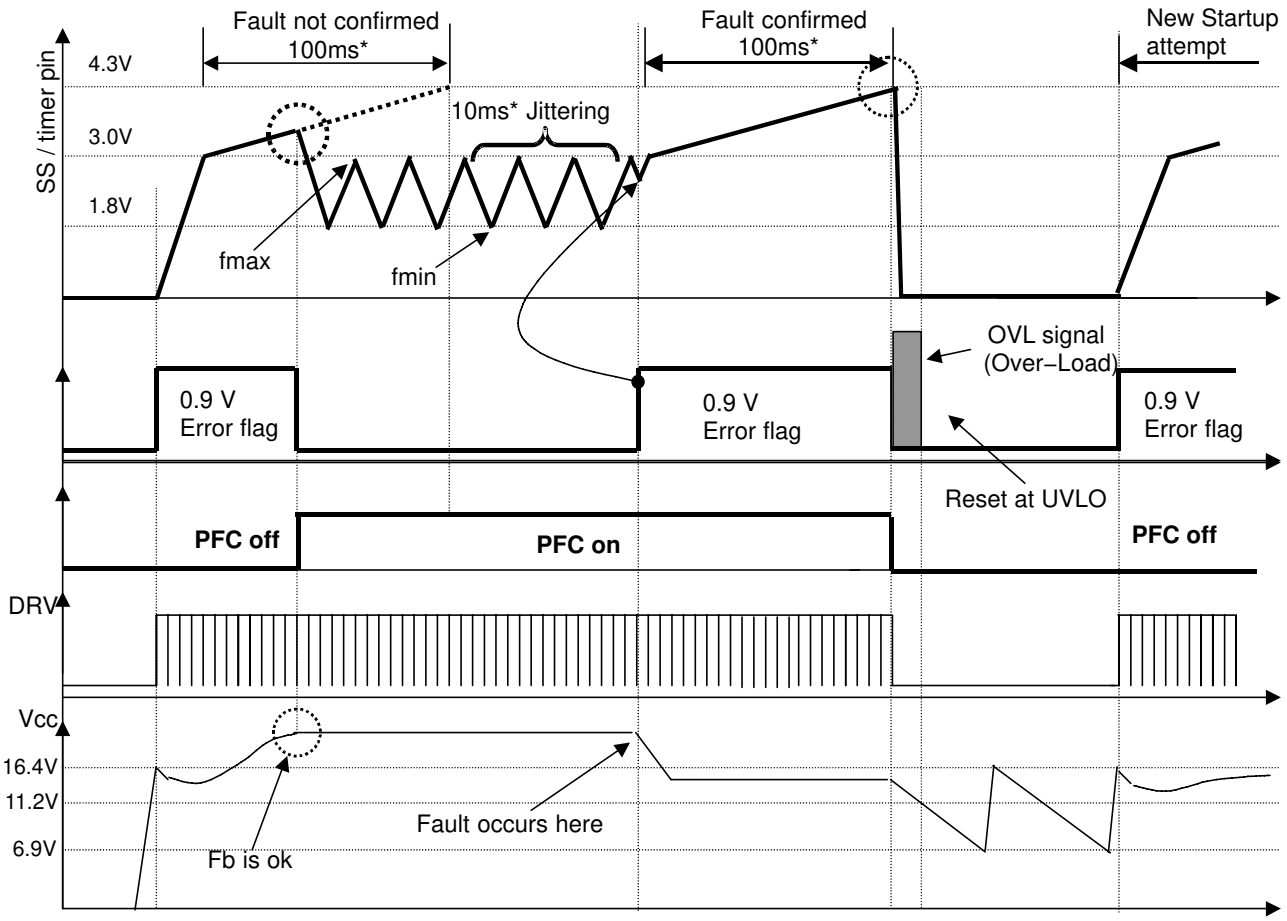


Figure 32. Kdmax Coefficient vs. Temperature @ V_{pin9} = 1 V (NCP1239V)

Fault Management

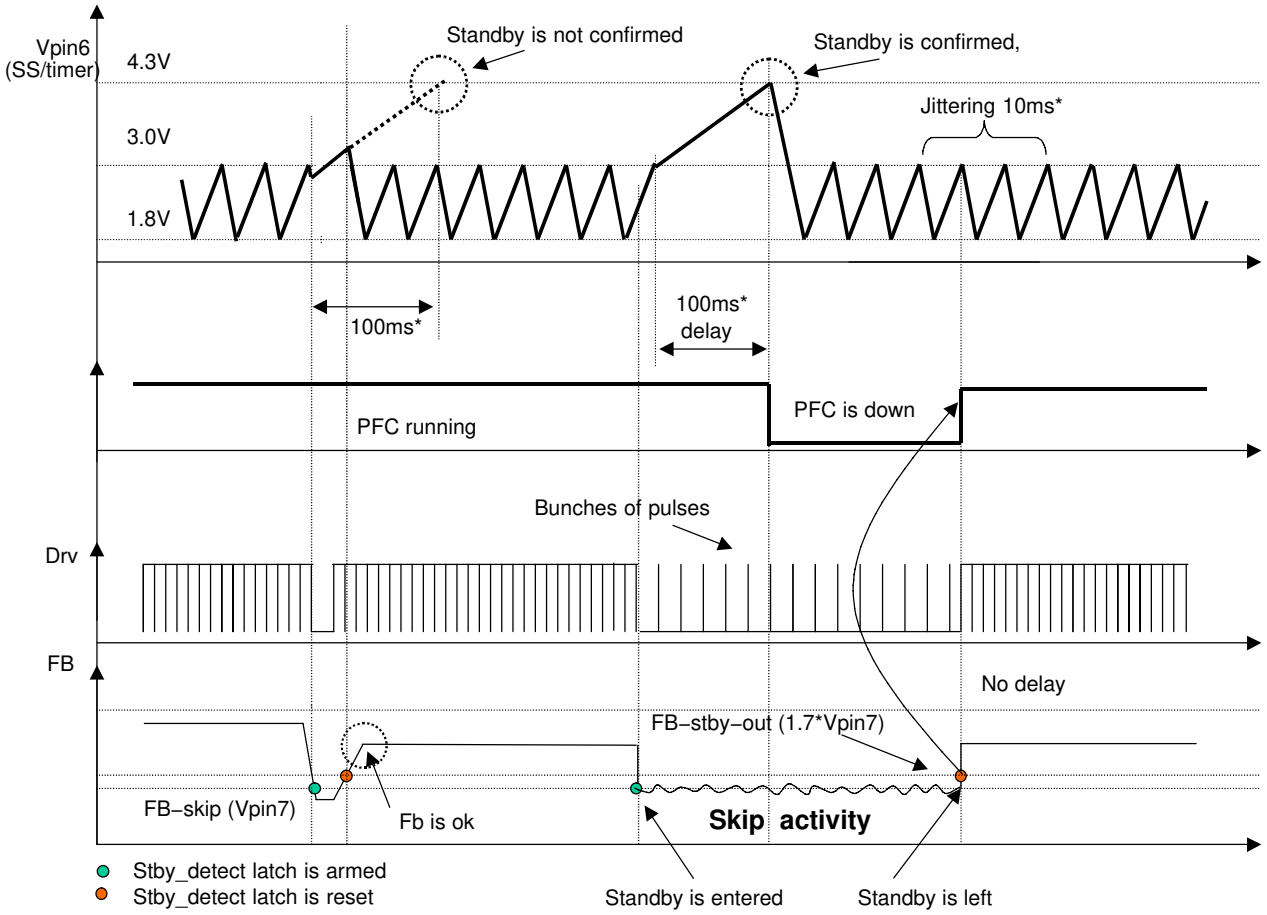


*This time is programmed by the Pin 6 capacitor. C_{pin6} = 390 nF nearly sets the following intervals:
- Soft−Start Time (T_{ss}):7.5 ms
- Jittering Period ($T_{jittering}$): 10 ms
- Fault Detection Delay (T_{delay}): 100 ms

More generally, the times approximately depend on C_{pin6} as follows:
- T_{ss} = 7.5 ms * C_{pin6} / 390 nF
- $T_{jittering}$ =10 ms * C_{pin6} / 390 nF
- T_{delay} =100 ms * C_{pin6} / 390 nF

Figure 33. Fault Management

Standby Detection



*This time is programmed by the Pin 6 capacitor. C_{pin6} = 390 nF nearly sets the following intervals:
- Soft−Start Time (T_{ss}):7.5 ms
- Jittering Period ($T_{jittering}$): 10 ms
- Fault Detection Delay (T_{delay}): 100 ms

More generally, the times approximately depend on C_{pin6} as follows:
- T_{ss} = 7.5 ms * C_{pin6} / 390 nF
- $T_{jittering}$ =10 ms * C_{pin6} / 390 nF
- T_{delay} =100 ms * C_{pin6} / 390 nF

Figure 34. Standby Detection

APPLICATION INFORMATION

The NCP1239 includes all necessary features to help building a rugged and safe switch−mode power supply. The following details the major benefits brought by implementing the NCP1239 controller:

Current−mode operation with internal ramp compensation: implementing peak current mode control, the NCP1239 offers an internal ramp compensation signal that can easily be summed up to the sensed current. Subharmonic oscillations can thus be fought via the inclusion of a simple resistor,

500 mV Current Sense threshold for Over Power Limit (NCP1239F): the NCP1239 operating in current mode, the circuit Pin 10 monitors the current to modulate its level according to the power demand. Due to the ramp compensation, one must generally note that the Pin 10 voltage is not the exact image of the inductor current. A precise current limitation being essential, the NCP1239 features a separate current sense pin (Pin 9) for an accurate overcurrent detection. The low threshold of this protection (500 mV) avoids excessive losses in the current sense resistor and improves the efficiency. In addition, Pin 9 sources a current that proportional to the high−voltage rail, compensates the current−sense and turn off delays at high line. A resistor inserted between Pin 9 and the sensing resistor offsets the Pin 9 current−sense information to build a precise overload protection, independent of the mains input.

Large V_{CC} operation: the NCP1239 offers an extended V_{CC} range up to 36 V, bringing greater flexibility in Flyback or Forward applications.

Internal high−voltage startup switch: reaching low levels of standby power represents a difficult exercise when the controller requires an external, lossy, resistor connected to the bulk capacitor. Due to an internal logic, the controller disables the high−voltage current source after startup which no longer hampers the consumption in no−load situations.

Skip−cycle capability: a continuous flow of pulses is not compatible with no−load standby power requirements. Slicing the switching pattern in bunch of pulses drastically reduces overall losses but can, in certain cases, bring acoustic noise in the transformer. Due to a skip operation taking place at low peak currents only, no mechanical noise appears in the transformer. Furthermore, the skip threshold is made programmable to allow the best trade−off between noise and efficiency.

Standby Detect/Shutdown of the PFC front−stage: The NCP1239 incorporates an internal logic that is able to detect a standby situation. Pin1 state changes in accordance to the detected mode (standby or normal mode). Simply connect a pnp transistor between the NCP1239 V_{CC} and the PFC controller one and drive it using Pin 1, to enable the PFC stage in normal mode and disable it in standby.

Soft−Start: the capacitor connected to Pin 6 provides a soft−start sequence that precludes the main power switch from being stressed upon startup. The same voltage is also used to perform frequency jittering and timing for the fault condition detection.

Major Fault Detection: the circuit detects when Pin 3 voltage exceeds 2.4 V. When this occurs, the NCP1239 considers that a major fault is present and as a consequence, the circuit gets permanently latched−off. In this mode, the circuit needs the V_{CC} to go down below 4.0 V to reset, for instance when the user un−plugs the SMPS. This capability is mainly intended to detect an overvoltage condition or/and an over−heating of the application that would be sensed by a thermistor.

Brown−out detection: by monitoring the level on Pin 5 during normal operation, the controller protects the SMPS against low mains conditions. When the Pin 5 voltage falls below 250 mV, the controllers stops pulsing until this level goes back to 500 mV to prevent any instability.

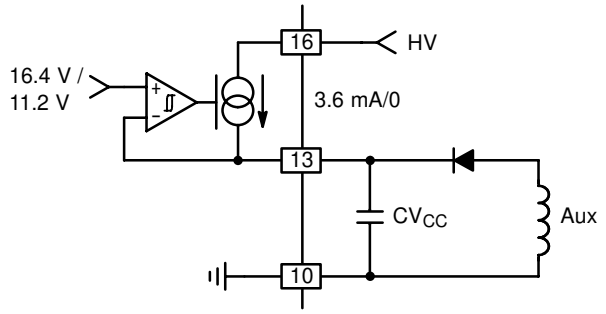
Short−circuit protection: short−circuit and especially overload protections are difficult to implement when a strong leakage inductance affects the transformer (the auxiliary winding level does not properly collapse…). Here, every time the feedback pin is at its maximum (higher than 5.0 V practically), an error flag is asserted and the circuit activates a timer that is programmed by the Pin 6 capacitor. If Pin 6 reaches 4.3 V while the error flag is still present, the controller stops the pulses and goes into a latch−off phase, operating in a low−frequency burst−mode. As soon as the fault disappears, the SMPS resumes its operation. The latch−off phase can also be initiated, more classically, when V_{CC} drops below UVLO (11.2 V typical).

Adjustable frequency and Internal dithering for improved EMI signature: Pin 4 offers a means to precisely adjust the switching frequency through a simple resistor to ground. Frequency operation is allowed up to 250 kHz. By modulating the internal switching frequency with the Pin 6 saw−tooth (100 Hz with 390 nF), natural energy spread appears and softens the controller's EMI signature.

5.0 V reference voltage: a 5.0 V regulator is provided to help biasing any external circuitry in the vicinity of the controller. This reference voltage can typically supply up to 10 mA.

Startup Sequence

When the power supply is first connected to the mains outlet, the internal current source (typically 3.6 mA) is biased and charges up the V_{CC} capacitor. When the voltage on this V_{CC} capacitor reaches the V_{CCON} level (typically 16.4 V), the current source turns off and no longer wastes any power. At this time, the energy stored by the V_{CC} capacitor serves to supply the controller and the auxiliary supply is supposed to take over before V_{CC} collapses below V_{CCOFF}. Figure 35 shows the internal arrangement of this structure:

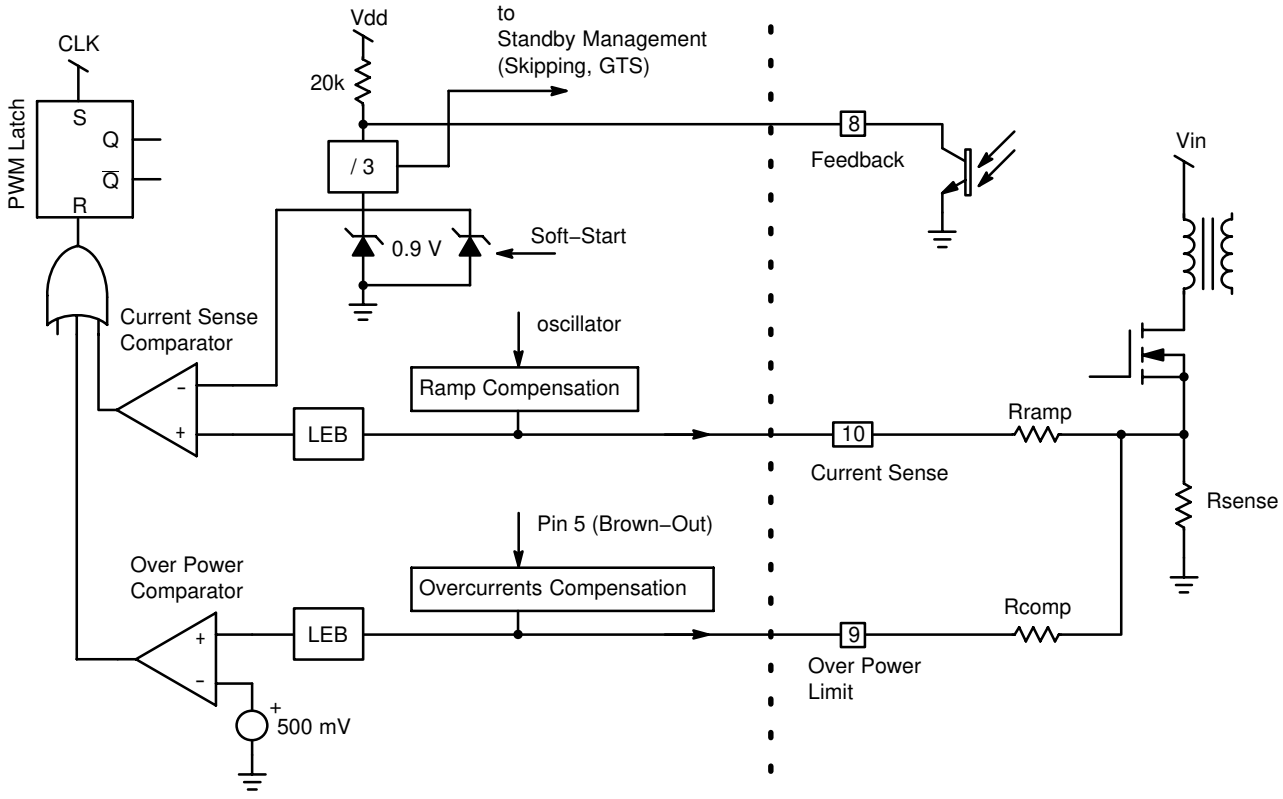


The current source brings V_{CC} above 16.4 V and then turns off

Figure 35.

As soon as V_{CC} reaches 16.4 V, driving pulses are delivered on Pin 12 and the auxiliary winding grows up the V_{CC} pin. Because the output voltage is below the target (the SMPS is starting up), the feedback pin is at its maximum voltage. A resistor divider outputs the third of the feedback voltage that forms the current setpoint. This setpoint is clamped and the limitation level slowly increases until it reaches 0.9V during the soft start time. In nominal operation, the setpoint clamp keeps equal to 0.9 V (refer to Figure 36).

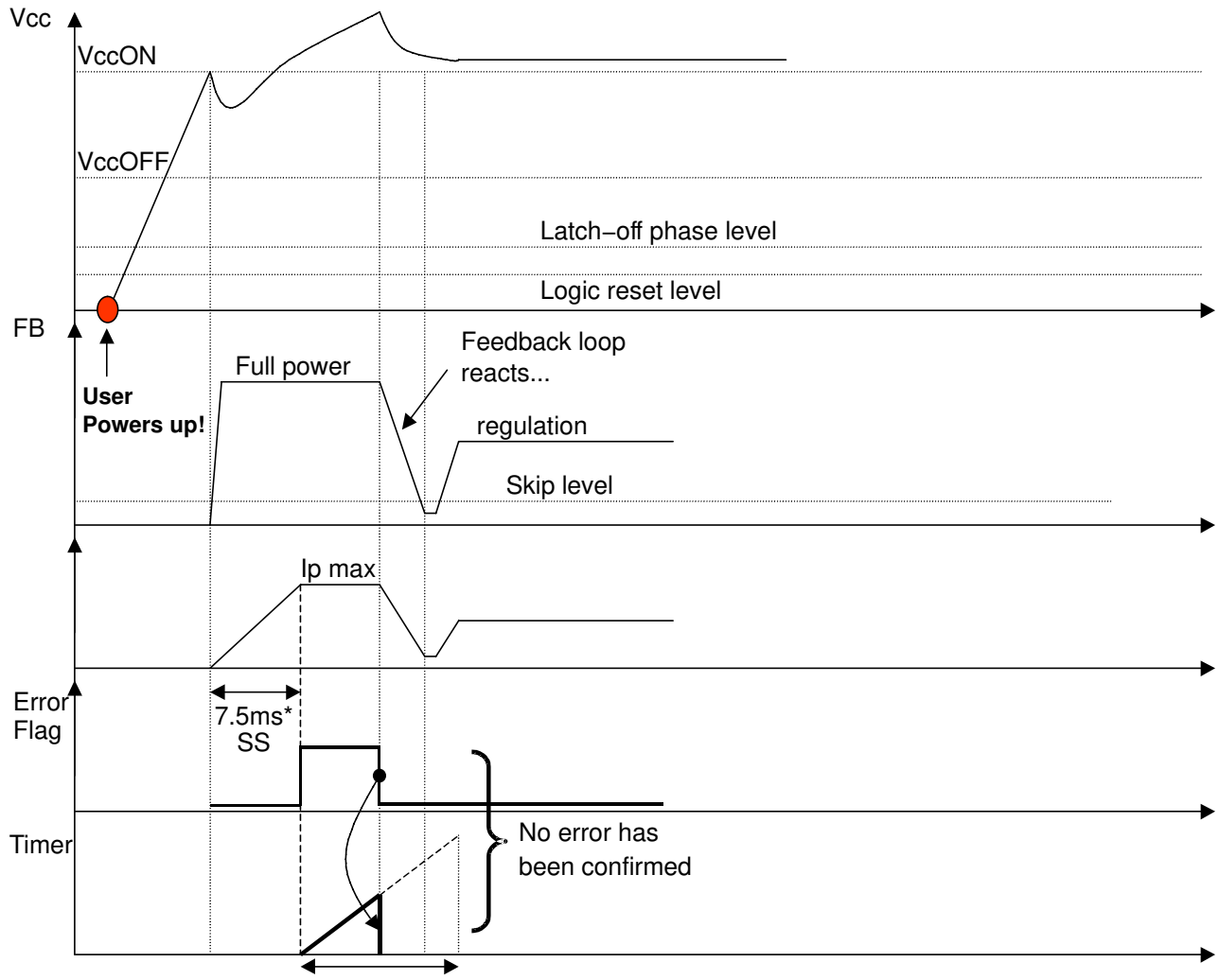
As soon as the feedback voltage is high enough to activate the 0.9 V setpoint clamp (during the startup period but also anytime an overload occurs), an internal error flag is asserted, testifying that the system is pushed to the maximum power. At that moment, a 100 ms time period (typically, with C_{pin6}=390 nF that also corresponds to 7.5 ms soft −start) starts while a logic block observes this error flag. If the error flag keeps asserted all along the 100ms period, then the controller assumes that the power supply really undergoes a fault condition and immediately stops all pulses to enter a safe burst operation. The 100 ms timer enables to distinguish a startup phase (shorter than 100 ms) from an overload condition. If the error flag is released before the 100 ms period has elapsed, the controller concludes that no error is present and resets the timer to use it for other purposes (e.g. frequency dithering).



Pin 10 monitors the power switch current and compares it to the current setpoint (one third of the feedback voltage). The current setpoint is limited by the soft−start during the power−on sequence and permanently clamped to 0.9 V In the NCP1239F, a second pin (Pin 9) monitors the current to clamp the power.

Figure 36. Current Control

Figure 37 depicts the V_{CC} evolution during a proper startup sequence, showing the state of the error flag:



*This time is programmed by the Pin 6 capacitor. C_{pin6} = 390 nF nearly sets the following intervals:
- Soft−Start Time (T_{ss}):7.5 ms
- Jittering Period ($T_{jittering}$): 10 ms
- Fault Detection Delay (T_{delay}): 100 ms

More generally, the times approximately depend on C_{pin6} as follows:
- T_{ss} = 7.5 ms * C_{pin6} / 390 nF
- $T_{jittering}$ =10 ms * C_{pin6} / 390 nF
- T_{delay} =100 ms * C_{pin6} / 390 nF

Figure 37.

PFC Startup Sequence

To ensure an adequate startup sequence of both PWM section and the PFC stage, some logic and timing need to be included as shown on the internal diagram. The key point here is the fact that the PFC *always* starts after the PWM section. As a result, the SMPS must be designed to cope with transient universal mains operation. Why this? Because of the light−to−heavy load transition where a case exists when the PFC is off, the PWM in standby and the load is suddenly applied. In this scenario, the PWM section must sustain the entire transient period that lasts until the PFC re−starts since it has been deactivated for standby.

The standby detection block generates an internal signal "pfcON" that controls Pin 1 in accordance to the operation mode:

– "pfcON" is high in normal mode and a current source draws 1 mA from Pin 1,

– "pfcON" is low in standby to disable the 1 mA current source. A 10 kΩ resistor pulls up Pin 1 to V_{CC}.

This configuration makes it ideal to drive a pnp transistor that connects or disconnects the NCP1239 V_{CC} to the PFC controller one (refer to Figure 39). The "pfcON" signal is activated following Figure 38 diagram. Let's split this drawing in different time periods to clearly depict signal assertions:

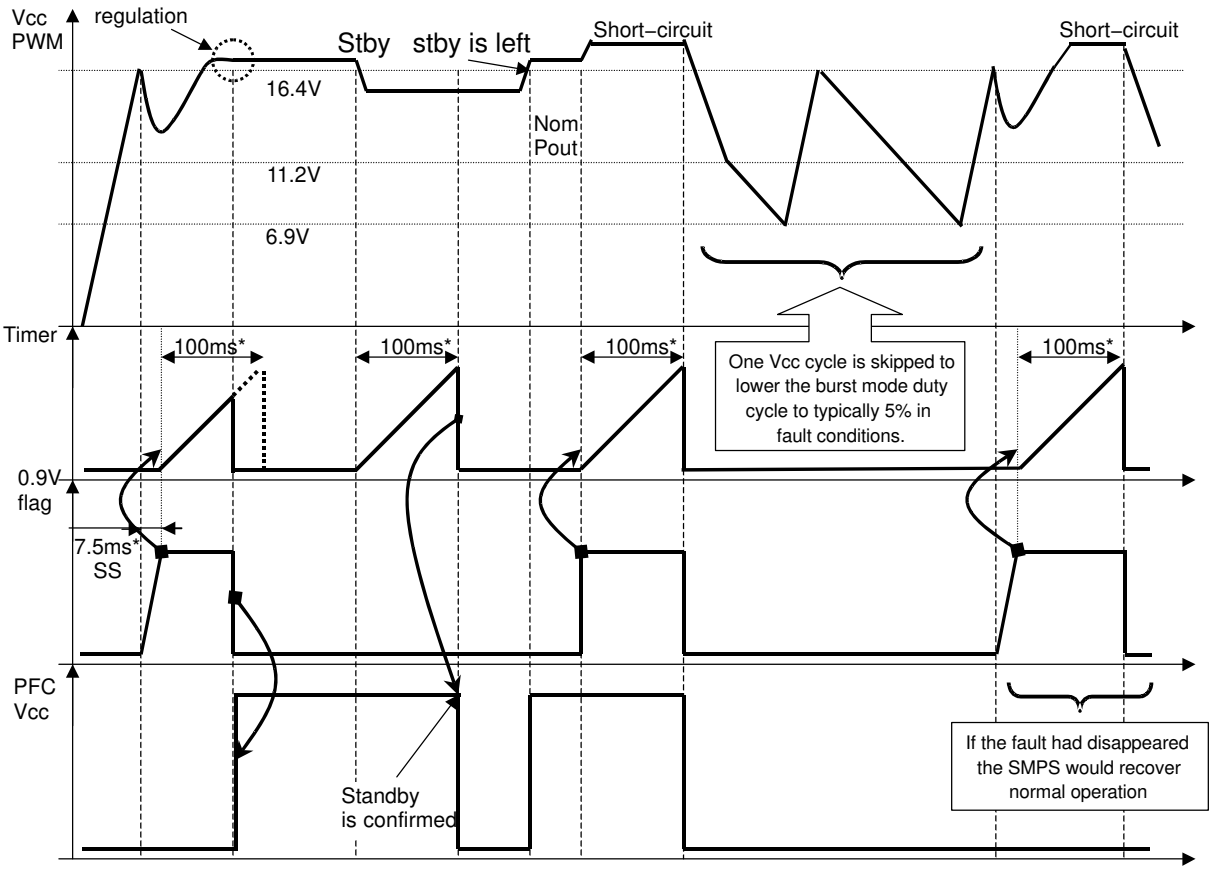
Power on: during this time, V_{CC} rises up, the V_{CC} capacitor being charged by the 3.6 mA current source. When V_{CC} exceeds V_{CCON} (16.4 V typ.), driving pulses are delivered to the MOSFET in an attempt to crank the power supply. V_{CC} collapses (because the V_{CC} capacitor alone delivers the energy) until sufficient auxiliary voltage is built up in order to take over the startup sequence and thus self−supply the controller. As long as the output voltage has not reached its wished value, the controller pushes for the maximum peak current. During the soft−start (7.5 ms with 390 nF on Pin 6), the maximum permissible current linearly increases till the maximum peak setpoint is reached, the internal 0.9 V Zener diode actively clamping the current amplitude to (0.9 V/Rsense). During this time, the NCP1239 asserts an error flag. A maximum current condition being observed, the circuit determines if this state results from either a normal response (startup or a transient period) or a fault condition. To make the difference, each time the error flag is asserted, a 100 ms timer starts to count down. If the error flag keeps asserted for the 100 ms period, there is a fault and the PWM controller enters a safe, auto−recovery, burst mode to limit the dissipated heat (see below for more details). During the Power−on sequence, "pfcON" keeps low to pullup Pin 1 to V_{CC} until the error flag is down. When the error flag is down, the power supply has entered regulation, its auxiliary voltage is stable, then Pin 1 can turn low (1 mA sink current) to safely allow PFC operation.

Entering Standby: when skip−cycle starts to activate, a 100 ms countdown takes place and the logic observes the skip activity. If the skip activity is still there at the end of the 100 ms, then standby is confirmed and the NCP1239 pulls up Pin 1 to V_{CC} to shut down the PFC.

Leaving standby: in this case, as soon as the skip−cycle activity disappears, the circuit immediately re−activates the 1 mA sinking current source of Pin 1, to enable the PFC: there is no reaction delay in this situation.

Short−circuit condition: a short circuit is detected on the primary side by measuring the time the error flag is asserted. As explained, if this flag is asserted longer than 100 ms, then the PWM stops oscillating and enters a safe burst mode. In this case, Pin 1 is pulled up to V_{CC} and the PFC is shut down. During the burst, it is not activated (PFC is off) until the fault goes away and the power supply resumes operation. The PFC being shut off in short−circuit conditions, it naturally reduces the main MOSFET stress.

Latch−off mode: if the controller is permanently latched−off due to a major fault (Pin 3 detection of an OVP or an excessive external temperature), the PFC is kept off (Pin 1 being tied to V_{CC}).

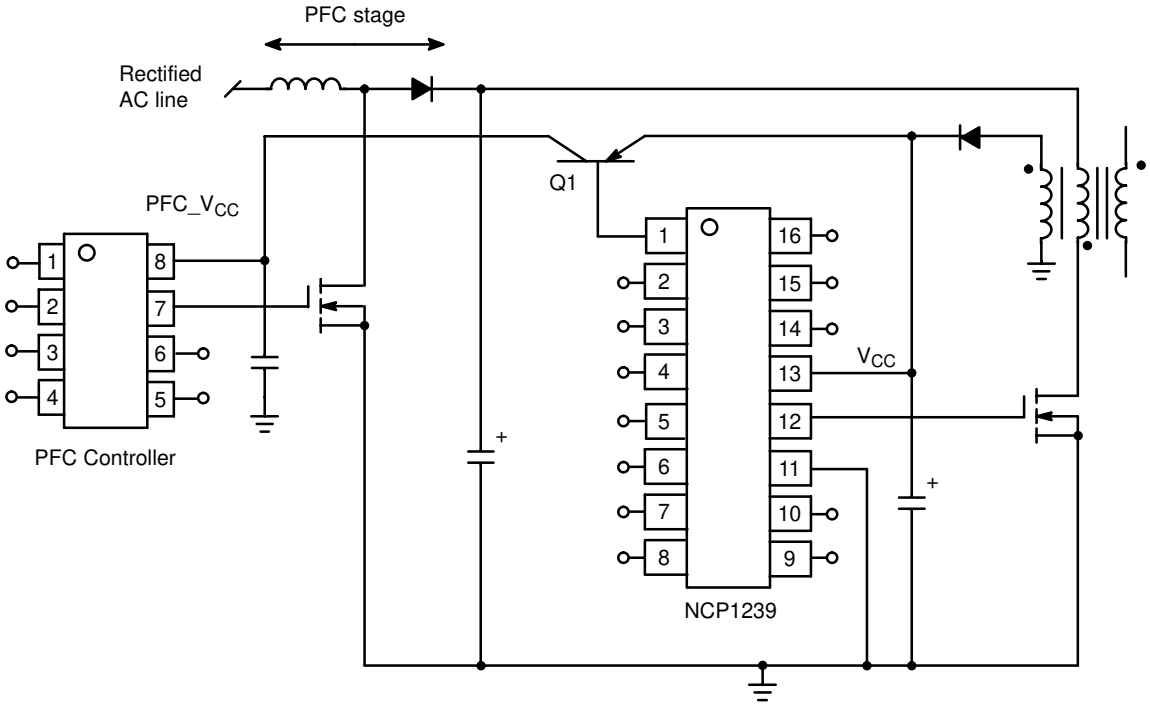


*This time is programmed by the Pin 6 capacitor. C_{pin6} = 390 nF nearly sets the following intervals:
- Soft−Start Time (T_{ss}):7.5 ms
- Jittering Period ($T_{jittering}$): 10 ms
- Fault Detection Delay (T_{delay}): 100 ms

More generally, the times approximately depend on C_{pin6} as follows:
- T_{ss} = 7.5 ms * C_{pin6} / 390 nF
- $T_{jittering}$ =10 ms * C_{pin6} / 390 nF
- T_{delay} =100 ms * C_{pin6} / 390 nF

Figure 38.

The PFC controller connection is really straightforward as testified by Figure 39: simply connect to Pin 1, the base of a pnp transistor that connects the PFC's V_{CC} to the NCP1239 one (perhaps add a small decoupling capacitor like a 0.1 μF on the PFC) and this is all! The PFC startup network goes away as it is fully supplied by the PWM auxiliary winding and even high quiescent current devices do not hamper the standby power since they are completely disconnected in standby.



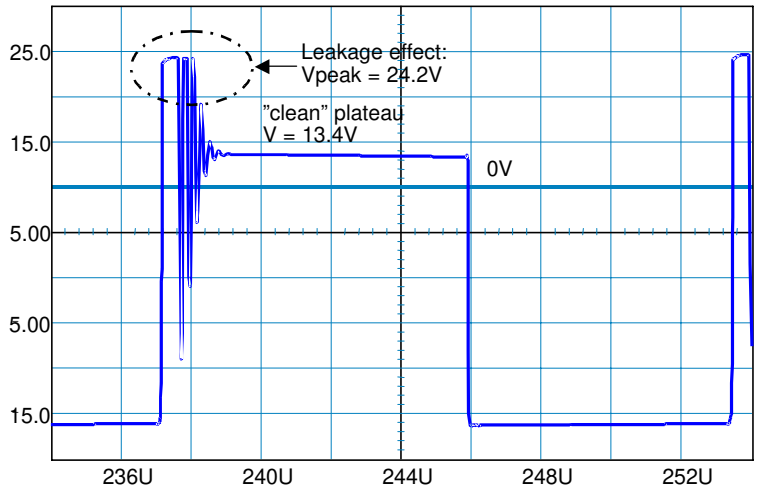
The NCP1239 turns off the pnp Q1 during the standby so that the PFC controller is no longer supplied in this mode.

Figure 39.

Short−Circuit or Overload Condition

The NCP1239 differs from other controllers in the sense that a fault condition is detected independently of the auxiliary voltage level. In auxiliary supply−based power supplies, it is necessary that the (isolated) secondary output conditions properly reflects on the (non−isolated) auxiliary winding in order to instruct the controller on what is happening on the other side of the transformer. For the following reasons, it sometimes becomes extremely difficult to build an efficient short−circuit protection circuitry and even more difficult to implement over power detection (e.g. the output load is 25% above the nominal value but Vout is still present).

The primary leakage inductance is high: this is probably the main reason why building efficient short−circuit detection is difficult. When the power switch opens, the leakage inductance superimposes a large overvoltage spike on the drain voltage. This spike is seen on the secondary side but also on the auxiliary winding. Unfortunately, since the V_{CC} capacitor and the auxiliary diode form a peak rectifier, the auxiliary V_{CC} often depends on this peak value rather than the true plateau which corresponds to the output level.



The leakage effect seen on the auxiliary side pulls−up the final level peak−rectified by the diode

Figure 40.

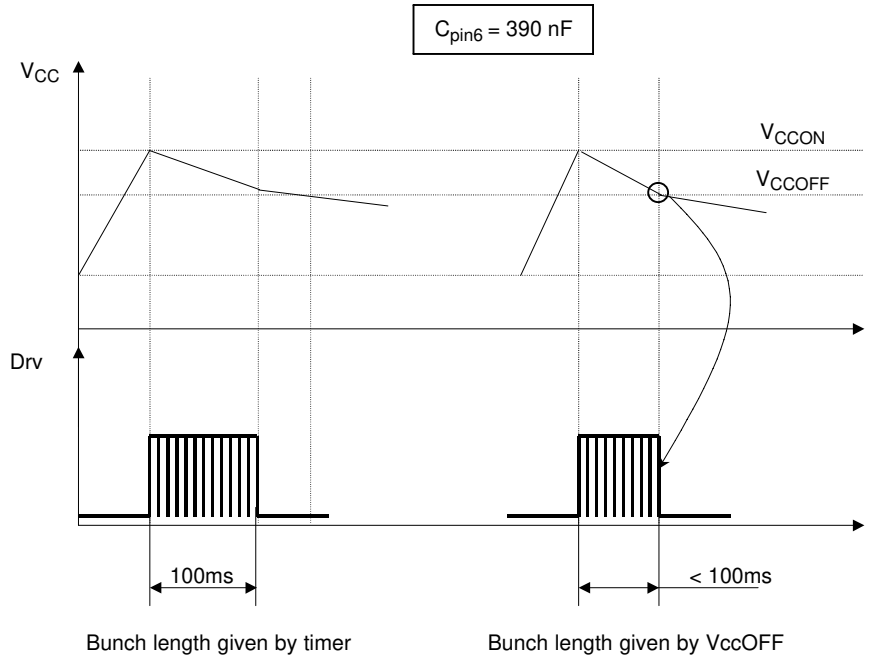
On Figure 40's example, one can clearly observe the difference between the peak and the real plateau DC level. The delta is around 10 V, which obviously degrades the auxiliary image of the secondary side. When a short−circuit occurs, the leakage can be so strong that the whole plateau has dropped to a few volts, but the leakage contribution becomes so energetic (Ip = Ip max.) that even a few μs duration is enough to prevent V_{CC} auxiliary from collapsing and thus stopping the pulses. Needless to say that over power detection is simply impossible.

Low standby power requirement decreases V_{CC} at no−load: this is particularly true if you try to reach less than 100 mW at high line. Due to skip−cycle, the continuous flow of pulses turns into bunches of pulses (sometimes 1−2 pulses only) that can be spaced by 50ms or more in certain cases. The energy content in each bunch of pulses does not suffer any attenuation. For instance, to lower Figure 40's peak, you could think of inserting a resistor with the auxiliary diode to form a low pass filter with the V_{CC} capacitor. Unfortunately, it would drastically reduce the V_{CC} capacitor refueling current and V_{CC} could not be maintained. To compensate that effect, a solution could be to increase the turn ratio, but then the peak rectification problem comes back again.

As one can see, a short−circuit protection free of the V_{CC} level would be the best solution. This is exactly what the NCP1239 delivers with the internal 100 ms timer (390 nF being connected to Pin 6). As soon as the internal 0.9 V error flag is asserted high, a 100 ms timer gets started. If the error flag keeps asserted during the 100 ms period, then the controller detects a true fault condition and stops pulsing the output. If this is a simple transient overload, e.g. the error flag goes back to a normal level before the 100 ms period has elapsed, nothing happens and the controller continues working normally.

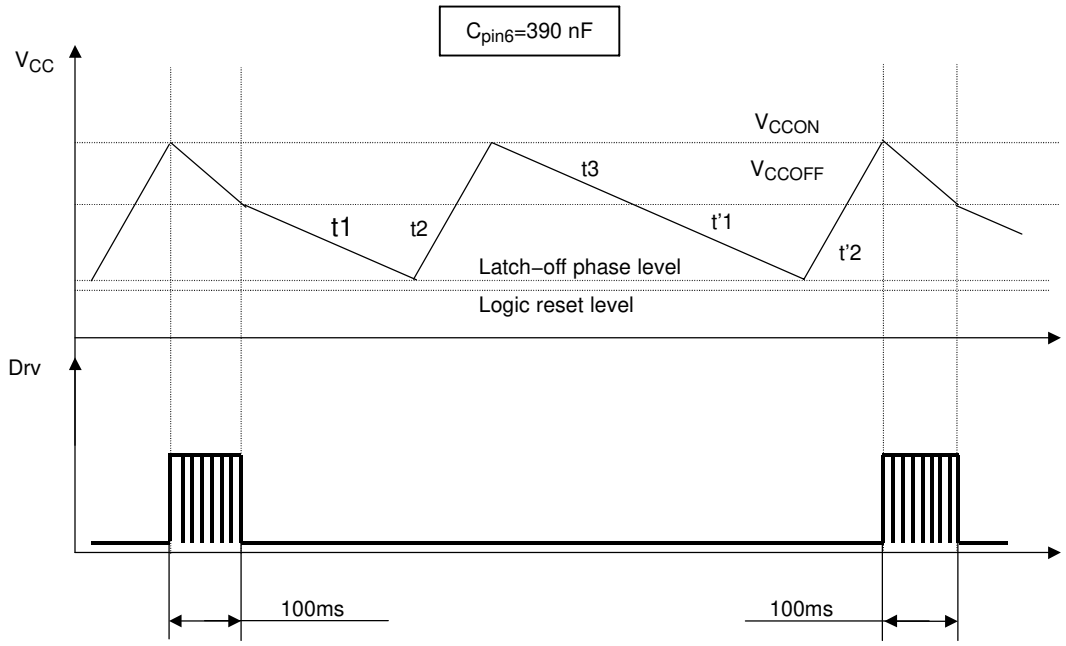
When a fault is detected, we have seen that the controller stops delivering pulses. At this time, V_{CC} starts to drop because the power supply is locked off. When the V_{CC} drops below V_{CCOFF} (11.2 V typical), it enters a so−called latch−off phase where the internal consumption is reduced down to about 400 μA. The V_{CC} capacitor continues to deplete, but at a lower rate. When V_{CC} finally reaches the latch−off level (around 6.9 V), the startup current source turns on and pulls V_{CC} above V_{CCON}, exactly as a startup sequence would do. When V_{CC} exceeds V_{CCON} (16.4 V), pulses are delivered and can last 100 ms maximum if there is enough voltage or can be prematurely interrupted if V_{CC} falls below V_{CCOFF}. Figure 41 shows the difference between these two cases. As already explained, in short−circuit bursts, the PFC section is not validated.

The short−circuit protection features a so−called auto−recovery circuitry. That is to say, during the 100 ms period, the power supply attempts to startup. If the fault has gone, then the controller resumes from the fault and the power supply operates again. If the fault is still present, the pulses are stopped at the end of the 100 ms section (Tpulse) for a given time period Tfault. At the end of Tfault, a new 100 ms attempt is made and so on. To avoid any thermal runaway, a burst duty−cycle defined by Tpulse/(Tfault+ Tpulse) below 10% is desirable ((Tfault+Tpulse) is the burst period). If the 100 ms is made by an internal timer in conjunction with the Pin 6 capacitor, the Tfault duration builds on the V_{CC} capacitor which is charged/discharged two times. Figure 42 on the following page portrays this behavior.



When V_{CC} drops faster than the timer, it prematurely interrupts the pulses flow.
The 100 ms delay could be shortened or lengthened by changing the Pin 6 capacitor.

Figure 41.



The burst period is ensured by the V_{CC} capacitor charge/discharge cycle
The 100 ms delay could be shortened or lengthened by changing the Pin 6 capacitor.

Figure 42.

If by design we have selected a 47 μF V_{CC} capacitor, it becomes easy to evaluate the burst period and its duty−cycle. This can be done by properly identifying all time events on Figure 42 and applying the classical formula: $t = C * \Delta V / i$. To simplify, let's consider t1 starts while $V_{CC} = V_{CCOFF}$.

Then:

- t1: I = $I_{CC}3$ = 400 μA, ΔV= 11.2 – 6.9 = 3 V → t1 = 505 ms
- t2: I = 3.6 mA, ΔV= 16.4 – 6.9 = 9.5 V → t2 = 124 ms
- t3: I = 400 μA, ΔV= 16.4 – 11.2 = 5.2 V → t3 = 611 ms
- t'1 = t1= 505 ms
- t'2 = t2 = 124 ms

The total period duration is thus the sum of all these events which leads to Tfault = 1793 ms. If Tpulse = 100 ms, then our burst duty−cycle equals 100/(1869 + 100) ≈ 5%, which is excellent.

In fact, the calculation assumption, t1 starts while $V_{CC} = V_{CCOFF}$, gives the worse case since the duty cycle is calculated in the case where Tpulse exactly equals the active phase duration (switching period when V_{CC} decreases from V_{CCON} to V_{CCOFF}).

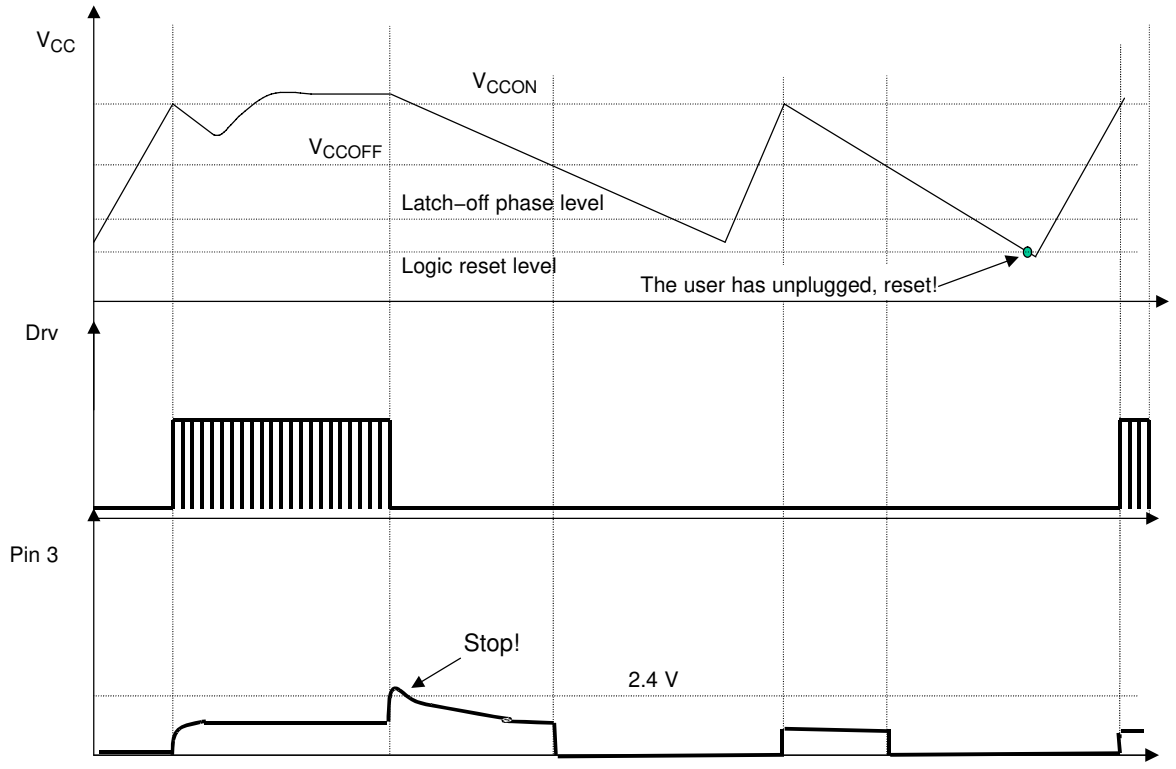
In fact, Tpulse is generally:

– shorter than the switching phase period. In this case, t1 is longer since the latched off phase starts earlier (at a V_{CC} higher than V_{CCOFF}). As a consequence, the final duty cycle is lower than previously estimated,

– longer than the switching phase period. In this case, the circuit detects an overload condition simply because V_{CC} drops below V_{CCOFF} (11.2 V) before the fault timer has elapsed. Tpulse is lower than 100 ms and as a result the duty cycle is also lower.

(Major) Fault Detection and Latched Off Mode

The NCP1239 features a fast comparator that permanently monitors the "Fault Detect" pin level. If for any reason this level exceeds 2.4 V (typical), the part immediately stops oscillating and stays latched off until the user cycles down the power supply. This enables the SMPS designer to externally shut down the part in particular when a major default occurs, e.g. an Overvoltage Protection (OVP). Figure 43 shows what happens when the part is latched:



When Vpin3 exceeds 2.4 V, NCP1239 permanently latches−off the output pulses…until its V_{CC} goes below 4 V. The figure can illustrate a case where a thermistor supplied by REF5V is connected to Pin 3 to detect excessive temperatures of the application (refer to application schematic).

Figure 43.

Pin 3 can serve to build an Overvoltage Protection by placing a Zener between the voltage to measure (e.g., V_{CC}) and Pin 3 (refer to application schematic). If a 15 V Zener is applied, the Pin 3 comparator will switch when (V_{CC} − 15 V) exceeds the 2.4 V internal reference, that is, when V_{CC} is higher than 17.5 V.

This pin can also monitor the temperature using an external thermistor (refer to application schematic). Thermistors can be of Negative Temperature Coefficient (NTC) type (the resistance decreases versus the temperature) or of Positive Temperature Coefficient (PTC) type (the resistance increases versus the temperature). Let's assume that a NTC thermistor is used (as in the application schematic). Placing it between the 5 V reference voltage (REF5V) and Pin 3, and a classical resistance between Pin 3 and ground, the Pin 3 voltage equals:

$$V_{pin3} = \frac{R}{R + R_{thermistor}} \cdot 5\ V$$

where R and $R_{thermistor}$ are respectively the resistor and the thermistor resistance.

$R_{thermistor}$ decreasing versus the temperature, the Pin 3 voltage (V_{pin3}) increases when the temperature grows up.

For instance, the thermistor resistance can be in the range of 500 kΩ at 25°C and as low as 5 kΩ at 130°C that as an example, one can take as the temperature limit the application must not exceed. Choosing R equal to 5k, the Pin 3 voltage at 130°C that equates:

$$V_{pin3(130^{\circ}C)} = \left[\frac{5\ k}{5\ k + 5\ k}\right] \cdot 5\ V = 2.5\ V$$

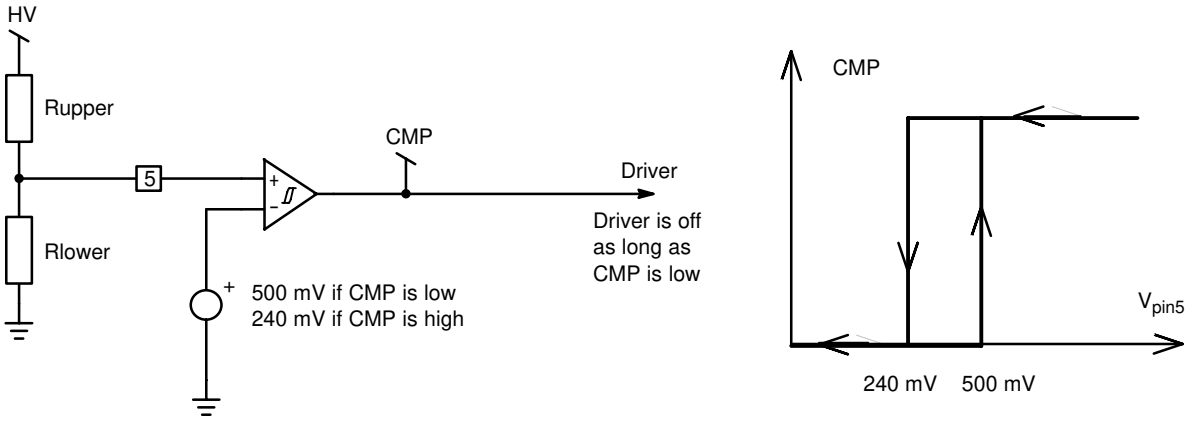
triggers the fault comparator.

This example illustrates that one must just select the bottom resistor so that it exhibits the same resistance as the thermistor at the temperature to be detected.

If the thermistor is a PTC, it must be placed between Pin 3 and ground. One must place a resistor between the 5 V reference voltage and Pin 3. Similarly, the resistor must be selected so that its resistance equals the thermistor one at the temperature to be detected.

Brown−Out and Over Power Limitation

SMPS are designed for a given input range. When the input voltage is too low (brown−out), the SMPS tends to compensate by sinking an increased current from the line. As a result the power components may suffer from an excessive heating and ultimately the SMPS may be destroyed. To avoid such a risk, the NCP1239 incorporates a brown−out detection that monitors the portion of the input voltage that is applied to Pin 5.



An hysteresis comparator monitors the SMPS input voltage

Figure 44.

Also called "Bulk OK" signal (BOK), the Brown−Out (BO) protection prevents the power supply from being adversely destroyed in case the mains drops to a very low value. When it detects such a situation, the NCP1239 no longer pulses but waits until the bulk voltage goes back to its normal level. A certain amount of hysteresis needs to be provided since the bulk capacitor is affected by some ripple, especially at low input levels. For that reason, when the BO comparator toggles, the internal reference voltage changes from 500 mV to 240 mV. This effect is not latched: that is to say, when the bulk capacitor is below the target, the controller does not deliver pulses. As soon as the input voltage grows−up and reaches the level imposed by the resistive divider, pulses are passed to the internal driver and activate the MOSFET.