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NCP12400

Fixed Frequency Current Mode Controller for Flyback Converters

The NCP12400 is a new fixed-frequency current-mode controller featuring the Dynamic Self-Supply. This function greatly simplifies the design of the auxiliary supply and the V_{CC} capacitor by activating the internal startup current source to supply the controller during start-up, transients, latch, stand-by etc. This device contains a special HV detector which detects the application unplug from the ac input line and triggers the X2 discharge current. This HV structure allows the brown-out detection as well.

It features a timer-based fault detection that ensures the detection of overload and an adjustable compensation to help keep the maximum power independent of the input voltage.

Due to frequency foldback, the controller exhibits excellent efficiency in light load condition while still achieving very low standby power consumption. Internal frequency jittering, ramp compensation, and a versatile latch input make this controller an excellent candidate for the robust power supply designs.

A dedicated Off Mode allows to reach the extremely low no load input power consumption via “sleeping” whole device and thus minimize the power consumption of the control circuitry.

Features

- Fixed-Frequency Current-Mode Operation 65 kHz or 100 kHz Frequency Options
- Frequency Foldback then Skip Mode for Maximized Performance in Light Load and Standby Conditions
- Timer-Based Overload Protection with Latched (Option A) or Autorecovery (Option B) Operation
- High-Voltage Current Source with Brown-Out Detection and Dynamic Self-Supply, Simplifying the Design of the V_{CC} Circuitry
- Frequency Modulation for Softened EMI Signature
- Adjustable Overpower Protection Dependant on the Mains Voltage
- Fault Input for Overvoltage and Over Temperature Protection
- V_{CC} Operation up to 28 V, with Overvoltage Detection
- 300/500 mA Source/Sink Drive Peak Current Capability
- 4/10 ms Soft-Start
- Internal Thermal Shutdown
- No-Load Standby Power < 30 mW
- X2 Capacitor in EMI Filter Discharging Feature
- These are Pb-Free Devices

Typical Applications

- Offline Adapters for Notebooks, LCD, and Printers
- Offline Battery Chargers
- Consumer Electronic Power Supplies
- Auxiliary/Housekeeping Power Supplies
- Offline Adapters for Notebooks



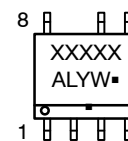
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SOIC-7
CASE 751U

MARKING DIAGRAM

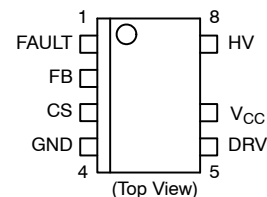


400VWXYZf = Specific Device Code
(see page 2)

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 43 of this data sheet.

NCP12400

TYPICAL APPLICATION SCHEMATIC

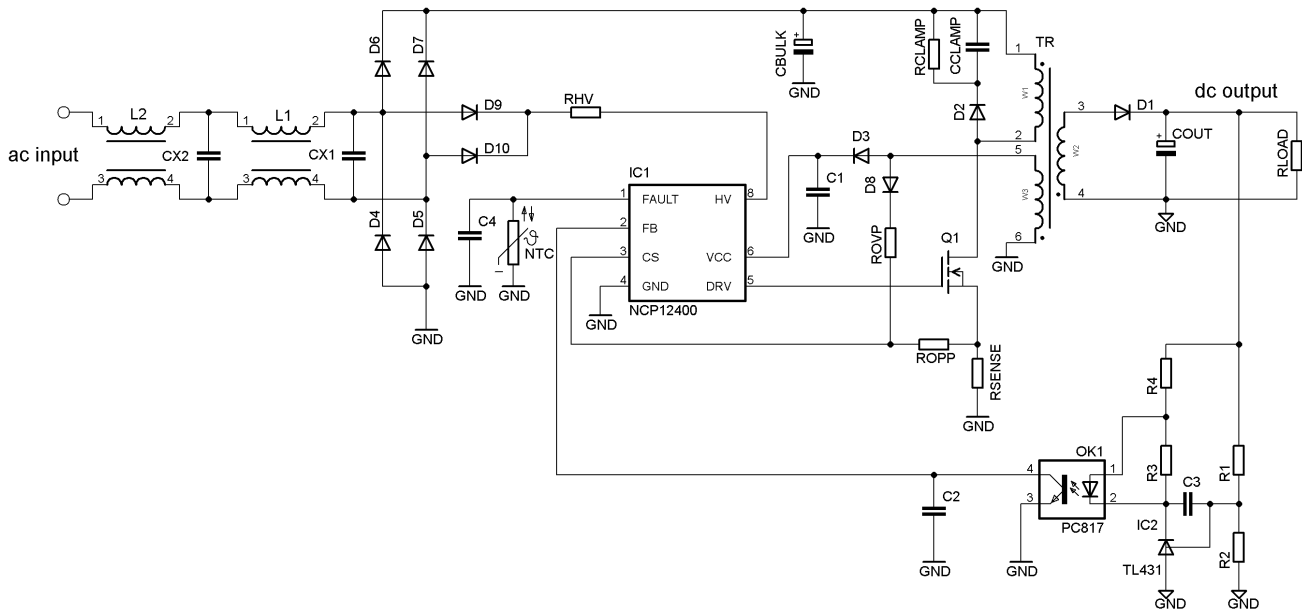


Figure 1. Flyback Converter Application using the NCP12400

Table 1. OPTIONS

OPN	Brown Out Start-Stop	OCP Fault	Frozen Current Setpoint	Quiet Skip	Soft Start	Frequency
NCP12400BAHAB0DR2G	103 – 96 V	Latched	300 mV	No, min. 3 pulses only	4 ms	65 kHz
NCP12400BAHBB0DR2G	103 – 96 V	Latched	300 mV	Yes, min. 3 pulses, 800 Hz burst	4 ms	65 kHz
NCP12400BBHAA1DR2G	103 – 96 V	Autorecovery	300 mV	No, min. 3 pulses only	10 ms	100 kHz
NCP12400CAHAB0DR2G	95 – 87 V	Latched	300 mV	No, min. 3 pulses only	4 ms	65 kHz
NCP12400CBAAB0DR2G	95 – 87 V	Autorecovery	No	No, min. 3 pulses only	4 ms	65 kHz
NCP12400CBHAA0DR2G	95 – 87 V	Autorecovery	300 mV	No, min. 3 pulses only	10 ms	65 kHz

Table 2. SPECIFIC DEVICE CODE KEY

400	V	W	X	Y	Z	f
Part	BO	OCP Fault	Frozen Current Setpoint	Quiet Skip	Soft Start	Frequency
	A – 229–211 V B – 111–103 V C – 95–87 V D – No BO E – Brown In, no BO	A – Latched B – Autorecovery	A – No B – 150 mV C – 170 mV D – 190 mV E – 210 mV F – 230 mV G – 250 mV H – 300 mV	A – No, min. 3 pulses B – Yes, min. 3 pulses, 800 Hz burst	A – 10 ms B – 4 ms	0 – 65 kHz 1 – 100 kHz 2 – 65 → 100 kHz

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Table 3. PIN FUNCTION DESCRIPTION

Pin #	Pin Name	Function	Pin Description
1	FAULT	FAULT Input	Pull the pin up or down to stop the controller. An internal current source allows the direct connection of an NTC for over temperature detection. Device can restart in autorecovery mode or can be latched depending on the option.
2	FB	Feedback + Shutdown Pin	An optocoupler connected to ground controls the output regulation. The part goes to the low consumption Off mode if the FB input pin is pulled to GND.
3	CS	Current Sense	This input senses the primary current for current-mode operation, and offers an overpower compensation adjustment. This pin implements over voltage protection as well.
4	GND		The controller ground.
5	DRV	Drive Output	Drives external MOSFET.
6	V _{CC}	V _{CC} Input	This supply pin accepts up to 28 Vdc, with overvoltage detection. The pin is connected to an external auxiliary voltage.
8	HV	High-Voltage Pin	Connects to the rectified ac line to perform the functions of start-up current source, Self-Supply, brown-out detection and X2 capacitor discharge function and the HV sensing for the overpower protection purposes. It is not allowed to connect this pin to a dc voltage.

NCP12400

SIMPLIFIED INTERNAL BLOCK SCHEMATIC

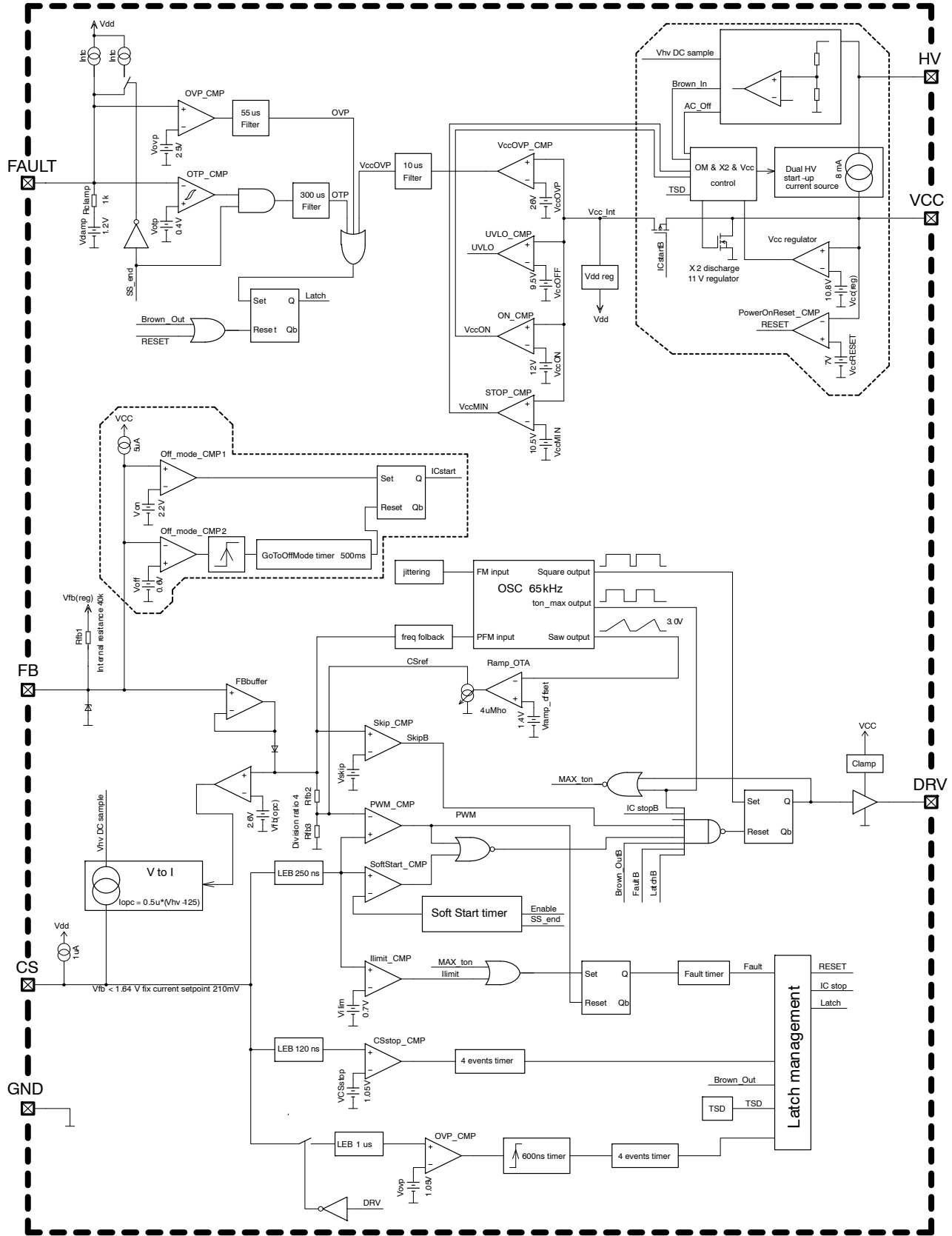


Figure 2. Simplified Internal Block Schematic

NCP12400

Table 4. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DRV (pin 5)	Maximum voltage on DRV pin (Dc-Current self-limited if operated within the allowed range) (Note 2)	-0.3 to 20 ±1000 (peak)	V mA
V _{CC} (pin 6)	V _{CC} Power Supply voltage, V _{CC} pin, continuous voltage Power Supply voltage, V _{CC} pin, continuous voltage (Note 2)	-0.3 to 36 ±30 (peak)	V mA
HV (pin 8)	Maximum voltage on HV pin (Dc-Current self-limited if operated within the allowed range)	-0.3 to 500 ±20	V mA
V _{max}	Maximum voltage on low power pins (except pin 5, pin 6 and pin 8) (Dc-Current self-limited if operated within the allowed range) (Note 2)	-0.3 to 5.5 ±10 (peak)	V mA
R _{θJ-A}	Thermal Resistance SOIC-7 Junction-to-Air, low conductivity PCB (Note 3) Junction-to-Air, medium conductivity PCB (Note 4) Junction-to-Air, high conductivity PCB (Note 5)	162 147 115	°C/W
R _{θJ-C}	Thermal Resistance Junction-to-Case	73	°C/W
T _{JMAX}	Operating Junction Temperature	-40 to +150	°C
T _{STRGMAX}	Storage Temperature Range	-60 to +150	°C
	ESD Capability, HBM model (All pins except HV) (Note 1)	> 4000	V
	ESD Capability, HBM model (pin 8, HV)	> 2000	V
	ESD Capability, Charge Discharge Model (Note 1)	> 500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- This device series contains ESD protection and exceeds the following tests:
Human Body Model 4000 V per JEDEC standard JESD22, Method A114E
Charge Discharge Model Method 500 V per JEDEC standard JESD22, Method C101E
- This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.
- As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 50 mm² of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51-1 conductivity test PCB. Test conditions were under natural convection or zero air flow.
- As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 100 mm² of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51-2 conductivity test PCB. Test conditions were under natural convection or zero air flow.
- As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 650 mm² of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51-3 conductivity test PCB. Test conditions were under natural convection or zero air flow.

Table 5. ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = -40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
HIGH VOLTAGE CURRENT SOURCE						
Minimum voltage for current source operation		V _{HV(min)}	-	30	40	V
Current flowing out of V _{CC} pin	V _{CC} = 0 V V _{CC} = V _{CC(on)} - 0.5 V	I _{start1} I _{start2}	0.2 5	0.5 8	0.8 11	mA
Off-state leakage current	V _{HV} = 500 V, V _{CC} = 15 V	I _{start(off)}	-	2	6	µA

SUPPLY

Turn-on threshold level, V _{CC} going up HV current source stop threshold (depending on the version)		V _{CC(on)}	11.0 15.0	12.0 16.2	13.0 17.5	V
HV current source restart threshold		V _{CC(min)}	9.5	10.5	11.5	V
Turn-off threshold		V _{CC(off)}	8.4	8.9	9.3	V
Overvoltage threshold		V _{CC(ovp)}	25	26.5	28	V
Blanking duration on V _{CC(off)} and V _{CC(ovp)} detection		t _{VCC(blank)}	-	10	-	µs
V _{CC} decreasing level at which the internal logic resets		V _{CC(reset)}	4.8	7.0	7.7	V

- Guaranteed by design.
- CS pin source current is a sum of I_{bias} and I_{OPC}, thus at V_{HV} = 125 V is observed the I_{bias} only, because I_{OPC} is switched off.

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Table 5. ELECTRICAL CHARACTERISTICS

(For typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{HV} = 125\text{ V}$, $V_{CC} = 11\text{ V}$ unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
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SUPPLY

V _{CC} level for I _{START1} to I _{START2} transition		V _{CC(inhibit)}	1.0	2.1	3.0	V
Internal current consumption	DRV open, V _{FB} = 3 V, 65 kHz	I _{CC1}	1.0	1.3	2.0	mA
	DRV open, V _{FB} = 3 V, 100 kHz		1.1	1.4	2.1	mA
	Cdrv = 1 nF, V _{FB} = 3 V, 65 kHz	I _{CC2}	1.5	2.1	2.9	mA
	Cdrv = 1 nF, V _{FB} = 3 V, 100 kHz		2.0	2.6	3.4	mA
	Skip or before start-up	I _{CC3}	400	500	650	μA
Fault mode (fault or latch)	I _{CC4}	300	430	550	μA	
Off-mode	I _{CC5}	–	25	–	μA	

BROWN-OUT

Brown-out thresholds (option A)	V _{HV} going up V _{HV} going down	V _{HV(start)} V _{HV(stop)}	210 194	229 211	248 228	V
Brown-out thresholds (option B)	V _{HV} going up V _{HV} going down	V _{HV(start)} V _{HV(stop)}	102 94	111 103	120 116	V
Brown-out thresholds (option BAHAB)	V _{HV} going up V _{HV} going down	V _{HV(start)} V _{HV(stop)}	93 90	103 100	113 110	V
Brown-out thresholds (option C)	V _{HV} going up V _{HV} going down	V _{HV(start)} V _{HV(stop)}	87 85	95 93	103 101	V
Brown-out thresholds (option E)	V _{HV} going up	V _{HV(start)}	90	100	110	V
Timer duration for line cycle drop-out (depending on the version)		t _{HV}	42 48	64 73	86 98	ms

X2 DISCHARGE

Comparator hysteresis observed at HV pin		V _{HV(hyst)}	2.0	3.0	4.0	V
HV signal sampling period		t _{sample}	–	1.0	–	ms
Timer duration for no line detection		t _{DET}	21	32	43	ms
Discharge timer duration		t _{DIS}	21	32	43	ms
Shunt regulator voltage at VCC pin during X2 discharge event		V _{CC(dis)}	10.0	11.0	12.0	V

OSCILLATOR

Oscillator frequency 65 kHz version		f _{OSC}	61	65	69	kHz
Oscillator frequency 100 kHz version			94	100	110	
Maximum duty-ratio (corresponding to maximum on time at maximum switching frequency)		D _{MAX}	75	80	85	%
Frequency jittering amplitude, in percentage of F _{OSC}		A _{jitter}	±3.0	±4.0	±5.0	kHz
Frequency jittering modulation frequency		F _{jitter}	85	125	165	Hz

FREQUENCY FOLDBACK

Feedback voltage threshold below which frequency foldback starts	T _J = 25°C	V _{FB(foldS)}	2.4	2.5	2.6	V
Feedback voltage threshold below which frequency foldback is complete	T _J = 25°C	V _{FB(foldE)}	2.05	2.15	2.25	V
Minimum switching frequency	V _{FB} = V _{skip(in)} + 0.1	f _{OSC(min)}	25	28	31	kHz

6. Guaranteed by design.

7. CS pin source current is a sum of I_{bias} and I_{OPC}, thus at V_{HV} = 125 V is observed the I_{bias} only, because I_{OPC} is switched off.

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Table 5. ELECTRICAL CHARACTERISTICS

(For typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{HV} = 125\text{ V}$, $V_{CC} = 11\text{ V}$ unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
OUTPUT DRIVER						
Rise time, 10 to 90% of V_{CC}	$V_{CC} = V_{CC(\text{off})} + 0.2\text{ V}$, $C_{\text{DRV}} = 1\text{ nF}$	t_{rise}	–	40	70	ns
Fall time, 90 to 10% of V_{CC}	$V_{CC} = V_{CC(\text{off})} + 0.2\text{ V}$, $C_{\text{DRV}} = 1\text{ nF}$	t_{fall}	–	30	60	ns
Current capability	$V_{CC} = V_{CC(\text{off})} + 0.2\text{ V}$, $C_{\text{DRV}} = 1\text{ nF}$ DRV high, $V_{\text{DRV}} = 0\text{ V}$ DRV low, $V_{\text{DRV}} = V_{CC}$	$I_{\text{DRV}(\text{source})}$ $I_{\text{DRV}(\text{sink})}$	– –	300 500	– –	mA
Clamping voltage (maximum gate voltage)	$V_{CC} = V_{CC(\text{ovp})} - 0.2\text{ V}$, DRV high, $R_{\text{DRV}} = 33\text{ k}\Omega$, $C_{\text{load}} = 220\text{ pF}$	$V_{\text{DRV}(\text{clamp})}$	10	12	14	V
High-state voltage drop	$V_{CC} = V_{CC(\text{min})} + 0.2\text{ V}$, $R_{\text{DRV}} = 33\text{ k}\Omega$, DRV high	$V_{\text{DRV}(\text{drop})}$	–	–	1	V
CURRENT SENSE						
Input Pull-up Current	$V_{CS} = 0.7\text{ V}$	I_{bias}	–	1	–	μA
Maximum internal current setpoint	$V_{FB} > 3.5\text{ V}$	V_{ILIM}	0.66	0.70	0.74	V
Propagation delay from V_{limit} detection to DRV off	$V_{CS} = V_{\text{ILIM}}$	t_{delay}	–	50	70	ns
Leading Edge Blanking Duration for V_{ILIM}		t_{LEB}	180	250	320	ns
Threshold for immediate fault protection activation		$V_{CS(\text{stop})}$	0.95	1.05	1.15	V
Leading Edge Blanking Duration for $V_{CS(\text{stop})}$ (Note 6)		t_{BCS}	75	120	150	ns
Soft-start duration (option A) Soft-start duration (option B)	From 1 st pulse to $V_{CS} = V_{\text{ILIM}}$	t_{SSTART}	– 3.2	10 4.0	13 4.8	ms
Frozen current setpoint (option H) Frozen current setpoint (option E) Frozen current setpoint (option D)		$V_{\text{I}(\text{freeze})}$	250 145 135	300 210 190	350 270 245	mV
Over voltage protection threshold when DRV is low	V_{CS} going up	$V_{\text{OVP}(\text{CS})}$	1.00	1.05	1.10	V
Blanking duration on OVP detection		$t_{\text{OVP,CS}}$	0.7	1.0	1.3	μs
Delay time constant before OTP confirmation		$t_{\text{OVP,del}}$	–	600	–	ns
INTERNAL SLOPE COMPENSATION						
Slope of the compensation ramp		$S_{\text{comp}(65\text{kHz})}$ $S_{\text{comp}(100\text{kHz})}$	– –	–32.5 –50	– –	mV / μs
FEEDBACK						
Internal pull-up resistor	$T_J = 25^\circ\text{C}$	$R_{\text{FB}(\text{up})}$	30	40	50	$\text{k}\Omega$
V_{FB} to internal current setpoint division ratio (Note 6)		K_{FB}	–	4	–	–
Internal pull-up voltage on the FB pin		$V_{\text{FB}(\text{ref})}$	4.5	5	5.5	V
Offset between FB pin and internal FB divider	$T_J = 25^\circ\text{C}$	$V_{\text{FB}(\text{off})}$	–	0.8	–	V
SKIP CYCLE MODE						
Feedback voltage thresholds for skip mode	V_{FB} going down, $T_J = 25^\circ\text{C}$ V_{FB} going up, $T_J = 25^\circ\text{C}$	$V_{\text{skip}(\text{in})}$ $V_{\text{skip}(\text{out})}$	0.9 1.05	1.0 1.15	1.1 1.25	V
Minimum number of pulses in burst		$n_{\text{P,skip}}$	3	–	–	
Skip out delay		t_{skip}	–	–	38	μs

6. Guaranteed by design.

7. CS pin source current is a sum of I_{bias} and I_{OPC} , thus at $V_{HV} = 125\text{ V}$ is observed the I_{bias} only, because I_{OPC} is switched off.

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Table 5. ELECTRICAL CHARACTERISTICS

 (For typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{HV} = 125\text{ V}$, $V_{CC} = 11\text{ V}$ unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
REMOTE CONTROL ON FB PIN						
The voltage above which the part enters the on mode	$V_{CC} > V_{CC(\text{off})}$, $V_{HV} = 60\text{ V}$	V_{ON}	–	2.2	–	V
The voltage below which the part enters the off mode	$V_{CC} > V_{CC(\text{off})}$	V_{OFF}	0.5	0.6	0.7	V
Minimum hysteresis between the V_{ON} and V_{OFF}	$V_{CC} > V_{CC(\text{off})}$, $V_{HV} = 60\text{ V}$	V_{HYST}	500	–	–	mV
Pull-up current in off mode	$V_{CC} > V_{CC(\text{off})}$	I_{OFF}	–	5	–	μA
Go To Off mode timer	$V_{CC} > V_{CC(\text{off})}$	t_{GTOM}	400	500	600	ms
OVERLOAD PROTECTION						
Fault timer duration		t_{fault}	108	128	178	ms
Fault timer reset time	$V_{CS} < 0.7\text{ V}$, $D < 90\% D_{MAX}$	$t_{\text{fault, res}}$	150	200	250	μs
Autorecovery mode latch-off time duration		t_{autorec}	0.85	1.00	1.35	s
OVERPOWER PROTECTION						
V_{HV} to I_{OPC} conversion ratio		K_{OPC}	–	0.54	–	$\mu\text{A} / \text{V}$
Current flowing out of CS pin (Note 7)	$V_{HV} = 125\text{ V}$ $V_{HV} = 162\text{ V}$ $V_{HV} = 325\text{ V}$ $V_{HV} = 365\text{ V}$	$I_{OPC(125)}$ $I_{OPC(162)}$ $I_{OPC(325)}$ $I_{OPC(365)}$	– – – 105	0 20 110 130	– – – 150	μA
FB voltage above which I_{OPC} is applied	$V_{HV} = 365\text{ V}$	$V_{FB(OPCF)}$	–	2.6	–	V
FB voltage below which is no I_{OPC} applied	$V_{HV} = 365\text{ V}$	$V_{FB(OPCE)}$	–	1.6	–	V
FAULT INPUT						
High threshold	V_{Latch} going up	V_{OVP}	2.43	2.50	2.57	V
Low threshold	V_{Latch} going down, $T_J = 25^\circ\text{C}$	V_{OTP}	0.380	0.400	0.420	V
OTP resistance threshold ($T_J = 25^\circ\text{C}$)	External NTC resistance is going down	R_{OTP}	7.6	8.0	8.5	$\text{k}\Omega$
OTP resistance threshold ($T_J = 80^\circ\text{C}$)	External NTC resistance is going down	R_{OTP}	–	8.5	–	$\text{k}\Omega$
OTP resistance threshold ($T_J = 110^\circ\text{C}$)	External NTC resistance is going down	R_{OTP}	–	9.5	–	$\text{k}\Omega$
Current source for direct NTC connection During normal operation During soft-start	$V_{Latch} = 0.2\text{ V}$	I_{NTC} $I_{NTC(SSTART)}$	30 60	50 100	70 140	μA
Current source for direct NTC connection During normal operation	$V_{Latch} = 0.2\text{ V}$, $T_J = 25^\circ\text{C}$	I_{NTC}	47	50	53	μA
Blanking duration on high latch detection		$t_{Latch(OVP)}$	35	50	70	μs
Blanking duration on low latch detection		$t_{Latch(OTP)}$	–	350	–	μs
Clamping voltage	$I_{Latch} = 0\text{ mA}$ $I_{Latch} = 1\text{ mA}$	$V_{\text{clamp0(Latch)}}$ $V_{\text{clamp1(Latch)}}$	1.0 1.8	1.2 2.4	1.4 3.0	V
TEMPERATURE SHUTDOWN						
Temperature shutdown	T_J going up	T_{TSD}	–	150	–	$^\circ\text{C}$
Temperature shutdown hysteresis	T_J going down	$T_{TSD(HYS)}$	–	30	–	$^\circ\text{C}$

6. Guaranteed by design.

 7. CS pin source current is a sum of I_{bias} and I_{OPC} , thus at $V_{HV} = 125\text{ V}$ is observed the I_{bias} only, because I_{OPC} is switched off.

TYPICAL CHARACTERISTIC

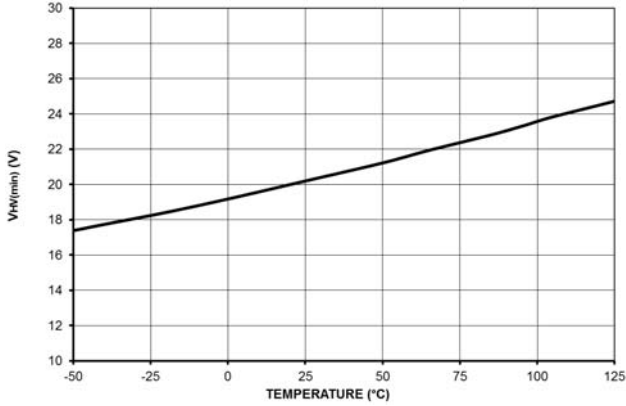


Figure 3. Minimum Voltage for HV Current Source Operation V_{HV(min)}

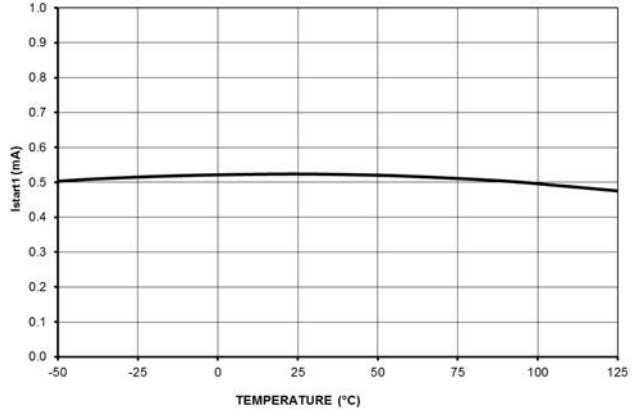


Figure 4. High Voltage Startup Current Flowing Out of V_{CC} Pin I_{start1} of V_{CC} Pin Fault/Short

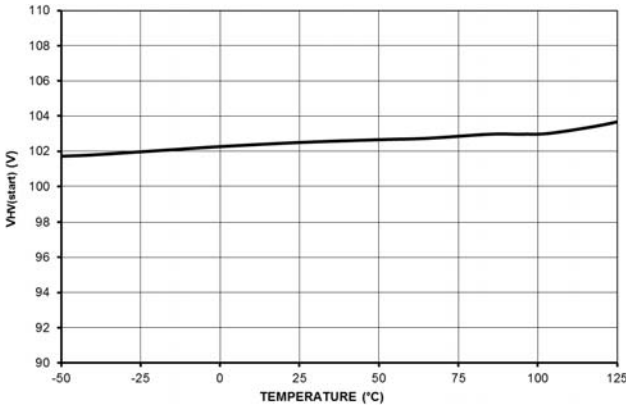


Figure 5. HV Pin Device Startup Threshold V_{HV(start)}

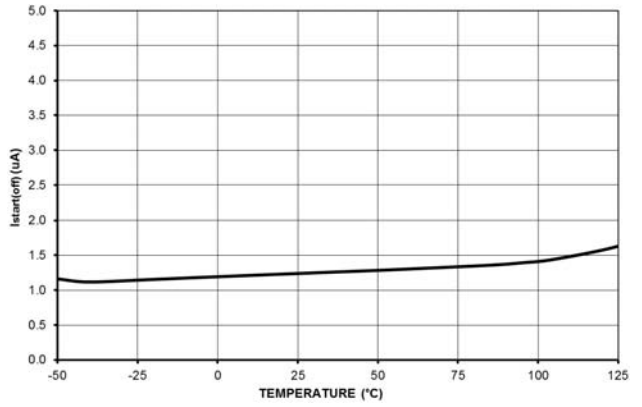


Figure 6. Off-state Leakage Current from HV Pin I_{start(off)}

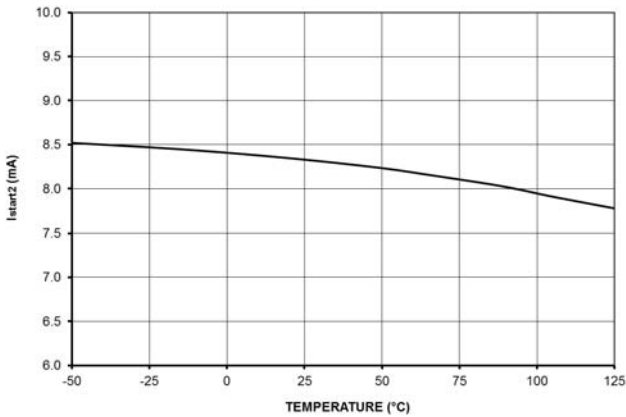


Figure 7. High Voltage Startup Current Flowing Out of V_{CC} Pin I_{start2}

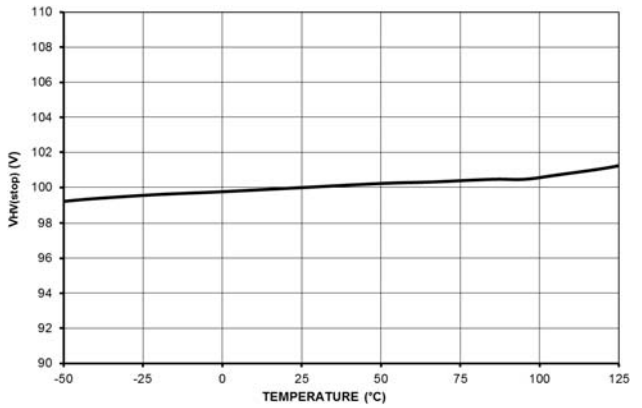


Figure 8. HV Pin Device Stop Threshold V_{HV(stop)}

NCP12400

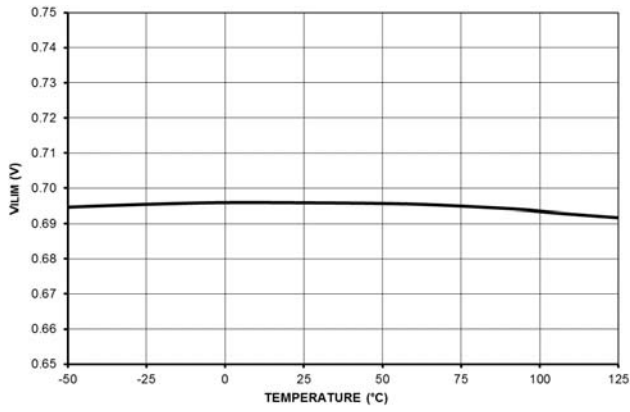


Figure 9. Maximum Internal Current Setpoint V_{ILIM}

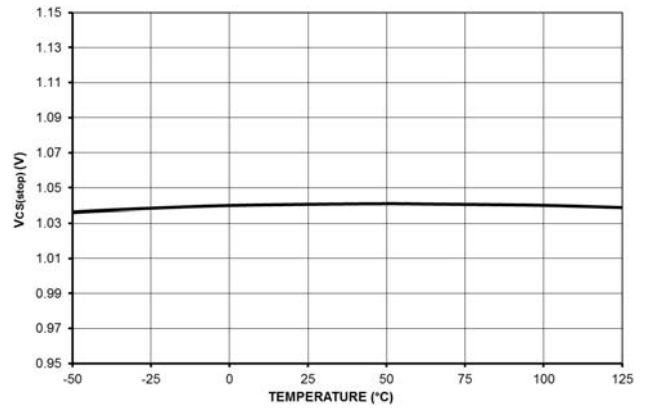


Figure 10. Threshold for the Very Fast Fault Protection Activation $V_{CS(stop)}$

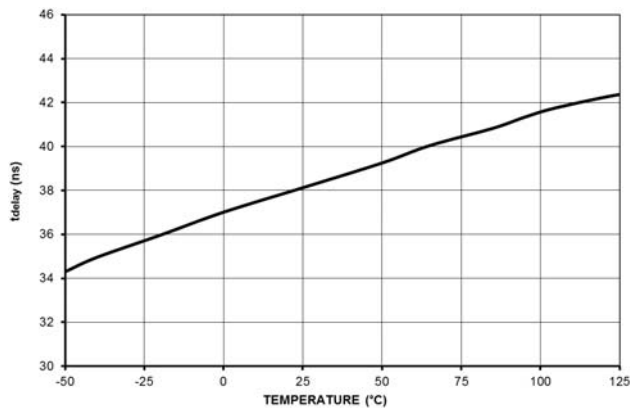


Figure 11. Propagation Delay t_{delay}

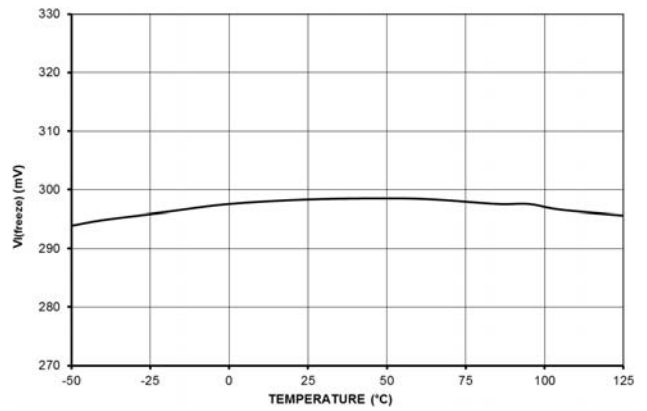


Figure 12. Frozen Current Setpoint $V_{I(freeze)}$ for the Light Load Operation

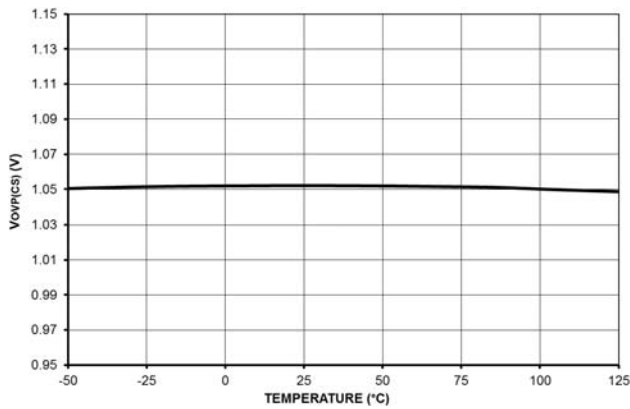


Figure 13. Over Voltage Protection Threshold at CS Pin $V_{OVP(CS)}$

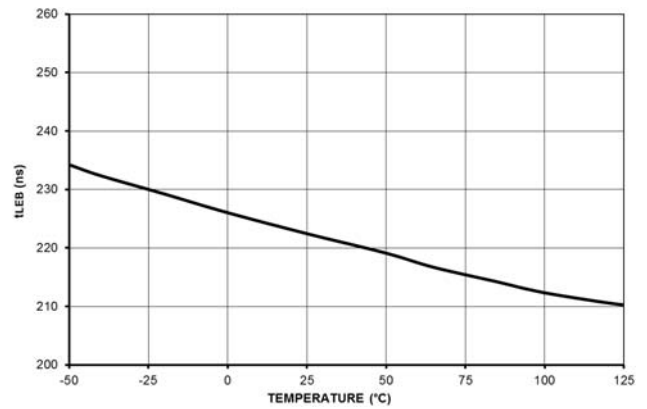


Figure 14. Leading Edge Blanking Duration t_{LEB}

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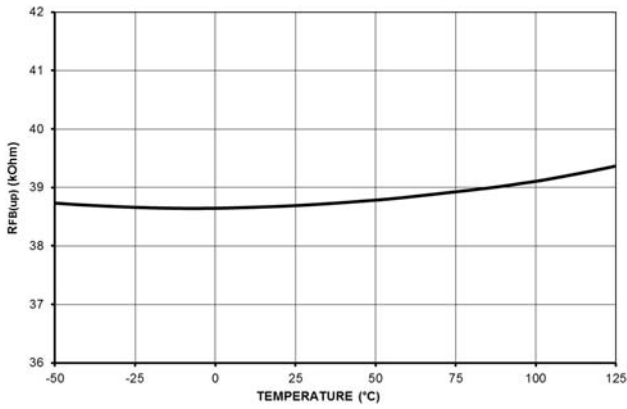


Figure 15. FB Pin Internal Pull-up Resistor $R_{FB(up)}$

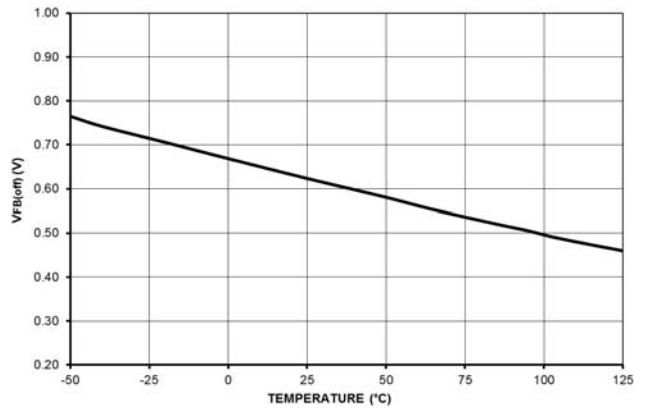


Figure 16. Built in Offset between FB Pin and Internal Divider $V_{FB(off)}$

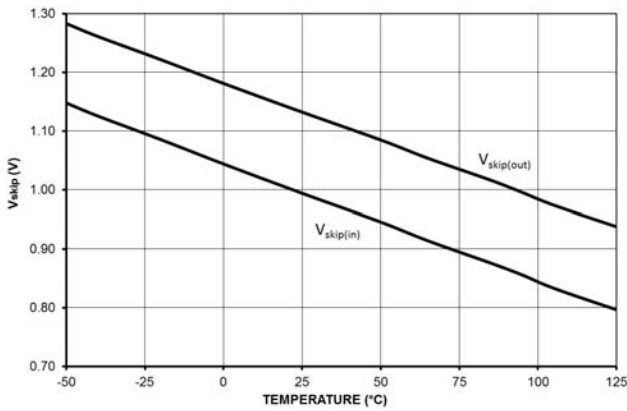


Figure 17. FB Pin Skip-In and Skip-Out Levels $V_{skip(in)}$ and $V_{skip(out)}$

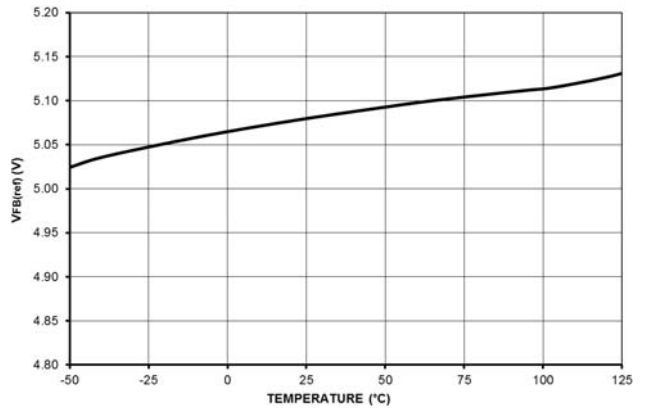


Figure 18. FB Pin Open Voltage $V_{FB(ref)}$

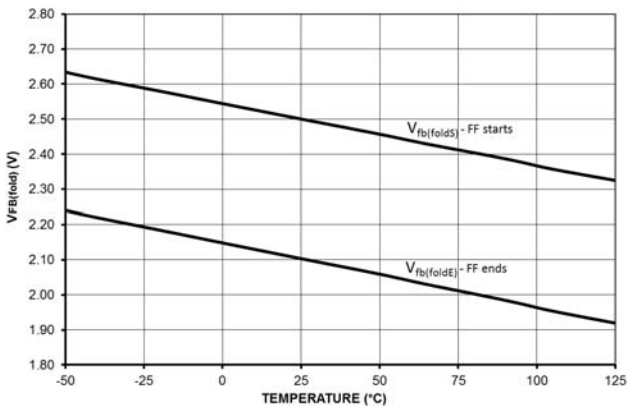


Figure 19. FB Pin Frequency Foldback Thresholds $V_{FB(foldS)}$ and $V_{FB(foldE)}$

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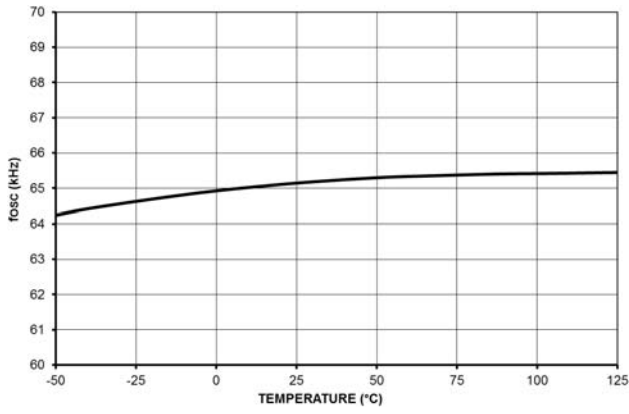


Figure 20. Oscillator Switching Frequency f_{osc}

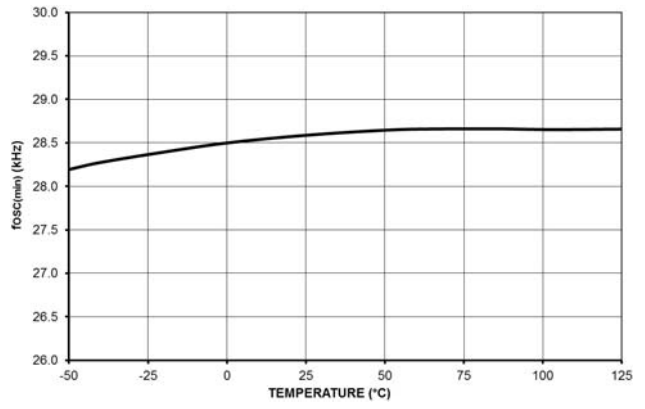


Figure 21. Minimum Switching Frequency $f_{osc(min)}$

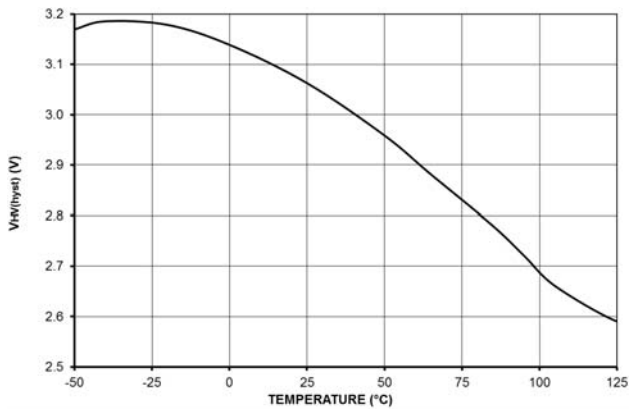


Figure 22. X2 Discharge Comparator Hysteresis Observed at HV Pin $V_{HV(hyst)}$

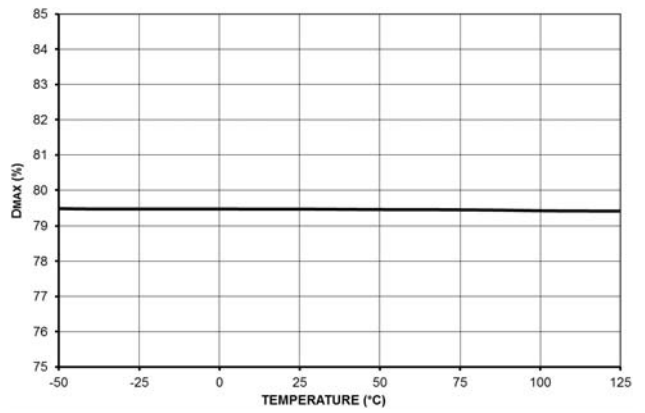


Figure 23. Maximum Duty Cycle D_{MAX}

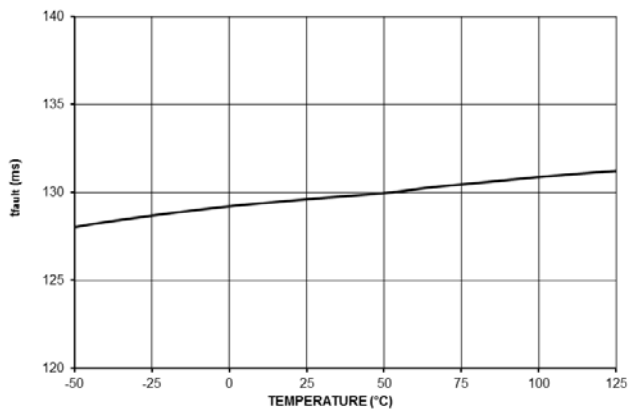


Figure 24. The Fault Timer Duration t_{fault}

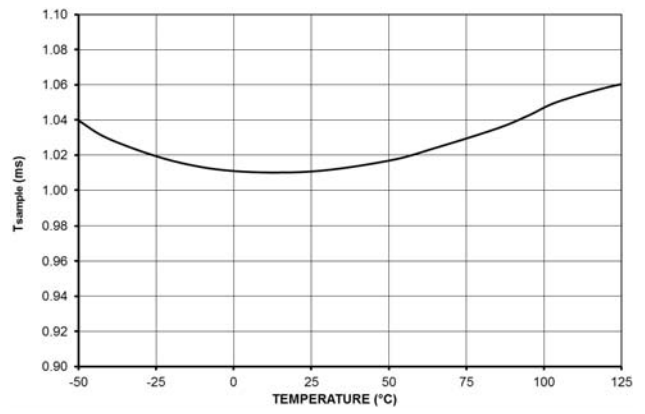


Figure 25. HV Signal Sampling Period T_{sample}

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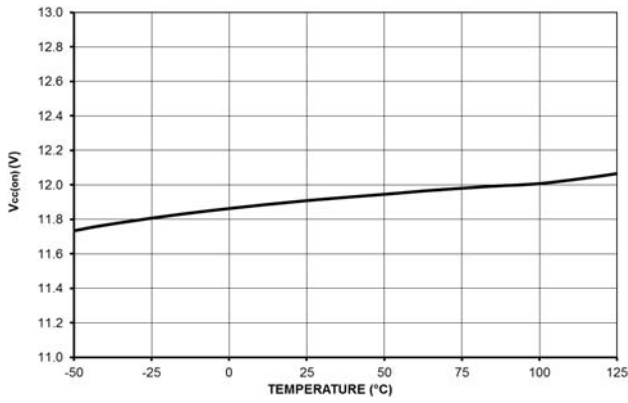


Figure 26. V_{CC} Turn-on Threshold Level, V_{CC} Going Up HV Current Source Stop Threshold V_{CC(on)}

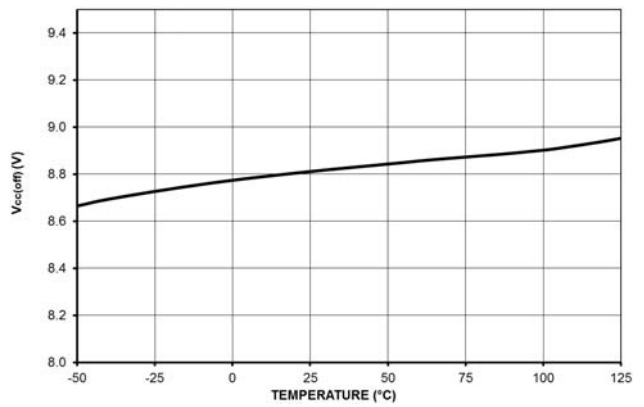


Figure 27. V_{CC} Turn-off Threshold (UVLO) V_{CC(off)}

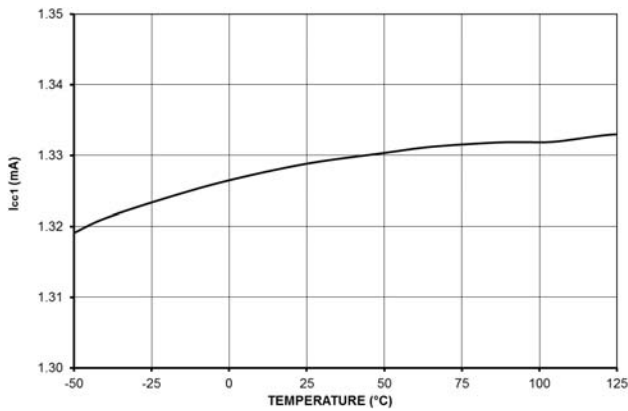


Figure 28. Internal Current Consumption when DRV Pin is Unloaded I_{CC1}

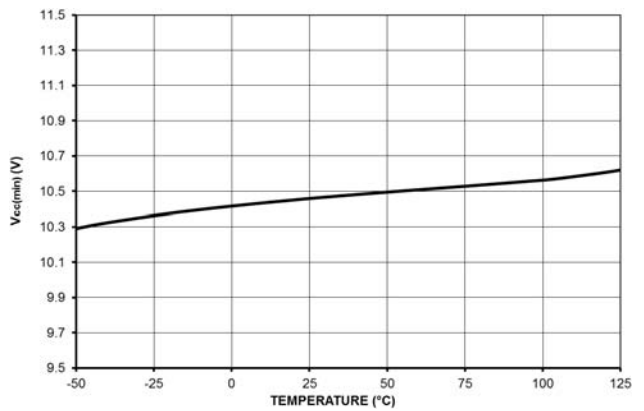


Figure 29. HV Current Source Restart Threshold V_{CC(min)}

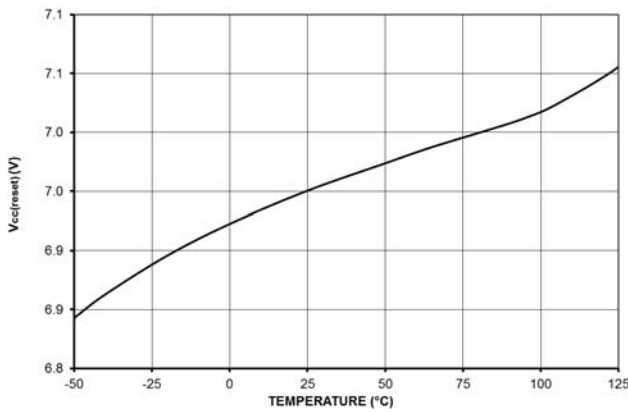


Figure 30. V_{CC} Decreasing Level at which the Internal Logic Resets V_{CC(reset)}

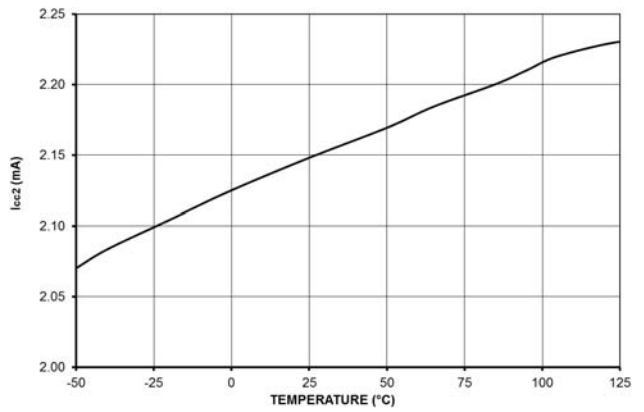


Figure 31. Internal Current Consumption when DRV Pin is Loaded by 1 nF Capacitance I_{CC2}

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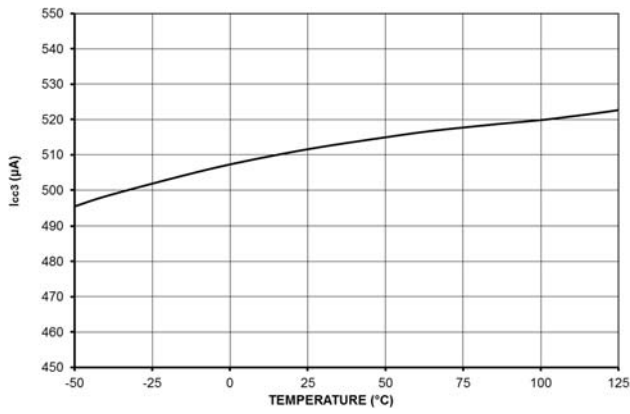


Figure 32. Internal Current Consumption in Skip Mode I_{CC3}

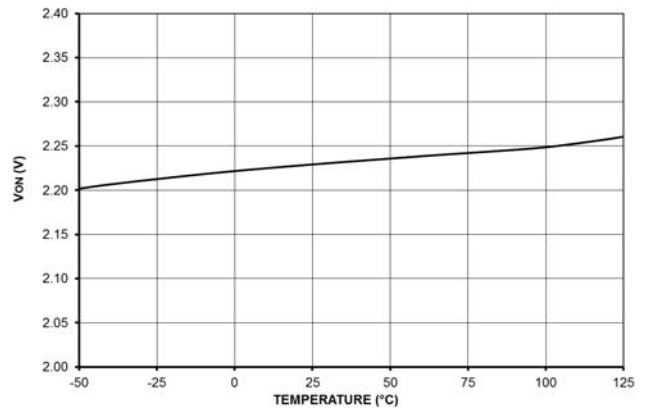


Figure 33. FB Pin Voltage Level Above which is Entered Normal Operating Mode V_{ON}

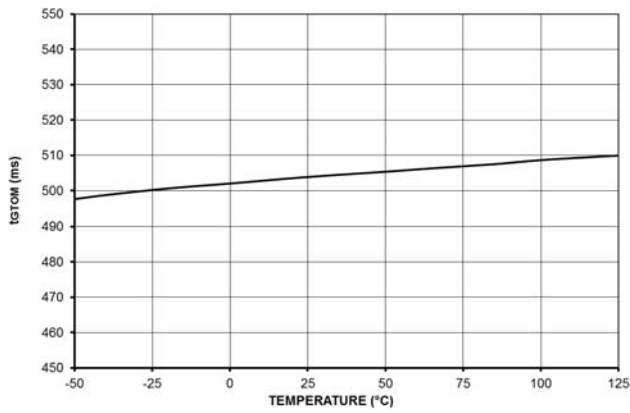


Figure 34. Go To Off Mode Timer Duration t_{GTOM}

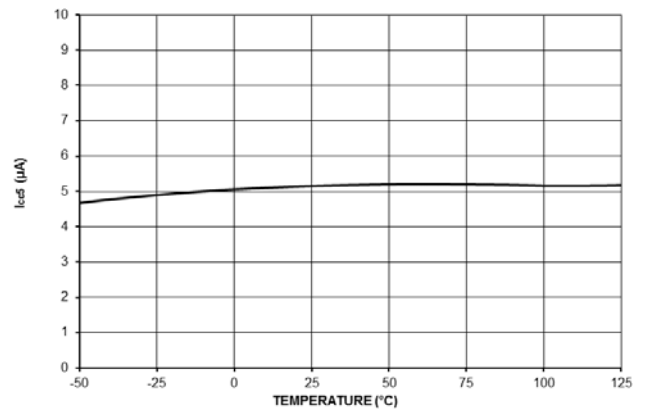


Figure 35. Internal Current Consumption in Off Mode I_{CC5}

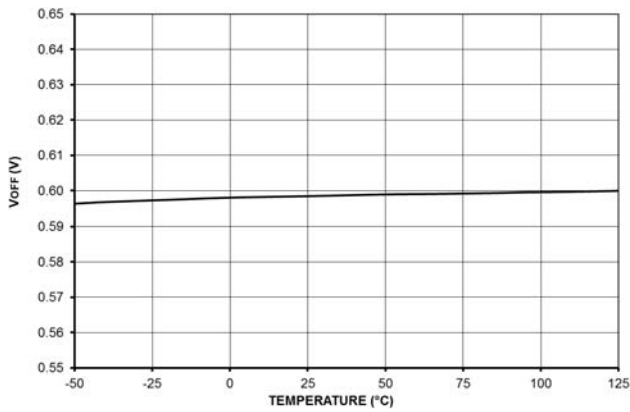


Figure 36. FB Pin Voltage Level Below which is Entered Off Mode V_{OFF}

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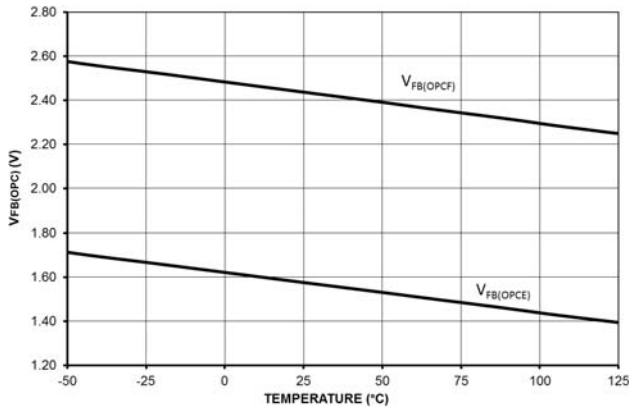


Figure 37. FB Pin Voltage Thresholds for Overpower Compensation

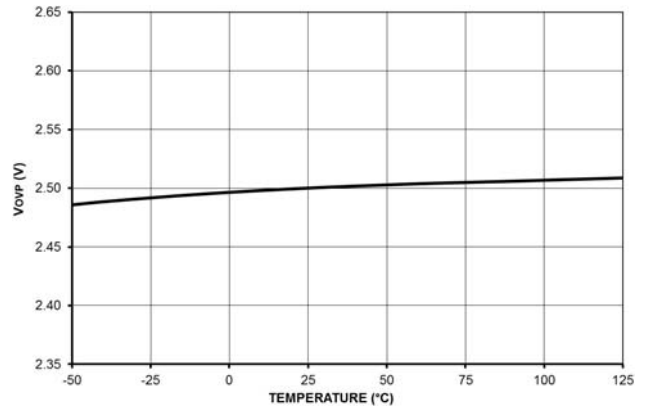


Figure 38. Fault Pin High Threshold for OVP V_{OVP}

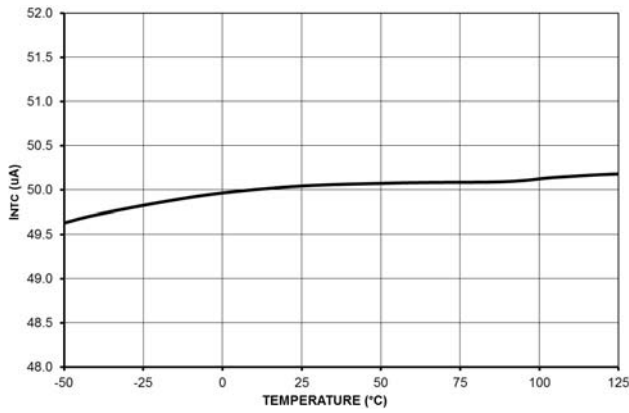


Figure 39. Current I_{NTC} Sourced Out from the Fault Pin, allowing Direct NTC Connection

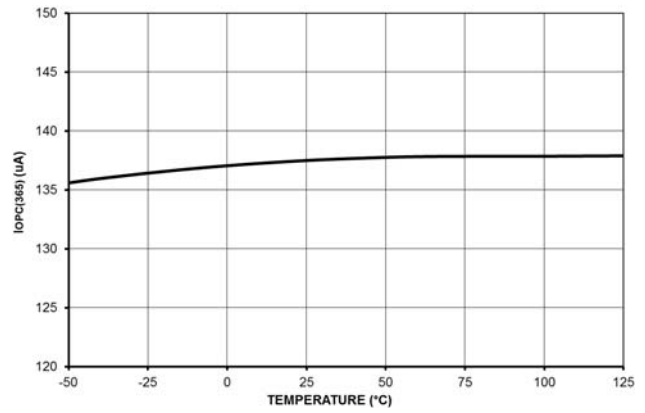


Figure 40. Current Flowing Out from CS Pin for Over Power Compensation @ 365 V at HV Pin I_{OP(365)}

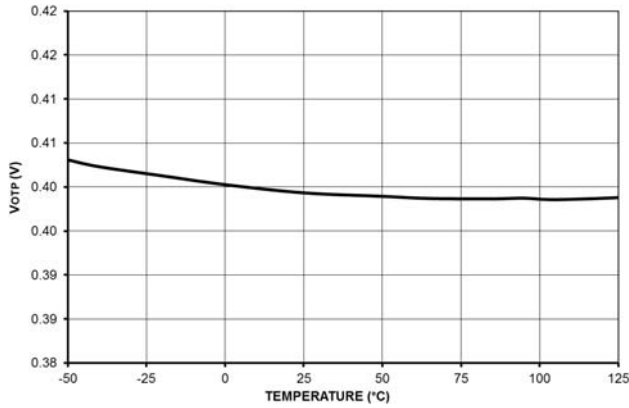
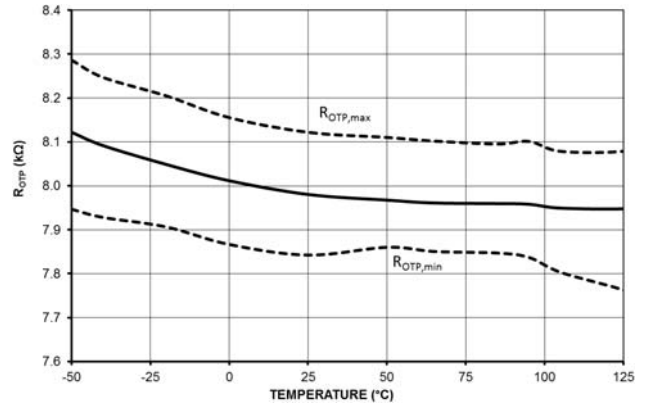


Figure 41. Fault Pin Low Threshold for OTP V_{OTP}



NOTE: The OTP resistance maximum and minimum courses are not the guaranteed limits, but the maximum and minimum measured data values from the device characterization.

Figure 42. The OTP Resistance Threshold R_{OTP}

APPLICATION INFORMATION

Functional Description

The NCP12400 includes all necessary features to build a safe and efficient power supply based on a fixed-frequency flyback converter. The NCP12400 is a multimode controller as illustrated in Figure 43. The mode of operation depends upon line and load condition. Under all modes of operation, the NCP12400 terminates the DRV signal based on the switch current. Thus, the NCP12400 always operates in current mode control so that the power MOSFET current is always limited.

Under normal operating conditions, the FB pin commands the operating mode of the NCP12400 at the voltage thresholds shown in Figure 43. At normal rated operating loads (from 100% to approximately 33% full rated power) the NCP12400 controls the converter in a fixed-frequency PWM mode. It can operate in the continuous conduction mode (CCM) or discontinuous conduction mode (DCM) depending upon the input voltage and loading conditions. If the controller is used in CCM with a wide input voltage range, the duty-ratio may increase up to 50%. The build-in slope compensation prevents the appearance of sub-harmonic oscillations in this operating area.

For loads that are between approximately 32% and 10% of full rated power, the converter operates in frequency foldback mode (FFM). If the feedback pin voltage is lower than 1.4 V the peak switch current is kept constant and the output voltage is regulated by modulating the switching frequency for a given and fixed input voltage V_{HV} .

Effectively, operation in FFM results in the application of constant volt-seconds to the flyback transformer each switching cycle. Voltage regulation in FFM is achieved by varying the switching frequency in the range from 65 kHz to 28 kHz. For extremely light loads (below approximately 6% full rated power), the converter is controlled using bursts of 28 kHz pulses. This mode is known as skip mode. The FFM, keeping constant peak current and skip mode allows design of the power supplies with increased efficiency under the light loading conditions. Keep in mind that the aforementioned boundaries of steady-state operation are approximate because they are subject to converter design parameters.

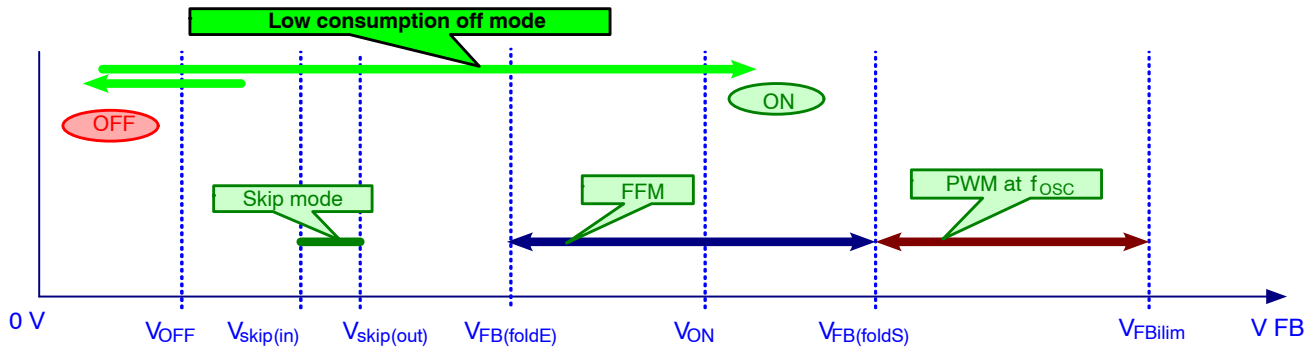
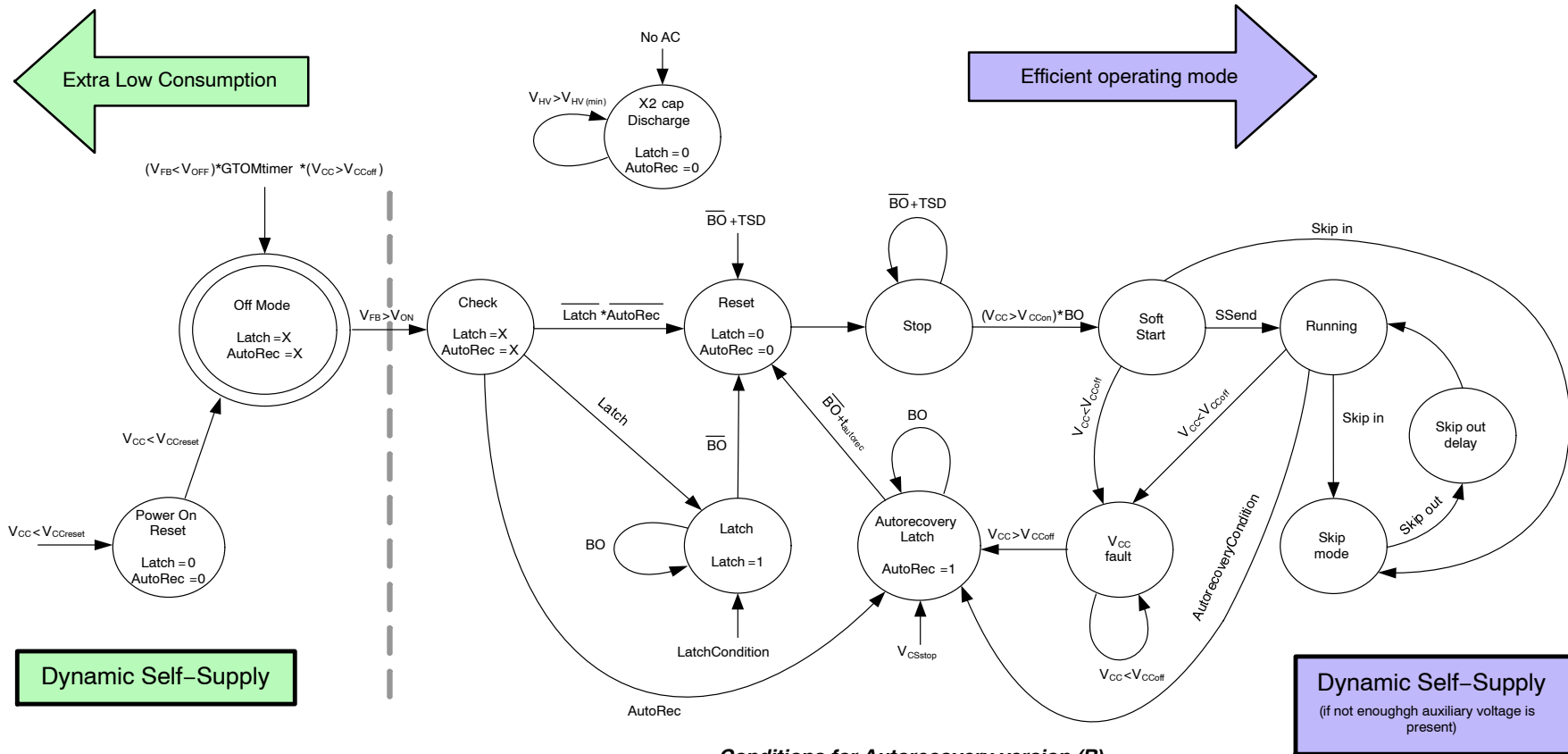


Figure 43. Mode Control with FB Pin Voltage

There was implemented the low consumption off mode allowing to reach extremely low no load input power. This mode is controlled by the FB pin and allows the remote control (or secondary side control) of the power supply shut-down. Most of the device internal circuitry is unbiased in the low consumption off mode. Only the FB pin control circuitry and X2 cap discharging circuitry is operating in the low consumption off mode. If the voltage at feedback pin

decreases below the 0.6 V the controller will enter the low consumption off mode. The controller can start if the FB pin voltage increases above the 2.2 V level.

See the detailed status diagrams for the both versions fully latched A and the autorecovery B on the following figures. The basic status of the device after wake-up by the V_{CC} is the off mode and mode is used for the overheating protection mode if the thermal shutdown protection is activated.



Conditions for Latched version (A)

$$LatchCondition = OVP + OTP + V_{CCovp} * t_{VCC(blank)} + (V_{CSstop} * 4clk) + (V_{ILIM} + MaxDC) * t_{fault}$$

Conditions for Autorecovery version (B)

$$LatchCondition = OVP + OTP + V_{CCovp} * t_{VCC(blank)}$$

$$AutoRecoveryCondition = (V_{CSstop} * 4clk) + (V_{ILIM} + MaxDC) * t_{fault} + (V_{CC} < V_{CCoff}) * t_{VCC(blank)}$$

Figure 44. Operating Status Diagram of the Device

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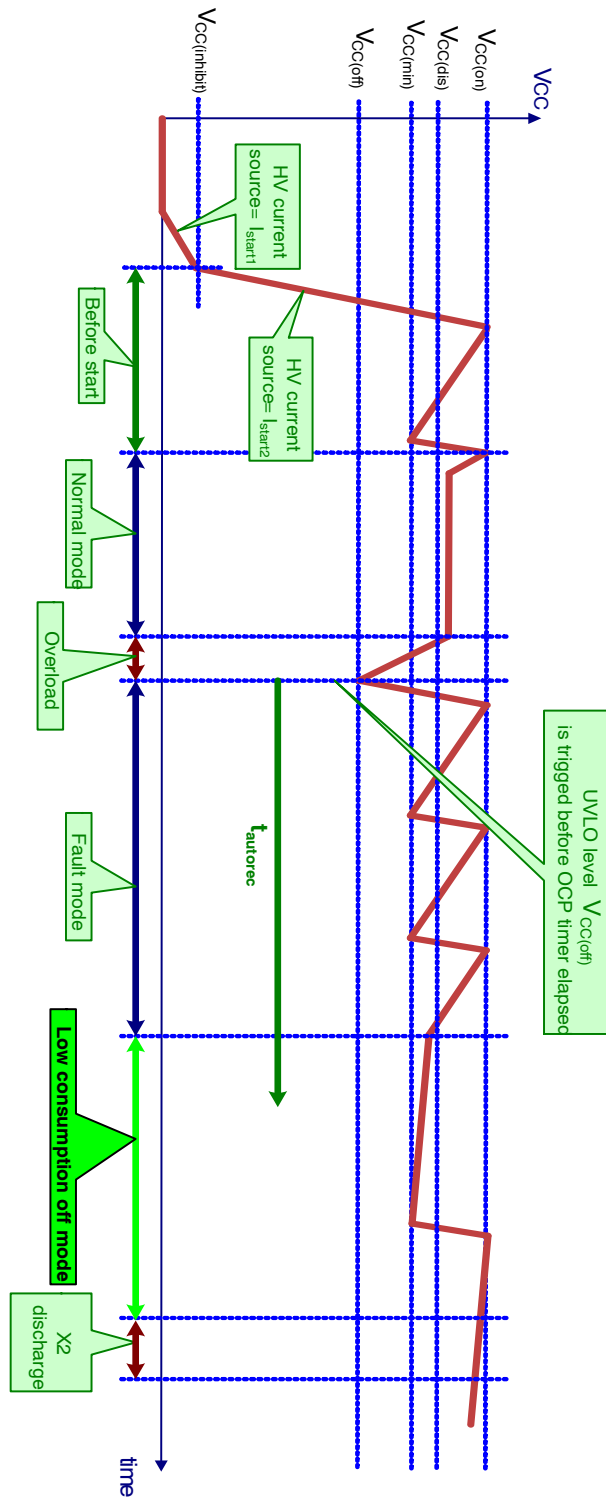


Figure 45. VCC Management Timing Diagram

The information about the fault (permanent Latch or Autorecovery) is kept during the low consumption off mode due the safety reason. The reason is not to allow unlatch the device by the remote control being in off mode.

Start-up of the Controller

At start-up, the current source turns on when the voltage on the HV pin is higher than $V_{HV(min)}$, and turns off when V_{CC} reaches $V_{CC(on)}$, then turns on again when V_{CC} reaches

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$V_{CC(min)}$, until the input voltage is high enough to ensure a proper start-up, i.e. when V_{HV} reaches $V_{HV(start)}$. The controller actually starts the next time V_{CC} reaches $V_{CC(on)}$. The controller then delivers pulses, starting with a soft-start period t_{SSTART} during which the peak current linearly increases before the current-mode control takes over.

Even though the Dynamic Self-Supply is able to maintain the V_{CC} voltage between $V_{CC(on)}$ and $V_{CC(min)}$ by turning the HV start-up current source on and off, it can only be used in light load condition, otherwise the power dissipation on

the die would be too much. As a result, an auxiliary voltage source is needed to supply V_{CC} during normal operation.

The Dynamic Self-Supply is useful to keep the controller alive when no switching pulses are delivered, e.g. in brown-out condition, or to prevent the controller from stopping during load transients when the V_{CC} might drop. The NCP12400 accepts a supply voltage as high as 28 V, with an overvoltage threshold $V_{CC(ovp)}$ that latches the controller off.

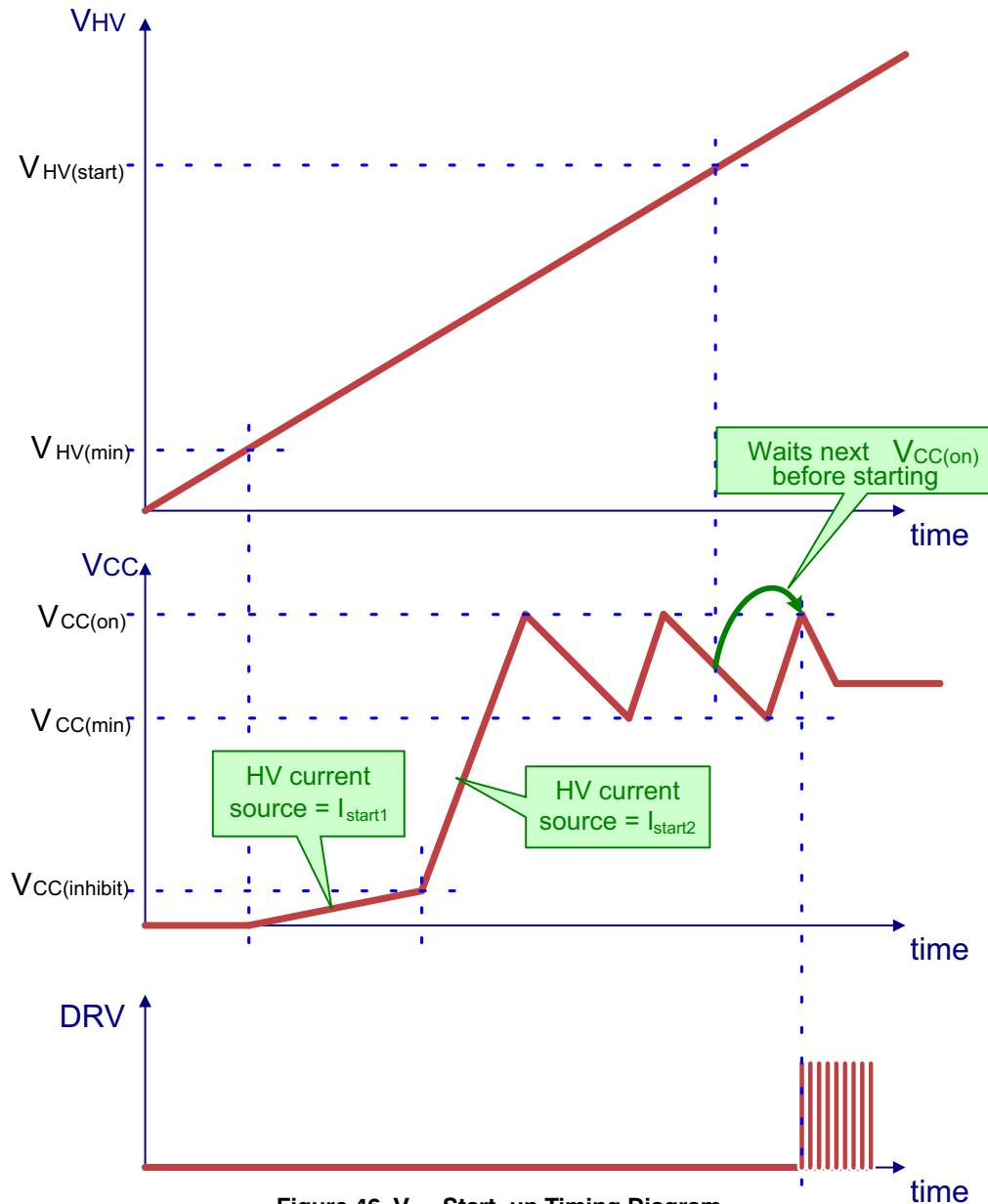


Figure 46. V_{CC} Start-up Timing Diagram

For safety reasons, the start-up current is lowered when V_{CC} is below $V_{CC(inhibit)}$, to reduce the power dissipation in case the V_{CC} pin is shorted to GND (in case of V_{CC} capacitor failure, or external pull-down on V_{CC} to disable the

controller). There is only one condition for which the current source doesn't turn on when V_{CC} reaches $V_{CC(inhibit)}$: the voltage on HV pin is too low (below $V_{HV(min)}$).

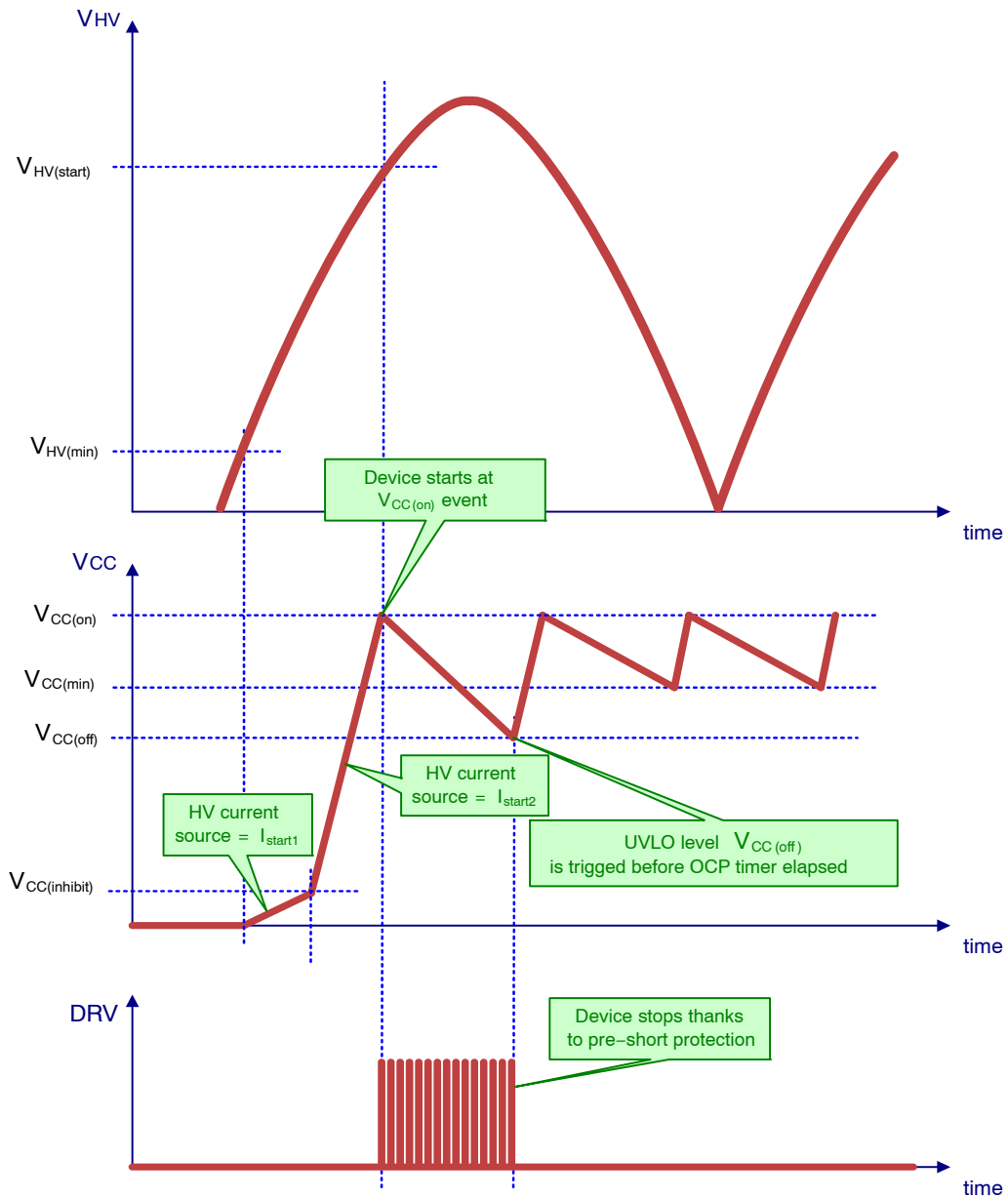


Figure 47. Latch After the Preshort

HV Sensing of Rectified AC Voltage

The NCP12400 features on its HV pin a true ac line monitoring circuitry. It includes a minimum start-up threshold and an autorecovery brown-out protection; both of them independent of the ripple on the input voltage. It is allowed only to work with an unfiltered, rectified ac input to ensure the X2 capacitor discharge function as well, which is described in following. The brown-out protection

thresholds are fixed, but they are designed to fit most of the standard ac-dc conversion applications.

When the input voltage goes below V_{HV(stop)}, a brown-out condition is detected, and the controller stops. The HV current source maintains V_{CC} between V_{CC(on)} and V_{CC(min)} levels until the input voltage is back above V_{HV(start)}.

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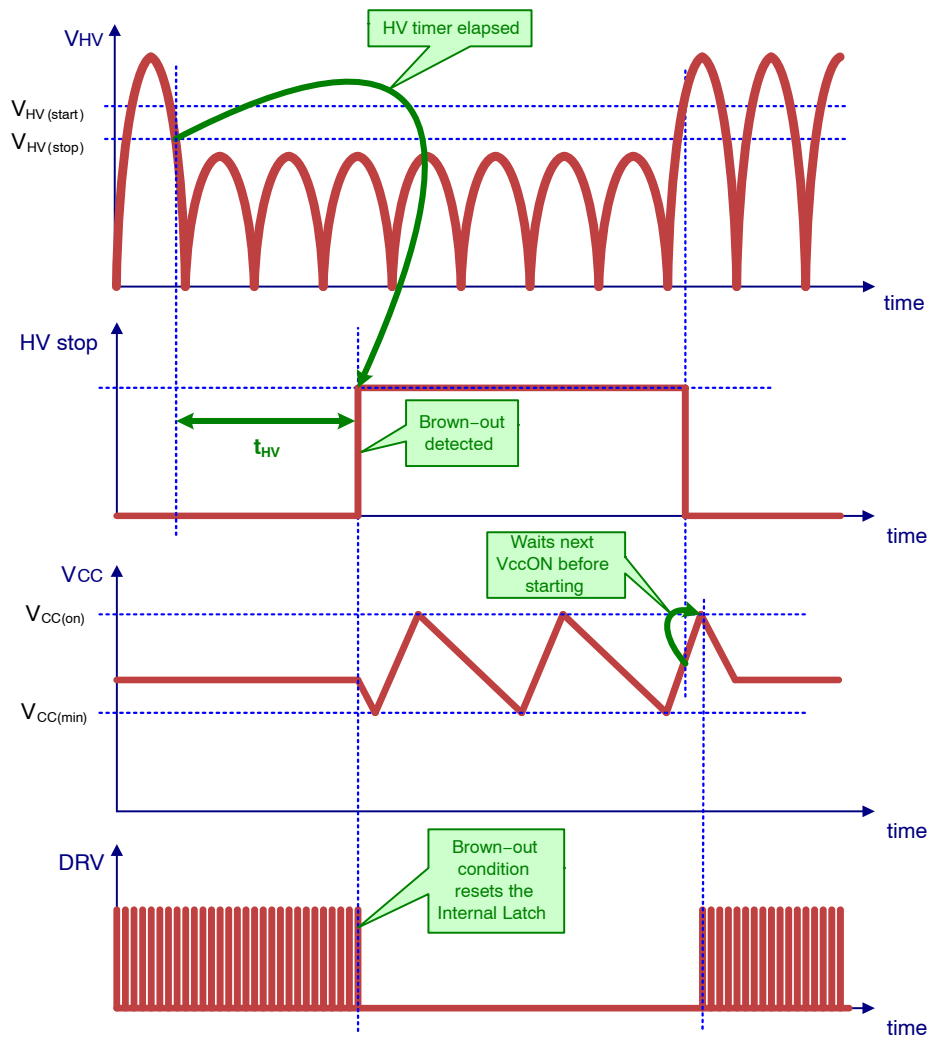


Figure 48. Ac Line Drop-out Timing Diagram

When V_{HV} crosses the $V_{HV(start)}$ threshold, the controller can start immediately. When it crosses $V_{HV(stop)}$, it triggers a timer of duration t_{HV} , this ensures that the controller doesn't stop in case of line cycle drop-out.

When V_{HV} crosses the $V_{HV(start)}$ threshold, the controller starts when the V_{CC} crosses the next $V_{CC(on)}$ event. When it crosses $V_{HV(stop)}$, it triggers a timer of duration t_{HV} , this ensures that the controller doesn't stop in case of line cycle

drop-out. The device restart after the ac line voltage drop-out is protected to the parasitic restart initiated e.g. the spikes induced at HV pin immediately after the device is stopped by the residual energy in the EMI filter. The device restart is allowed only after the 1st watch dog signal event. The basic principle is shown at Figure 49 and detail of the device restart is shown at Figure 50.

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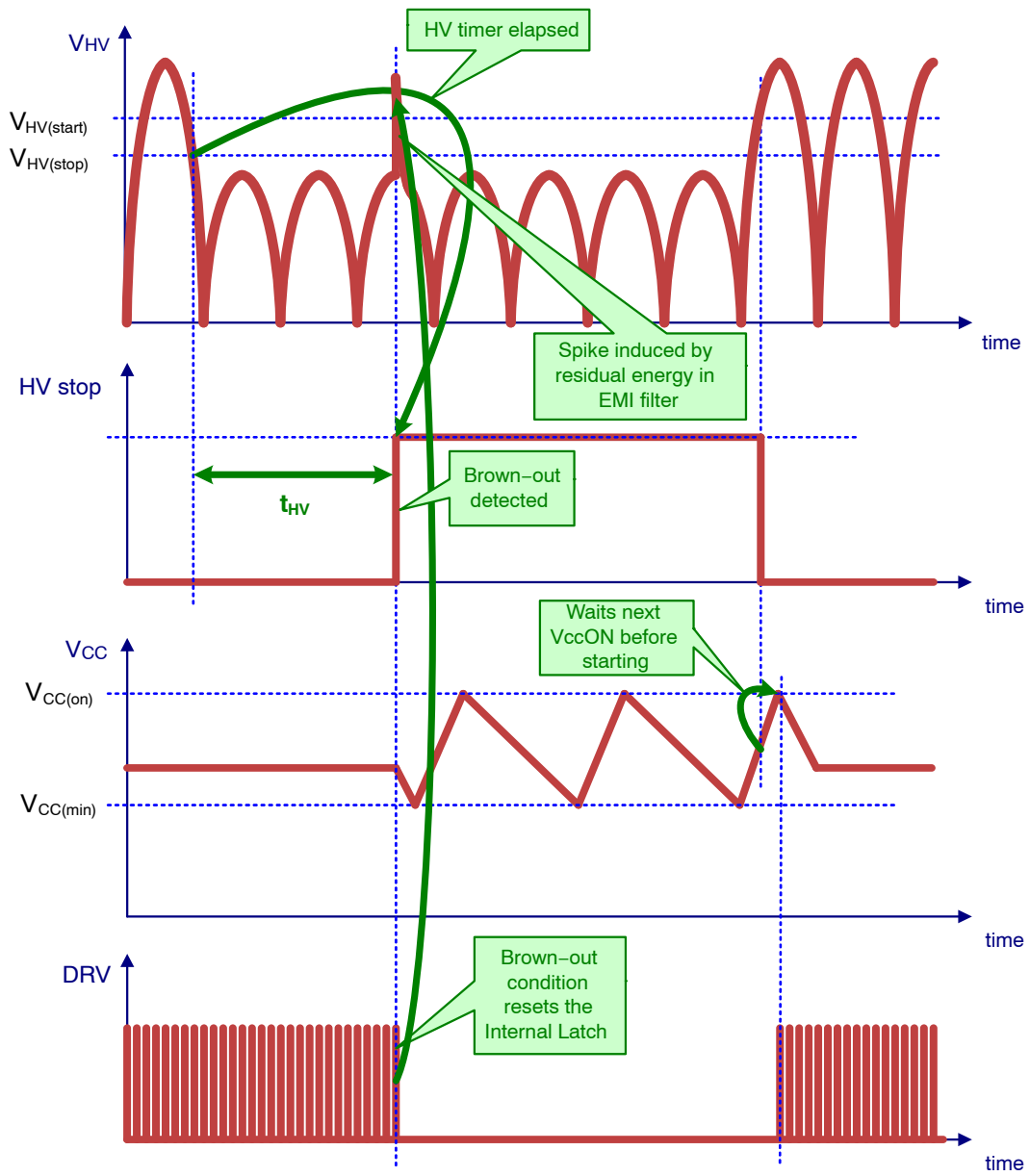


Figure 49. Ac Line Drop-out Timing Diagram with the Parasitic Spike

NCP12400

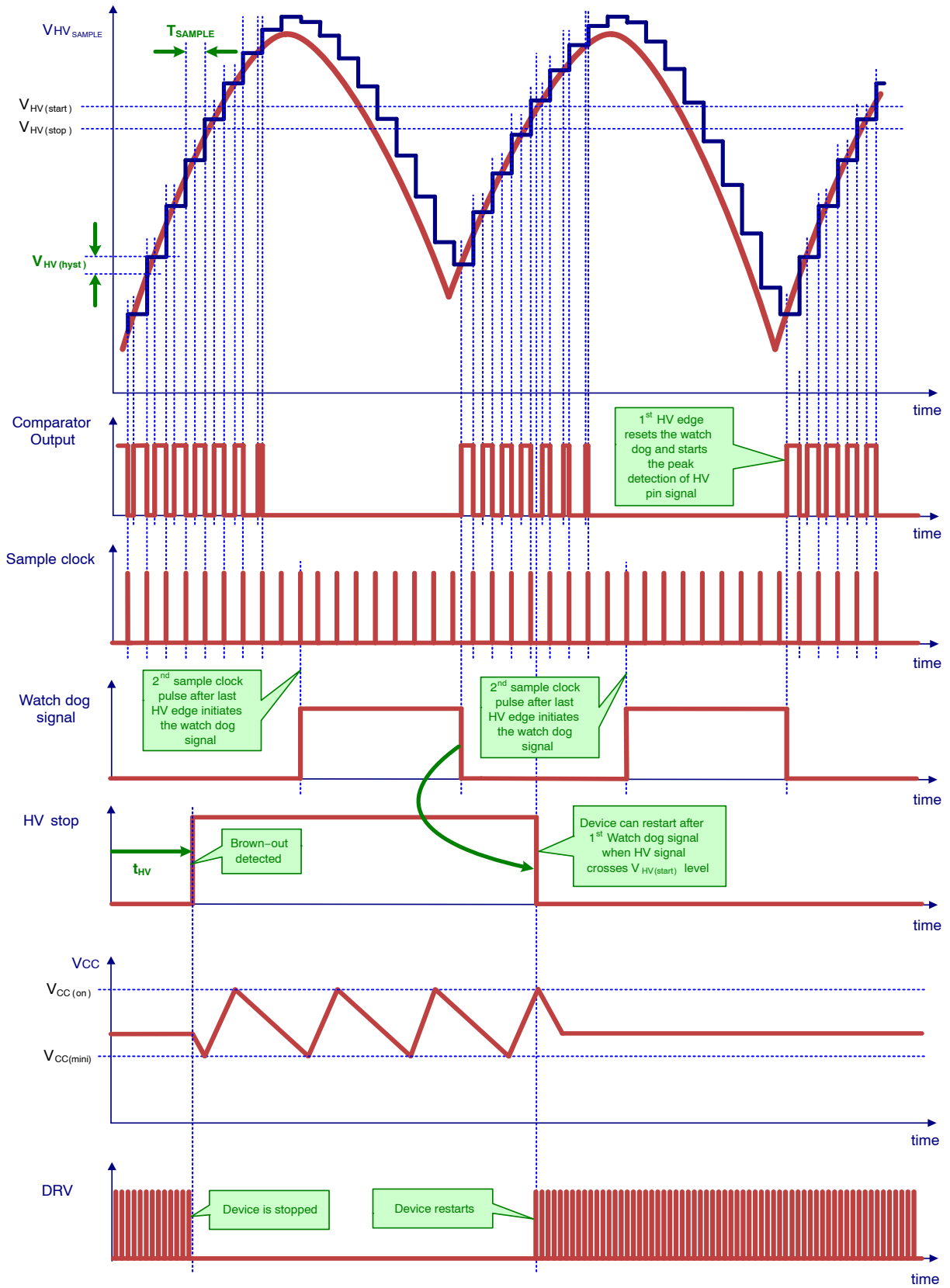


Figure 50. Detailed Timing Diagram of the Device Restart after the Short ac Line Drop-out

X2 Cap Discharge Feature

The X2 capacitor discharging feature is offered by usage of the NCP12400. This feature save approx. 16 mW – 25 mW input power depending on the EMI filter X2 capacitors volume and it saves the external components count as well. The discharge feature is ensured via the start-up current source with a dedicated control circuitry for this function. The X2 capacitors are being discharged by current defined as I_{start2} when this need is detected.

There is used a dedicated structure called ac line unplug detector inside the X2 capacitor discharge control circuitry. See the Figure 51 for the block diagram for this structure and Figures 52, 53, 54 and 55 for the timing diagrams. The basic idea of ac line unplug detector lies in comparison of the direct sample of the high voltage obtained via the high voltage sensing structure with the delayed sample of the high voltage. The delayed signal is created by the sample & hold structure.

The comparator used for the comparison of these signals is without hysteresis inside. The resolution between the slopes of the ac signal and dc signal is defined by the sampling time T_{SAMPLE} and additional internal offset N_{OS} . These parameters ensure the noise immunity as well. The additional offset is added to the picture of the sampled HV signal and its analog sum is stored in the C_1 storage capacitor. If the voltage level of the HV sensing structure output crosses this level the comparator CMP output signal resets the detection timer and no dc signal is detected. The additional offset N_{OS} can be measured as the $V_{HV(hyst)}$ on the HV pin. If the comparator output produces pulses it means that the slope of input signal is higher than set resolution level and the slope is positive. If the comparator output produces the low level it means that the slope of input signal is lower than set resolution level or the slope is negative. There is used the detection timer which is reset by any edge of the comparator output. It means if no edge comes before the timer elapses there is present only dc signal or signal with the small ac ripple at the HV pin. This type of the ac detector detects only the positive slope, which fulfils the requirements for the ac line presence detection.

In case of the dc signal presence on the high voltage input, the direct sample of the high voltage obtained via the high voltage sensing structure and the delayed sample of the high voltage are equivalent and the comparator produces the low level signal during the presence of this signal. No edges are present at the output of the comparator, that's why the detection timer is not reset and dc detect signal appears.

The minimum detectable slope by this ac detector is given by the ration between the maximum hysteresis observed at HV pin $V_{HV(hyst),max}$ and the sampling time:

$$S_{min} = \frac{V_{HV(hyst),max}}{T_{sample}} \quad (eq. 1)$$

Than it can be derived the relationship between the minimum detectable slope and the amplitude and frequency of the sinusoidal input voltage:

$$\begin{aligned} V_{max} &= \frac{V_{HV(hyst),max}}{2 \cdot \pi \cdot f \cdot T_{sample}} = \frac{5}{2 \cdot \pi \cdot 35 \cdot 1 \cdot 10^{-3}} = \\ &= 22.7 \text{ V} \end{aligned} \quad (eq. 2)$$

The minimum detectable AC RMS voltage is 16 V at frequency 35 Hz, if the maximum hysteresis is 5 V and sampling time is 1 ms.

The X2 capacitor discharge feature is available in any controller operation mode to ensure this safety feature. The detection timer is reused for the time limiting of the discharge phase, to protect the device against overheating. The discharging process is cyclic and continues until the ac line is detected again or the voltage across the X2 capacitor is lower than $V_{HV(min)}$. This feature ensures to discharge quite big X2 capacitors used in the input line filter to the safe level. **It is important to note that it is not allowed to connect HV pin to any dc voltage due this feature. e.g. directly to bulk capacitor.**

During the HV sensing or X2 cap discharging the V_{CC} net is kept above the $V_{CC(off)}$ voltage by the Self-Supply in any mode of device operation to supply the control circuitry. During the discharge sequence is not allowed to start-up the device.

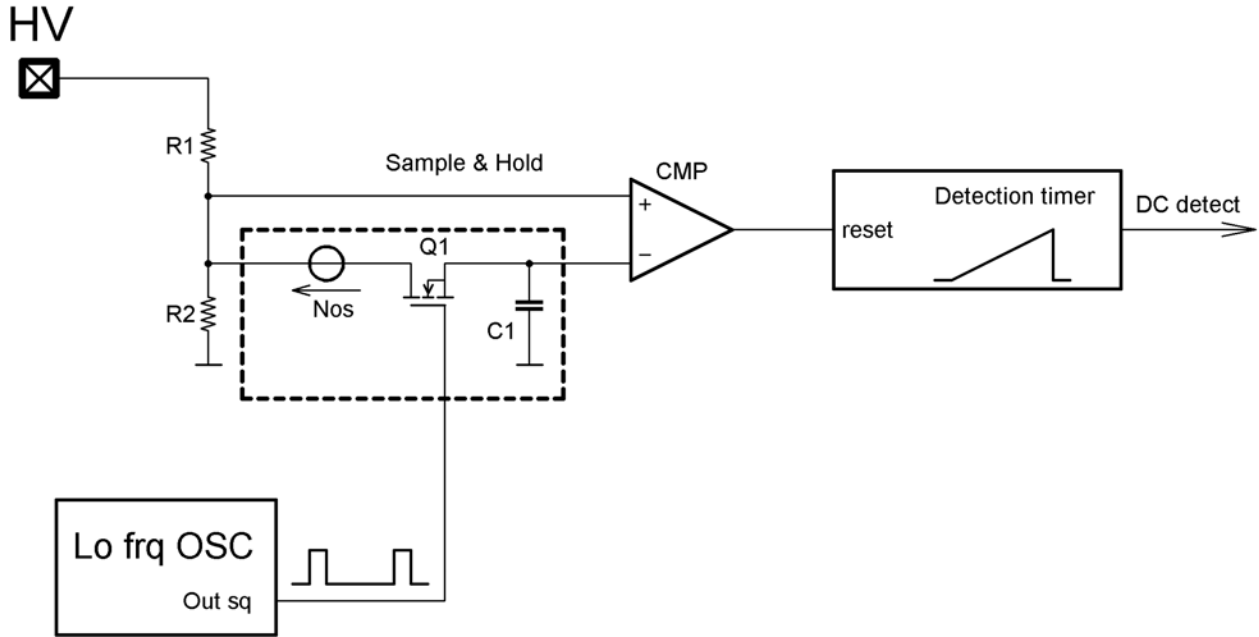


Figure 51. The ac Line Unplug Detector Structure Used for X2 Capacitor Discharge System

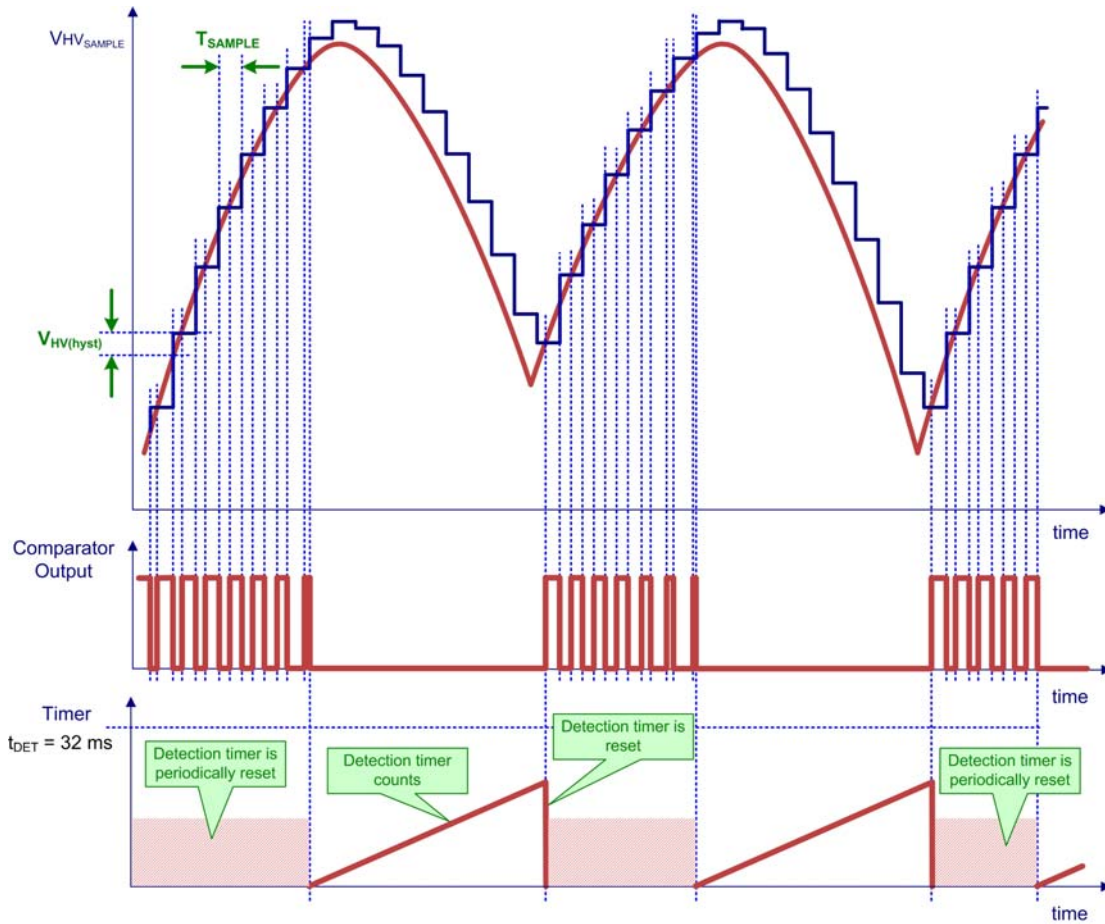


Figure 52. The ac Line Unplug Detector Timing Diagram