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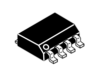
NCP1240

Fixed Frequency Current Mode Controller for Flyback Converters

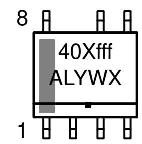
ON Semiconductor®

www.onsemi.com

MARKING DIAGRAM

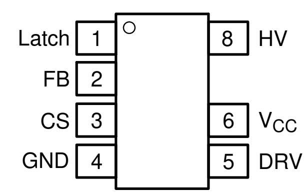


SOIC−7
CASE 751U



40Xfff	= Specific Device Code	
	X = A, B, E or F	
	fff = 065 or 100	
A	= Assembly Location	
L	= Wafer Lot	
Y	= Year	
W	= Work Week	
▪	= Pb−Free Package	

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 44 of this data sheet.

The NCP1240 is a new fixed−frequency current−mode controller featuring the Dynamic Self−Supply. This function greatly simplifies the design of the auxiliary supply and the V_{CC} capacitor by activating the internal startup current source to supply the controller during start−up, transients, latch, stand−by etc. This device contains a special HV detector which detect the application unplug from the AC input line and triggers the X2 discharge current. This HV structure allows the brown−out detection as well.

It features a timer−based fault detection that ensures the detection of overload and an adjustable compensation to help keep the maximum power independent of the input voltage.

Due to frequency foldback, the controller exhibits excellent efficiency in light load condition while still achieving very low standby power consumption. Internal frequency jittering, ramp compensation, and a versatile latch input make this controller an excellent candidate for the robust power supply designs.

A dedicated Off mode allows to reach the extremely low no load input power consumption via “sleeping” whole device and thus minimize the power consumption of the control circuitry.

Features

- Fixed−Frequency Current−Mode Operation (65 kHz and 100 kHz frequency options)
- Frequency Foldback then Skip Mode for Maximized Performance in Light Load and Standby Conditions
- Timer−Based Overload Protection with Latched (Options A and E) or Auto−Recovery (Options B and F) Operation
- High−voltage Current Source with Brown−Out Detection and Dynamic Self−Supply, Simplifying the Design of the V_{CC} Circuitry
- Frequency Modulation for Softened EMI Signature
- Adjustable Overpower Protection Dependant on the Bulk Voltage
- Latch−off Input Combined with the Overpower Protection Sensing Input
- V_{CC} Operation up to 28 V, With Overvoltage Detection
- 500/800 mA Source/Sink Drive Peak Current Capability
- 10 ms Soft−Start
- Internal Thermal Shutdown
- No−Load Standby Power < 30 mW
- X2 Capacitor in EMI Filter Discharging Feature
- These Devices are Pb−Free and Halogen Free/BFR Free

Typical Applications

- AC−DC Adapters for Notebooks, LCD, and Printers
- Offline Battery Chargers
- Consumer Electronic Power Supplies
- Auxiliary/Housekeeping Power Supplies
- Offline Adapters for Notebooks

July, 2015 − Rev. 1

Publication Order Number:
NCP1240/D

TYPICAL APPLICATION EXAMPLE

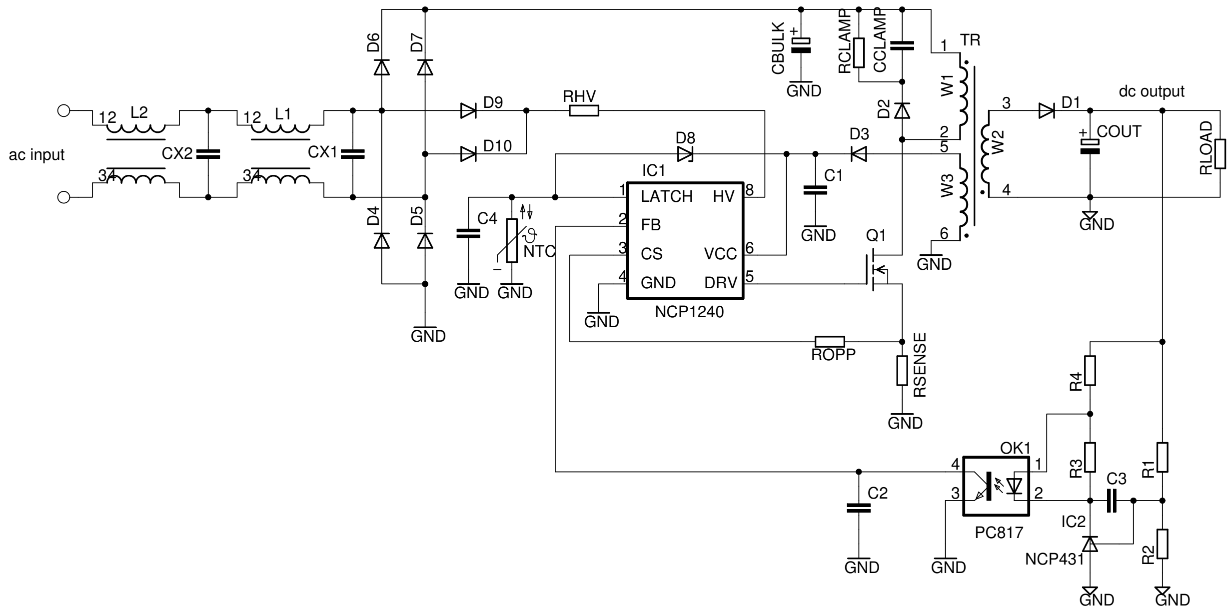


Figure 1. Flyback Converter Application Using the NCP1240

OPTIONS

Part	Option	Frequency	OCP Fault
NCP1240	A	65 kHz	Latched
	A	100 kHz	Latched
	B	65 kHz	Autorecovery
	B	100 kHz	Autorecovery
	E	65 kHz	Latched
	F	65 kHz	Autorecovery

PIN FUNCTION DESCRIPTION

Pin No	Pin Name	Function	Pin Description
1	LATCH	Latch−Off Input	Pull the pin up or down to latch−off the controller. An internal current source allows the direct connection of an NTC for over temperature detection.
2	FB	Feedback + Shutdown pin	An optocoupler collector to ground controls the output regulation. The part goes to the low consumption Off mode if the FB input pin is pulled to GND.
3	CS	Current Sense	This Input senses the Primary Current for current−mode operation, and offers an overpower compensation adjustment.
4	GND	−	The controller ground
5	DRV	Drive output	Drives external MOSFET
6	VCC	VCC input	This supply pin accepts up to 28 Vdc, with overvoltage detection. The pin is connected to an external auxiliary voltage. It is not allowed to connect another circuit to this pin to keep low input power consumption.
8	HV	High−voltage pin	Connects to the rectified AC line to perform the functions of Start−up Current Source, Self−Supply, brown−out detection and X2 capacitor discharge function and the HV sensing for the overpower protection purposes. It is not allowed to connect this pin to DC voltage.

SIMPLIFIED INTERNAL BLOCK SCHEMATIC

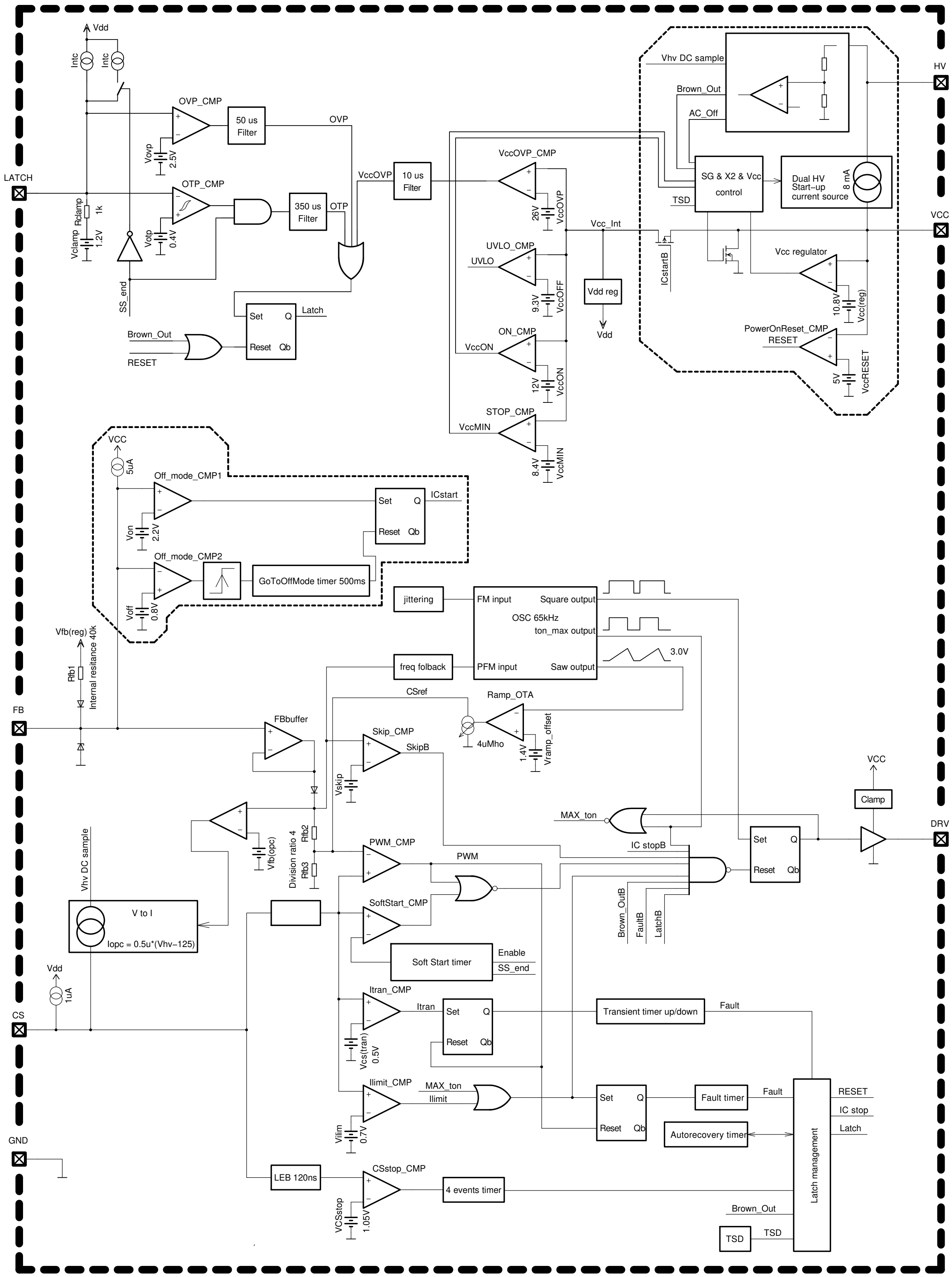


Figure 2. Simplified Internal Block Schematic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DRV (pin 5)	Maximum voltage on DRV pin (Dc−Current self−limited if operated within the allowed range) (Note 1)	−0.3 to 20 ±1000 (peak)	V mA
V_{CC} (pin 6)	V_{CC}Power Supply voltage, V_{CC} pin, continuous voltage Power Supply voltage, V_{CC} pin, continuous voltage (Note 1)	−0.3 to 28 ±30 (peak)	V mA
HV (pin 8)	Maximum voltage on HV pin (Dc−Current self−limited if operated within the allowed range)	−0.3 to 500 ±20	V mA
V_{max}	Maximum voltage on low power pins (except pin 5, pin 6 and pin 8) (Dc−Current self−limited if operated within the allowed range) (Note 1)	−0.3 to 10 ±10 (peak)	V mA
$R_{\theta J-A}$	Thermal Resistance SOIC−7 Junction-to-Air, low conductivity PCB (Note 2) Junction-to-Air, medium conductivity PCB (Note 3) Junction-to-Air, high conductivity PCB (Note 4)	 162 147 115	°C/W
$R_{\theta J-C}$	Thermal Resistance Junction−to−Case	73	°C/W
T_{JMAX}	Operating Junction Temperature	−40 to +150	°C
$T_{STRGMAX}$	Storage Temperature Range	−60 to +150	°C
	ESD Capability, HBM model (All pins except HV) per JEDEC Standard JESD22, Method A114E	> 2000	V
	ESD Capability, Machine Model per JEDEC Standard JESD22, Method A115A	> 200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.
2. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 50 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51-1 conductivity test PCB. Test conditions were under natural convection or zero air flow.
3. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 100 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51-2 conductivity test PCB. Test conditions were under natural convection or zero air flow.
4. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 650 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51-3 conductivity test PCB. Test conditions were under natural convection or zero air flow.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
HIGH VOLTAGE CURRENT SOURCE						
Minimum Voltage for Current Source Operation		$V_{HV(min)}$	–	30	40	V
Current Flowing Out of V_{CC} Pin (X2 discharge current value is equal to I_{start2})	V_{CC} = 0 V V_{CC} = $V_{CC(on)}$ − 0.5 V	I_{start1} I_{start2}	0.2 5	0.5 8	0.8 11	mA
Off−state Leakage Current	V_{HV} = 500 V, V_{CC} = 15 V	$I_{start(off)}$	10	25	50	µA
Off−mode HV Supply Current	V_{HV} = 141 V, V_{HV} = 325 V, V_{CC} loaded by 4.7 µF cap	$I_{HV(off)}$	– –	45 50	60 70	µA
SUPPLY						
HV Current Source Regulation Threshold		$V_{CC(reg)}$	8	11	–	V
Turn−on Threshold Level, V_{CC} Going Up HV Current Source Stop Threshold		$V_{CC(on)}$	11.0	12.0	13.0	V
HV Current Source Restart Threshold		$V_{CC(min)}$	7.8	8.4	9.0	V
Turn−off Threshold (Note 5)		$V_{CC(off)}$	8.8	9.3	9.8	V
Overvoltage Threshold		$V_{CC(ovp)}$	25	26.5	28	V

5. $V_{CC(off)} < V_{CC(min)}$ with the minimum gap 0.5 V.
6. Internal supply current only, currents sourced via FB pin is not included (current is flowing in GND pin only).
7. Guaranteed by design.
8. CS pin source current is a sum of I_{bias} and I_{OPC}, thus at V_{HV} = 125 V is observed the I_{bias} only, because I_{OPC} is switched off.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
SUPPLY						
Blanking Duration on $V_{CC(off)}$ and $V_{CC(ovp)}$ Detection		$t_{VCC(blank)}$	–	10	–	μs
V_{CC} Decreasing Level at Which the Internal Logic Resets		$V_{CC(reset)}$	4.8	7.0	7.7	V
V_{CC} Level for I_{START1} to I_{START2} Transition		$V_{CC(inhibit)}$	0.2	0.8	1.25	V
Internal Current Consumption (Note 6)	DRV open, V_{FB} = 3 V, 65 kHz DRV open, V_{FB} = 3 V, 100 kHz Cdrv = 1 nF, V_{FB} = 3 V, 65 kHz Cdrv = 1 nF, V_{FB} = 3 V, 100 kHz Off mode (skip or before start−up) Fault mode (fault or latch)	I_{CC1} I_{CC1} I_{CC2} I_{CC2} I_{CC3} I_{CC4}	1.3 1.3 1.8 2.0 0.5 0.35	1.85 1.85 2.6 2.9 0.65 0.5	2.2 2.2 3.0 3.2 0.8 0.7	mA
BROWN−OUT						
Brown−Out Thresholds	V_{HV} going up V_{HV} going down	$V_{HV(start)}$ $V_{HV(stop)}$	102 94	111 103	120 112	V
Timer Duration for Line Cycle Drop−out		t_{HV}	35	50	75	ms
X2 DISCHARGE						
Comparator Hysteresis Observed at HV Pin		$V_{HV(hyst)}$	1.5	3.5	5	V
HV Signal Sampling Period		T_{sample}	–	1.0	–	ms
Timer Duration for No Line Detection		t_{DET}	43	64	86	ms
Discharge Timer Duration		t_{DIS}	43	64	86	ms
OSCILLATOR						
Oscillator Frequency		f_{OSC}	58 87	65 100	72 109	kHz
Maximum On Time for T_J = 25°C to +125°C Only	f_{OSC} = 65 kHz f_{OSC} = 100 kHz	$t_{ONmax(65kHz)}$ $t_{ONmax(100kHz)}$	11.5 7.5	12.3 8.0	13.1 8.5	μs
Maximum On Time	f_{OSC} = 65 kHz f_{OSC} = 100 kHz	$t_{ONmax(65kHz)}$ $t_{ONmax(100kHz)}$	11.3 7.4	12.3 8.0	13.1 8.5	μs
Maximum Duty Cycle (corresponding to maximum on time at maximum switching frequency)	f_{OSC} = 65 kHz f_{OSC} = 100 kHz	D_{MAX}	–	80	–	%
Frequency Jittering Amplitude, in Percentage of F_{OSC}		A_{jitter}	±3	±5.5	±8	%
Frequency Jittering Modulation Frequency		F_{jitter}	85	125	165	Hz
FREQUENCY FOLDBACK						
Feedback Voltage Threshold Below Which Frequency Foldback Starts	T_J = 25°C	$V_{FB(foldS)}$	2.35	2.5	2.6	V
Feedback Voltage Threshold Below Which Frequency Foldback is Complete	T_J = 25°C	$V_{FB(foldE)}$	1.4	1.5	1.6	V
Minimum Switching Frequency (NCP1240A/B) (NCP1240E/F)	V_{FB} = $V_{skip(in)}$ + 0.1	$f_{OSC(min)}$	 23 21	 27 27	 32 32	kHz

5. $V_{CC(off)} < V_{CC(min)}$ with the minimum gap 0.5 V.
6. Internal supply current only, currents sourced via FB pin is not included (current is flowing in GND pin only).
7. Guaranteed by design.
8. CS pin source current is a sum of I_{bias} and I_{OPC}, thus at V_{HV} = 125 V is observed the I_{bias} only, because I_{OPC} is switched off.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = –40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
OUTPUT DRIVER						
Rise Time, 10% to 90% of V_{CC}	$V_{CC} = V_{CC(min)}$ + 0.2 V, C_{DRV} = 1 nF	t_{rise}	–	40	70	ns
Fall Time, 90% to 10% of V_{CC}	$V_{CC} = V_{CC(min)}$ + 0.2 V, C_{DRV} = 1 nF	t_{fall}	–	40	70	ns
Current Capability	$V_{CC} = V_{CC(min)}$ + 0.2 V, C_{DRV} = 1 nF DRV high, V_{DRV} = 0 V DRV low, $V_{DRV} = V_{CC}$	 $I_{DRV(source)}$ $I_{DRV(sink)}$	 – –	 500 800	 – –	mA
Clamping Voltage (maximum gate voltage)	$V_{CC} = V_{CCmax}$ – 0.2 V, DRV high, R_{DRV} = 33 kΩ, C_{load} = 220 pF	$V_{DRV(clamp)}$	11	13.5	16	V
High–state Voltage Drop	$V_{CC} = V_{CC(min)}$ + 0.2 V, R_{DRV} = 33 kΩ, DRV high	$V_{DRV(drop)}$	–	–	1	V
CURRENT SENSE						
Input Pull–up Current	V_{CS} = 0.7 V	I_{bias}	–	1	–	μA
Maximum Internal Current Setpoint	V_{FB} > 3.5 V	V_{ILIM}	0.66	0.70	0.74	V
Propagation Delay from V_{Ilimit} Detection to DRV Off	$V_{CS} = V_{ILIM}$	t_{delay}	–	80	110	ns
Leading Edge Blanking Duration for V_{ILIM}		t_{LEB}	200	250	340	ns
Threshold for Fast Fault Protection Activation		$V_{CS(stop)}$	0.95	1.05	1.15	V
Leading Edge Blanking Duration for $V_{CS(stop)}$ (Note 7)		t_{BCS}	90	120	150	ns
Soft–start Duration	From 1st pulse to $V_{CS} = V_{ILIM}$	t_{SSTART}	8	11	14	ms
INTERNAL SLOPE COMPENSATION						
Slope of the Compensation Ramp		$S_{comp(65kHz)}$ $S_{comp(100kHz)}$	– –	–32.5 –50	– –	mV / μs
FEEDBACK						
Internal Pull–up Resistor	T_J = 25°C	$R_{FB(up)}$	30	40	50	kΩ
V_{FB} to Internal Current Setpoint Division Ratio		K_{FB}	–	4	–	–
Internal Pull–up Voltage on the FB Pin (Note 7)		$V_{FB(ref)}$	4.5	5	5.5	V
Feedback Voltage Below which the Peak Current is Frozen	T_J = 25°C	$V_{FB(off)}$	–	0.8	–	V
SKIP CYCLE MODE						
Feedback Voltage Thresholds for Skip Mode	V_{FB} going down, T_J = 25°C V_{FB} going up, T_J = 25°C	$V_{skip(in)}$ $V_{skip(out)}$	1.1 1.2	1.2 1.3	1.3 1.4	V
REMOTE CONTROL ON FB PIN						
The Voltage Above which the Part Enters the On Mode	$V_{CC} > V_{CC(off)}$, V_{HV} = 60 V	V_{ON}	–	2.2	–	V
The Voltage Below which the Part Enters the Off Mode	$V_{CC} > V_{CC(off)}$	V_{OFF}	0.5	0.6	0.7	V
Minimum Hysteresis Between the V_{ON} and V_{OFF}	$V_{CC} > V_{CC(off)}$, V_{HV} = 60 V	V_{HYST}	500	–	–	mV
Pull–up Current in Off Mode	$V_{CC} > V_{CC(off)}$	I_{OFF}	–	5	–	μA

5. $V_{CC(off)} < V_{CC(min)}$ with the minimum gap 0.5 V.
6. Internal supply current only, currents sourced via FB pin is not included (current is flowing in GND pin only).
7. Guaranteed by design.
8. CS pin source current is a sum of I_{bias} and I_{OPC}, thus at V_{HV} = 125 V is observed the I_{bias} only, because I_{OPC} is switched off.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
REMOTE CONTROL ON FB PIN						
Go To Off Mode Timer	$V_{CC} > V_{CC(off)}$	t_{GTOM}	400	500	600	ms
OVERLOAD PROTECTION						
Fault Timer Duration (NCP1240A/B) (NCP1240E/F)		t_{fault}	44 9.1	64 14	84 23.2	ms
Autorecovery Mode Latch−off Time Duration		$t_{autorec}$	0.85	1.00	1.35	s
CS Threshold for Transient Peak Timer Activation		$V_{CS(tran)}$	0.46	0.49	0.52	V
Transient Peak Power Timer Duration (NCP1240A/B) (NCP1240E/F)	$V_{CS(peak)} = V_{CS(tran)}$ + 0.1 V from 1st time $V_{CS} > V_{CS(tran)}$ to DRV stop	t_{tran}	 4.1 44	 6.1 64	 8.1 84	 s ms
OVERPOWER PROTECTION						
V_{HV} to I_{OPC} Conversion Ratio		K_{OPC}	–	0.54	–	μA / V
Current Flowing out of CS Pin (Note 8)	V_{HV} = 125 V V_{HV} = 162 V V_{HV} = 325 V V_{HV} = 365 V	$I_{OPC(125)}$ $I_{OPC(162)}$ $I_{OPC(325)}$ $I_{OPC(365)}$	– – – 105	0 20 110 130	– – – 150	μA
FB Voltage Above which I_{OPC} is Applied	V_{HV} = 365 V	$V_{FB(OPCF)}$	–	2.6	–	V
FB Voltage Below which is No I_{OPC} Applied	V_{HV} = 365 V	$V_{FB(OPCE)}$	–	2.1	–	V
LATCH−OFF INPUT						
High Threshold	V_{Latch} going up	V_{OVP}	2.35	2.5	2.65	V
Low Threshold	V_{Latch} going down	V_{OTP}	–	0.4	–	V
OTP Resistance Threshold (T_J = 25°C) (T_J = 80°C) (T_J = 110°C)	External NTC resistance is going down	R_{OTP}	6.6 – –	7.7 8.5 9.5	8.6 – –	kΩ
Current Source for Direct NTC Connection During Sormal Operation During Soft−start	V_{Latch} = 0 V	 I_{NTC} $I_{NTC(SSTART)}$	 20 60	 50 100	 70 140	μA
Blanking Duration On High Latch Detection	65 kHz version 100 kHz version	$t_{Latch(OVP)}$	35 20	50 35	70 55	μs
Blanking Duration On Low Latch Detection		$t_{Latch(OTP)}$	–	350	–	μs
Clamping voltage	I_{Latch} = 0 mA I_{Latch} = 1 mA	$V_{clamp0(Latch)}$ $V_{clamp1(Latch)}$	1.0 1.8	1.2 2.4	1.4 3.0	V
TEMPERATURE SHUTDOWN						
Temperature shutdown	T_J going up	T_{TSD}	–	150	–	°C
Temperature shutdown hysteresis	T_J going down	$T_{TSD(HYS)}$	–	30	–	°C

5. $V_{CC(off)} < V_{CC(min)}$ with the minimum gap 0.5 V.
6. Internal supply current only, currents sourced via FB pin is not included (current is flowing in GND pin only).
7. Guaranteed by design.
8. CS pin source current is a sum of I_{bias} and I_{OPC}, thus at V_{HV} = 125 V is observed the I_{bias} only, because I_{OPC} is switched off.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTIC

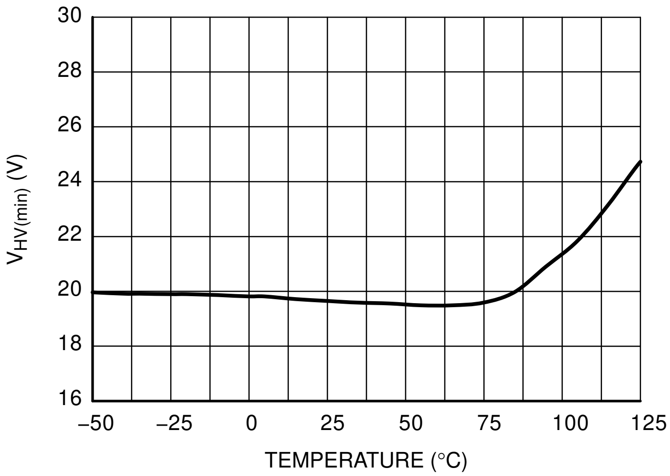


Figure 3. Minimum Current Source Operation $V_{HV(min)}$

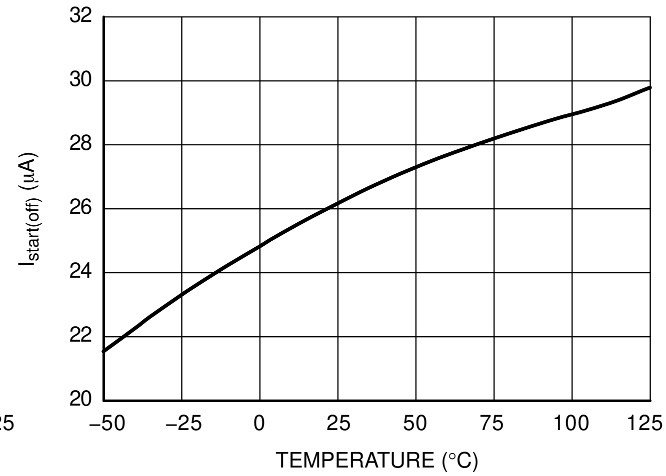


Figure 4. Off–State Leakage Current $I_{start(off)}$

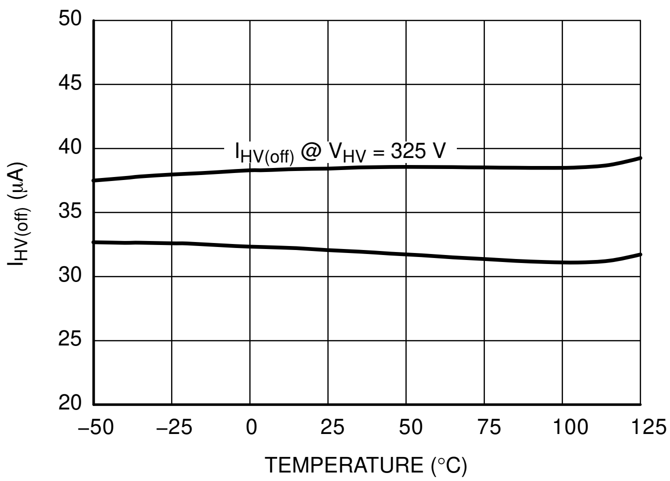


Figure 5. Off–Mode HV Supply Current $I_{HV(off)}$

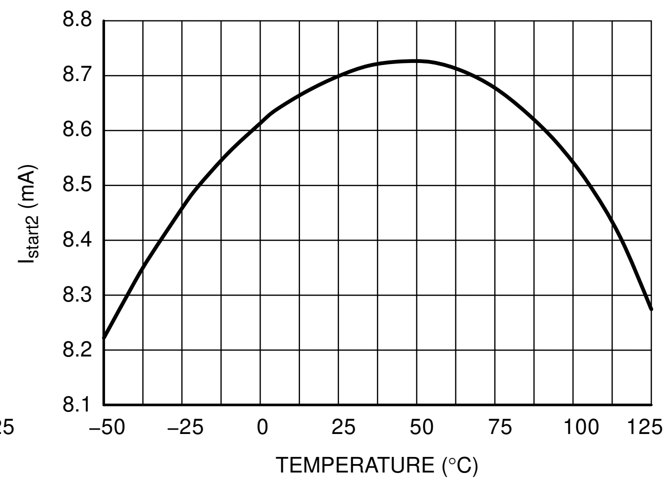


Figure 6. High Voltage Startup Current Flowing Out of V_{CC} Pin I_{start2}

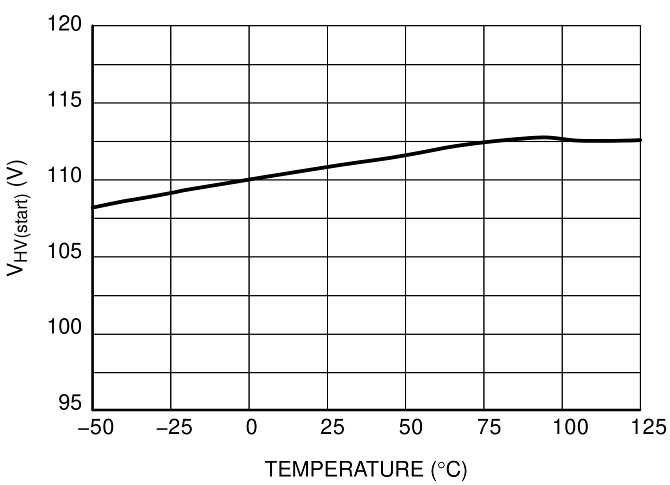


Figure 7. Brown–out Device Start Threshold $V_{HV(start)}$

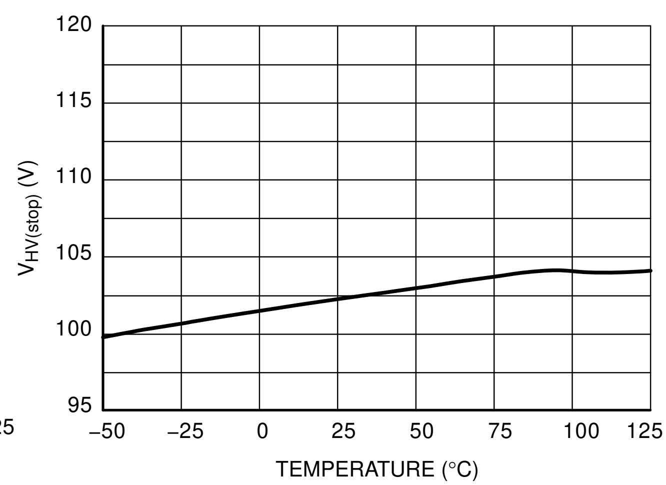


Figure 8. Brown–out Device Stop Threshold $V_{HV(stop)}$

TYPICAL CHARACTERISTIC

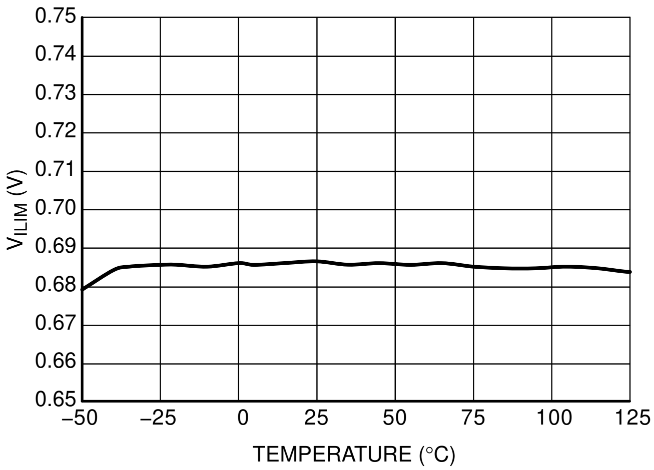


Figure 9. Maximum Internal Current Setpoint V_{ILIM}

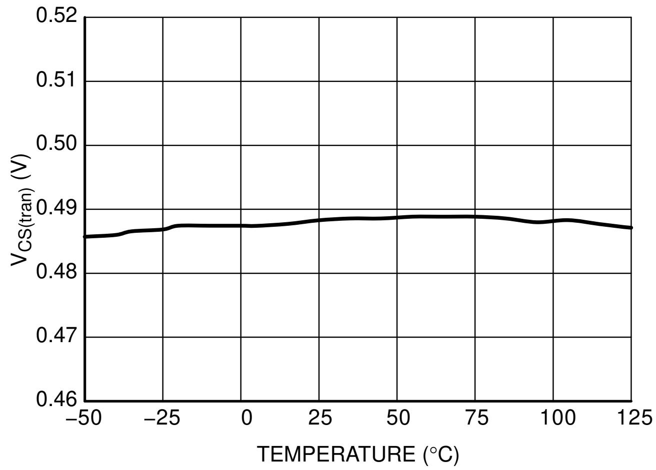


Figure 10. Threshold for Transient Peak Power Timer Activation $V_{CS(tran)}$

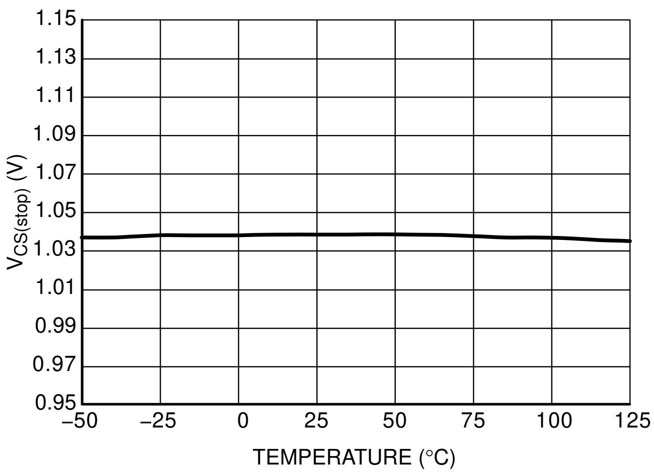


Figure 11. Threshold for Immediate Fault Protection Activation $V_{CS(stop)}$

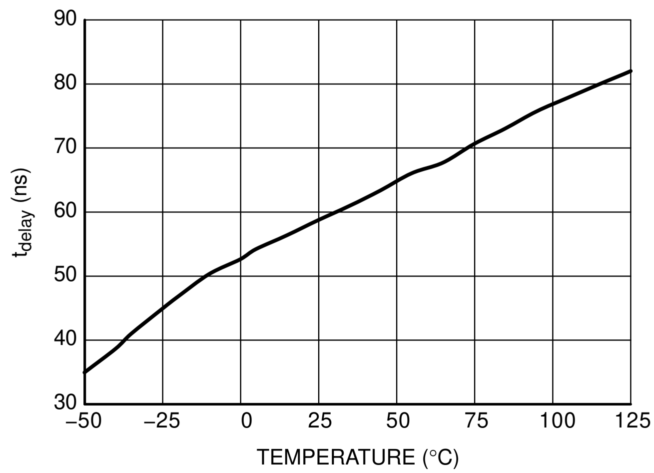


Figure 12. Propagation Delay t_{delay}

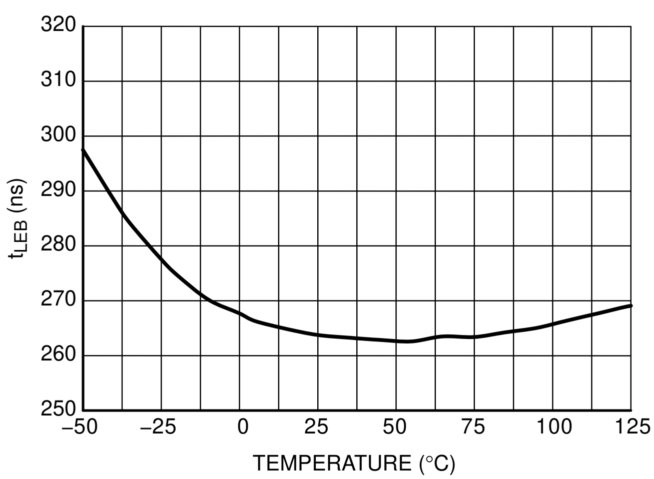


Figure 13. Leading Edge Blanking Duaration t_{LEB}

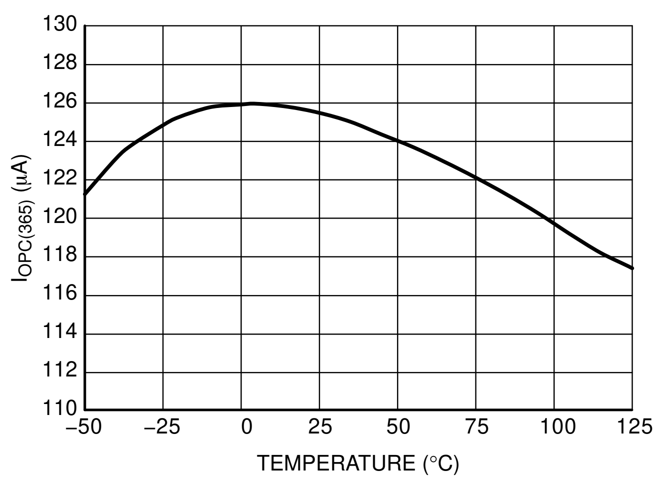


Figure 14. Maximum Overpower Compensating Current $I_{OPC(365)}$ Flowing Out of CS Pin

TYPICAL CHARACTERISTIC

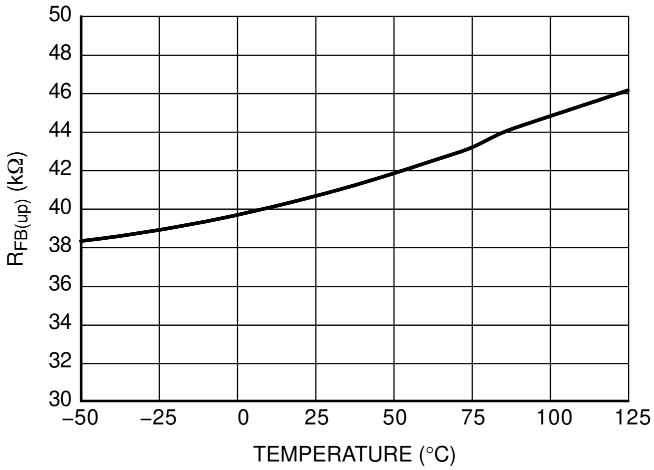


Figure 15. FB Pin Internal Pull−up Resistor $R_{FB(up)}$

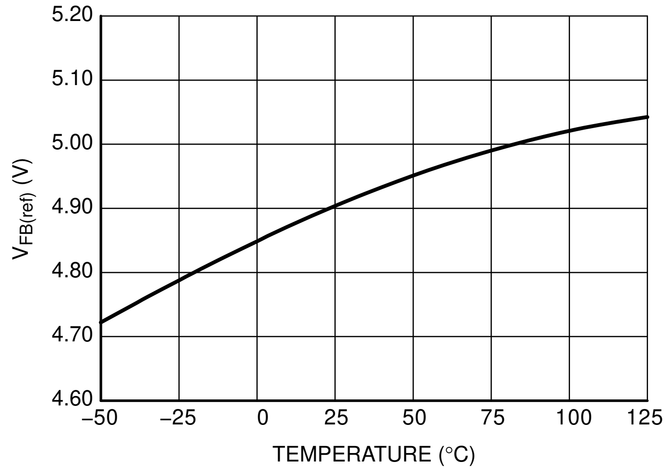


Figure 16. FB Pin Open Voltage $V_{FB(ref)}$

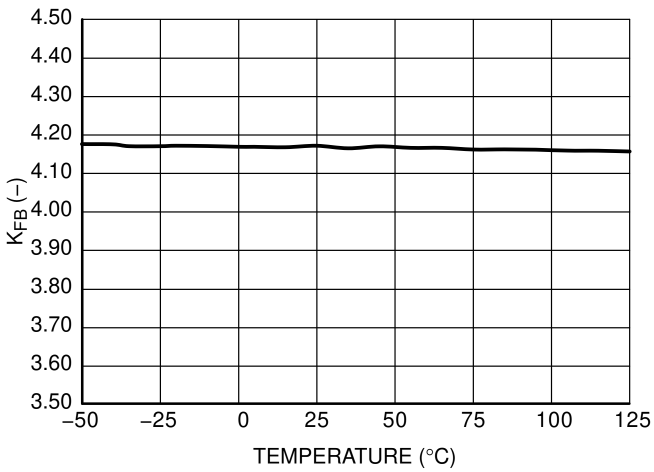


Figure 17. V_{FB} to Internal Current Setpoint Division Ratio K_{FB}

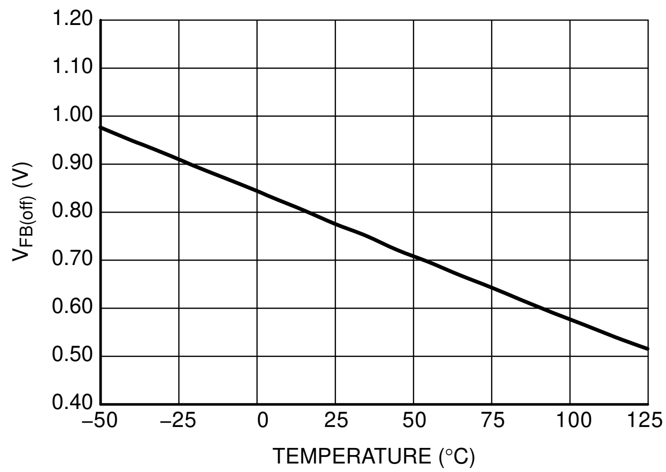


Figure 18. Offset Voltage $V_{FB(off)}$ between FB Pin and Internal FB Divider

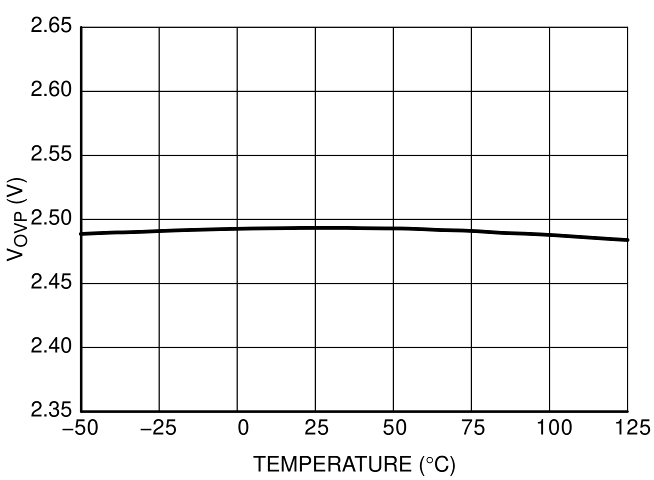


Figure 19. Latch Pin High Threshold V_{OVP}

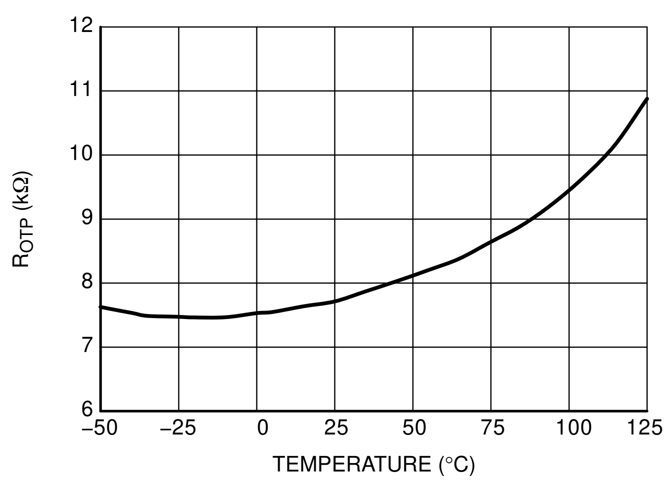


Figure 20. OTP Reistance Threshold R_{OTP} at Latch Pin

TYPICAL CHARACTERISTIC

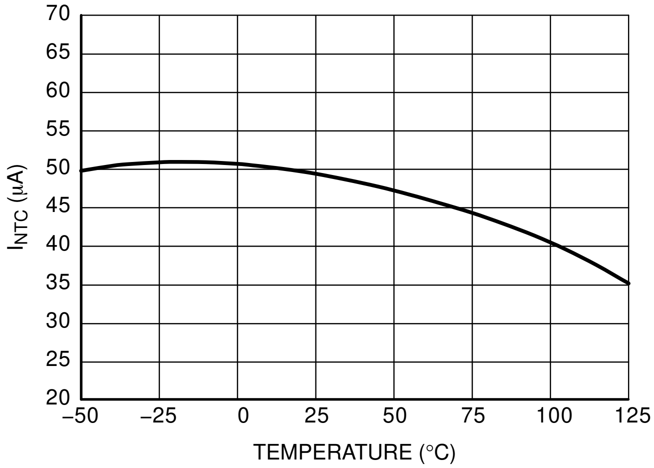


Figure 21. Current I_{NTC} Sourced from the Latch Pin, Allowing Direct NTC Connection

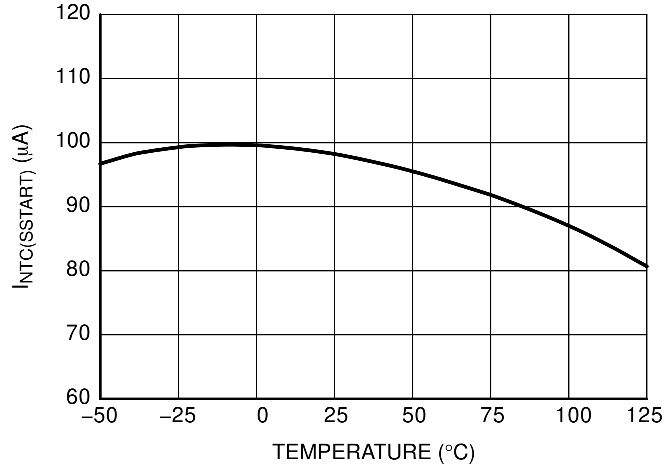


Figure 22. Current $I_{NTC(SSTART)}$ Sourced from the Latch Pin, During Soft−Start

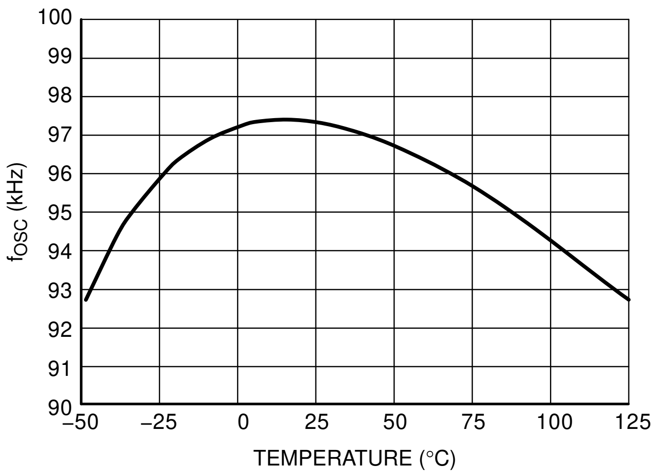


Figure 23. Oscillator f_{OSC} for the 65 kHz Version (NCP1240A/B only)

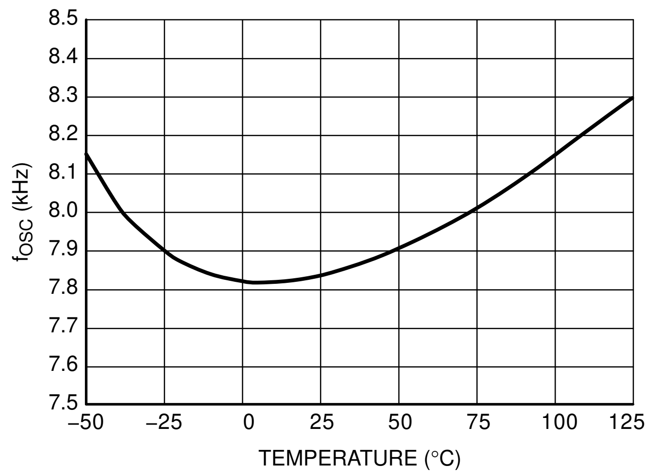


Figure 24. Maximum ON Time t_{ONmax} for the 65 kHz Version (NCP1240A/B only)

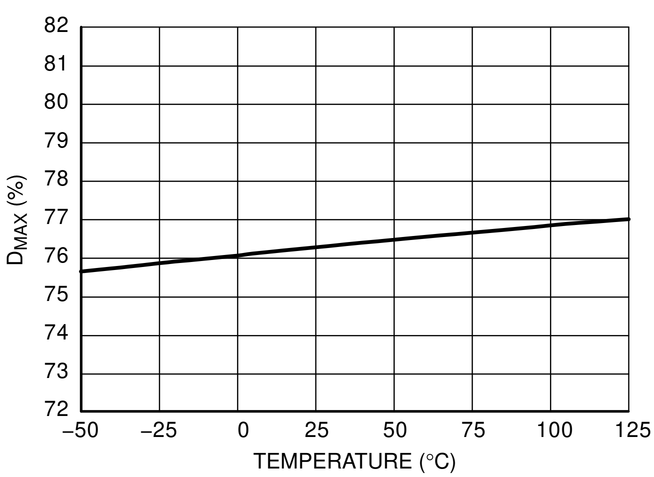


Figure 25. Maximum Duty Ratio D_{MAX}

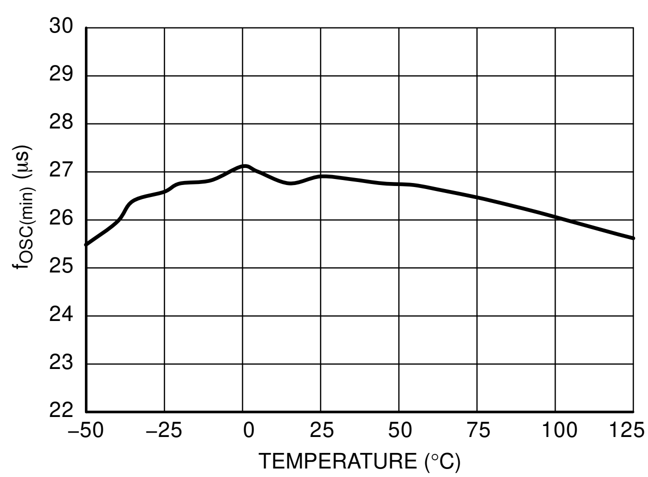


Figure 26. Minimum Switching Frequency $f_{OSC(min)}$

TYPICAL CHARACTERISTIC

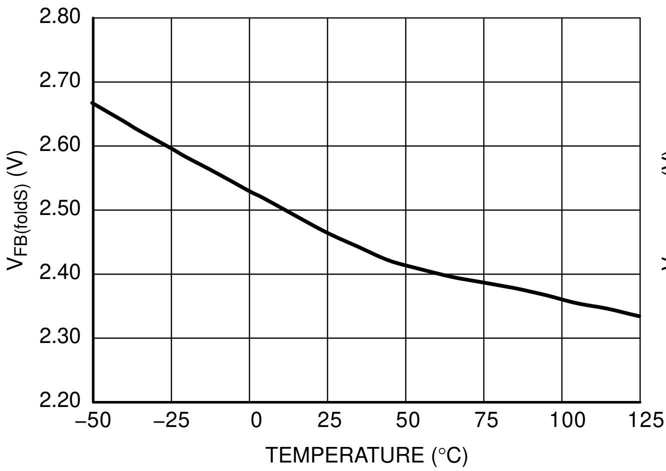


Figure 27. FB Pin Voltage Below Which Frequency Foldback Starts $V_{FB(foldS)}$

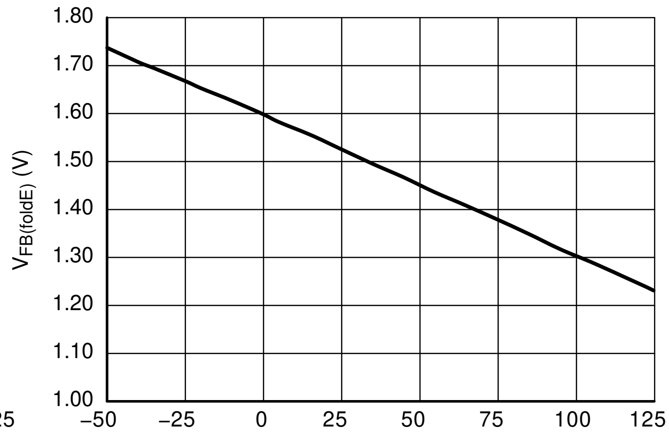


Figure 28. FB Pin Voltage Below Which Frequency Foldback Complete $V_{FB(foldE)}$

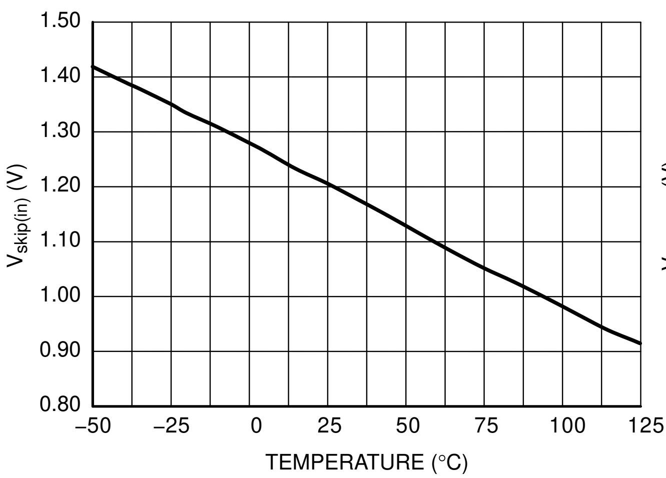


Figure 29. FB Pin Skip−In Level $V_{skip(in)}$

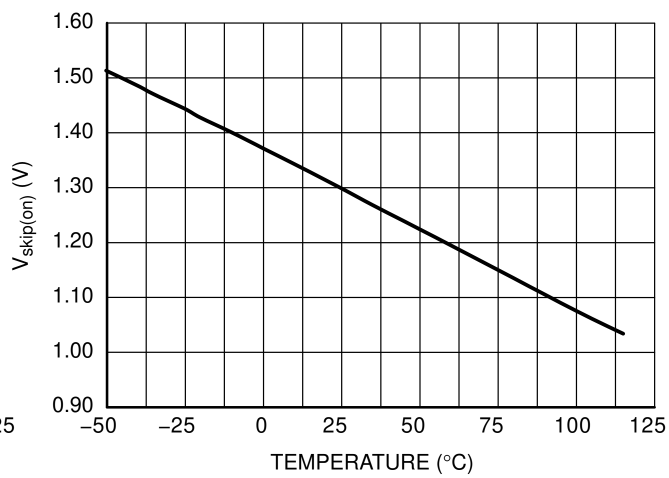


Figure 30. FB Pin Skip−Out Level $V_{skip(out)}$

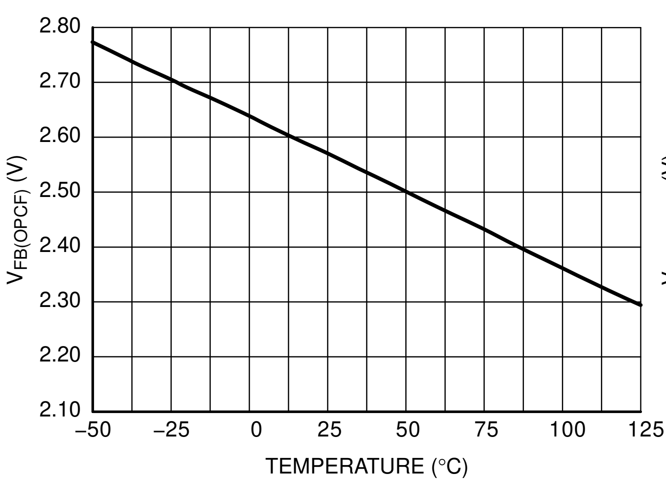


Figure 31. FB Pin Level $V_{FB(OPCF)}$ Above Which is the Overpower Compensation Applied

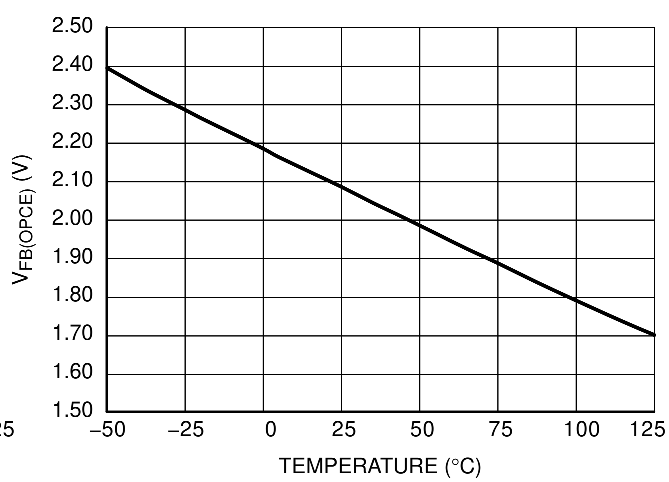


Figure 32. FB Pin Level $V_{FB(OPCE)}$ Below Which is No Overpower Compensation Applied

TYPICAL CHARACTERISTIC

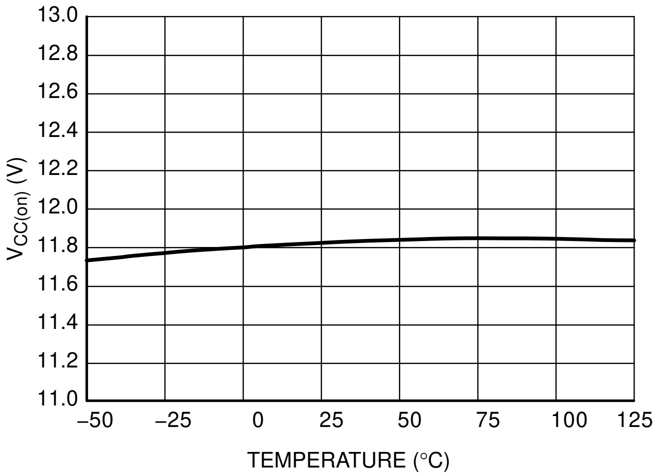


Figure 33. V_{CC} Turn−on Threshold Level, V_{CC} Going Up HV Current Source Stop Threshold $V_{CC(on)}$

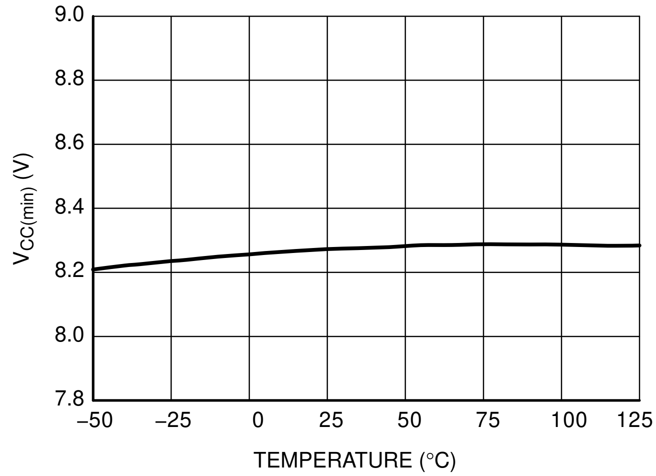


Figure 34. HV Current Source Restart Threshold $V_{CC(min)}$

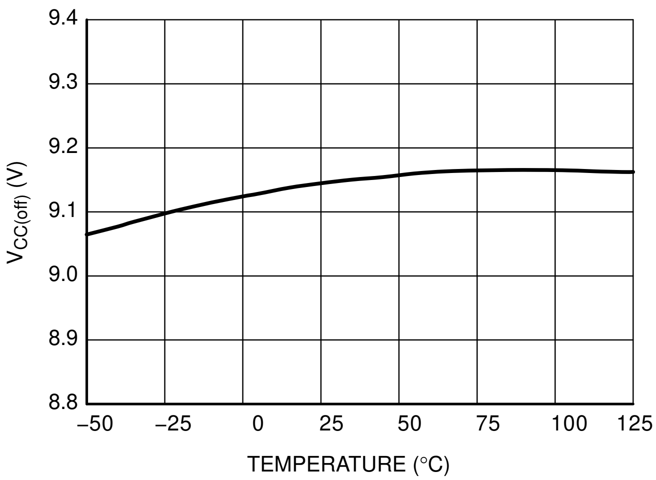


Figure 35. V_{CC} Turn−off Threshold (UVLO) $V_{CC(off)}$

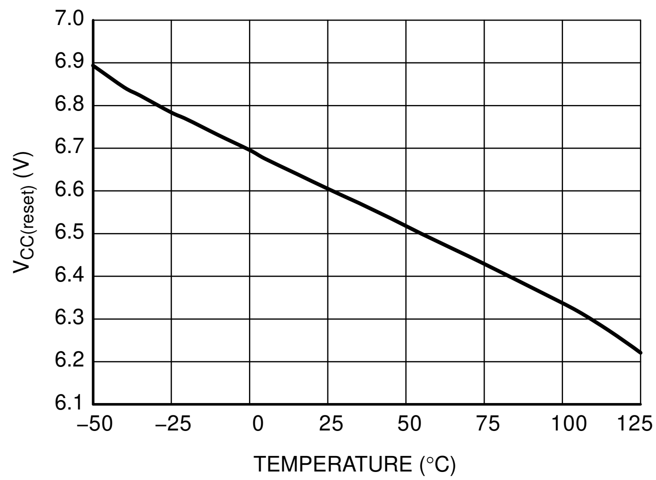


Figure 36. V_{CC} Decreasing Level at Which the Internal Logic Resets $V_{CC(reset)}$

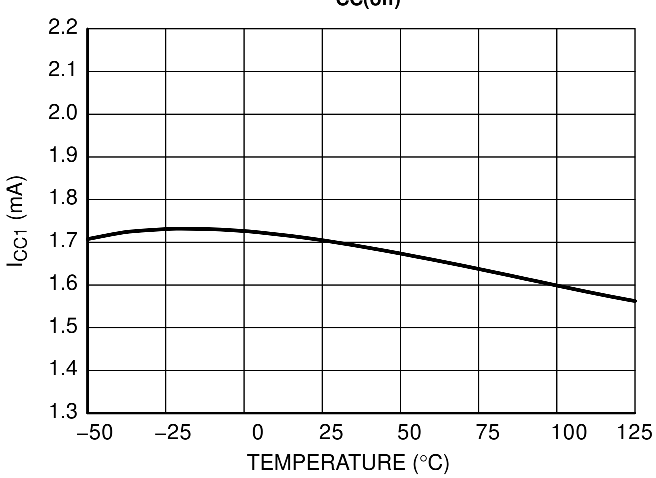


Figure 37. Internal Current Consumption when DRV Pin is Unloaded

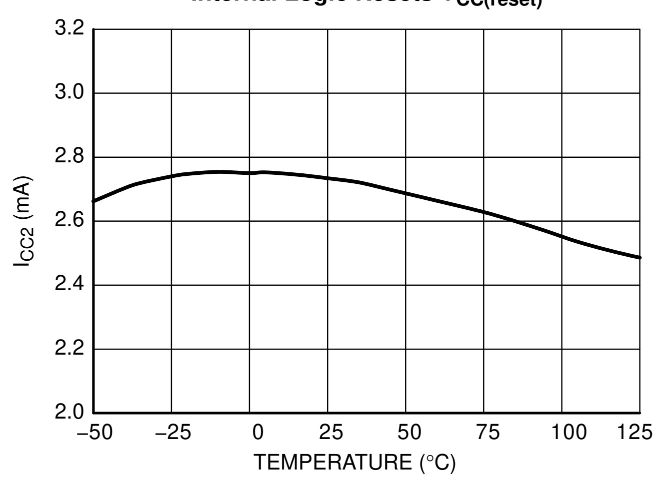


Figure 38. Internal Current Consumption when DRV Pin is Loaded by 1 nF

TYPICAL CHARACTERISTIC

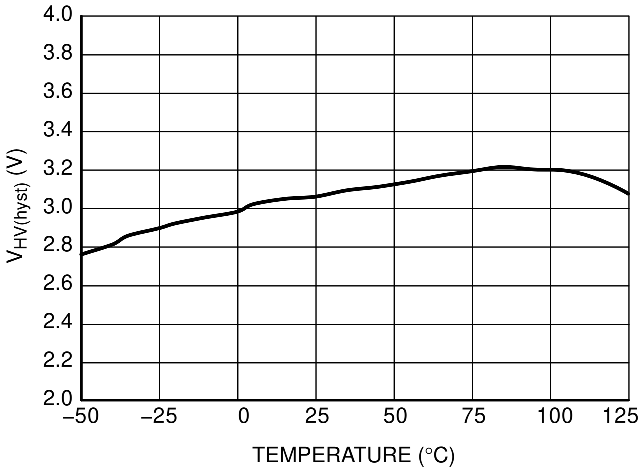


Figure 39. X2 Discharge Comparator Hysteresis Observed at HV Pin $V_{HV(hyst)}$

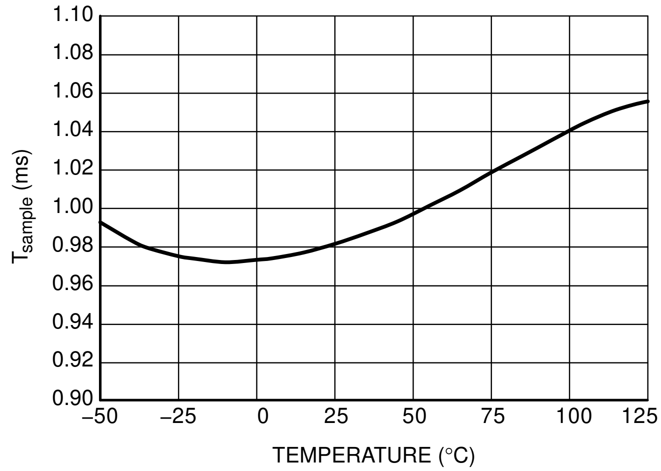


Figure 40. HV Signal Sampling Period T_{sample}

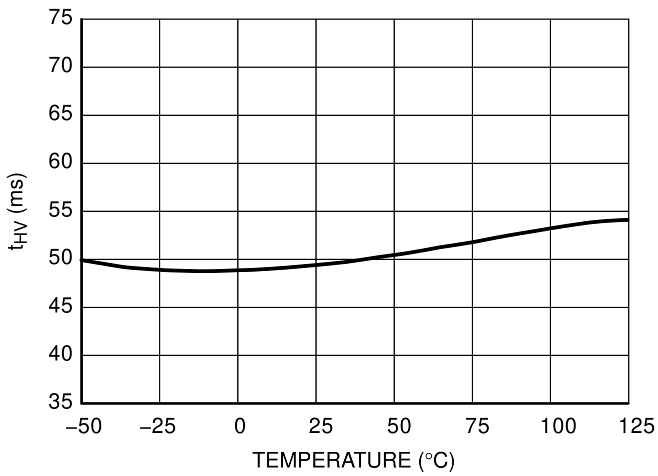


Figure 41. Timer Duration for Line Cycle Drop−out t_{HV}

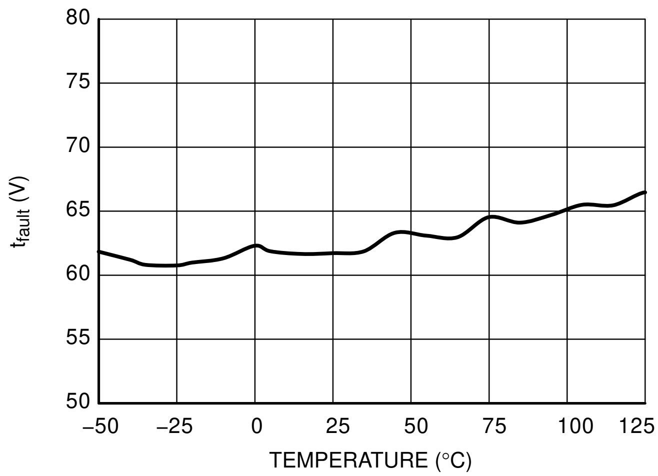


Figure 42. Fault Timer Duration t_{fault} (NCP1240A/B only)

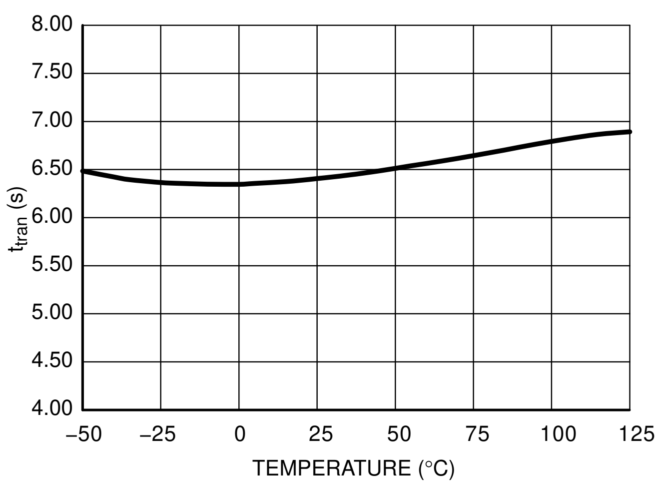


Figure 43. Transient Peak Power Timer Timer Duration t_{tran} (NCP1240A/B only)

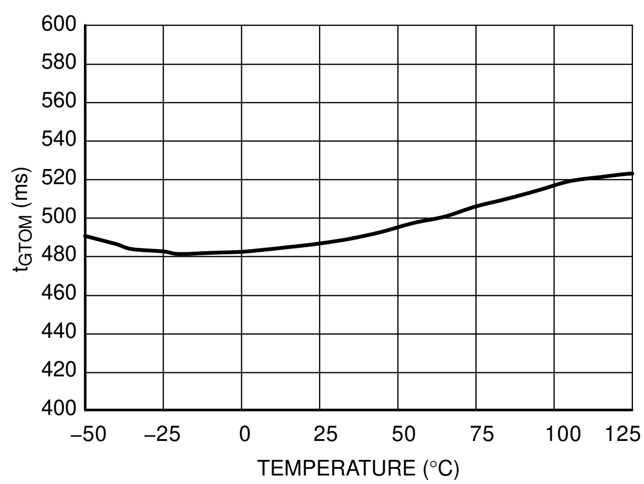


Figure 44. Go To Off Mode Timer Duration t_{GTOM}

APPLICATION INFORMATION

Functional Description

The NCP1240 includes all necessary features to build a safe and efficient power supply based on a fixed−frequency flyback converter. The NCP1240 is a multimode controller as illustrated in Figure 45. The mode of operation depends upon line and load condition. Under all modes of operation, the NCP1240 terminates the DRV signal based on the switch current. Thus, the NCP1240 always operates in current mode control so that the power MOSFET current is always limited.

Under normal operating conditions, the FB pin commands the operating mode of the NCP1240 at the voltage thresholds shown in Figure 45. At normal rated operating loads (from 100% to approximately 33% full rated power) the NCP1240 controls the converter in fixed frequency PWM mode. It can operate in the continuous conduction mode (CCM) or discontinuous conduction mode (DCM) depending upon the input voltage and loading conditions. If the controller is used in CCM with a wide input voltage range, the duty−ratio may increase up to 50%. The build−in slope compensation prevents the appearance of sub−harmonic oscillations in this operating area.

The converter operates in frequency foldback mode (FFM) for loads that are between approximately 17% and 48% of full rated power.

Effectively, operation in FFM results in the application of constant volt−seconds to the flyback transformer each switching cycle. Voltage regulation in FFM is achieved by varying the switching frequency in the range from 65 kHz (or 100 kHz) to 27 kHz. For extremely light loads (below approximately 6% full rated power), the converter is controlled using bursts of 27 kHz pulses. This mode is called as skip mode. The FFM, keeping constant peak current and skip mode allows design of the power supplies with increased efficiency under the light loading conditions. Keep in mind that the aforementioned boundaries of steady−state operation are approximate because they are subject to converter design parameters.

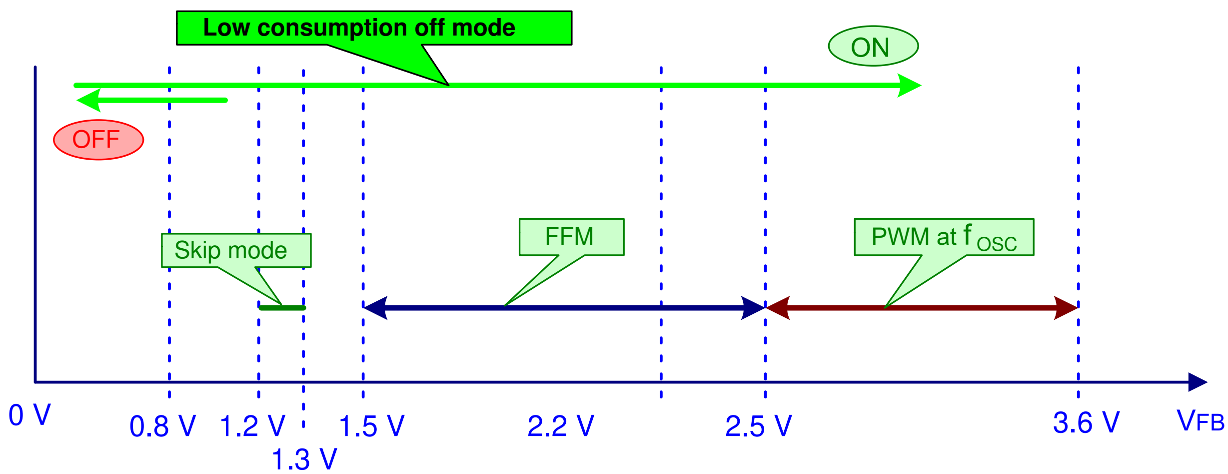


Figure 45. Mode Control with FB Pin Voltage

There was implemented the low consumption off mode allowing to reach extremely low no load input power. This mode is controlled by the FB pin and allows the remote control (or secondary side control) of the power supply shut−down. Most of the device internal circuitry is unbiased in the low consumption off mode. Only the FB pin control circuitry and X2 cap discharging circuitry is operating in the low consumption off mode. If the voltage at feedback pin decreases below the 0.6 V the controller will enter the low consumption off mode. The controller can start if the FB pin voltage increases above the 2.2 V level.

See the detailed status diagrams for the versions fully latched A and the autorecovery B on the following figures. The basic status of the device after wake−up by the V_{CC} is the off mode and mode is used for the overheating protection mode if the thermal shutdown protection is activated.

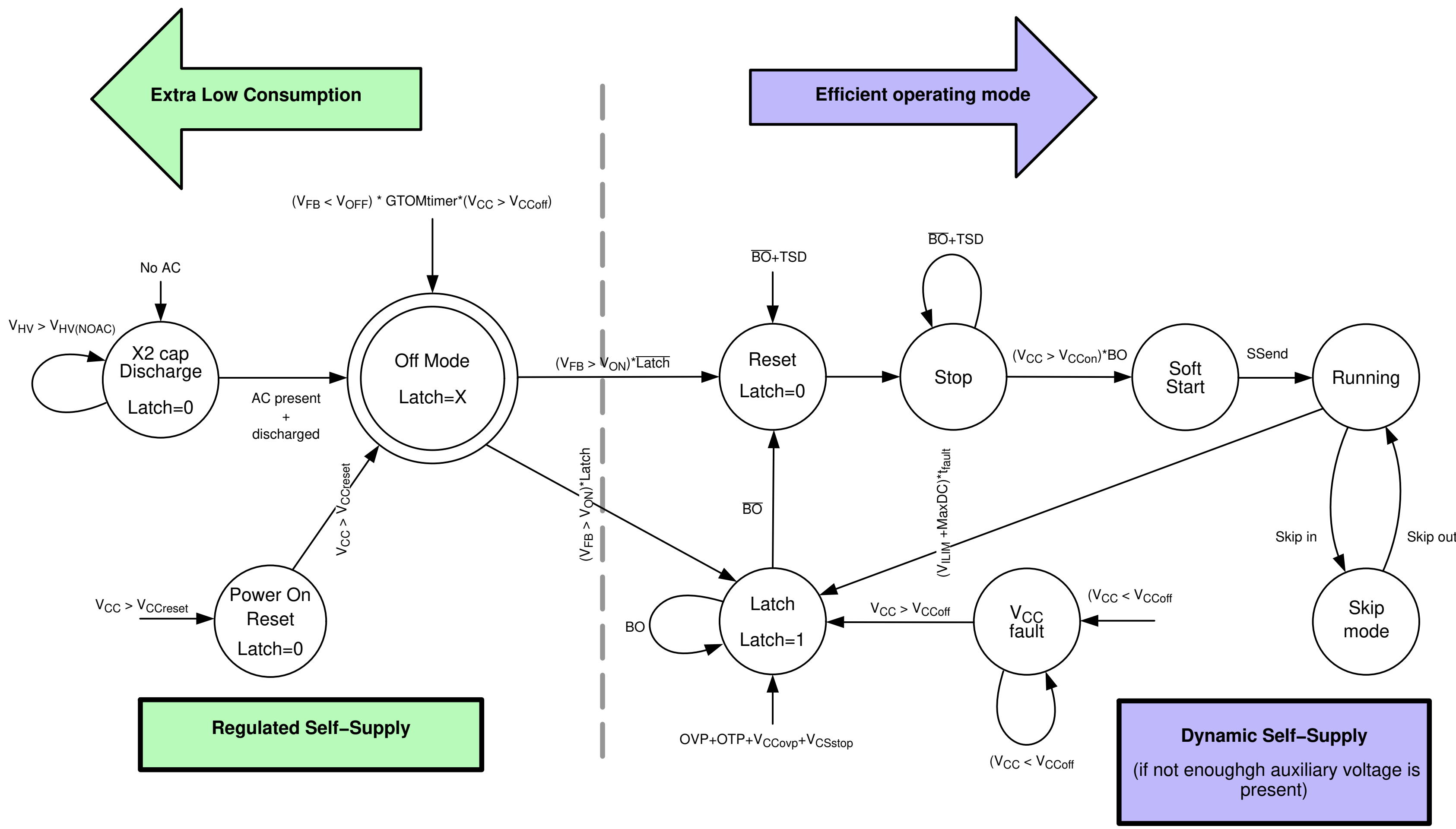


Figure 46. Operating Status Diagram for the Fully Latched Versions A and E of the Device

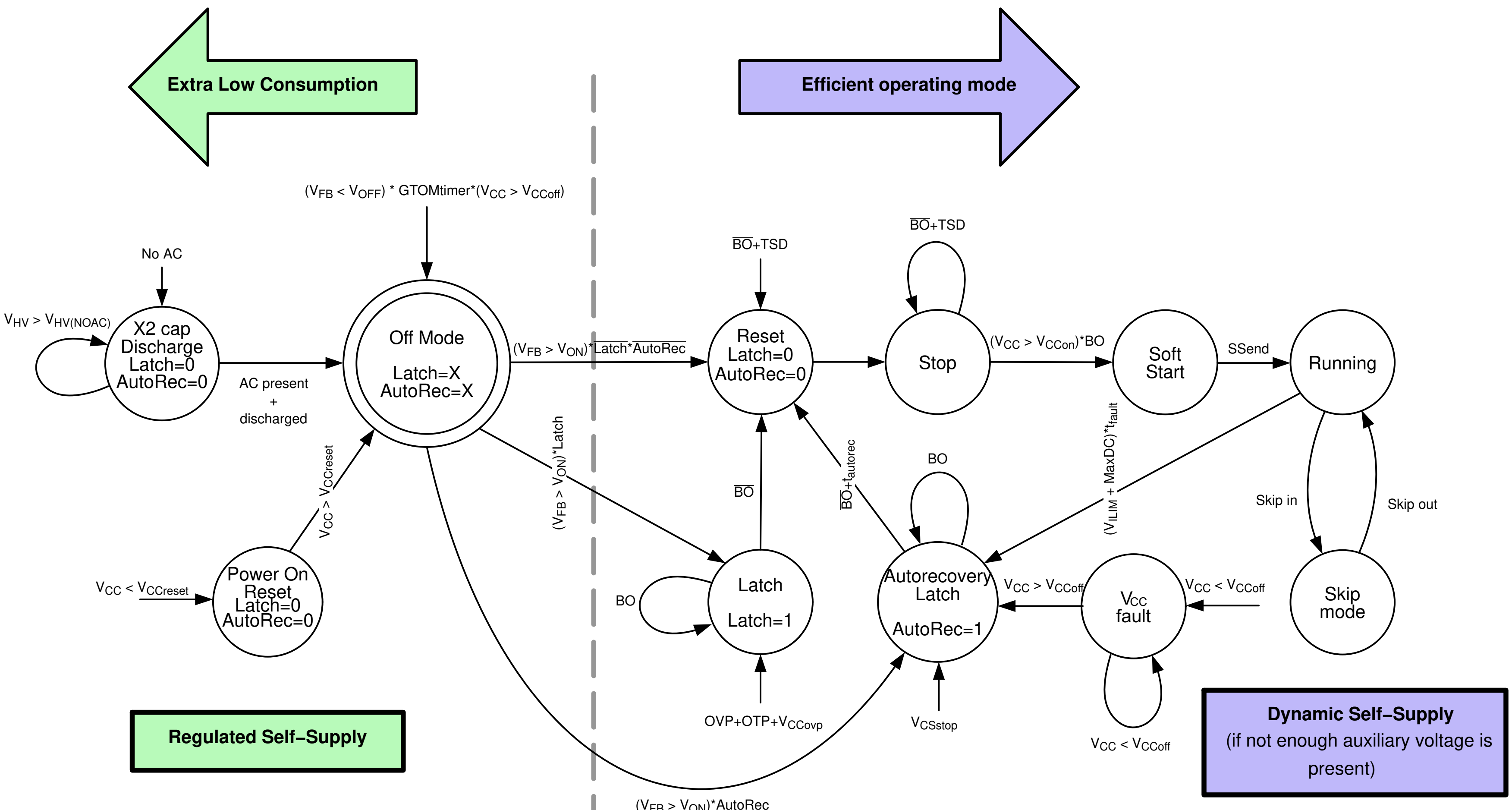


Figure 47. Operating Status Diagram for the Autorecovery Versions B and F of the Device

The information about the fault (permanent Latch or Autorecovery) is kept during the low consumption off mode due the safety reason. The reason is not to allow unlatch the device by the remote control being in off mode.

Start−up of the Controller

At start−up, the current source turns on when the voltage on the HV pin is higher than $V_{HV(min)}$, and turns off when V_{CC} reaches $V_{CC(on)}$, then turns on again when V_{CC} reaches $V_{CC(min)}$, until the input voltage is high enough to ensure a proper start−up, i.e. when V_{HV} reaches $V_{HV(start)}$. The controller actually starts the next time V_{CC} reaches $V_{CC(on)}$. The controller then delivers pulses, starting with a soft−start period t_{SSTART} during which the peak current linearly increases before the current−mode control takes over.

Even though the Dynamic Self−Supply is able to maintain the V_{CC} voltage between $V_{CC(on)}$ and $V_{CC(min)}$ by turning the HV start−up current source on and off, it can only be used in light load condition, otherwise the power dissipation on the die would be too much. As a result, an auxiliary voltage source is needed to supply V_{CC} during normal operation.

The Dynamic Self−Supply is useful to keep the controller alive when no switching pulses are delivered, e.g. in brown−out condition, or to prevent the controller from stopping during load transients when the V_{CC} might drop. The NCP1240 accepts a supply voltage as high as 28 V, with an overvoltage threshold $V_{CC(ovp)}$ that latches the controller off.

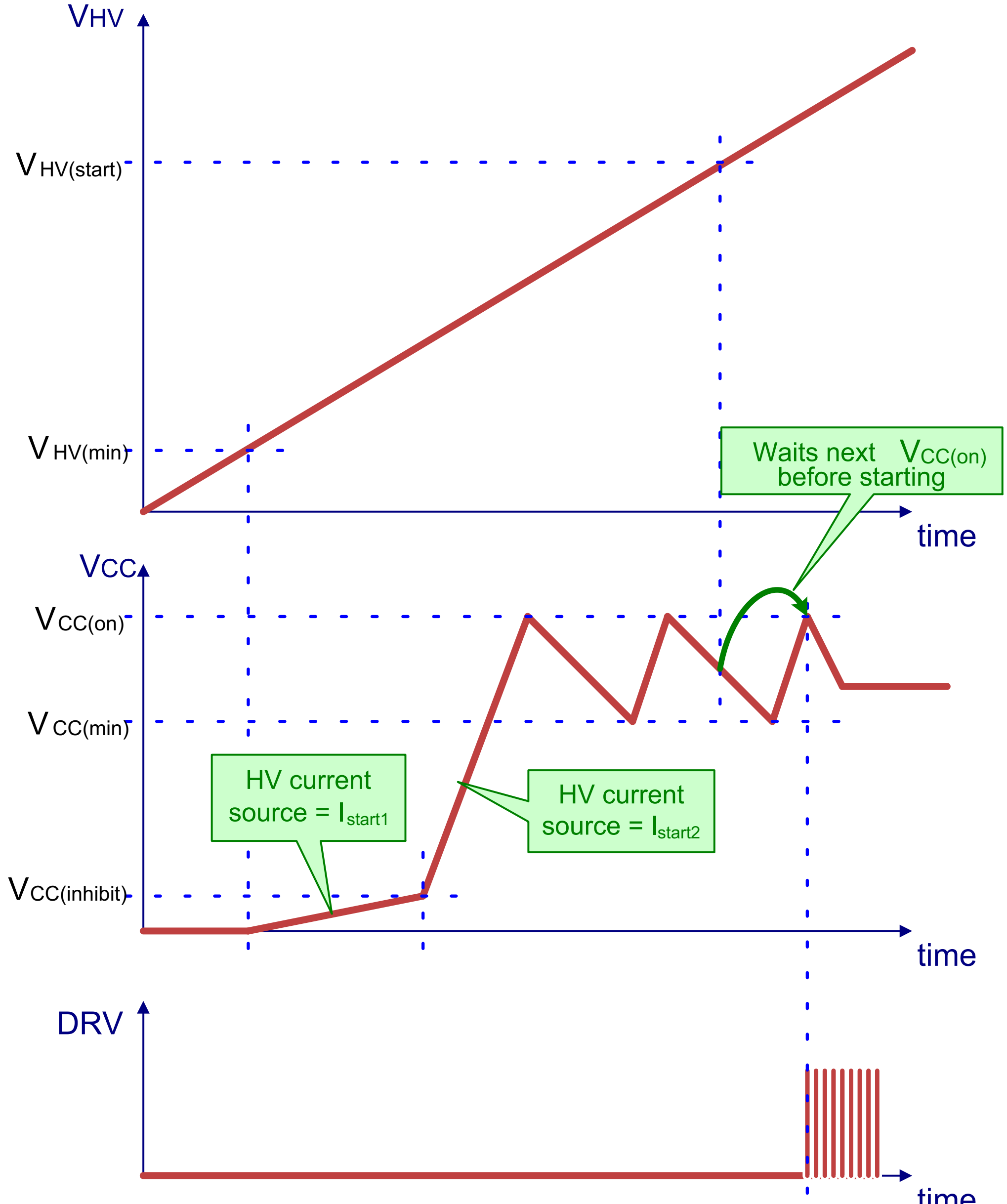


Figure 48. V_{CC} Start−up Timing Diagram

For safety reasons, the start−up current is lowered when V_{CC} is below $V_{CC(inhibit)}$, to reduce the power dissipation in case the V_{CC} pin is shorted to GND (in case of V_{CC} capacitor failure, or external pull−down on V_{CC} to disable the controller). There is only one condition for which the current source doesn't turn on when V_{CC} reaches $V_{CC(inhibit)}$: the voltage on HV pin is too low (below $V_{HV(min)}$).

HV Sensing of Rectified AC Voltage

The NCP1240 features on its HV pin a true ac line monitoring circuitry. It includes a minimum start−up threshold and an autorecovery brown−out protection; both of them independent of the ripple on the input voltage. It is allowed only to work with an unfiltered, rectified ac input to ensure the X2 capacitor discharge function as well, which is described in following. The brown−out protection thresholds are fixed, but they are designed to fit most of the standard ac−dc conversion applications.

When the input voltage goes below $V_{HV(stop)}$, a brown−out condition is detected, and the controller stops. The HV current source maintains V_{CC} at $V_{CC(min)}$ level until the input voltage is back above $V_{HV(start)}$.

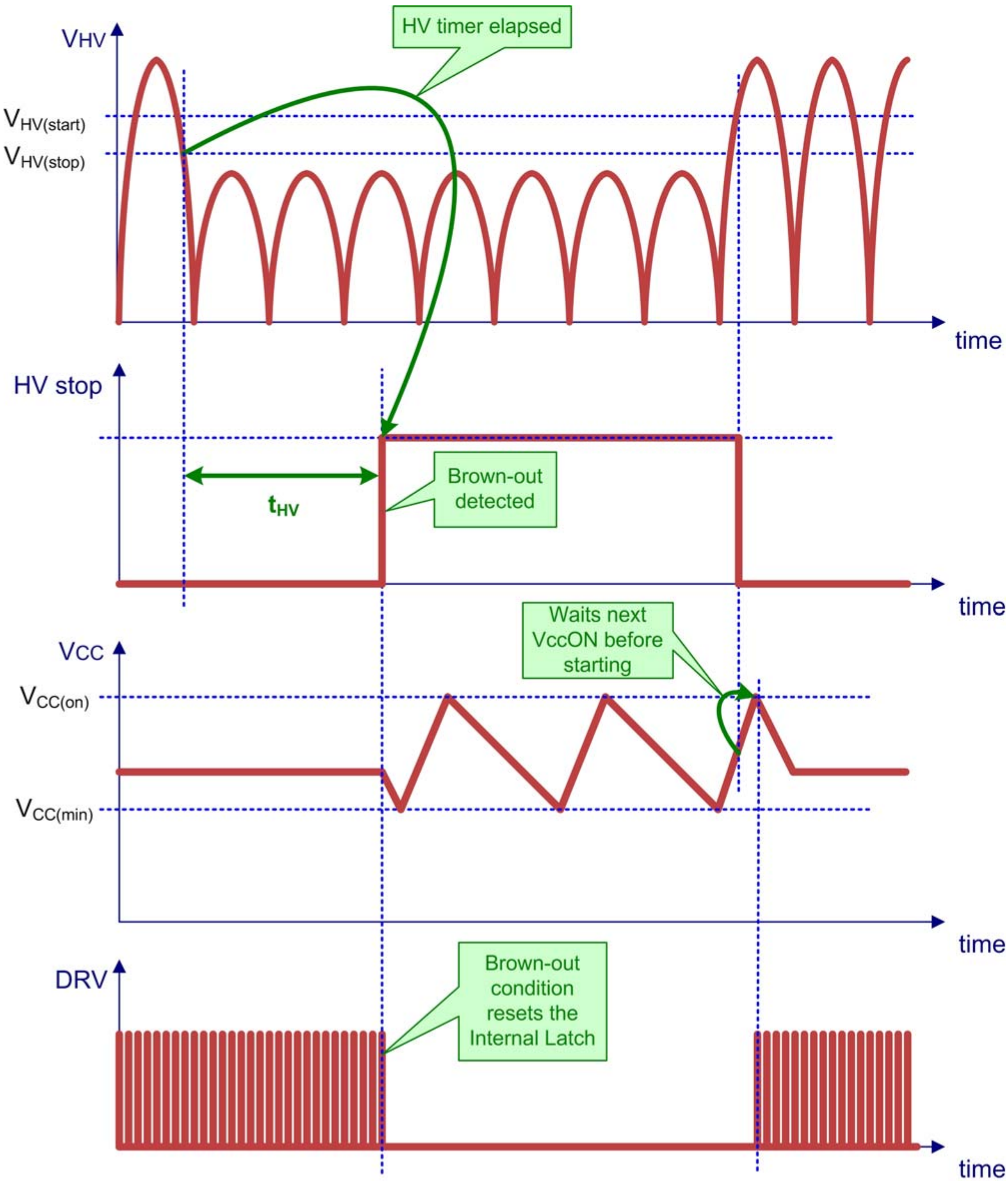


Figure 49. Ac Line Drop−out Timing Diagram

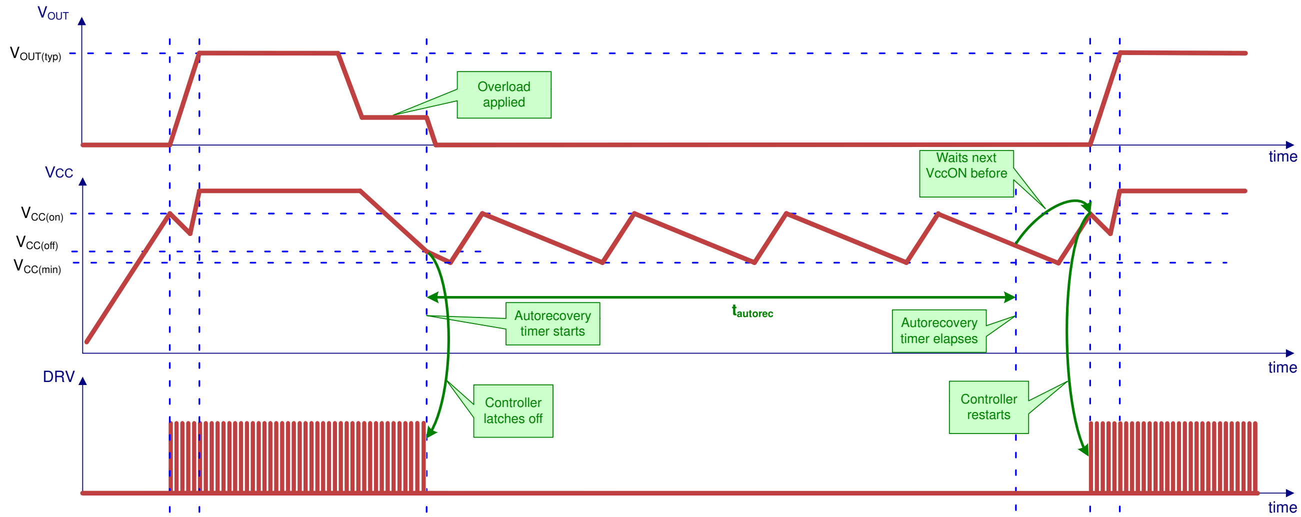


Figure 50. V_{CC} Collapses After Overload and Its Recovery

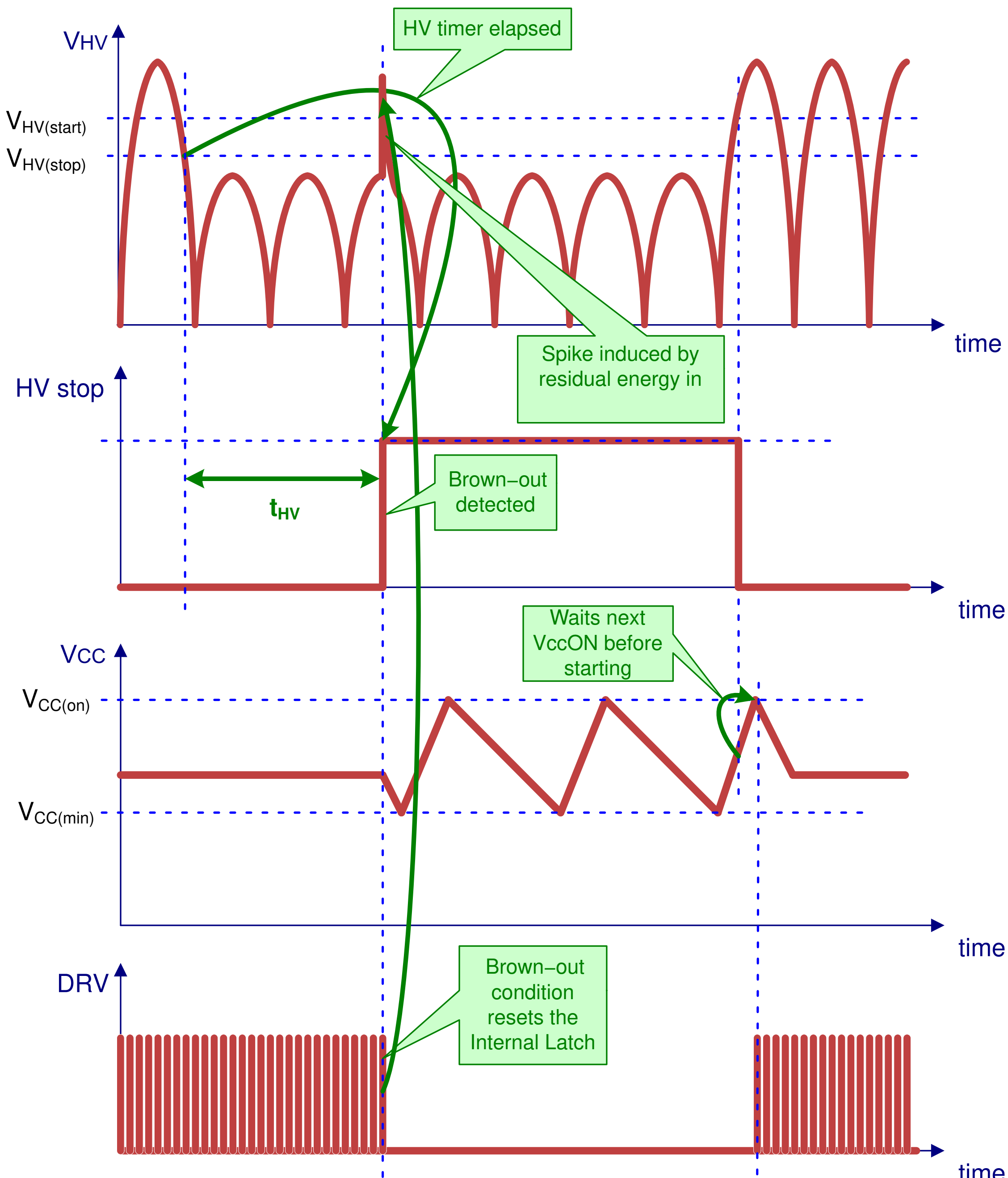


Figure 51. Ac Line Drop−out Timing Diagram with Parasitic Spike

When V_{HV} crosses the $V_{HV(start)}$ threshold, the controller can start immediately. When it crosses $V_{HV(stop)}$, it triggers a timer of duration t_{HV}, this ensures that the controller doesn't stop in case of line cycle drop−out. The device restart after the ac line voltage drop-out is protected to the parasitic restart initiated e.g. the spikes induced at HV pin immediately after the device is stopped by the residual energy in the EMI filter. The device restart is allowed only after the 1st watch dog signal event. The basic principle is shown at Figure 49 and detail of the device restart is shown at Figure 52.

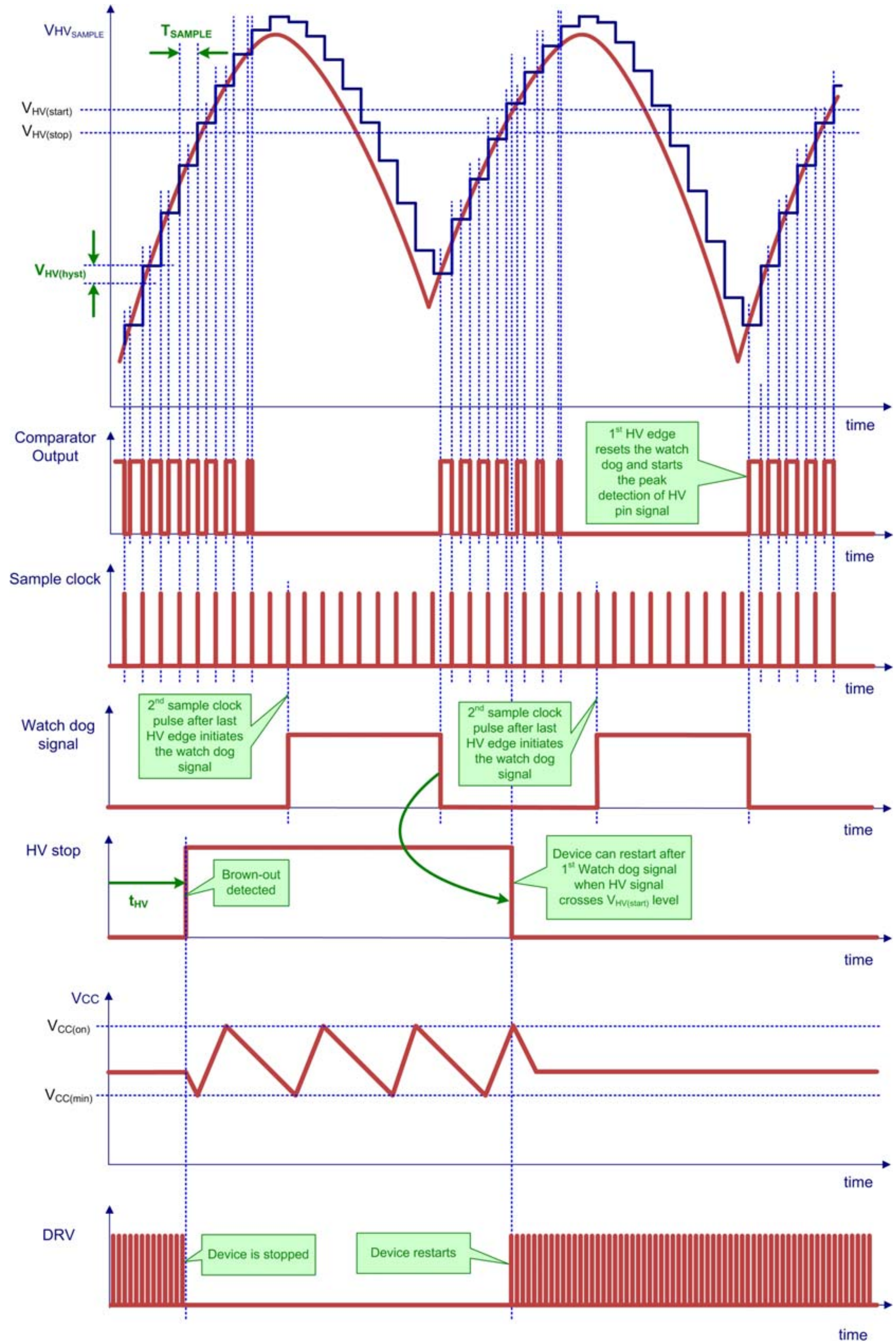


Figure 52. Detailed Timing Diagram of the Device Restart After the Short ac Line Drop−out

X2 Cap Discharge Feature

The X2 capacitor discharging feature is offered by usage of the NCP1240. This feature saves approximately 16 mW – 25 mW input power depending on the EMI filter X2 capacitors volume and it saves the external components count as well. The discharge feature is ensured via the start–up current source with a dedicated control circuitry for this function. The X2 capacitors are being discharged by current defined as I_{start2} when this discharge event is detected.

There is used a dedicated structure called ac line unplug detector inside the X2 capacitor discharge control circuitry. See the Figure 53 for the block diagram for this structure and Figures 54, 55, 56 and 57 for the timing diagrams. The basic idea of ac line unplug detector lies in comparison of the direct sample of the high voltage obtained via the high voltage sensing structure with the delayed sample of the high voltage. The delayed signal is created by the sample & hold structure.

The comparator used for the comparison of these signals is without hysteresis inside. The resolution between the slopes of the ac signal and dc signal is defined by the sampling time T_{SAMPLE} and additional internal offset N_{OS}. These parameters ensure the noise immunity as well. The additional offset is added to the picture of the sampled HV signal and its analog sum is stored in the C_1 storage capacitor. If the voltage level of the HV sensing structure output crosses this level the comparator CMP output signal resets the detection timer and no dc signal is detected. The additional offset N_{OS} can be measured as the $V_{HV(hyst)}$ on the HV pin. If the comparator output produces pulses it means that the slope of input signal is higher than set resolution level and the slope is positive. If the comparator output produces the low level it means that the slope of input signal is lower than set resolution level or the slope is negative. There is used the detection timer which is reset by any edge of the comparator output. It means if no edge comes before the timer elapses there is present only dc signal or signal with the small ac ripple at the HV pin. This type of the ac detector detects only the positive slope, which fulfils the requirements for the ac line presence detection.

In case of the dc signal presence on the high voltage input, the direct sample of the high voltage obtained via the high voltage sensing structure and the delayed sample of the high voltage are equivalent and the comparator produces the low level signal during the presence of this signal. No edges are present at the output of the comparator, that's why the detection timer is not reset and dc detect signal appears.

The minimum detectable slope by this ac detector is given by the ration between the maximum hysteresis observed at HV pin $V_{HV(hyst),max}$ and the sampling time:

$$S_{min} = \frac{V_{HV(hyst),max}}{T_{sample}} \qquad \text{(eq. 1)}$$

Than it can be derived the relationship between the minimum detectable slope and the amplitude and frequency of the sinusoidal input voltage:

$$V_{max} = \frac{V_{HV(hyst),max}}{2 \cdot \pi \cdot f \cdot T_{sample}} = \frac{5}{2 \cdot \pi \cdot 35 \cdot 1 \cdot 10^{-3}} \qquad \text{(eq. 2)}$$

$$= 22.7\ \text{V}$$

The minimum detectable AC RMS voltage is 16 V at frequency 35 Hz, if the maximum hysteresis is 5 V and sampling time is 1 ms.

The X2 capacitor discharge feature is available in any controller operation mode to ensure this safety feature. The detection timer is reused for the time limiting of the discharge phase, to protect the device against overheating. The discharging process is cyclic and continues until the ac line is detected again or the voltage across the X2 capacitor is lower than $V_{HV(min)}$. This feature ensures to discharge quite big X2 capacitors used in the input line filter to the safe level. **It is important to note that it is not allowed to connect HV pin to any dc voltage due this feature. e.g. directly to bulk capacitor.**

During the HV sensing or X2 cap discharging the V_{CC} net is kept above the $V_{CC(off)}$ voltage by the Self–Supply in any mode of device operation to supply the control circuitry. During the discharge sequence is not allowed to start–up the device.

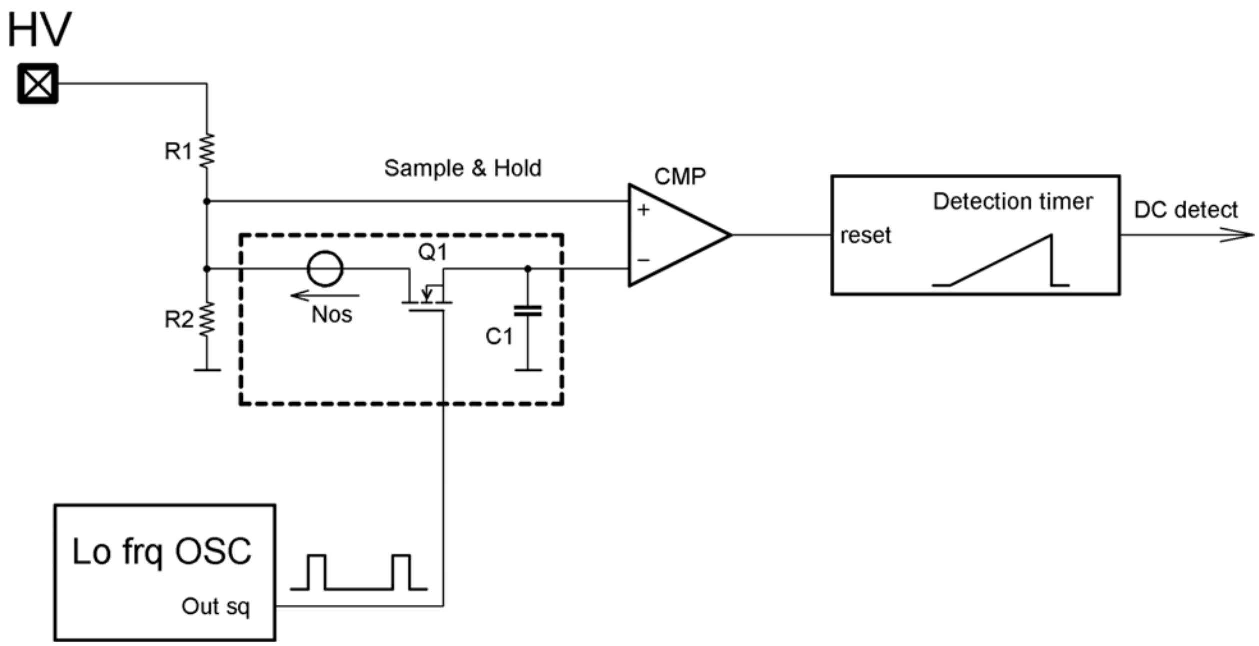


Figure 53. The ac Line Unplug Detector Structure Used for X2 Capacitor Discharge System

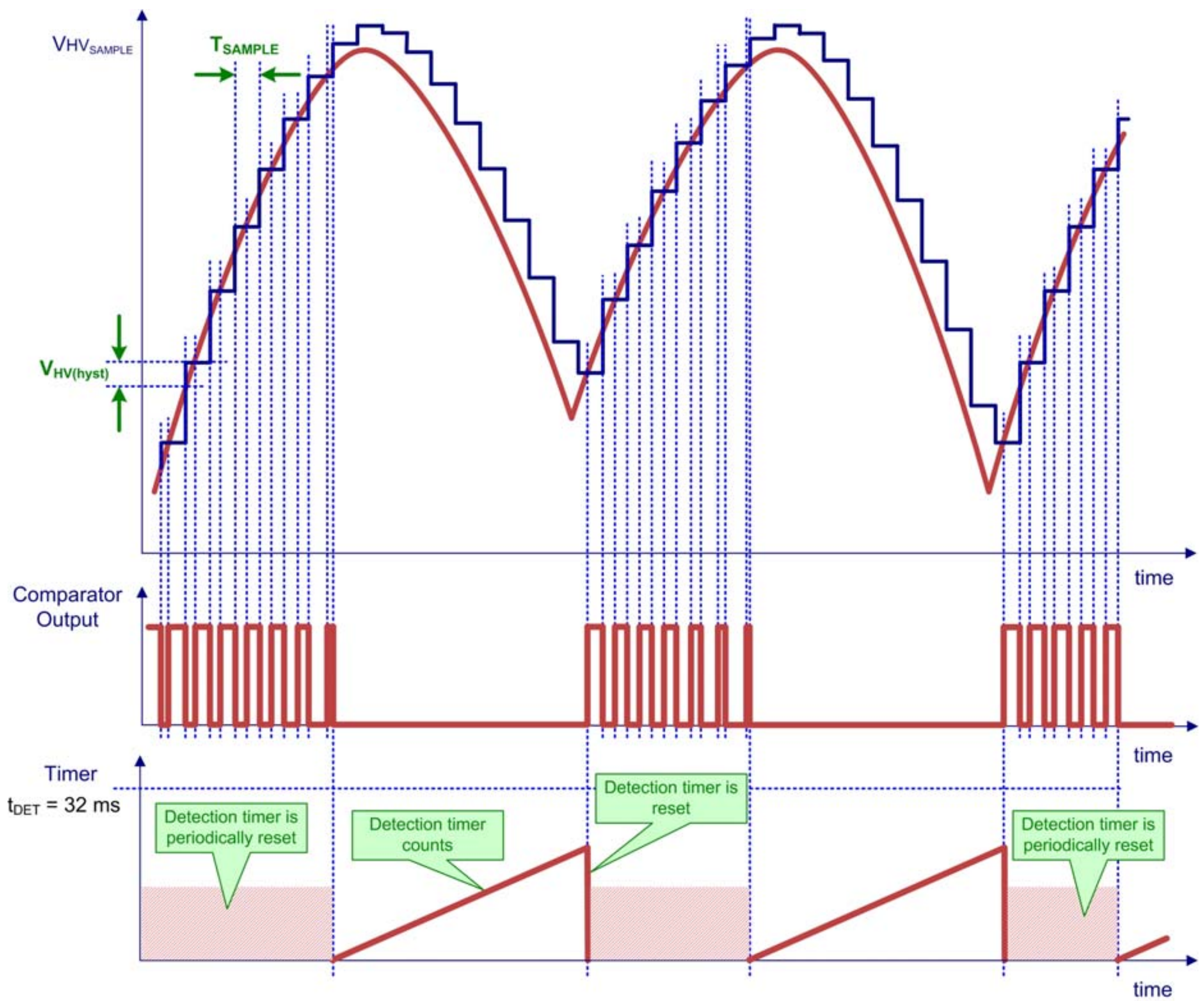


Figure 54. The ac Line Unplug Detector Timing Diagram