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# NCP1246

## Fixed Frequency Current Mode Controller for Flyback Converters

The NCP1246 is a new fixed-frequency current-mode controller featuring the Dynamic Self-Supply. This function greatly simplifies the design of the auxiliary supply and the  $V_{CC}$  capacitor by activating the internal startup current source to supply the controller during start-up, transients, latch, stand-by etc. This device contains a special HV detector which detect the application unplug from the AC input line and triggers the X2 discharge current. This HV structure allows the brown-out detection as well.

It features a timer-based fault detection that ensures the detection of overload and an adjustable compensation to help keep the maximum power independent of the input voltage.

Due to frequency foldback, the controller exhibits excellent efficiency in light load condition while still achieving very low standby power consumption. Internal frequency jittering, ramp compensation, and a versatile latch input make this controller an excellent candidate for the robust power supply designs.

A dedicated Off mode allows to reach the extremely low no load input power consumption via “sleeping” whole device and thus minimize the power consumption of the control circuitry.

### Features

- Fixed-Frequency Current-Mode Operation (65 kHz and 100 kHz frequency options)
- Frequency Foldback then Skip Mode for Maximized Performance in Light Load and Standby Conditions
- Timer-Based Overload Protection with Latched (Option A) or Auto-Recovery (Option B) Operation
- High-voltage Current Source with Brown-Out Detection and Dynamic Self-Supply, Simplifying the Design of the  $V_{CC}$  Circuitry
- Frequency Modulation for Softened EMI Signature
- Adjustable Overpower Protection Dependant on the Bulk Voltage
- Latch-off Input Combined with the Overpower Protection Sensing Input
- $V_{CC}$  Operation up to 28 V, With Overvoltage Detection
- 500/800 mA Source/Sink Drive Peak Current Capability
- 10 ms Soft-Start, 4 ms Soft-Start (AL/BL Versions)
- Internal Thermal Shutdown
- No-Load Standby Power < 30 mW
- X2 Capacitor in EMI Filter Discharging Feature
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



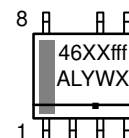
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### MARKING DIAGRAM

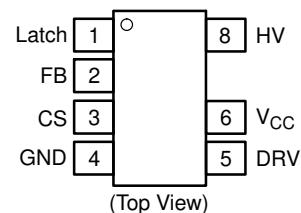


SOIC-7  
CASE 751U



46XXfff = Specific Device Code  
XX = A, B or AL  
fff = 065 or 100  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 38 of this data sheet.

### Typical Applications

- AC-DC Adapters for Notebooks, LCD, and Printers
- Offline Battery Chargers
- Consumer Electronic Power Supplies
- Auxiliary/Housekeeping Power Supplies
- Offline Adapters for Notebooks

# NCP1246

## TYPICAL APPLICATION EXAMPLE

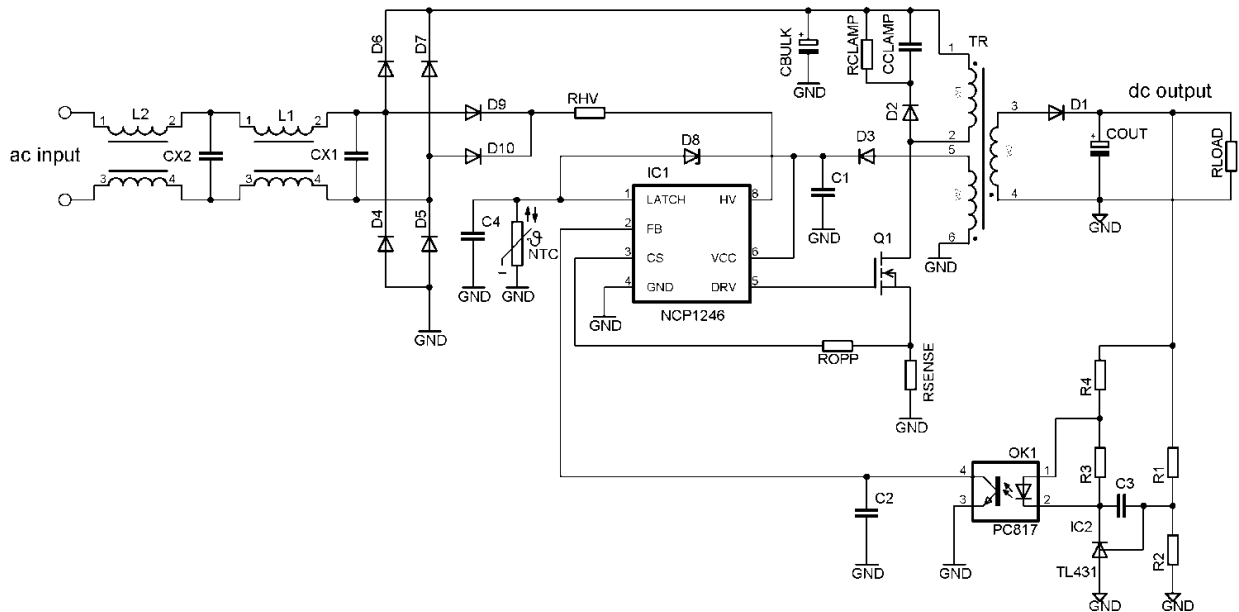


Figure 1. Flyback Converter Application Using the NCP1246

### PIN FUNCTION DESCRIPTION

Pin No	Pin Name	Function	Pin Description
1	LATCH	Latch-Off Input	Pull the pin up or down to latch-off the controller. An internal current source allows the direct connection of an NTC for over temperature detection.
2	FB	Feedback + Shutdown pin	An optocoupler collector to ground controls the output regulation. The part goes to the low consumption Off mode if the FB input pin is pulled to GND.
3	CS	Current Sense	This Input senses the Primary Current for current-mode operation, and offers an overpower compensation adjustment.
4	GND	-	The controller ground
5	DRV	Drive output	Drives external MOSFET
6	VCC	VCC input	This supply pin accepts up to 28 Vdc, with overvoltage detection. The pin is connected to an external auxiliary voltage. It is not allowed to connect another circuit to this pin to keep low input power consumption.
8	HV	High-voltage pin	Connects to the rectified AC line to perform the functions of Start-up Current Source, Self-Supply, brown-out detection and X2 capacitor discharge function and the HV sensing for the overpower protection purposes. It is not allowed to connect this pin to DC voltage.

# NCP1246

## SIMPLIFIED INTERNAL BLOCK SCHEMATIC

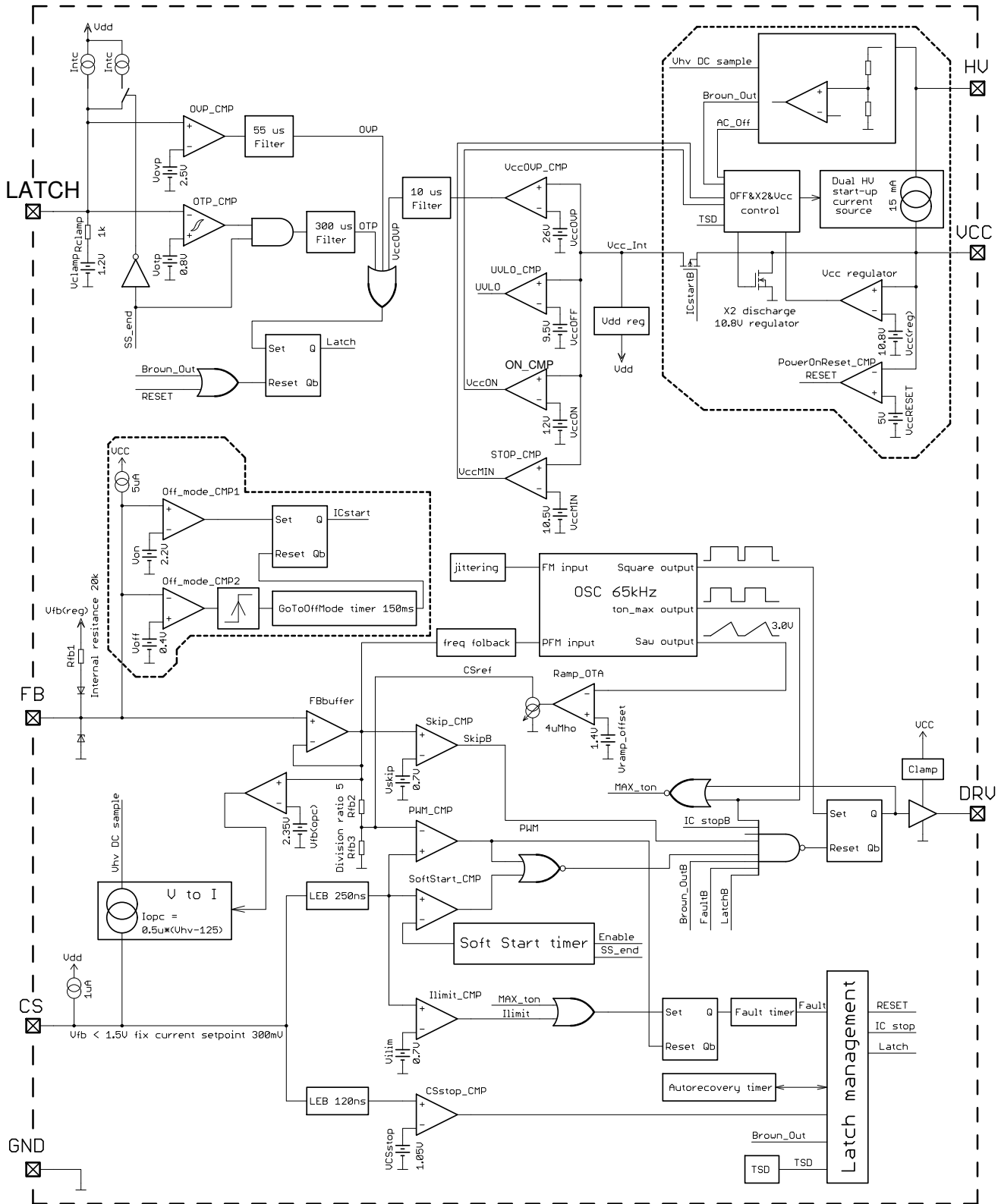


Figure 2. Simplified Internal Block Schematic

# NCP1246

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DRV (pin 5)	Maximum voltage on DRV pin (Dc-Current self-limited if operated within the allowed range) (Note 1)	-0.3 to 20 ±1000 (peak)	V mA
V <sub>CC</sub> (pin 6)	V <sub>CC</sub> Power Supply voltage, V <sub>CC</sub> pin, continuous voltage Power Supply voltage, V <sub>CC</sub> pin, continuous voltage (Note 1)	-0.3 to 28 ±30 (peak)	V mA
HV (pin 8)	Maximum voltage on HV pin (Dc-Current self-limited if operated within the allowed range)	-0.3 to 500 ±20	V mA
V <sub>max</sub>	Maximum voltage on low power pins (except pin 5, pin 6 and pin 8) (Dc-Current self-limited if operated within the allowed range) (Note 1)	-0.3 to 10 ±10 (peak)	V mA
R <sub>θJ-A</sub>	Thermal Resistance SOIC-7 Junction-to-Air, low conductivity PCB (Note 2) Junction-to-Air, medium conductivity PCB (Note 3) Junction-to-Air, high conductivity PCB (Note 4)	162 147 115	°C/W
R <sub>θJ-C</sub>	Thermal Resistance Junction-to-Case	73	°C/W
T <sub>JMAX</sub>	Operating Junction Temperature	-40 to +150	°C
T <sub>STRGMAX</sub>	Storage Temperature Range	-60 to +150	°C
	ESD Capability, HBM model (All pins except HV) per JEDEC Standard JESD22, Method A114E	> 2000	V
	ESD Capability, HBM model (HV pin) per JEDEC Standard JESD22, Method A114E	> 1000	V
	ESD Capability, Machine Model per JEDEC Standard JESD22, Method A115A	> 200	V
	ESD Capability, Charged Device Model per JEDEC Standard JESD22-C101D	> 1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.
2. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 50 mm<sup>2</sup> of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51-1 conductivity test PCB. Test conditions were under natural convection or zero air flow.
3. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 100 mm<sup>2</sup> of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51-2 conductivity test PCB. Test conditions were under natural convection or zero air flow.
4. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 650 mm<sup>2</sup> of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51-3 conductivity test PCB. Test conditions were under natural convection or zero air flow.

# NCP1246

**ELECTRICAL CHARACTERISTICS** (For typical values  $T_J = 25^\circ\text{C}$ , for min/max values  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{HV} = 125\text{ V}$ ,  $V_{CC} = 11\text{ V}$  unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
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## HIGH VOLTAGE CURRENT SOURCE

Minimum voltage for current source operation		$V_{HV(\min)}$	–	30	40	V
Current flowing out of $V_{CC}$ pin	$V_{CC} = 0\text{ V}$ $V_{CC} = V_{CC(\text{on})} - 0.5\text{ V}$	$I_{\text{start1}}$ $I_{\text{start2}}$	0.2 5	0.5 8	0.8 11	mA
Off-state leakage current	$V_{HV} = 500\text{ V}$ , $V_{CC} = 15\text{ V}$	$I_{\text{start(off)}}$	10	25	50	$\mu\text{A}$
Off-mode HV supply current	$V_{HV} = 141\text{ V}$ , $V_{HV} = 325\text{ V}$ , $V_{CC}$ loaded by $4.7\text{ }\mu\text{F}$ cap	$I_{HV(\text{off})}$	– –	45 50	60 70	$\mu\text{A}$

## SUPPLY

HV current source regulation threshold		$V_{CC(\text{reg})}$	8	11	–	V
Turn-on threshold level, $V_{CC}$ going up HV current source stop threshold		$V_{CC(\text{on})}$	11.0	12.0	13.0	V
HV current source restart threshold		$V_{CC(\text{min})}$	9.5	10.5	11.5	V
Turn-off threshold		$V_{CC(\text{off})}$	8.5	8.9	9.3	V
Overvoltage threshold		$V_{CC(\text{ovp})}$	25	26.5	28	V
Blanking duration on $V_{CC(\text{off})}$ and $V_{CC(\text{ovp})}$ detection		$t_{V_{CC}(\text{blank})}$	–	10	–	$\mu\text{s}$
$V_{CC}$ decreasing level at which the internal logic resets		$V_{CC(\text{reset})}$	4.8	7.0	7.7	V
$V_{CC}$ level for $I_{\text{START1}}$ to $I_{\text{START2}}$ transition		$V_{CC(\text{inhibit})}$	0.2	0.8	1.25	V
Internal current consumption (Note 5)	DRV open, $V_{FB} = 3\text{ V}$ , 65 kHz DRV open, $V_{FB} = 3\text{ V}$ , 100 kHz  Cdrv = 1 nF, $V_{FB} = 3\text{ V}$ , 65 kHz Cdrv = 1 nF, $V_{FB} = 3\text{ V}$ , 100 kHz  Off mode (skip or before start-up)  Fault mode (fault or latch)	$I_{CC1}$ $I_{CC1}$  $I_{CC2}$ $I_{CC2}$  $I_{CC3}$  $I_{CC4}$	1.3 1.3  1.8 2.3  0.67  0.3	1.85 1.85  2.6 2.9  0.9  0.6	2.2 2.2  3.0 3.5  1.13  0.9	mA

## BROWN-OUT

Brown-Out thresholds	$V_{HV}$ going up $V_{HV}$ going down	$V_{HV(\text{start})}$ $V_{HV(\text{stop})}$	102 94	111 103	120 112	V
Brown-Out thresholds (AL/BL Versions)	$V_{HV}$ going up $V_{HV}$ going down	$V_{HV(\text{start})}$ $V_{HV(\text{stop})}$	92 84	101 93	110 102	V
Timer duration for line cycle drop-out		$t_{HV}$	43	–	86	ms

## X2 DISCHARGE

Comparator hysteresis observed at HV pin		$V_{HV(\text{hyst})}$	1.5	3.5	5	V
HV signal sampling period		$T_{\text{sample}}$	–	1.0	–	ms
Timer duration for no line detection		$t_{\text{DET}}$	21	32	43	ms
Discharge timer duration		$t_{\text{DIS}}$	21	32	43	ms

## OSCILLATOR

Oscillator frequency		$f_{\text{OSC}}$	58 87	65 100	72 109	kHz
Maximum on time for $T_J = 25^\circ\text{C}$ to $+125^\circ\text{C}$ only	$f_{\text{OSC}} = 65\text{ kHz}$ $f_{\text{OSC}} = 100\text{ kHz}$	$t_{\text{ONmax}(65\text{kHz})}$ $t_{\text{ONmax}(100\text{kHz})}$	11.5 7.5	12.3 8.0	13.1 8.5	$\mu\text{s}$

- Internal supply current only, currents sourced via FB pin is not included (current is flowing in GND pin only).
- Guaranteed by design.
- CS pin source current is a sum of  $I_{\text{bias}}$  and  $I_{\text{OPC}}$ , thus at  $V_{HV} = 125\text{ V}$  is observed the  $I_{\text{bias}}$  only, because  $I_{\text{OPC}}$  is switched off.

# NCP1246

**ELECTRICAL CHARACTERISTICS** (For typical values  $T_J = 25^\circ\text{C}$ , for min/max values  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{HV} = 125\text{ V}$ ,  $V_{CC} = 11\text{ V}$  unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
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## OSCILLATOR

Maximum on time	$f_{\text{OSC}} = 65\text{ kHz}$ $f_{\text{OSC}} = 100\text{ kHz}$	$t_{\text{ONmax}}(65\text{kHz})$ $t_{\text{ONmax}}(100\text{kHz})$	11.3 7.4	12.3 8.0	13.1 8.5	$\mu\text{s}$
Maximum duty cycle (corresponding to maximum on time at maximum switching frequency)	$f_{\text{OSC}} = 65\text{ kHz}$ $f_{\text{OSC}} = 100\text{ kHz}$	$D_{\text{MAX}}$	–	80	–	%
Frequency jittering amplitude, in percentage of $F_{\text{OSC}}$		$A_{\text{jitter}}$	$\pm 4$	$\pm 6$	$\pm 8$	%
Frequency jittering modulation frequency		$F_{\text{jitter}}$	85	125	165	Hz

## FREQUENCY FOLDBACK

Feedback voltage threshold below which frequency foldback starts		$V_{\text{FB}}(\text{foldS})$	1.8	2.0	2.2	V
Feedback voltage threshold below which frequency foldback is complete		$V_{\text{FB}}(\text{foldE})$	0.8	0.9	1.0	V
Minimum switching frequency	$V_{\text{FB}} = V_{\text{skip(in)}} + 0.1$	$f_{\text{OSC(min)}}$	23	27	32	kHz

## OUTPUT DRIVER

Rise time, 10 to 90% of $V_{\text{CC}}$	$V_{\text{CC}} = V_{\text{CC(min)}} + 0.2\text{ V}$ , $C_{\text{DRV}} = 1\text{ nF}$	$t_{\text{rise}}$	–	40	70	ns
Fall time, 90 to 10% of $V_{\text{CC}}$	$V_{\text{CC}} = V_{\text{CC(min)}} + 0.2\text{ V}$ , $C_{\text{DRV}} = 1\text{ nF}$	$t_{\text{fall}}$	–	40	70	ns
Current capability	$V_{\text{CC}} = V_{\text{CC(min)}} + 0.2\text{ V}$ , $C_{\text{DRV}} = 1\text{ nF}$ DRV high, $V_{\text{DRV}} = 0\text{ V}$ DRV low, $V_{\text{DRV}} = V_{\text{CC}}$	$I_{\text{DRV(source)}}$ $I_{\text{DRV(sink)}}$	– –	500 800	– –	mA
Clamping voltage (maximum gate voltage)	$V_{\text{CC}} = V_{\text{CCmax}} - 0.2\text{ V}$ , DRV high, $R_{\text{DRV}} = 33\text{ k}\Omega$ , $C_{\text{load}} = 220\text{ pF}$	$V_{\text{DRV(clamp)}}$	11	13.5	16	V
High-state voltage drop	$V_{\text{CC}} = V_{\text{CC(min)}} + 0.2\text{ V}$ , $R_{\text{DRV}} = 33\text{ k}\Omega$ , DRV high	$V_{\text{DRV(drop)}}$	–	–	1	V

## CURRENT SENSE

Input Pull-up Current	$V_{\text{CS}} = 0.7\text{ V}$	$I_{\text{bias}}$	–	1	–	$\mu\text{A}$
Maximum internal current setpoint	$V_{\text{FB}} > 3.5\text{ V}$	$V_{\text{ILIM}}$	0.66	0.70	0.74	V
Propagation delay from $V_{\text{ILimit}}$ detection to DRV off	$V_{\text{CS}} = V_{\text{ILIM}}$	$t_{\text{delay}}$	–	80	110	ns
Leading Edge Blanking Duration for $V_{\text{ILIM}}$		$t_{\text{LEB}}$	200	250	320	ns
Threshold for immediate fault protection activation		$V_{\text{CS(stop)}}$	0.95	1.05	1.15	V
Leading Edge Blanking Duration for $V_{\text{CS(stop)}}$ (Note 6)		$t_{\text{BCS}}$	90	120	150	ns
Soft-start duration	From 1 <sup>st</sup> pulse to $V_{\text{CS}} = V_{\text{ILIM}}$ AL/BL Versions	$t_{\text{SSTART}}$	8 2.8	11 4.0	14 5.2	ms
Frozen current setpoint		$V_{\text{I(freeze)}}$	275	300	325	mV

## INTERNAL SLOPE COMPENSATION

Slope of the compensation ramp		$S_{\text{comp}}(65\text{kHz})$ $S_{\text{comp}}(100\text{kHz})$	– –	–32.5 –50	– –	mV / $\mu\text{s}$
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## FEEDBACK

Internal pull-up resistor	$T_J = 25^\circ\text{C}$	$R_{\text{FB(up)}}$	15	20	25	k $\Omega$
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- Internal supply current only, currents sourced via FB pin is not included (current is flowing in GND pin only).
- Guaranteed by design.
- CS pin source current is a sum of  $I_{\text{bias}}$  and  $I_{\text{OPC}}$ , thus at  $V_{\text{HV}} = 125\text{ V}$  is observed the  $I_{\text{bias}}$  only, because  $I_{\text{OPC}}$  is switched off.

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**ELECTRICAL CHARACTERISTICS** (For typical values  $T_J = 25^\circ\text{C}$ , for min/max values  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{HV} = 125\text{ V}$ ,  $V_{CC} = 11\text{ V}$  unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
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## FEEDBACK

$V_{FB}$ to internal current setpoint division ratio		$K_{FB}$	4.7	5	5.3	–
Internal pull-up voltage on the FB pin (Note 6)		$V_{FB(ref)}$	4.5	5	5.5	V
Feedback voltage below which the peak current is frozen		$V_{FB(freeze)}$	1.35	1.5	1.65	V

## SKIP CYCLE MODE

Feedback voltage thresholds for skip mode	$V_{FB}$ going down $V_{FB}$ going up	$V_{skip(in)}$ $V_{skip(out)}$	0.63 0.72	0.70 0.80	0.77 0.88	V
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## REMOTE CONTROL ON FB PIN

The voltage above which the part enters the on mode	$V_{CC} > V_{CC(off)}$ , $V_{HV} = 60\text{ V}$	$V_{ON}$	–	2.2	–	V
The voltage below which the part enters the off mode	$V_{CC} > V_{CC(off)}$	$V_{OFF}$	0.35	0.40	0.45	V
Minimum hysteresis between the $V_{ON}$ and $V_{OFF}$	$V_{CC} > V_{CC(off)}$ , $V_{HV} = 60\text{ V}$	$V_{HYST}$	500	–	–	mV
Pull-up current in off mode	$V_{CC} > V_{CC(off)}$	$I_{OFF}$	–	5	–	$\mu\text{A}$
Go To Off mode timer	$V_{CC} > V_{CC(off)}$	$t_{GTOM}$	100	150	300	ms

## OVERLOAD PROTECTION

Fault timer duration		$t_{fault}$	108	128	178	ms
Autorecovery mode latch-off time duration		$t_{autorec}$	0.85	1.00	1.35	s

## OVERPOWER PROTECTION

$V_{HV}$ to $I_{OPC}$ conversion ratio		$K_{OPC}$	–	0.54	–	$\mu\text{A} / \text{V}$
Current flowing out of CS pin (Note 7)	$V_{HV} = 125\text{ V}$ $V_{HV} = 162\text{ V}$ $V_{HV} = 325\text{ V}$ $V_{HV} = 365\text{ V}$	$I_{OPC(125)}$ $I_{OPC(162)}$ $I_{OPC(325)}$ $I_{OPC(365)}$	– – – 105	0 20 110 130	– – – 150	$\mu\text{A}$
FB voltage above which $I_{OPC}$ is applied	$V_{HV} = 365\text{ V}$	$V_{FB(OPCF)}$	2.12	2.35	2.58	V
FB voltage below which is no $I_{OPC}$ applied	$V_{HV} = 365\text{ V}$	$V_{FB(OPCE)}$	–	2.15	–	V

## LATCH-OFF INPUT

High threshold	$V_{Latch}$ going up	$V_{OVP}$	2.35	2.5	2.65	V
Low threshold	$V_{Latch}$ going down	$V_{OTP}$	0.76	0.8	0.84	V
Current source for direct NTC connection During normal operation During soft-start	$V_{Latch} = 0\text{ V}$	$I_{NTC}$ $I_{NTC(SSSTART)}$	65 130	95 190	105 210	$\mu\text{A}$
Blanking duration on high latch detection	65 kHz version 100 kHz version	$t_{Latch(OVP)}$	35 20	50 35	70 50	$\mu\text{s}$
Blanking duration on low latch detection		$t_{Latch(OTP)}$	–	350	–	$\mu\text{s}$
Clamping voltage	$I_{Latch} = 0\text{ mA}$ $I_{Latch} = 1\text{ mA}$	$V_{clamp0(Latch)}$ $V_{clamp1(Latch)}$	1.0 1.8	1.2 2.4	1.4 3.0	V

## TEMPERATURE SHUTDOWN

Temperature shutdown	$T_J$ going up	$T_{TSD}$	–	150	–	$^\circ\text{C}$
Temperature shutdown hysteresis	$T_J$ going down	$T_{TSD(HYS)}$	–	30	–	$^\circ\text{C}$

5. Internal supply current only, currents sourced via FB pin is not included (current is flowing in GND pin only).

6. Guaranteed by design.

7. CS pin source current is a sum of  $I_{bias}$  and  $I_{OPC}$ , thus at  $V_{HV} = 125\text{ V}$  is observed the  $I_{bias}$  only, because  $I_{OPC}$  is switched off.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



TYPICAL CHARACTERISTIC

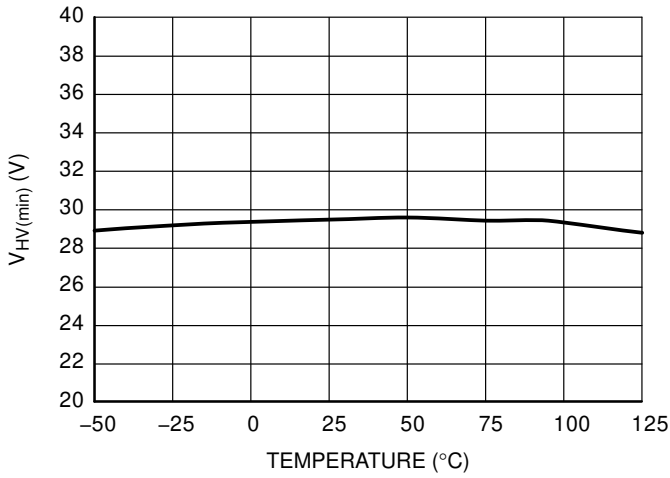


Figure 3. Minimum Current Source Operation  
V<sub>HV(min)</sub>

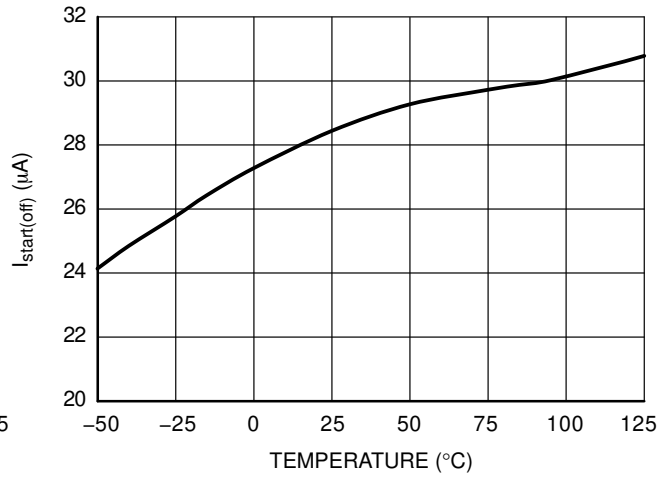


Figure 4. Off-State Leakage Current I<sub>start(off)</sub>

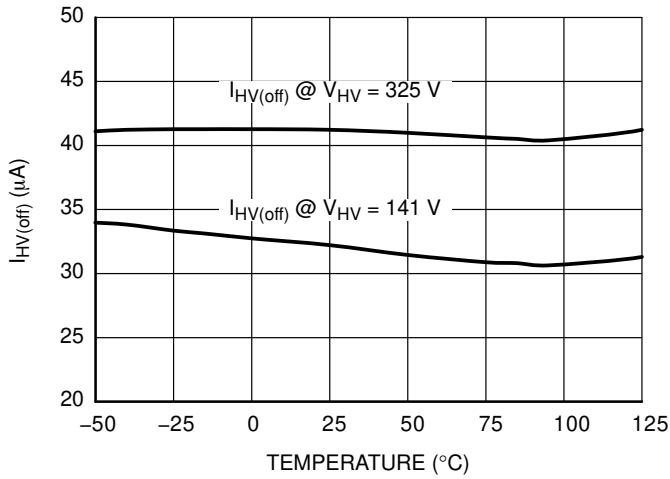


Figure 5. Off-Mode HV Supply Current I<sub>HV(off)</sub>

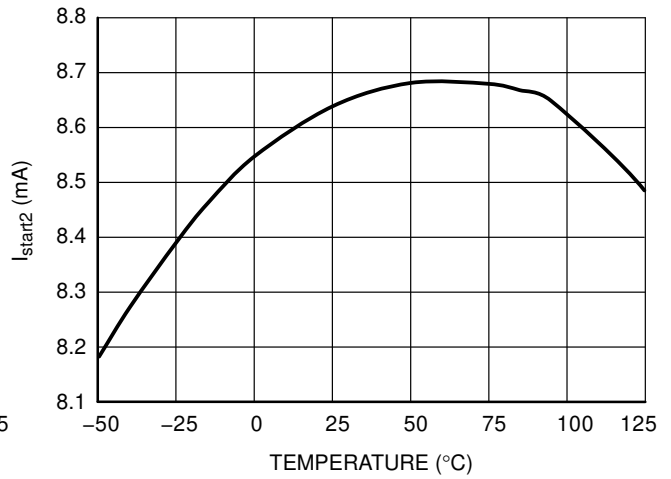


Figure 6. High Voltage Startup Current  
Flowing Out of V<sub>CC</sub> Pin I<sub>start2</sub>

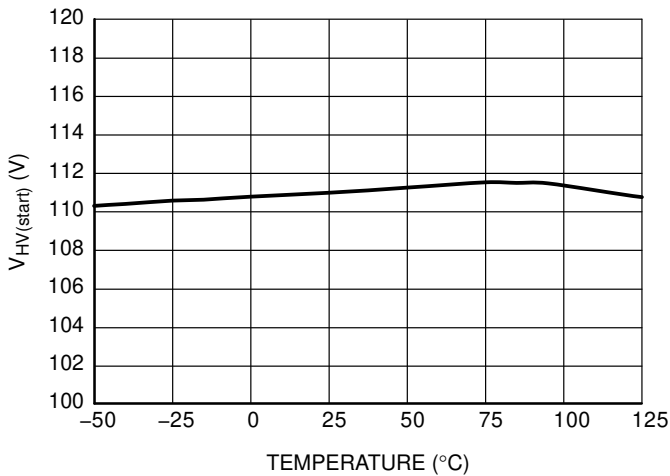


Figure 7. Brown-out Device Start Threshold  
V<sub>HV(start)</sub>

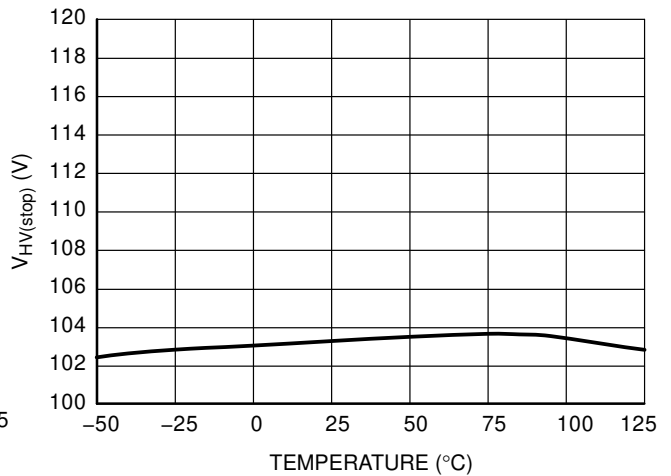
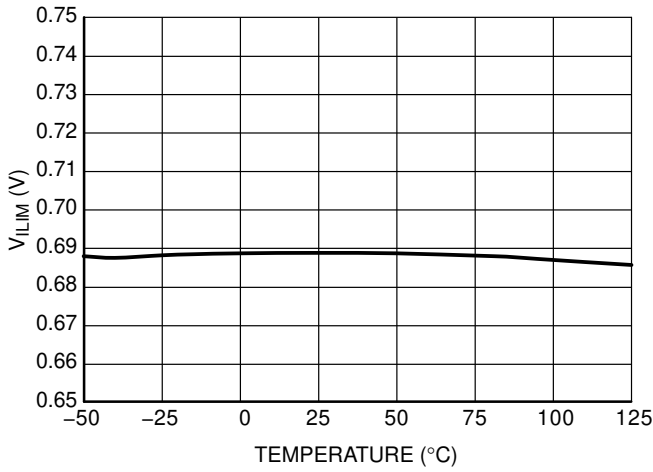


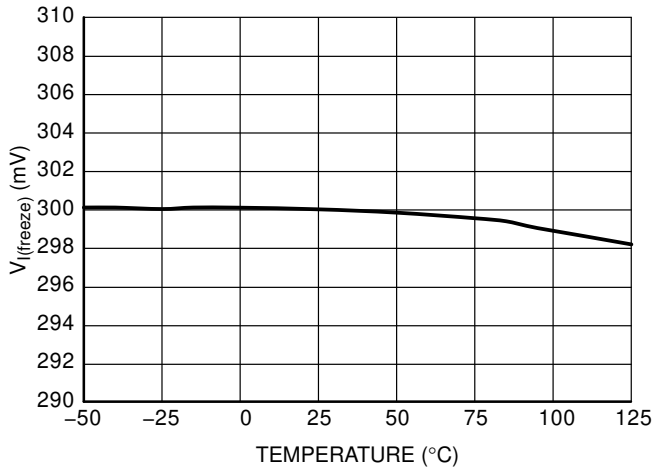
Figure 8. Brown-out Device Stop Threshold  
V<sub>HV(stop)</sub>

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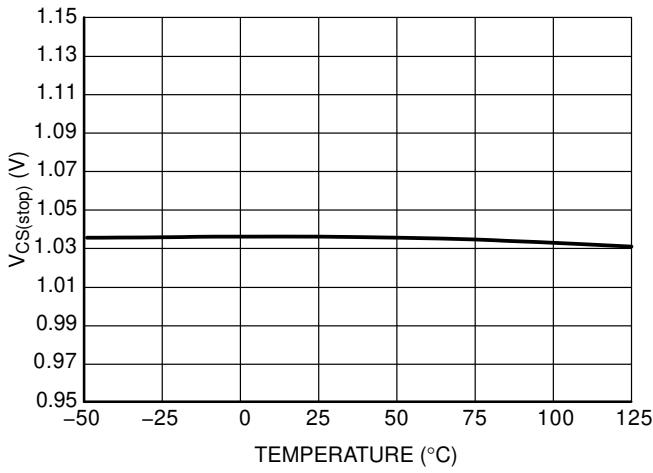
## TYPICAL CHARACTERISTIC



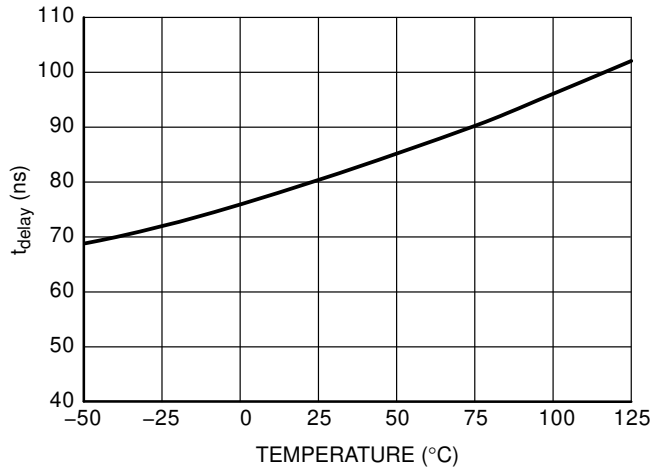
**Figure 9. Maximum Internal Current Setpoint  $V_{ILIM}$**



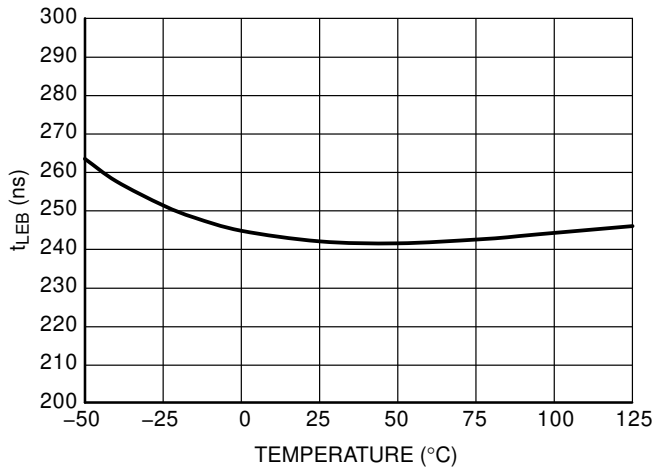
**Figure 10. Frozen Current Setpoint  $V_{I(freeze)}$  for the Light Load Operation**



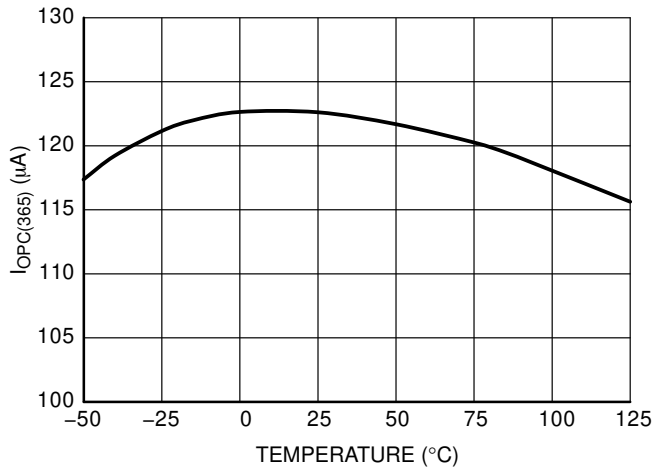
**Figure 11. Threshold for Immediate Fault Protection Activation  $V_{CS(stop)}$**



**Figure 12. Propagation Delay  $t_{delay}$**



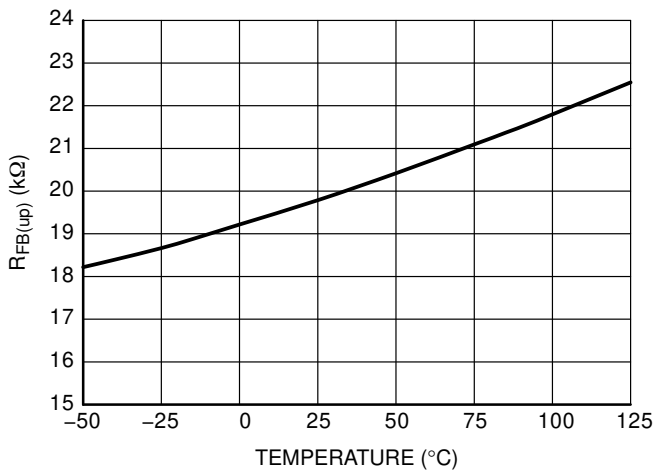
**Figure 13. Leading Edge Blanking Duration  $t_{LEB}$**



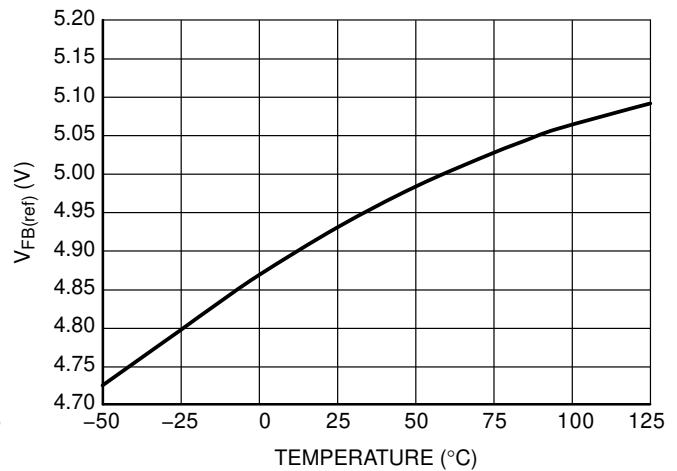
**Figure 14. Maximum Overpower Compensating Current  $I_{OP(365)}$  Flowing Out of CS Pin**

# NCP1246

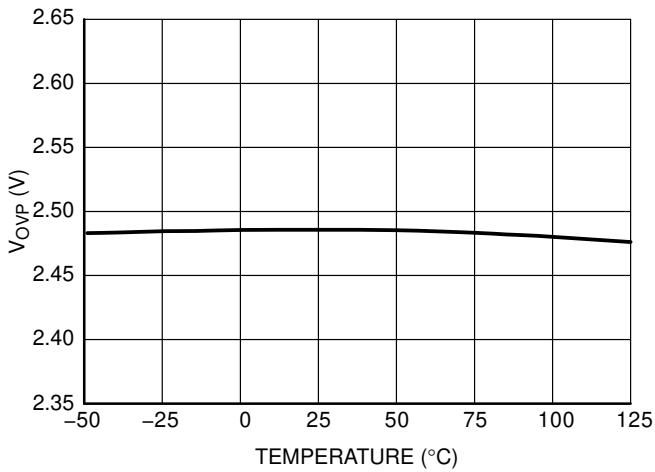
## TYPICAL CHARACTERISTIC



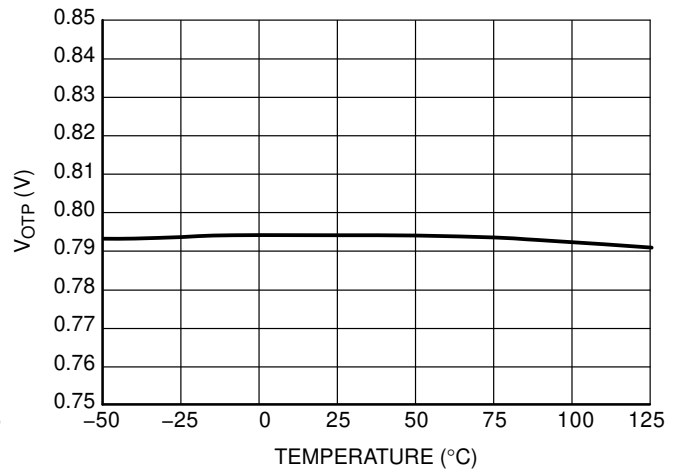
**Figure 15. FB Pin Internal Pull-up Resistor  $R_{FB(up)}$**



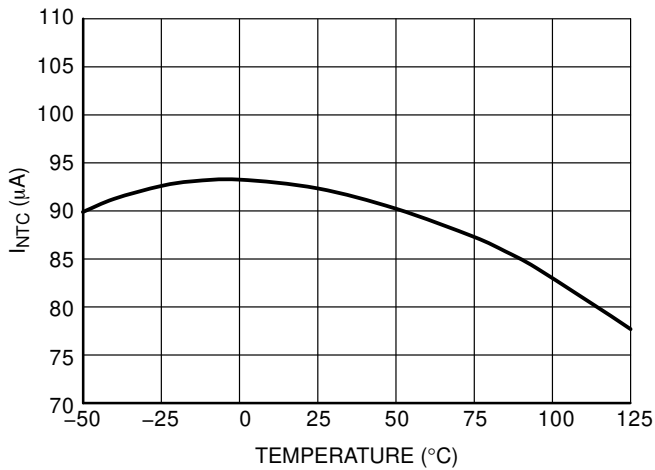
**Figure 16. FB Pin Open Voltage  $V_{FB(ref)}$**



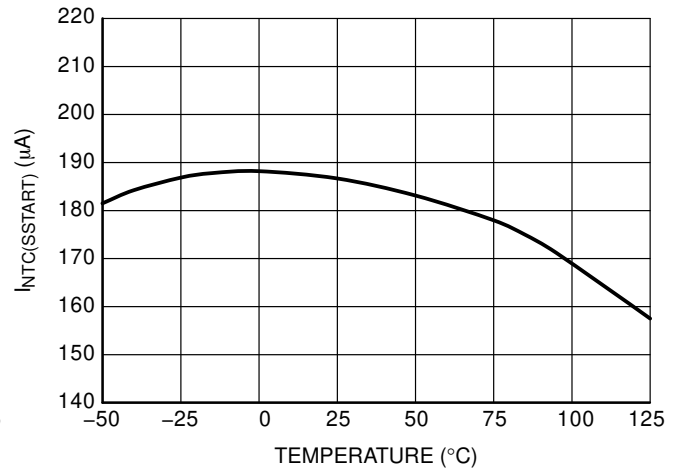
**Figure 17. Latch Pin High Threshold  $V_{OVP}$**



**Figure 18. Latch Pin Low Threshold  $V_{OTP}$**



**Figure 19. Current  $I_{NTC}$  Sourced from the Latch Pin, Allowing Direct NTC Connection**



**Figure 20. Current  $I_{NTC(SSSTART)}$  Sourced from the Latch Pin, During Soft-Start**

# NCP1246

## TYPICAL CHARACTERISTIC

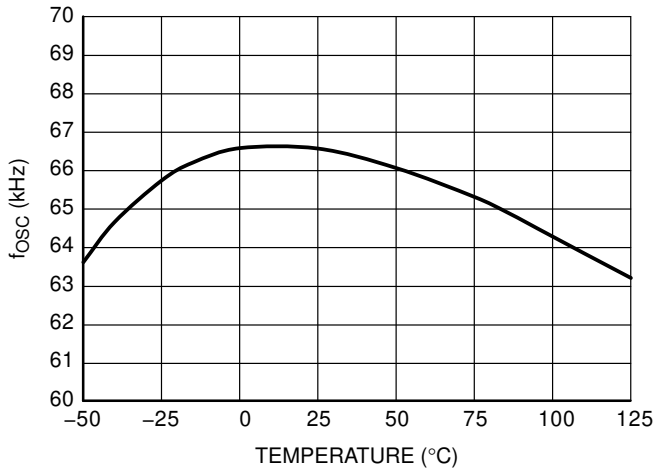


Figure 21. Oscillator  $f_{osc}$  for the 65 kHz Version

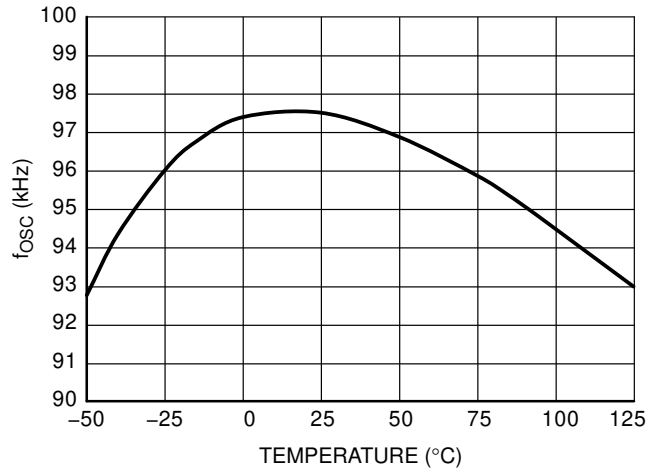


Figure 22. Oscillator  $f_{osc}$  for the 100 kHz Version

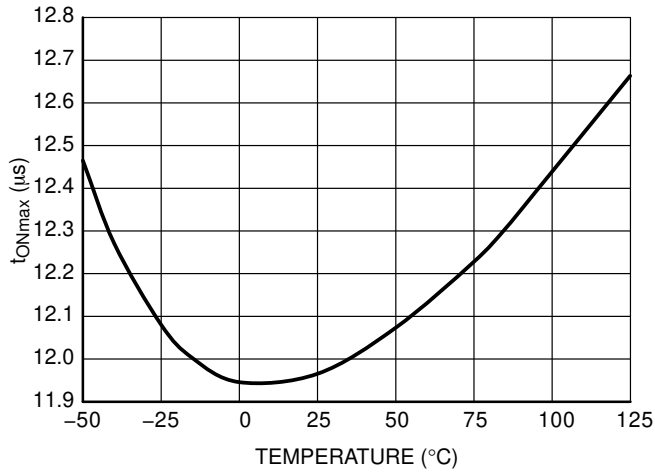


Figure 23. Maximum ON Time  $t_{ONmax}$  for the 65 kHz Version

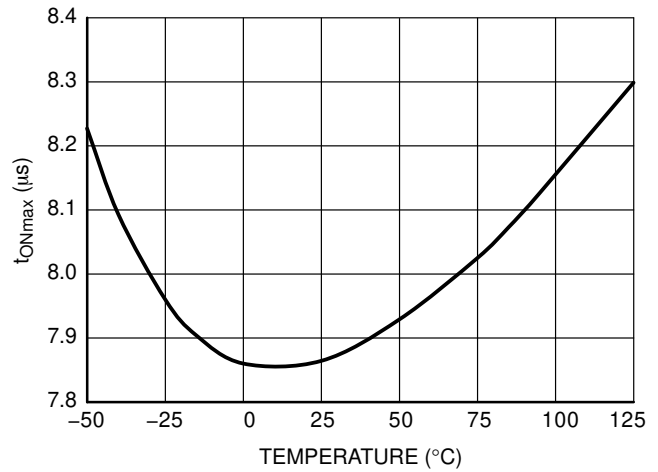


Figure 24. Maximum ON Time  $t_{ONmax}$  for the 100 kHz Version

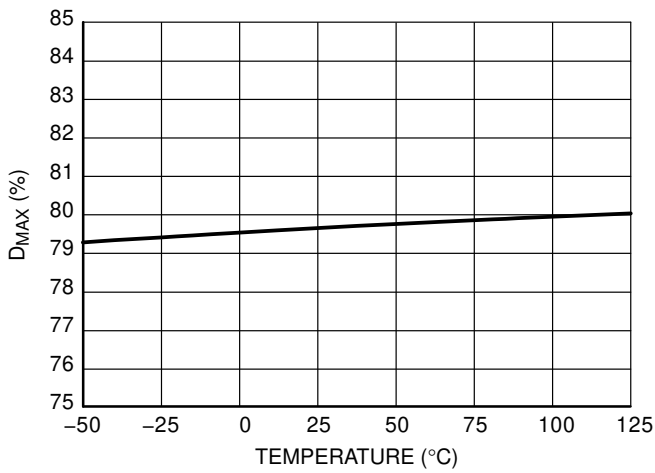


Figure 25. Maximum Duty Ratio  $D_{MAX}$

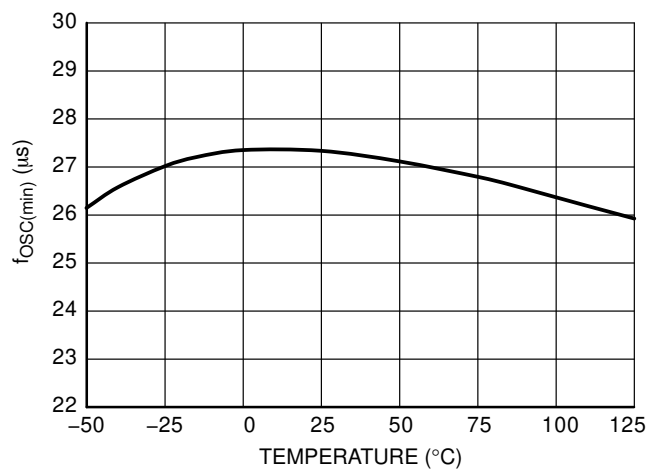
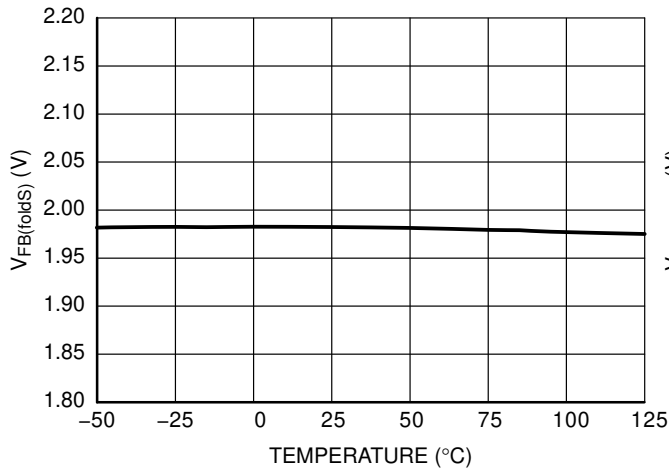


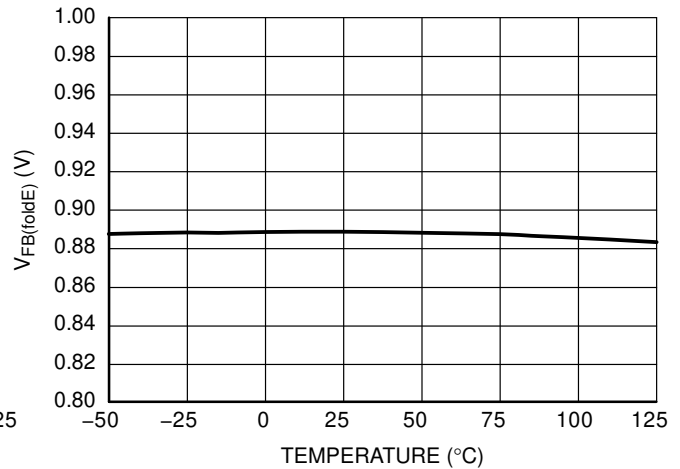
Figure 26. Minimum Switching Frequency  $f_{osc(min)}$

# NCP1246

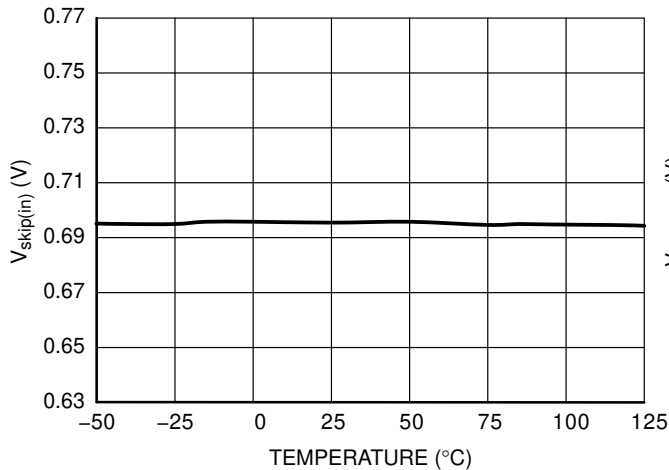
## TYPICAL CHARACTERISTIC



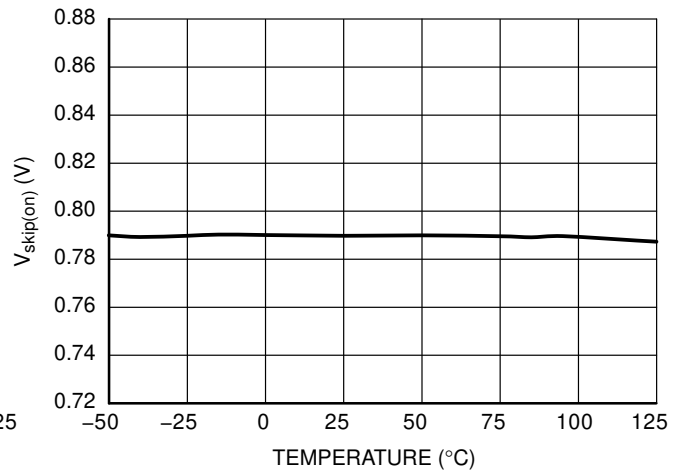
**Figure 27. FB Pin Voltage Below Which Frequency Foldback Starts  $V_{FB(foldS)}$**



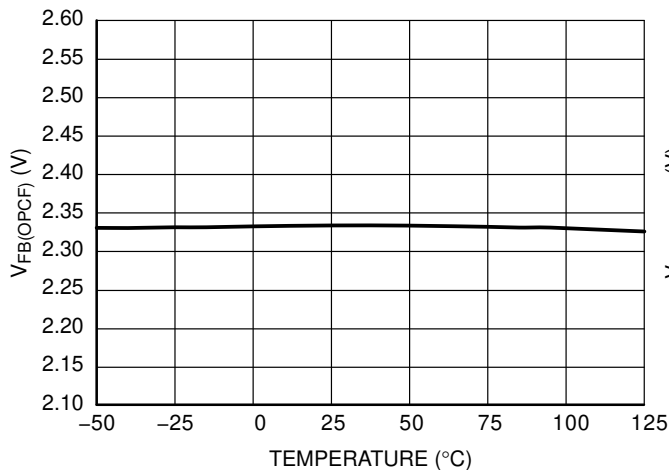
**Figure 28. FB Pin Voltage Below Which Frequency Foldback Complete  $V_{FB(foldE)}$**



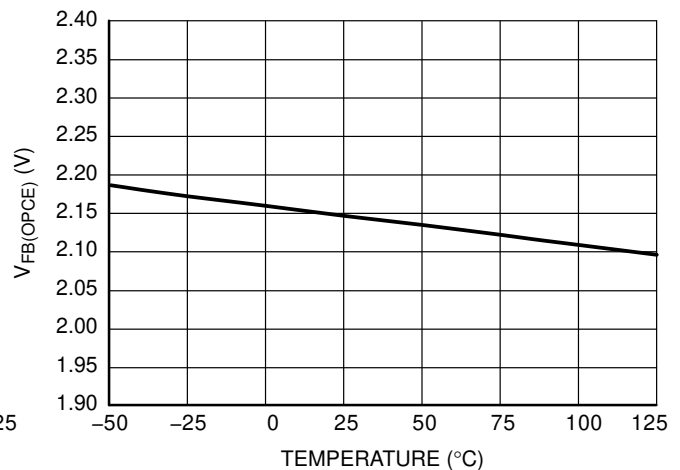
**Figure 29. FB Pin Skip-In Level  $V_{skip(in)}$**



**Figure 30. FB Pin Skip-Out Level  $V_{skip(out)}$**



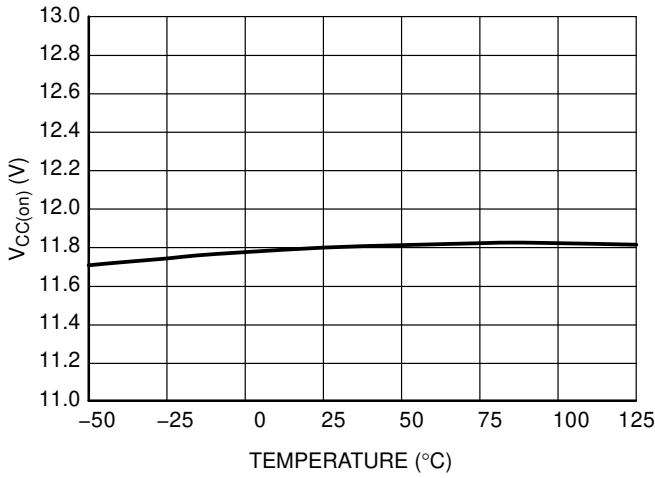
**Figure 31. FB Pin Level  $V_{FB(OPCF)}$  Above Which is the Overpower Compensation Applied**



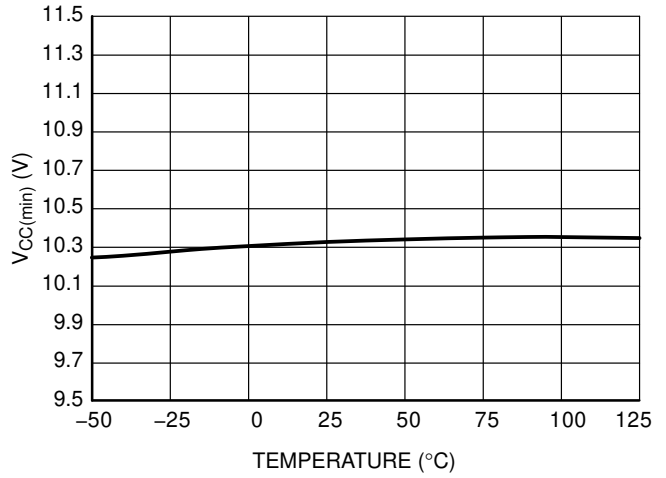
**Figure 32. FB Pin Level  $V_{FB(OPCE)}$  Below Which is No Overpower Compensation Applied**

# NCP1246

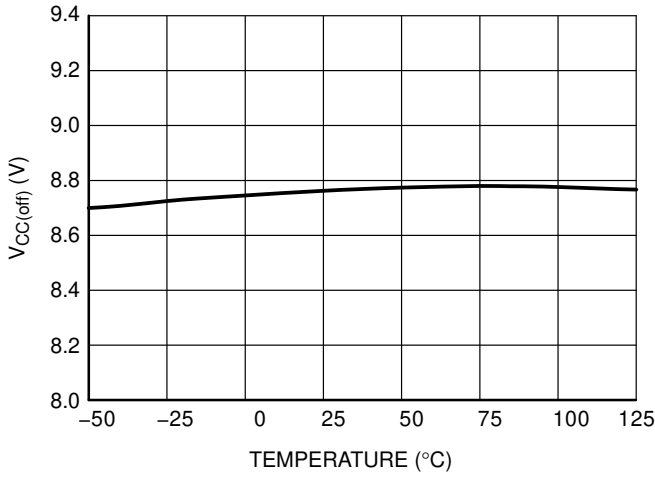
## TYPICAL CHARACTERISTIC



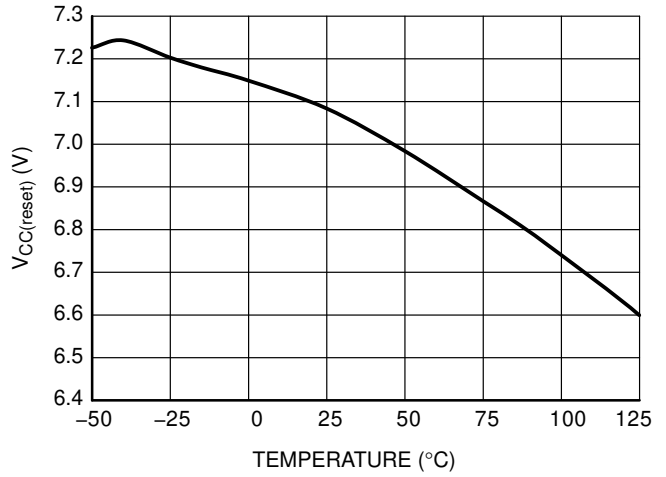
**Figure 33. V<sub>CC</sub> Turn-on Threshold Level, V<sub>CC</sub> Going Up HV Current Source Stop Threshold V<sub>CC(on)</sub>**



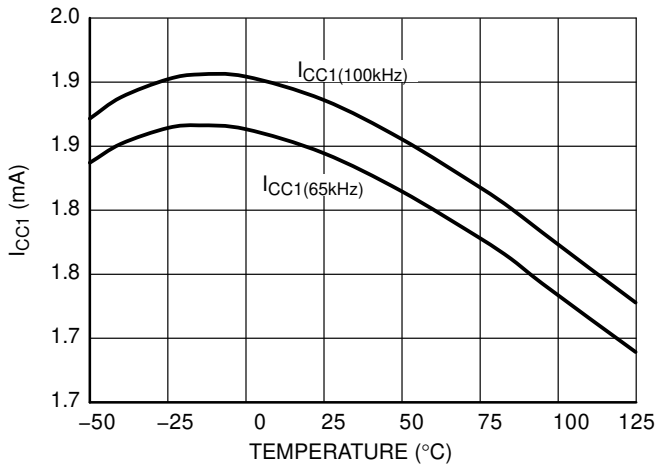
**Figure 34. HV Current Source Restart Threshold V<sub>CC(min)</sub>**



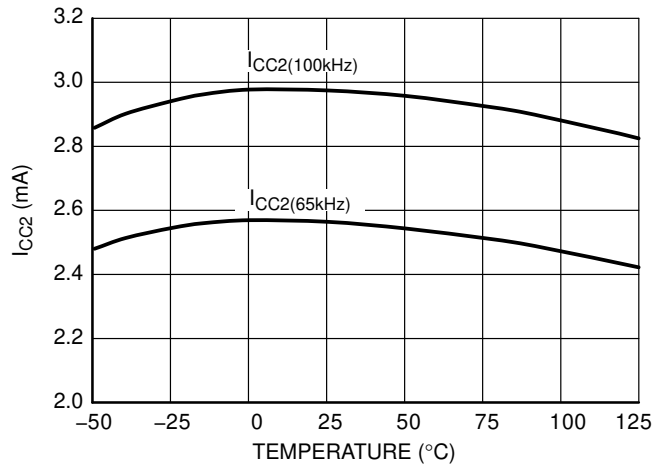
**Figure 35. V<sub>CC</sub> Turn-off Threshold (UVLO) V<sub>CC(off)</sub>**



**Figure 36. V<sub>CC</sub> Decreasing Level at Which the Internal Logic Resets V<sub>CC(reset)</sub>**



**Figure 37. Internal Current Consumption when DRV Pin is Unloaded**



**Figure 38. Internal Current Consumption when DRV Pin is Loaded by 1 nF**

TYPICAL CHARACTERISTIC

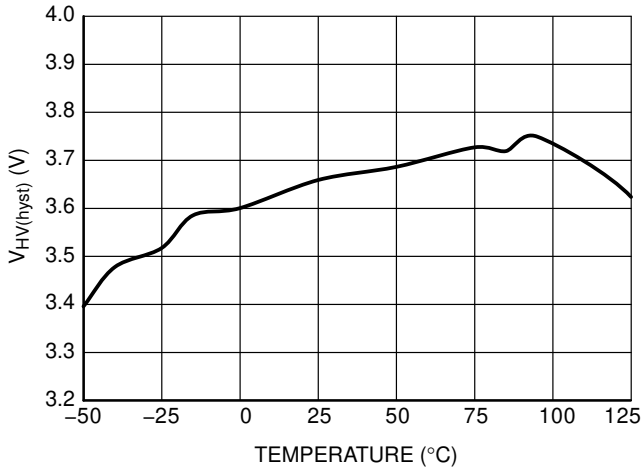


Figure 39. X2 Discharge Comparator Hysteresis Observed at HV Pin  $V_{HV(hyst)}$

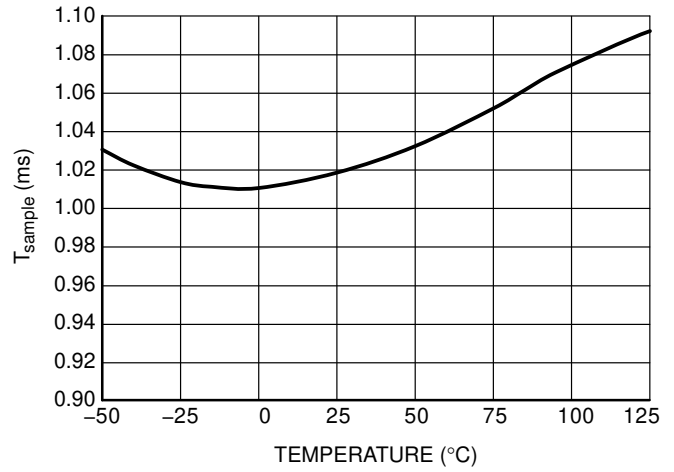


Figure 40. HV Signal Sampling Period  $T_{sample}$

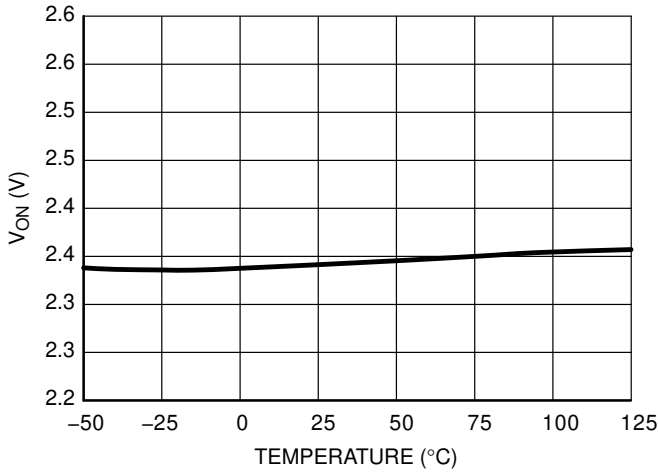


Figure 41. FB Pin Voltage Level Above Which is Entered On Mode  $V_{ON}$

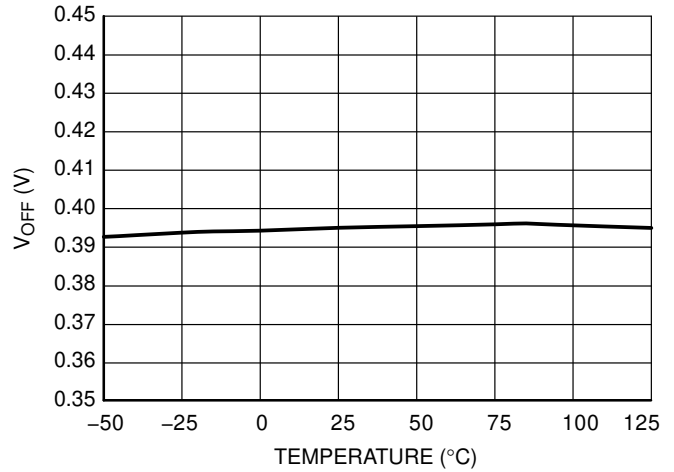


Figure 42. FB Pin Voltage Level Below Which is Entered Off Mode  $V_{OFF}$

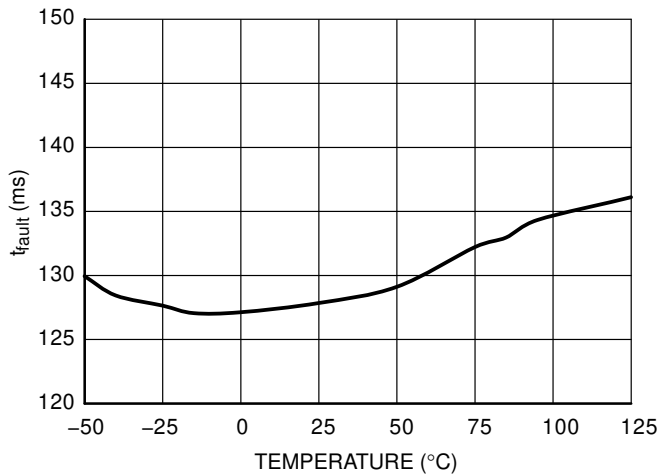


Figure 43. Fault Timer Duration  $t_{fault}$

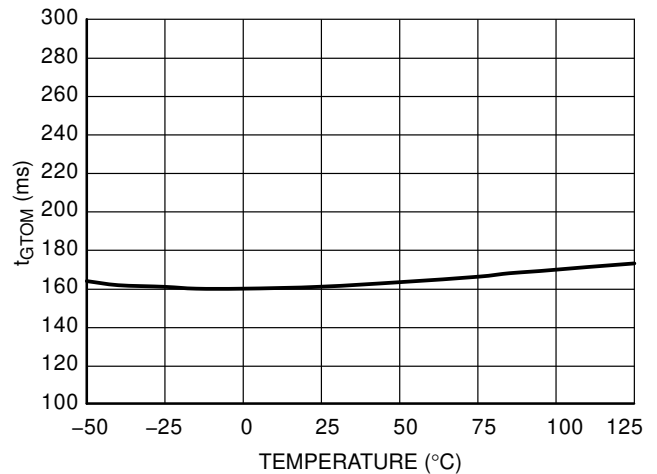


Figure 44. Go To Off Mode Timer Duration  $t_{GTOM}$

APPLICATION INFORMATION

Functional Description

The NCP1246 includes all necessary features to build a safe and efficient power supply based on a fixed-frequency flyback converter. The NCP1246 is a multimode controller as illustrated in Figure 45. The mode of operation depends upon line and load condition. Under all modes of operation, the NCP1246 terminates the DRV signal based on the switch current. Thus, the NCP1246 always operates in current mode control so that the power MOSFET current is always limited.

Under normal operating conditions, the FB pin commands the operating mode of the NCP1246 at the voltage thresholds shown in Figure 45. At normal rated operating loads (from 100% to approximately 33% full rated power) the NCP1246 controls the converter in fixed frequency PWM mode. It can operate in the continuous conduction mode (CCM) or discontinuous conduction mode (DCM) depending upon the input voltage and loading conditions. If the controller is used in CCM with a wide input voltage range, the duty-ratio may increase up to 50%. The build-in slope compensation prevents the appearance of sub-harmonic oscillations in this operating area.

For loads that are between approximately 32% and 10% of full rated power, the converter operates in frequency foldback mode (FFM). If the feedback pin voltage is lower than 1.5 V the peak switch current is kept constant and the output voltage is regulated by modulating the switching frequency for a given and fixed input voltage  $V_{HV}$ .

Effectively, operation in FFM results in the application of constant volt-seconds to the flyback transformer each switching cycle. Voltage regulation in FFM is achieved by varying the switching frequency in the range from 65 kHz (or 100 kHz) to 27 kHz. For extremely light loads (below approximately 6% full rated power), the converter is controlled using bursts of 27 kHz pulses. This mode is called as skip mode. The FFM, keeping constant peak current and skip mode allows design of the power supplies with increased efficiency under the light loading conditions. Keep in mind that the aforementioned boundaries of steady-state operation are approximate because they are subject to converter design parameters.

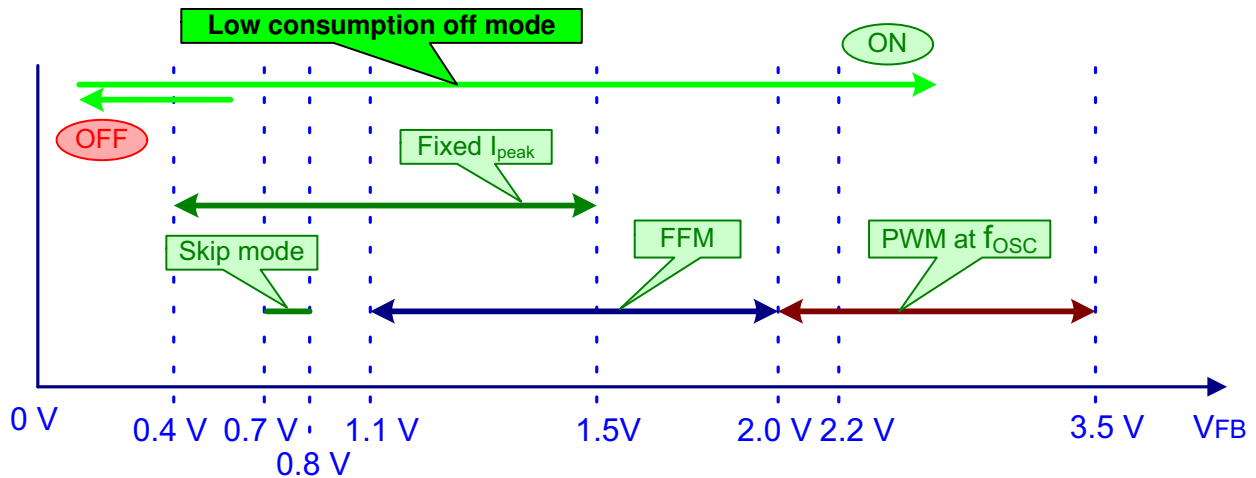


Figure 45. Mode Control with FB pin voltage

There was implemented the low consumption off mode allowing to reach extremely low no load input power. This mode is controlled by the FB pin and allows the remote control (or secondary side control) of the power supply shut-down. Most of the device internal circuitry is unbiased in the low consumption off mode. Only the FB pin control circuitry and X2 cap discharging circuitry is operating in the low consumption off mode. If the voltage at feedback pin

decreases below the 0.4 V the controller will enter the low consumption off mode. The controller can start if the FB pin voltage increases above the 2.2 V level.

See the detailed status diagrams for the both versions fully latched A and the autorecovery B on the following figures. The basic status of the device after wake-up by the  $V_{CC}$  is the off mode and mode is used for the overheating protection mode if the thermal shutdown protection is activated.



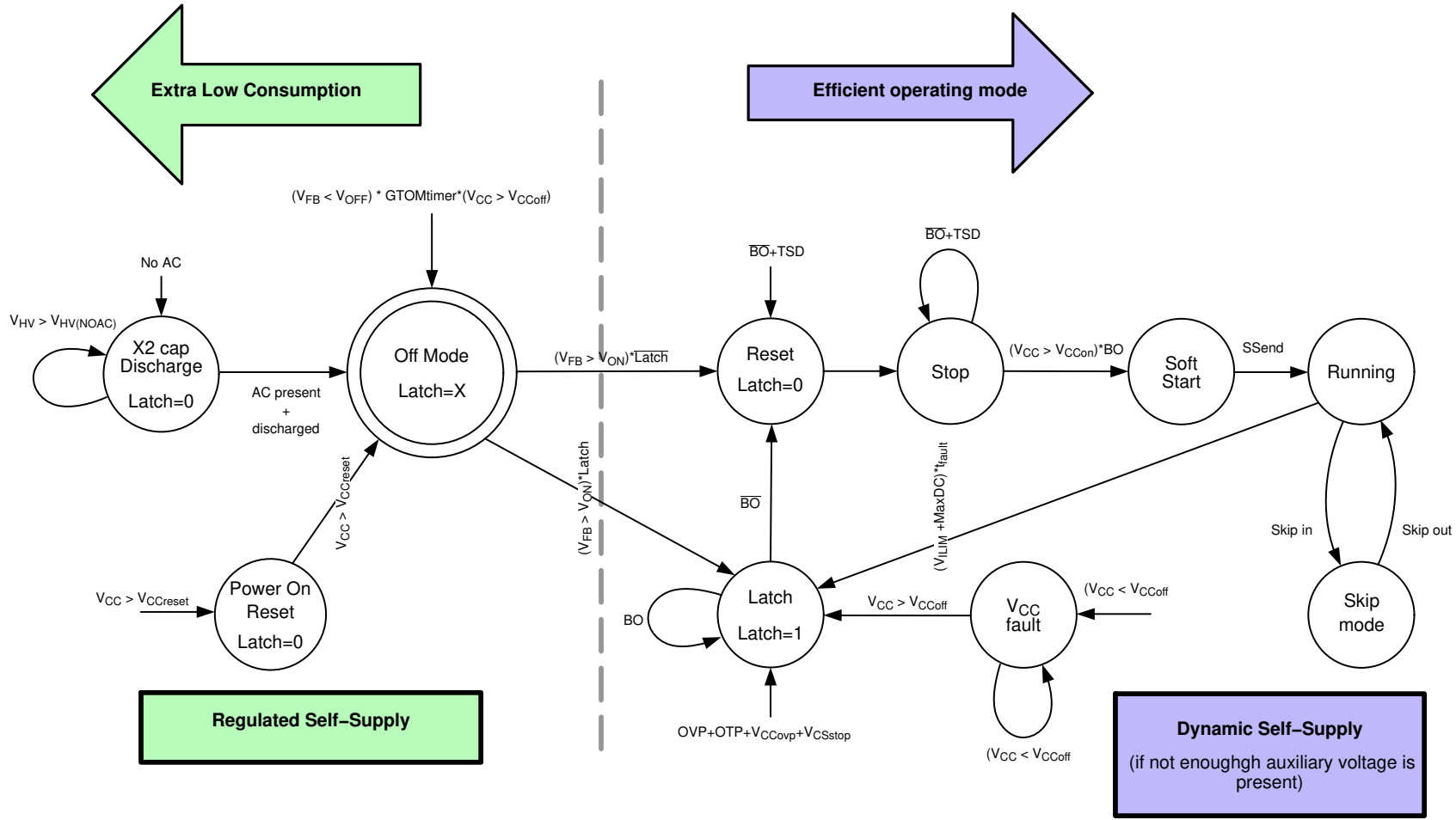


Figure 46. Operating Status Diagram for the Fully Latched Version A of the Device

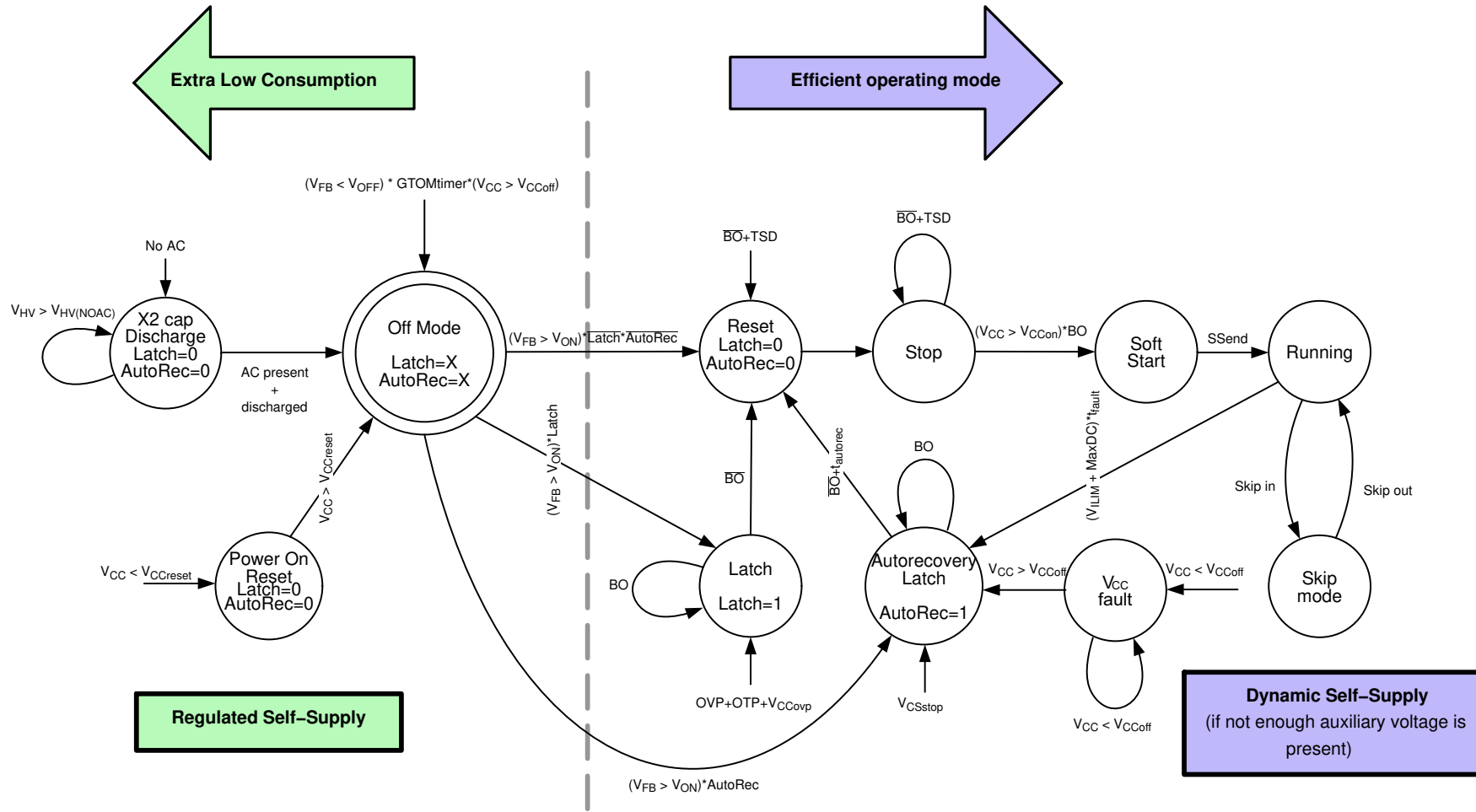


Figure 47. Operating Status Diagram for the Autorecovery Version B of the Device

The information about the fault (permanent Latch or Autorecovery) is kept during the low consumption off mode due the safety reason. The reason is not to allow unlatch the device by the remote control being in off mode.

**Start-up of the Controller**

At start-up, the current source turns on when the voltage on the HV pin is higher than  $V_{HV(min)}$ , and turns off when  $V_{CC}$  reaches  $V_{CC(on)}$ , then turns on again when  $V_{CC}$  reaches  $V_{CC(min)}$ , until the input voltage is high enough to ensure a proper start-up, i.e. when  $V_{HV}$  reaches  $V_{HV(start)}$ . The controller actually starts the next time  $V_{CC}$  reaches  $V_{CC(on)}$ . The controller then delivers pulses, starting with a soft-start period  $t_{SSTART}$  during which the peak current linearly increases before the current-mode control takes over.

Even though the Dynamic Self-Supply is able to maintain the  $V_{CC}$  voltage between  $V_{CC(on)}$  and  $V_{CC(min)}$  by turning the HV start-up current source on and off, it can only be used in light load condition, otherwise the power dissipation on the die would be too much. As a result, an auxiliary voltage source is needed to supply  $V_{CC}$  during normal operation.

The Dynamic Self-Supply is useful to keep the controller alive when no switching pulses are delivered, e.g. in brown-out condition, or to prevent the controller from stopping during load transients when the  $V_{CC}$  might drop. The NCP1246 accepts a supply voltage as high as 28 V, with an overvoltage threshold  $V_{CC(ovp)}$  that latches the controller off.

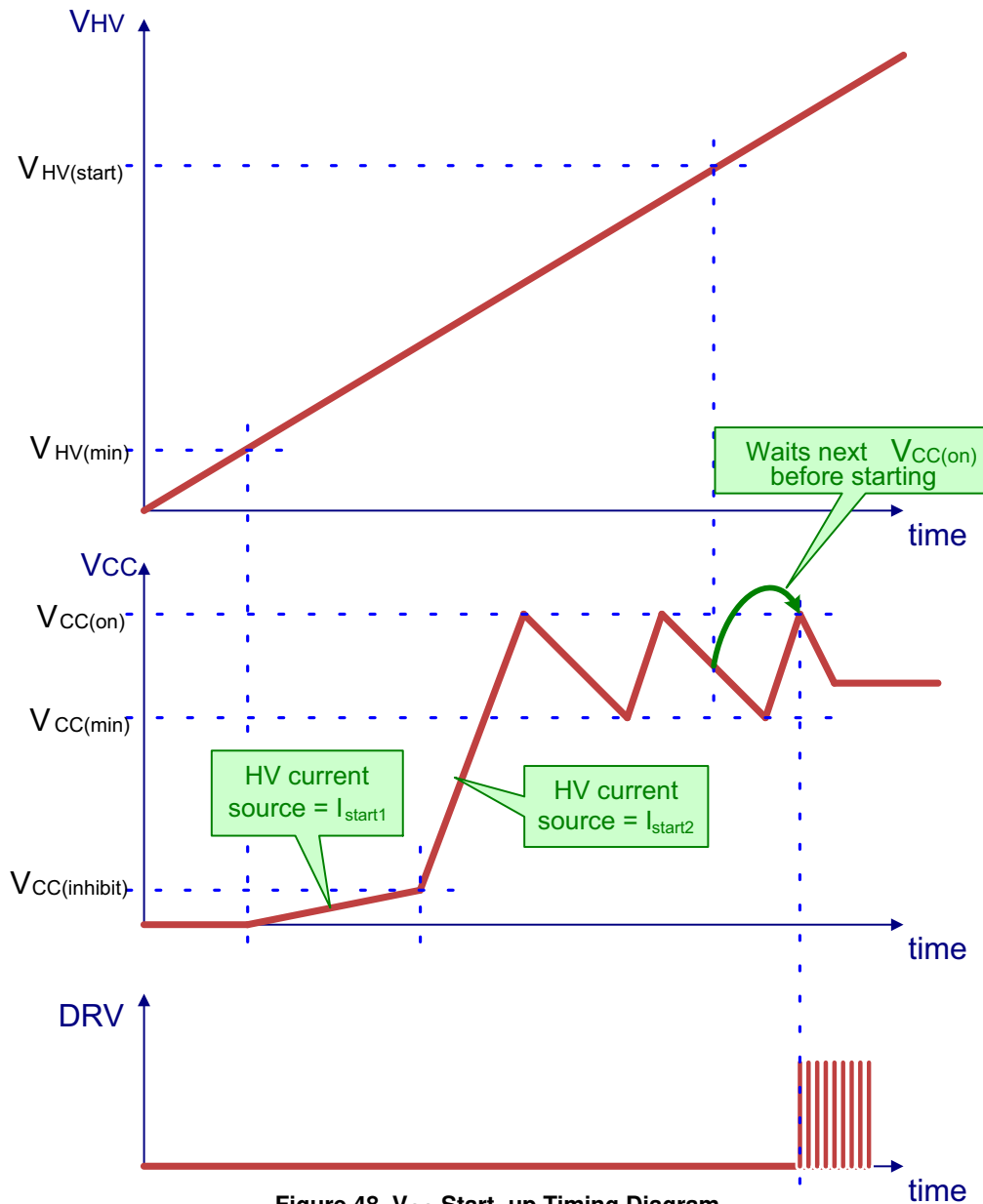


Figure 48.  $V_{CC}$  Start-up Timing Diagram

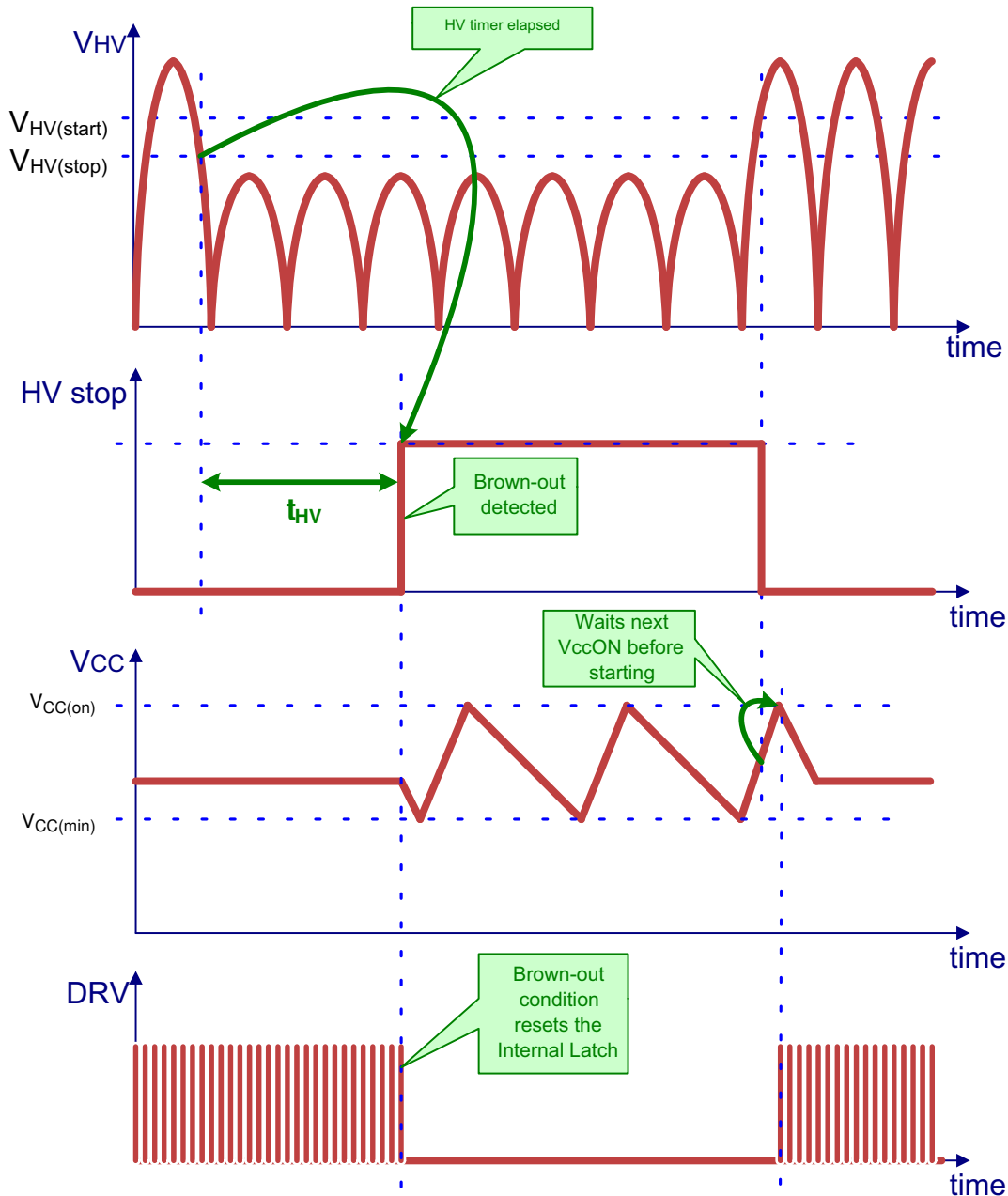
For safety reasons, the start-up current is lowered when  $V_{CC}$  is below  $V_{CC(inhibit)}$ , to reduce the power dissipation in case the  $V_{CC}$  pin is shorted to GND (in case of  $V_{CC}$  capacitor failure, or external pull-down on  $V_{CC}$  to disable the controller). There is only one condition for which the current source doesn't turn on when  $V_{CC}$  reaches  $V_{CC(inhibit)}$ : the voltage on HV pin is too low (below  $V_{HV(min)}$ ).

**HV Sensing of Rectified AC Voltage**

The NCP1246 features on its HV pin a true ac line monitoring circuitry. It includes a minimum start-up

threshold and an autorecovery brown-out protection; both of them independent of the ripple on the input voltage. It is allowed only to work with an unfiltered, rectified ac input to ensure the X2 capacitor discharge function as well, which is described in following. The brown-out protection thresholds are fixed, but they are designed to fit most of the standard ac-dc conversion applications.

When the input voltage goes below  $V_{HV(stop)}$ , a brown-out condition is detected, and the controller stops. The HV current source maintains  $V_{CC}$  at  $V_{CC(min)}$  level until the input voltage is back above  $V_{HV(start)}$ .



**Figure 49. Ac Line Drop-out Timing Diagram**

When  $V_{HV}$  crosses the  $V_{HV(start)}$  threshold, the controller can start immediately. When it crosses  $V_{HV(stop)}$ , it triggers

a timer of duration  $t_{HV}$ , this ensures that the controller doesn't stop in case of line cycle drop-out.

### X2 Cap Discharge Feature

The X2 capacitor discharging feature is offered by usage of the NCP1246. This feature save approx. 16 mW – 25 mW input power depending on the EMI filter X2 capacitors volume and it saves the external components count as well. The discharge feature is ensured via the start-up current source with a dedicated control circuitry for this function. The X2 capacitors are being discharged by current defined as  $I_{start2}$  when this need is detected.

There is used a dedicated structure called ac line unplug detector inside the X2 capacitor discharge control circuitry. See the Figure 50 for the block diagram for this structure and Figures 51, 52, 53 and 54 for the timing diagrams. The basic idea of ac line unplug detector lies in comparison of the direct sample of the high voltage obtained via the high voltage sensing structure with the delayed sample of the high voltage. The delayed signal is created by the sample & hold structure.

The comparator used for the comparison of these signals is without hysteresis inside. The resolution between the slopes of the ac signal and dc signal is defined by the sampling time  $T_{SAMPLE}$  and additional internal offset  $N_{OS}$ . These parameters ensure the noise immunity as well. The additional offset is added to the picture of the sampled HV signal and its analog sum is stored in the  $C_1$  storage capacitor. If the voltage level of the HV sensing structure output crosses this level the comparator CMP output signal resets the detection timer and no dc signal is detected. The additional offset  $N_{OS}$  can be measured as the  $V_{HV(hyst)}$  on the HV pin. If the comparator output produces pulses it means that the slope of input signal is higher than set resolution level and the slope is positive. If the comparator output produces the low level it means that the slope of input signal is lower than set resolution level or the slope is negative. There is used the detection timer which is reset by any edge of the comparator output. It means if no edge comes before the timer elapses there is present only dc signal or signal with the small ac ripple at the HV pin. This type of the ac detector detects only the positive slope, which fulfils the requirements for the ac line presence detection.

In case of the dc signal presence on the high voltage input, the direct sample of the high voltage obtained via the high voltage sensing structure and the delayed sample of the high voltage are equivalent and the comparator produces the low level signal during the presence of this signal. No edges are present at the output of the comparator, that's why the detection timer is not reset and dc detect signal appears.

The minimum detectable slope by this ac detector is given by the ration between the maximum hysteresis observed at HV pin  $V_{HV(hyst),max}$  and the sampling time:

$$S_{min} = \frac{V_{HV(hyst),max}}{T_{sample}} \quad (\text{eq. 1})$$

Than it can be derived the relationship between the minimum detectable slope and the amplitude and frequency of the sinusoidal input voltage:

$$\begin{aligned} V_{max} &= \frac{V_{HV(hyst),max}}{2 \cdot \pi \cdot f \cdot T_{sample}} = \frac{5}{2 \cdot \pi \cdot 35 \cdot 1 \cdot 10^{-3}} \quad (\text{eq. 2}) \\ &= 22.7 \text{ V} \end{aligned}$$

The minimum detectable AC RMS voltage is 16 V at frequency 35 Hz, if the maximum hysteresis is 5 V and sampling time is 1 ms.

The X2 capacitor discharge feature is available in any controller operation mode to ensure this safety feature. The detection timer is reused for the time limiting of the discharge phase, to protect the device against overheating. The discharging process is cyclic and continues until the ac line is detected again or the voltage across the X2 capacitor is lower than  $V_{HV(min)}$ . This feature ensures to discharge quite big X2 capacitors used in the input line filter to the safe level. **It is important to note that it is not allowed to connect HV pin to any dc voltage due this feature. e.g. directly to bulk capacitor.**

During the HV sensing or X2 cap discharging the  $V_{CC}$  net is kept above the  $V_{CC(off)}$  voltage by the Self-Supply in any mode of device operation to supply the control circuitry. During the discharge sequence is not allowed to start-up the device.

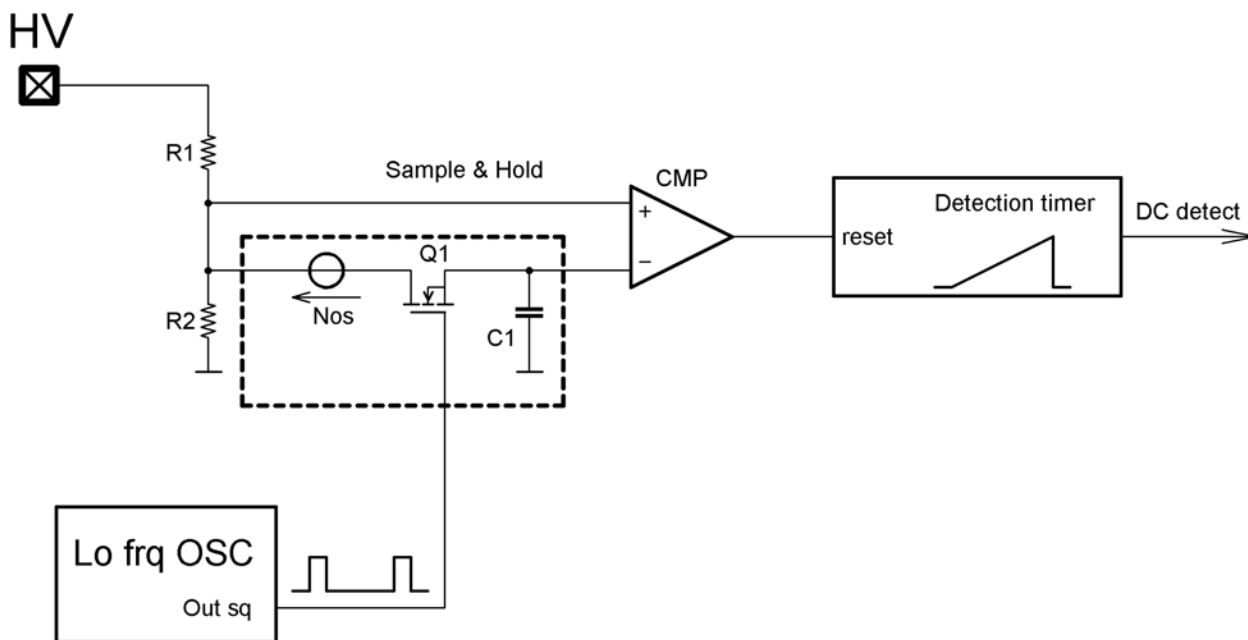


Figure 50. The ac Line Unplug Detector Structure Used for X2 Capacitor Discharge System

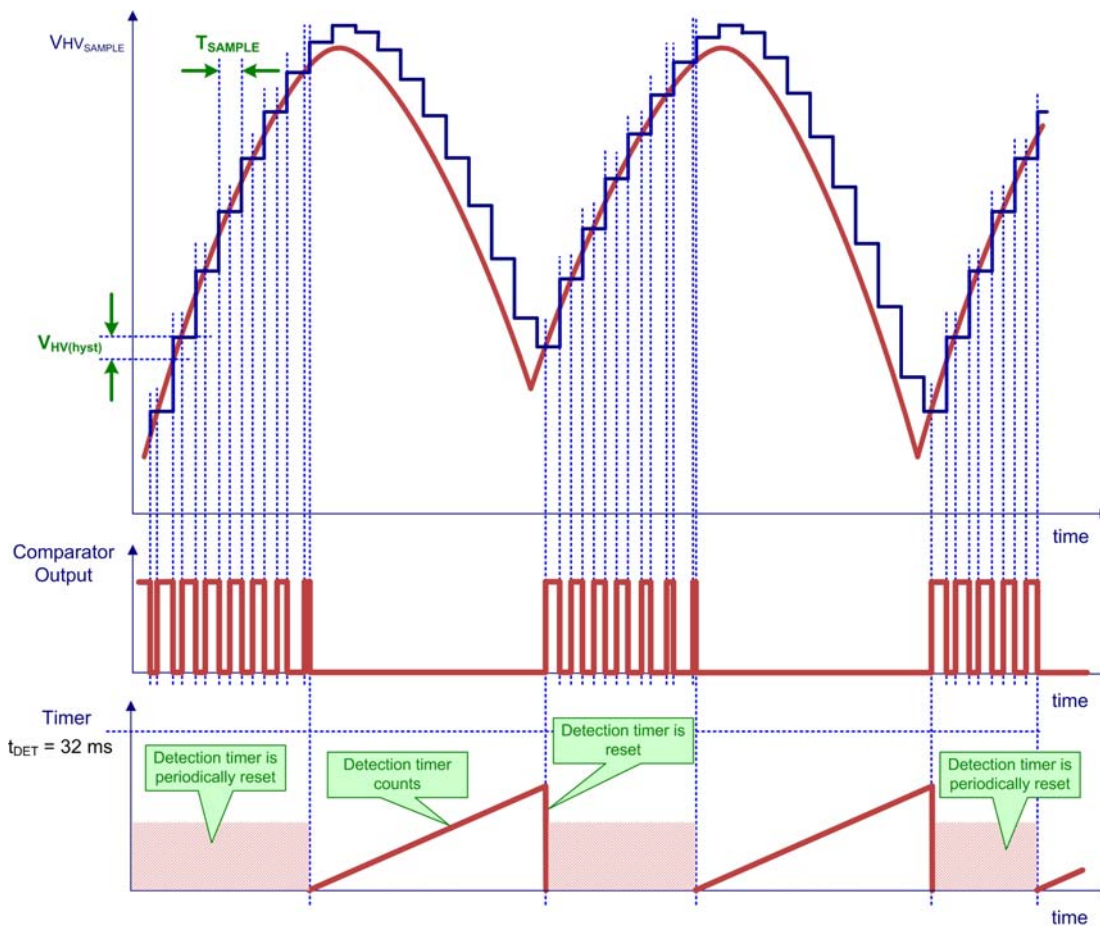


Figure 51. The ac Line Unplug Detector Timing Diagram

# NCP1246

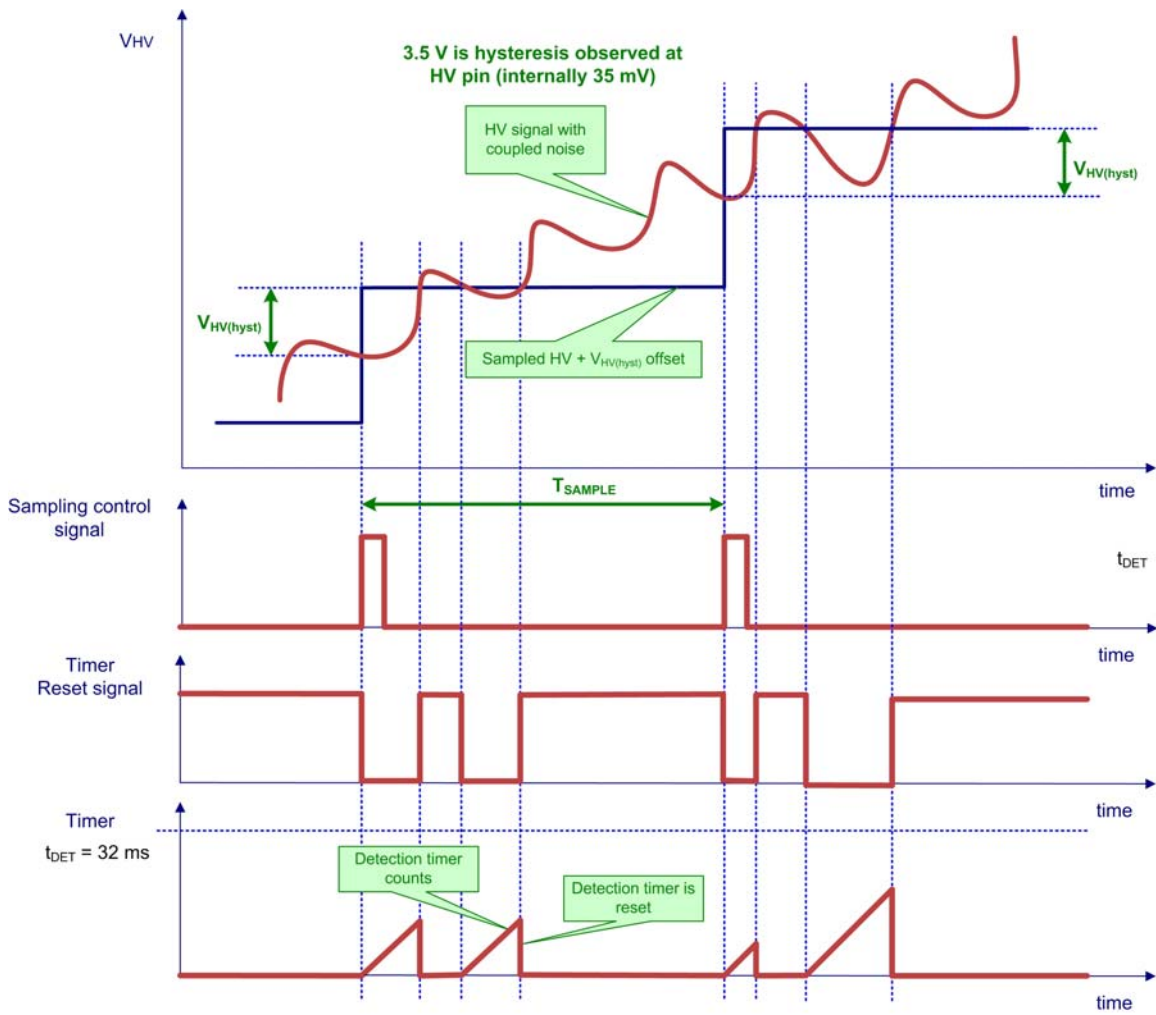


Figure 52. The ac Line Unplug Detector Timing Diagram Detail with Noise Effects

# NCP1246

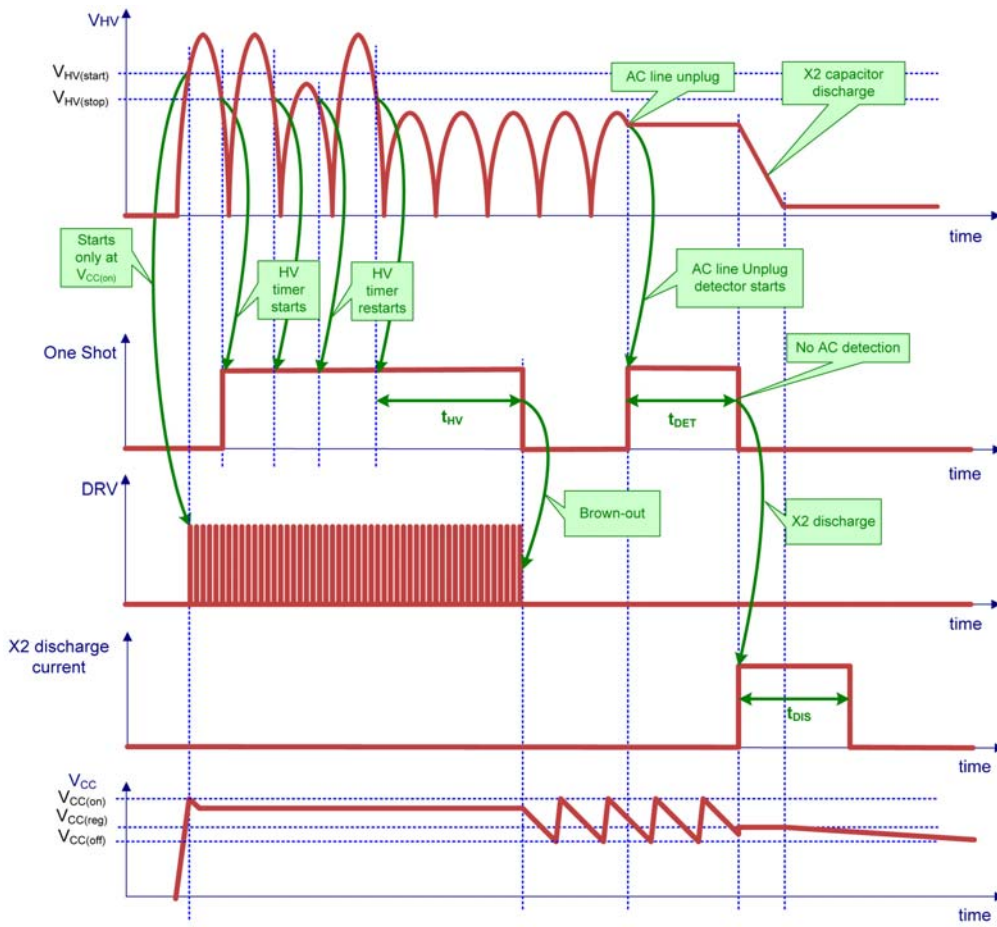


Figure 53. HV Pin ac Input Timing Diagram with X2 Capacitor Discharge Sequence When the Application is Unplugged Under Extremely Low Line Condition



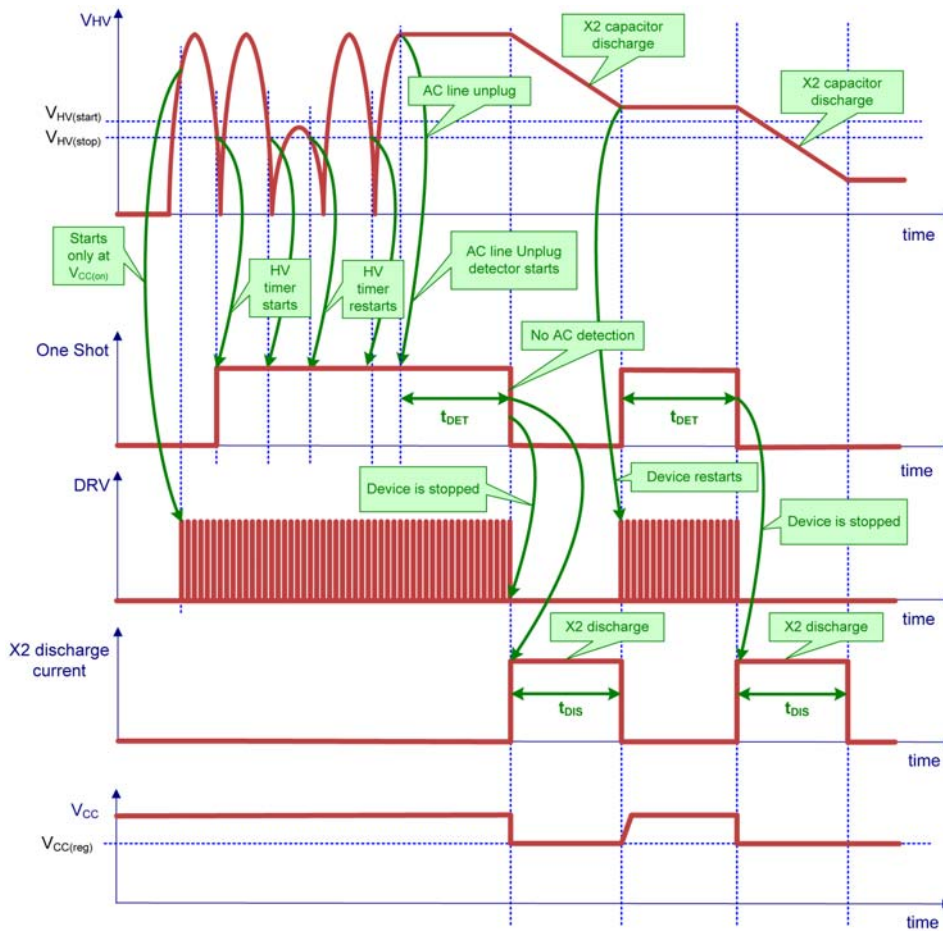


Figure 54. HV Pin ac Input Timing Diagram with X2 Capacitor Discharge Sequence When the Application is Unplugged Under High Line Condition

**The Low Consumption Off Mode**

There was implemented the low consumption off mode allowing to reach extremely low no load input power as described in previous chapters. If the voltage at feedback pin decreases below the 0.4 V the controller enters the off mode. The internal  $V_{CC}$  is turned-off, the IC consumes extremely low  $V_{CC}$  current and only the voltage at external  $V_{CC}$  capacitor is maintained by the Self-Supply circuit. The Self-Supply circuit keeps the  $V_{CC}$  voltage at the  $V_{CC(reg)}$  level. The supply for the FB pin watch dog circuitry and FB pin bias is provided via the low consumption current sources from the external  $V_{CC}$  capacitor. The controller can only start, if the FB pin voltage increases above the 2.2 V level. See Figure 55 for timing diagrams.

Only the X2 cap discharge and Self-Supply features is enabled in the low consumption off mode. The X2 cap discharging feature is enable due the safety reasons and the Self-Supply is enabled to keep the  $V_{CC}$  supply, but only very low  $V_{CC}$  consumption appears in this mode. Any other features are disabled in this mode.

The information about the latch status of the device is kept in the low consumption off mode and this mode is used for the TSD protection as well. The protection timer GoToOffMode  $t_{GTOM}$  is used to protect the application against the false activation of the low consumption off mode by the fast drop outs of the FB pin voltage below the 0.4 V level. E.g. in case when is present high FB pin voltage ripple during the skip mode.

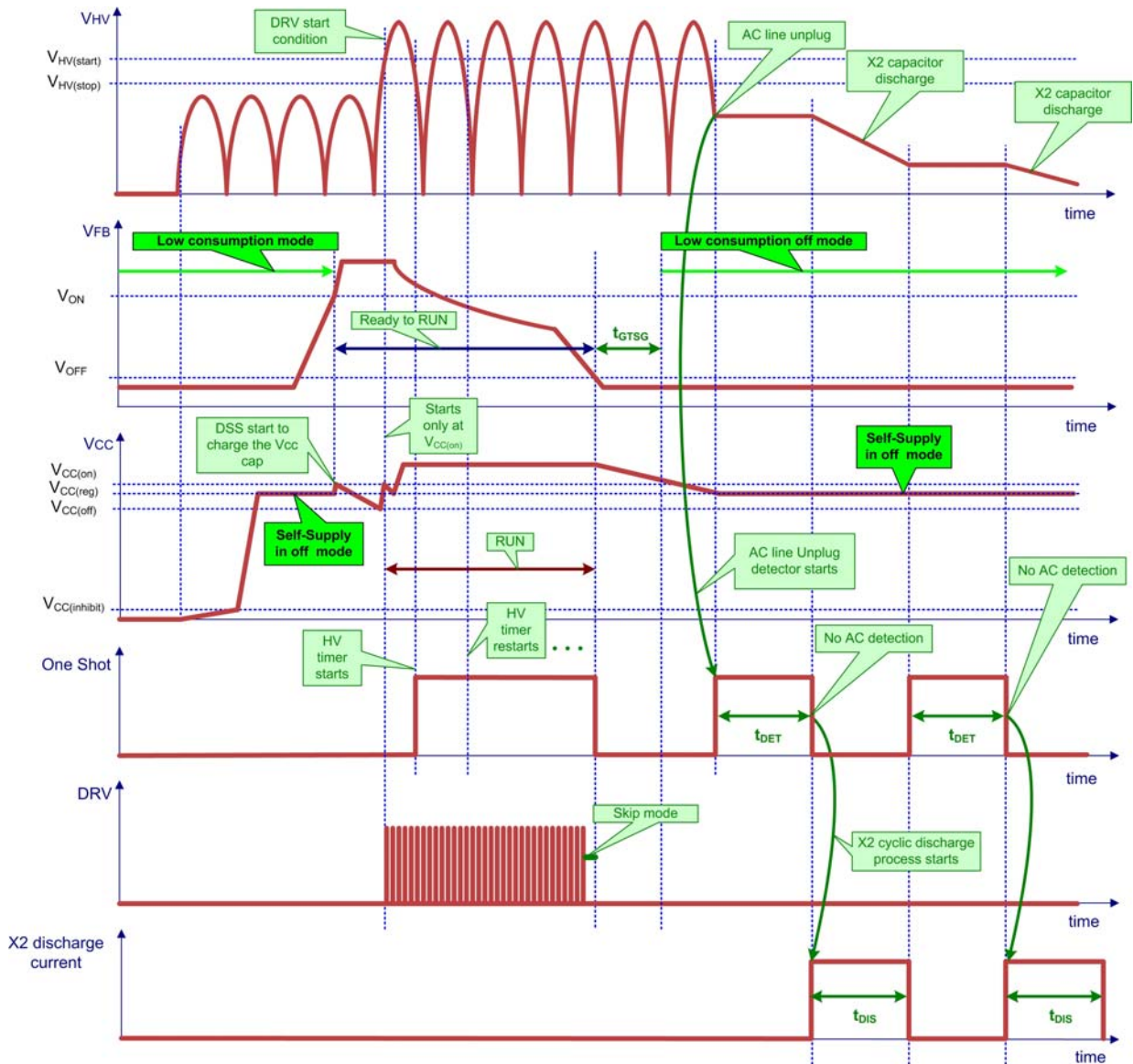


Figure 55. Start-up, Shutdown and AC Line Unplug Time Diagram

**Oscillator with Maximum On Time and Frequency Jittering**

The NCP1246 includes an oscillator that sets the switching frequency 65 kHz or 100 kHz depending on the version. The maximum on time is 12.3  $\mu$ s (for 65 kHz version) or 8  $\mu$ s (for 100 kHz version) with an accuracy of  $\pm 7\%$ . The maximum on time corresponds to maximum duty cycle of the DRV pin is 80% at full switching frequency. In order to improve the EMI signature, the switching frequency jitters  $\pm 6\%$  around its nominal value, with a triangle-wave shape and at a frequency of 125 Hz. This frequency jittering is active even when the frequency is decreased to improve the efficiency in light load condition.

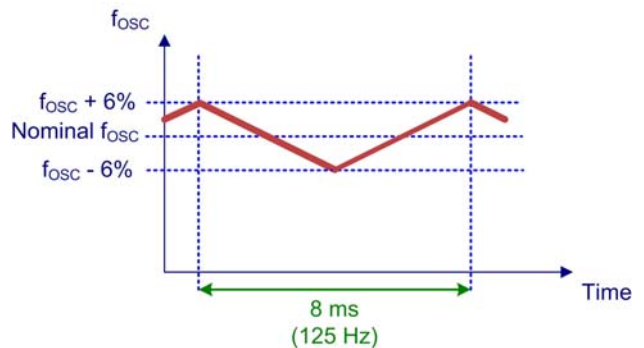


Figure 56. Frequency Modulation of the Maximum Switching Frequency