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NCP1249C, NCP1249D

High-Voltage Current-Mode PWM Controller Featuring Peak Power Excursion and Self-Relaxing Off Mode

The NCP1249 is a highly integrated high-voltage PWM controller capable of delivering a rugged and high performance offline power supply with extremely low no-load consumption. With a supply range up to 30 V, the controller hosts a jittered 65 kHz switching circuitry operated in peak current mode control. When the power on the secondary side starts to decrease, the controller automatically folds back its switching frequency down to a minimum level of 26 kHz. As the power further goes down, the part enters skip cycle while freezing the peak current setpoint.

To help build rugged converters, the controller features several key protective features: a internal brown-out, a non-dissipative Over Power Protection for a constant maximum output current regardless of the input voltage and two latched over voltage protection inputs – either through a dedicated pin or via the VCC input.

The controller architecture is arranged to authorize a transient peak power excursion when the peak current hits the limit. At this point, the switching frequency is increased from 65 kHz to 130 kHz until the peak requirement disappears. The timer duration is then modulated as the converter crosses a peak power excursion mode (long) or undergoes a short circuit (short).

Features

- High-Voltage Current Source for Lossless Start-up Sequence
- Automatic and Lossless X2 Capacitors Discharge Function
- 65 kHz Fixed-Frequency Current-Mode Control Operation with 130 kHz Excursion
- Internal and Adjustable Over Power Protection (OPP) Circuit
- Internal Brown-Out Protection Circuit
- Frequency Foldback Down to 26 kHz and Skip-Cycle in Light Load Conditions
- Adjustable Ramp Compensation
- Internally Fixed 4 ms Soft-Start
- Adjustable Timer-Based Auto-Recovery Overload/Short-Circuit Protection
- 100% to 25% Timer Reduction from Overload to Short-Circuit Fault
- Frequency Jittering in Normal and Frequency Foldback Modes
- Latched OVP Input for Improved Robustness and Latched OVP on VCC
- Up to 30 V VCC Maximum Rating
- +300 mA/ -500 mA Source/Sink Drive Capability
- Extremely Low No-Load Standby Power via Controlled Self-Relaxing Off Mode
- Option for Auto-Recovery or Latched Short-Circuit Protection
- Internal Thermal Shutdown with Hysteresis
- These are Pb-Free Devices

Typical Applications

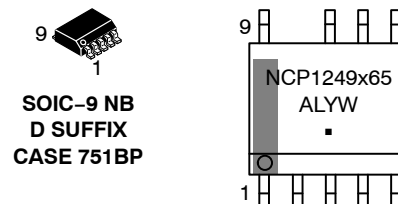
- Converters Requiring Peak-power Capability such as Printers Power Supplies, ac-dc Adapters for Game Stations



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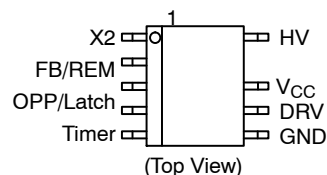
<http://onsemi.com>

MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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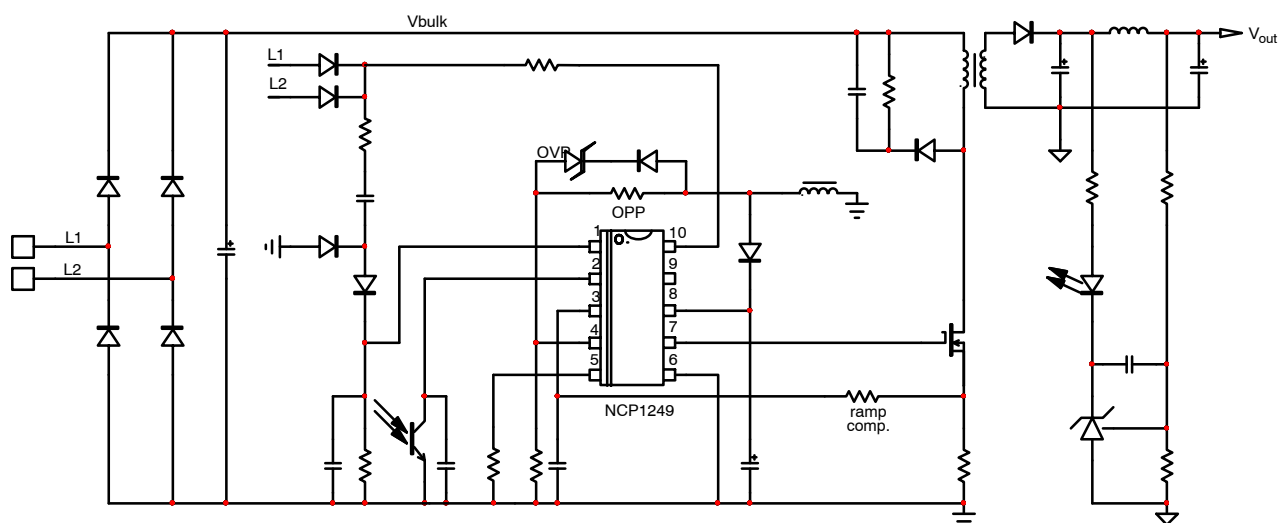


Figure 1. Typical Application Example

Table 1. PIN FUNCTIONS

Pin No	Pin Name	Function	Pin Description
1	X2	X2-capacitors discharge	When the voltage on this pin disappears, the controller ensures the X2-capacitors discharge.
2	FB/REM	Combined feedback and remote pin	Connecting an opto-coupler to this pin allows regulation. The opto-coupler can pull the feedback pin down and brings the controller in a deep sleep mode.
3	CS	Current sense + ramp compensation	This pin monitors the primary peak current but also offers a means to introduce slope compensation.
4	OPP/LATCH	Adjust the Over Power Protection Latches off the part	A resistive divider from the auxiliary winding to this pin sets the OPP compensation level. When brought above 3 V, the part is fully latched off.
5	TIMER	Fault timer adjustment	A resistor to ground adjusts the timer duration in fault condition.
6	GND	-	The controller ground.
7	DRV	Driver output	The driver's output to an external MOSFET gate.
8	VCC	Supplies the controller	This pin is connected to an external auxiliary voltage and supplies the controller. When above a certain level, the part fully latches off.
9	NC	-	Increases insulation distance between high and low voltage pins.
10	HV	High-voltage input	This pin provides a charging current during start-up and auto-recovery faults but also a means to efficiently discharge the input X2 capacitors.

Table 2. OPTIONS AND ORDERING INFORMATION

Device	Overload Protection	Switching Frequency	Peak Frequency	Package	Shipping†
NCP1249CD65R2G	Latched	65 kHz	130 kHz	SOIC-9 (Pb-Free)	2500 / Tape & Reel
NCP1249DD65R2G	Autorecovery	65 kHz	130 kHz	SOIC-9 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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Table 3. MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
V _{CC}	Power Supply voltage, V _{CC} pin, continuous voltage	-0.3 to 30	V
V _{HV}	High Voltage (HV) Pin (pin 10)	-0.3 to 500	V
V _{pin_x}	Maximum voltage on low power pins (X2, CS, OPP, Timer)	-0.3 to 10	V
V _{FB/REM}	Maximum voltage on FB/REM pin	-0.3 to 5	V
V _{DRV}	Maximum voltage on drive pin	-0.3 to V _{CC} + 0.3	V
I _{OPP}	Maximum injected current into the OPP pin	-2	mA
R _{θJ-A}	Thermal Resistance Junction-to-Air	211	°C/W
T _{J,max}	Maximum Junction Temperature	150	°C
	Storage Temperature Range	-60 to +150	°C
	ESD Capability, HBM model (All pins except HV) per JEDEC standard JESD22, Method A114E	2	kV
	ESD Capability, Machine Model per JEDEC standard JESD22, Method A115A	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.

Table 4. ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = -40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
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HV STARTUP CURRENT SOURCE

V _{HV_min}	Minimum voltage for current source operation (V _{CC} = 4 V)	10	-	30	60	V
I _{start1}	Current flowing out of V _{CC} pin (V _{CC} = 0 V)	8, 10	0.2	0.7	1	mA
I _{start2}	Current flowing out of V _{CC} pin (V _{CC} = V _{CC_ON} - 0.5 V)	8, 10	6	10	16	mA
V _{CC_inhibit}	V _{CC} level for I _{start1} to I _{start2} transition	8	0.5	1	1.25	V
I _{start_off}	Off-state leakage current (V _{HV} = 500 V, V _{CC} = 15 V)	10	-	15	-	μA
I _{HV_off-mode_1}	HV pin leakage current when off-mode is active (V _{HV} = 141 V)	10	-	-	15	μA
I _{HV_off-mode_2}	HV pin leakage current when off-mode is active (V _{HV} = 325 V)	10	-	-	19	μA
V _{HV_min_off-mode}	Minimum voltage on HV pin during off-mode (V _{FB} = 0 V, V _{CC} = 0 V)	10	-	-	10	V

SUPPLY SECTION

V _{CC_ON}	V _{CC} increasing level at which driving pulses are authorized	8	16	18	20	V
V _{CC_OFF}	V _{CC} decreasing level at which driving pulses are stopped	8	9.5	10	11	V
V _{CC_HYST}	Hysteresis V _{CC_ON} - V _{CC_OFF}	8	6	-	-	V
V _{CC_bias}	V _{CC} level during a fault	8	4.7	5.5	6.5	V
I _{CC1}	Internal IC consumption with I _{FB} = 75 μA, f _{SW} = 65 kHz and C _L = 0	8	-	1.6	2.6	mA
I _{CC2}	Internal IC consumption with I _{FB} = 75 μA, f _{SW} = 65 kHz and C _L = 1 nF	8	-	2.3	3.4	mA
I _{CC3}	Internal IC consumption with I _{FB} = 75 μA, f _{SW} = 130 kHz and C _L = 0	8	-	1.9	2.9	mA
I _{CC4}	Internal IC consumption with I _{FB} = 75 μA, f _{SW} = 130 kHz and C _L = 1 nF	8	-	3.3	4.4	mA
I _{CC_skip}	Internal IC consumption while in skip mode	8	660	960	1360	μA
I _{CC_latch}	Internal IC consumption during Latch-off mode	8	-	350	520	μA

BROWN-OUT

V _{BO_on}	Brown-Out turn-on threshold (V _{HV} going up)	10	92	101	110	V
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2. Guaranteed by design
3. See characterization table for linearity over negative bias voltage – we recommend keeping the level on pin 5 below -300 mV.
4. A 1 MΩ resistor is connected from pin 4 to the ground for the measurement.

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Table 4. ELECTRICAL CHARACTERISTICS (For typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, Max $T_J = 150^\circ\text{C}$, $V_{CC} = 12\text{ V}$ unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
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BROWN-OUT

V_{BO_off}	Brown-Out turn-off threshold (V_{HV} going down)	10	84	93	102	V
BO_Timer	Timer duration for line cycle drop-out	10	40	-	100	ms

X2 DISCHARGE CIRCUITRY

V_{th_X2}	X2 timer disable switch threshold voltage	1	1	1.5	2	V
$V_{th_X2_hyst}$	Hysteresis on the X2 pin	1	-	100	-	mV
V_{X2_clamp}	X2 input clamp voltage	1	-	4	-	V
X2_Timer	X2 timer duration	1	70	-	140	ms
I_{X2_leak}	X2 input leakage current ($V_{X2} = 2.5\text{ V}$)	1	-	-	0.3	μA
I_{X2_dis}	Maximum discharge switch current ($V_{CC} = 10\text{ V}$)	10	6	10	13	mA

DRIVE OUTPUT

T_r	Output voltage rise-time @ $C_L = 1\text{ nF}$, 10–90% of output signal	7	-	40	80	ns
T_f	Output voltage fall-time @ $C_L = 1\text{ nF}$, 10–90% of output signal	7	-	30	70	ns
R_{OH}	Source resistance	7	-	13	-	Ω
R_{OL}	Sink resistance	7	-	6	-	Ω
I_{source}	Peak source current, $V_{GS} = 0\text{ V}$ (Note 2)	7		300		mA
I_{sink}	Peak sink current, $V_{GS} = 12\text{ V}$ (Note 2)	7		500		mA
V_{DRV_low}	DRV pin level at V_{CC} close to V_{CC_OFF} with a 33 k Ω resistor to GND	7	8	-	-	V
V_{DRV_high}	DRV pin level at $V_{CC} = V_{OVP} - 0.2\text{ V}$, DRV unloaded	7	10	12	14	V

CURRENT COMPARATOR

I_{IB}	Input Bias Current @ 0.8 V input level on pin 3	3		0.02		μA
V_{limit}	Maximum internal current setpoint – $T_J = 25^\circ\text{C}$ – pin 4 grounded	3	0.744	0.8	0.856	V
V_{limit}	Maximum internal current setpoint – T_J from -40°C to 125°C – pin 4 grounded	3	0.72	0.8	0.88	V
V_{fold_cs}	Default internal voltage set point for frequency foldback trip point $\approx 47\%$ of V_{limit}	3		475		mV
V_{freeze_cs}	Internal peak current setpoint freeze ($\approx 31\%$ of V_{limit})	3		250		mV
T_{DEL}	Propagation delay from current detection to gate off-state	3		100	150	ns
T_{LEB}	Leading Edge Blanking Duration	3		300		ns
T_{SS}	Internal soft-start duration activated upon startup, auto-recovery	-		4		ms
I_{OPP0}	Setpoint decrease for pin 5 biased to -250 mV – (Note 3)	3		31.3		%
I_{OPV}	Voltage setpoint for pin 5 biased to -250 mV – (Note 3) T_J from -40°C to 125°C	3	0.5	0.55	0.62	V
I_{OPPs}	Setpoint decrease for pin 4 grounded	3		0		%

INTERNAL OSCILLATOR

f_{OSC_nom}	Oscillation frequency, $V_{FB} < V_{FBtrans}$, pin 4 grounded	-	57	65	71	kHz
$V_{FBtrans}$	Feedback voltage above which f_{sw} increases	2		3.2		V
f_{OSC_max}	Maximum oscillation frequency for V_{FB} above V_{FBmax}	-	115	130	140	kHz
V_{FBmax}	Feedback voltage above which f_{sw} is constant	2	3.8	4	4.2	V
D_{max}	Maximum duty ratio	-	76	80	84	%

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Table 4. ELECTRICAL CHARACTERISTICS (For typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, Max $T_J = 150^\circ\text{C}$, $V_{CC} = 12\text{ V}$ unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
INTERNAL OSCILLATOR						
f_{jitter}	Frequency jittering in percentage of f_{OSC}	-		± 5		%
f_{swing}	Swing frequency over the whole frequency range	-		240		Hz
FEEDBACK / REMOTE SECTION						
$R_{\text{Up(FB)}}$	Internal pull-up resistor	2		17		k Ω
R_{eq}	Equivalent ac resistor from FB to GND	2	10	15	20	k Ω
I_{ratio}	Pin 2 to current setpoint division ratio	2,3		4		-
$V_{\text{freeze_FB}}$	Feedback voltage below which the peak current is frozen	2		1		V
$V_{\text{REM_off}}$	Feedback voltage below which the part enters into off-mode	2		0.4		V
$V_{\text{REM_on}}$	Feedback voltage above which is the off-mode deactivated	2	1.5	2	2.5	V
I_{FBREM}	Feedback current that lifts the feedback pin upon off-mode exit	2		2.4	4	μA
FREQUENCY FOLDBACK						
$V_{\text{fold_FB}}$	Frequency foldback level on the feedback pin – =47% of maximum peak current	2		1.9		V
f_{trans}	Transition frequency below which skip-cycle occurs	-	22	26	30	kHz
$V_{\text{fold_end}}$	End of frequency foldback feedback level, $f_{\text{sw}} = f_{\text{min}}$	2		1.5		V
V_{skip}	Skip-cycle level voltage on the feedback pin	2		400		mV
Skip hysteresis	Hysteresis on the skip comparator (Note 2)	2		30		mV
INTERNAL SLOPE COMPENSATION						
V_{ramp}	Internal ramp level @ 25°C (Note 4)	3		2.5		V
R_{ramp}	Internal ramp resistance to CS pin	3		20		k Ω
PROTECTIONS						
V_{latch}	Latching level input	4	2.7	3	3.3	V
$T_{\text{latch-blank}}$	Blanking time after drive turn off	4		1		μs
$T_{\text{latch-count}}$	Number of clock cycles before latch confirmation	-		4		-
$T_{\text{latch-del}}$	OVP detection time constant	4		600		ns
V_{OVL}	Feedback voltage at which an overload is considered – OPP pin is grounded	2		3.2		V
V_{SC}	Feedback voltage above which a short-circuit is considered	2	3.9	4.1	4.3	V
Timer ₁	Fault timer duration for a 22 k Ω resistor from pin 5 to ground – overload	5	350	500	650	ms
Timer ₂	Fault timer duration when $V_{\text{FB}} > 4.1\text{ V}$ is Timer ₁ /4 – short-circuit condition	5	88	125	162	ms
Timer _{fault1}	Timer duration when pin 5 is shorted to ground – fault condition	5		50		ms
Timer _{fault2}	Timer duration when pin 5 is open – fault condition	5		1000		ms
V_{OVP}	Latched Over voltage protection on the V_{CC} rail	8	26	27.5	29	V
$T_{\text{OVP_del}}$	Delay before OVP on V_{CC} confirmation	8		20	30	μs
$T_{\text{A-rec_timer}}$	Auto-recovery timer duration	-	1.4	-	-	s
TEMPERATURE SHUTDOWN						
T_{TSD}	Temperature shutdown T_J going up	-		150		$^\circ\text{C}$
$T_{\text{TSD(HYS)}}$	Temperature shutdown hysteresis	-		30		$^\circ\text{C}$

2. Guaranteed by design

3. See characterization table for linearity over negative bias voltage – we recommend keeping the level on pin 5 below -300 mV .

4. A 1 M Ω resistor is connected from pin 4 to the ground for the measurement.

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TYPICAL CHARACTERISTICS

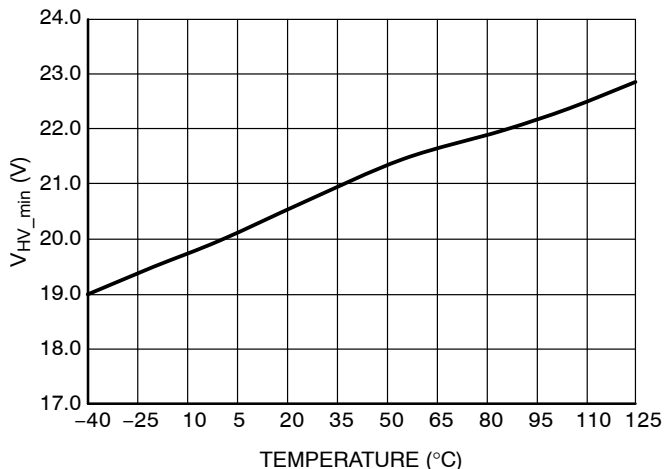


Figure 3. Minimum Current Source Operation, V_{HV_min}

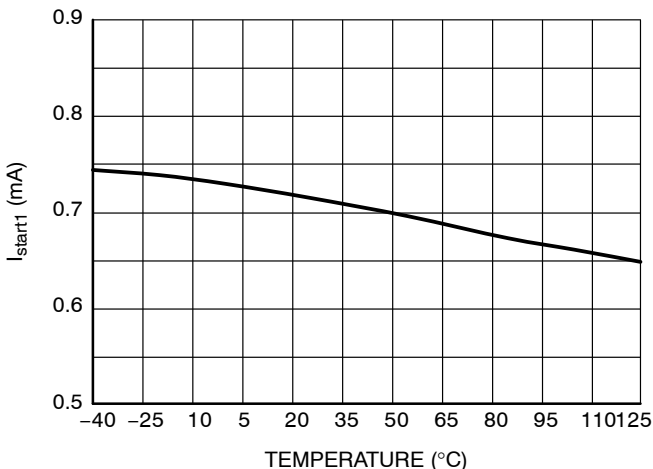


Figure 4. High Voltage Startup Current Flowing Out of V_{CC} Pin, I_{start1}

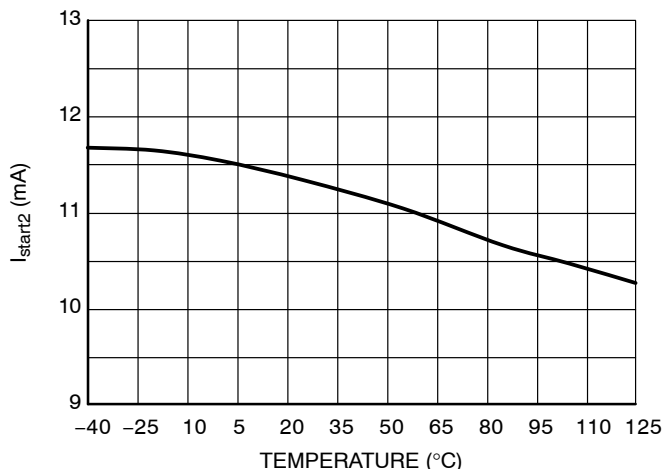


Figure 5. High Voltage Startup Current Flowing Out of V_{CC} Pin, I_{start2}

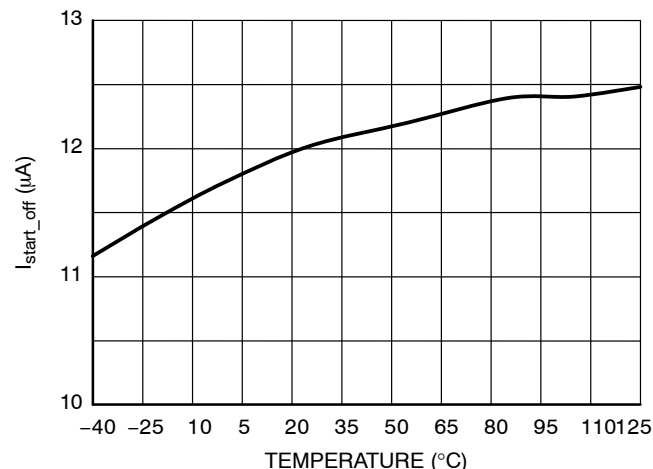


Figure 6. Off-state Leakage Current, I_{start_off}

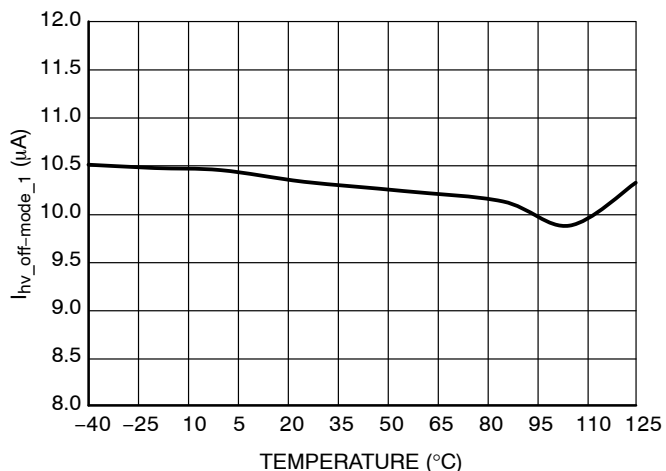


Figure 7. HV Pin Current during Off-mode, $I_{HV_off_mode_1}$

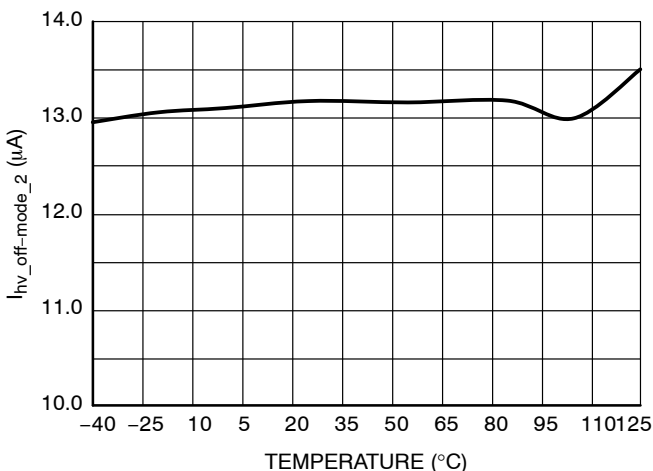


Figure 8. HV Pin Current during Off-mode, $I_{HV_off_mode_2}$

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TYPICAL CHARACTERISTICS

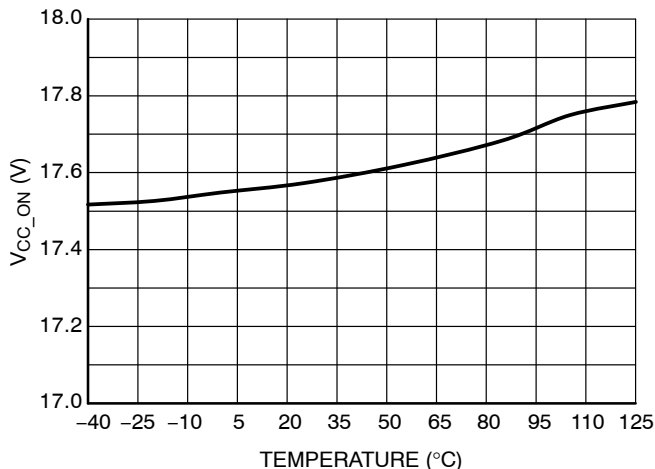


Figure 9. V_{CC} Increasing Level at which Driving Pulses are Authorized, V_{CC_ON}

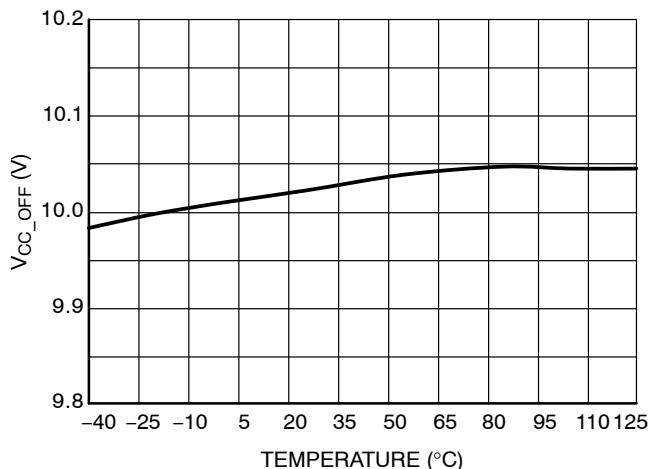


Figure 10. V_{CC} Decreasing Level at which Driving Pulses are Stopped, V_{CC_OFF}

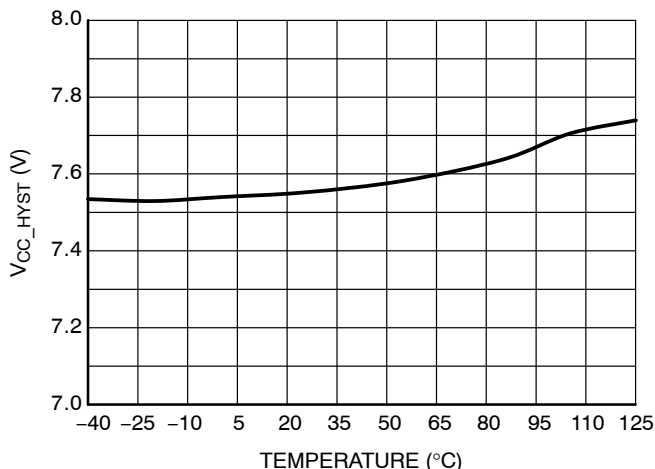


Figure 11. V_{CC} Hysteresis, V_{CC_HYST}

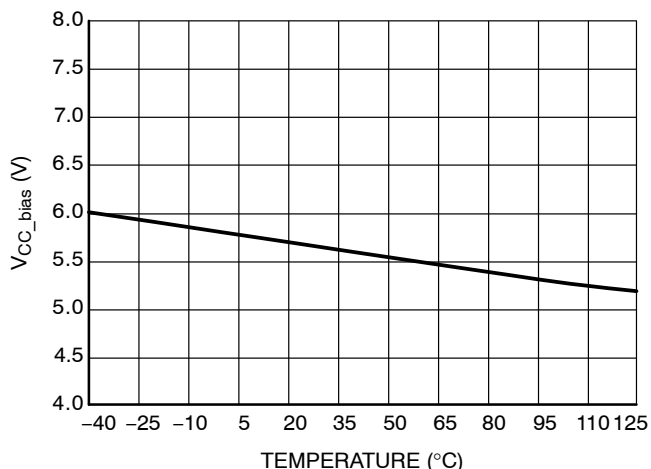


Figure 12. V_{CC} Level at Fault Modes, V_{CC_bias}

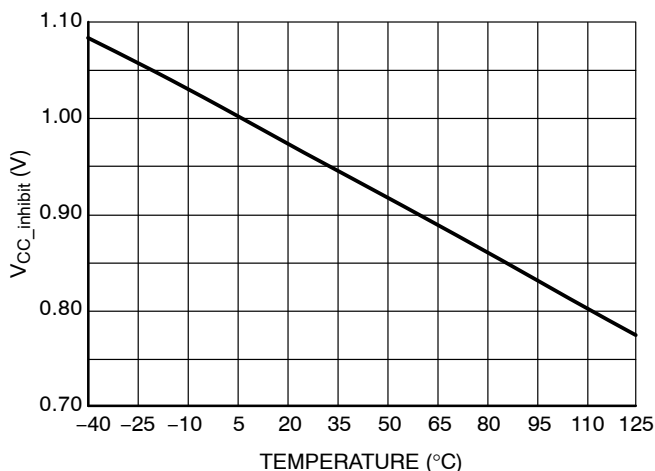


Figure 13. V_{CC} Level for I_{start1} to I_{start2} Transition, V_{CC_inhibit}

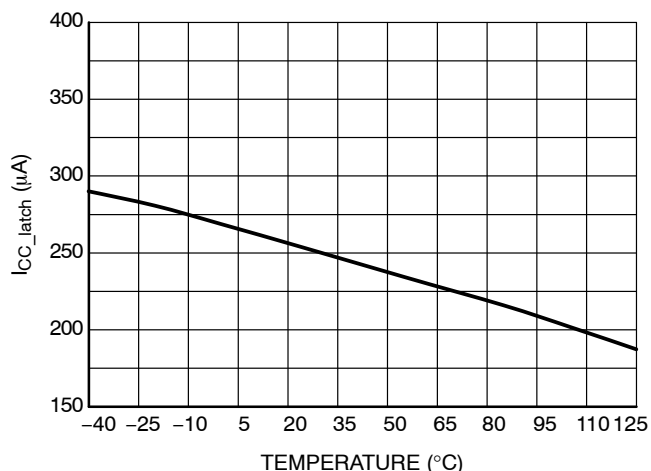


Figure 14. Internal IC Consumption During Latch-off Mode, I_{CC_latch}

TYPICAL CHARACTERISTICS

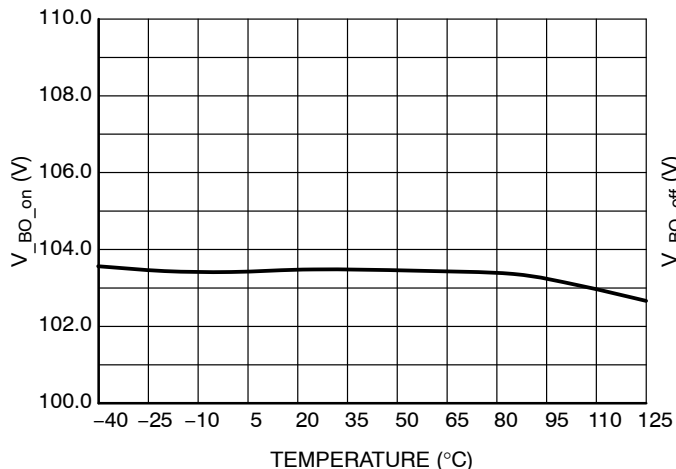


Figure 15. Brown-Out Turn-on Threshold, V_{BO_on}

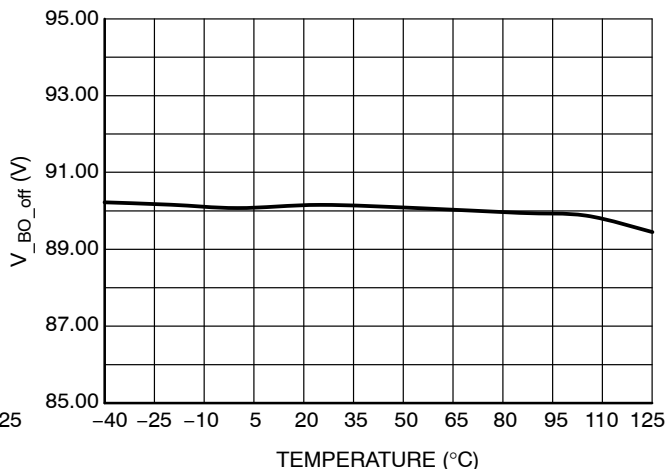


Figure 16. Brown-Out Turn-off Threshold, V_{BO_off}

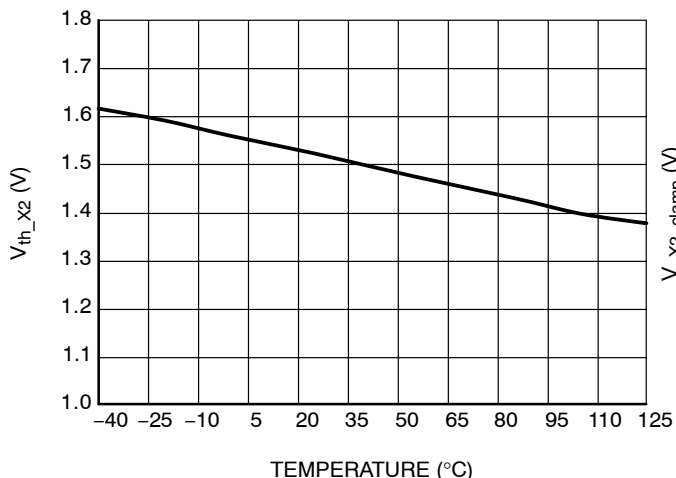


Figure 17. X2 Timer Disable Switch Threshold, V_{th_X2}

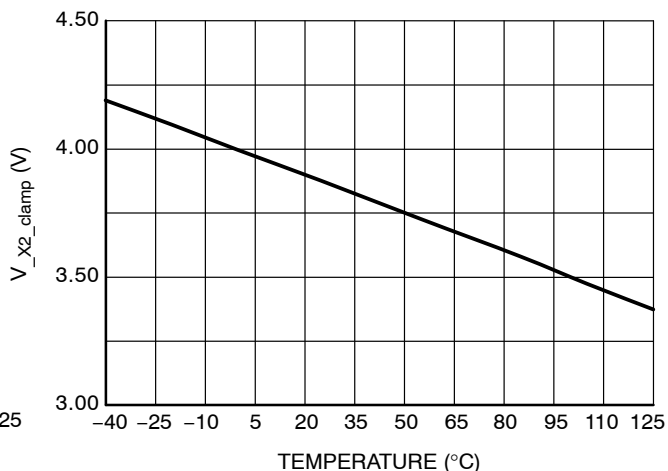


Figure 18. X2 Input Clamp Voltage, V_{X2_clamp}

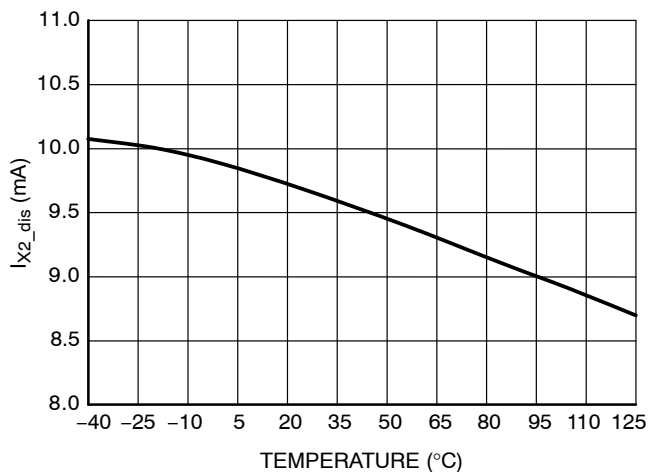


Figure 19. Maximum X2 Cap Discharge Current, I_{X2_dis}

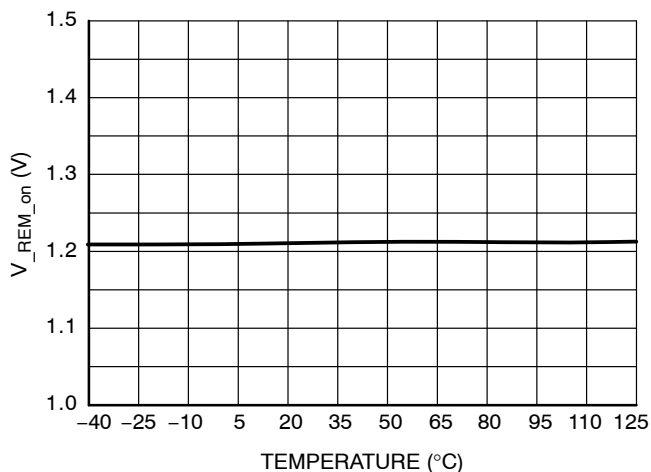


Figure 20. Off-mode Turn-off Threshold, V_{REM_on}

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TYPICAL CHARACTERISTICS

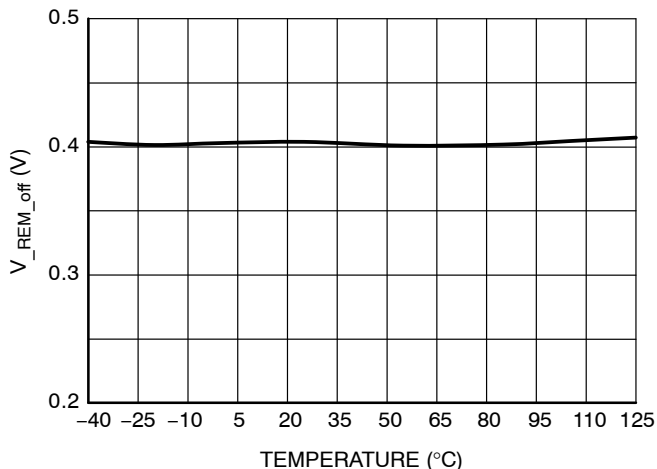


Figure 21. Off-mode Turn-on Threshold, V_{REM_off}

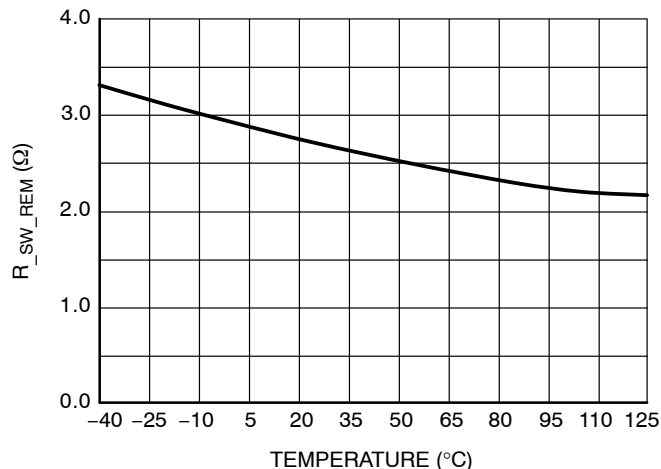


Figure 22. Internal Remote Pull Down Switch Resistance, R_{SW_REM}

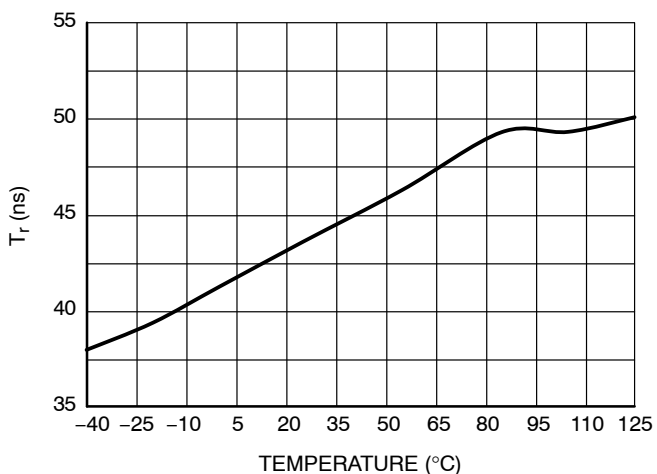


Figure 23. Output Voltage Rise-time, T_r

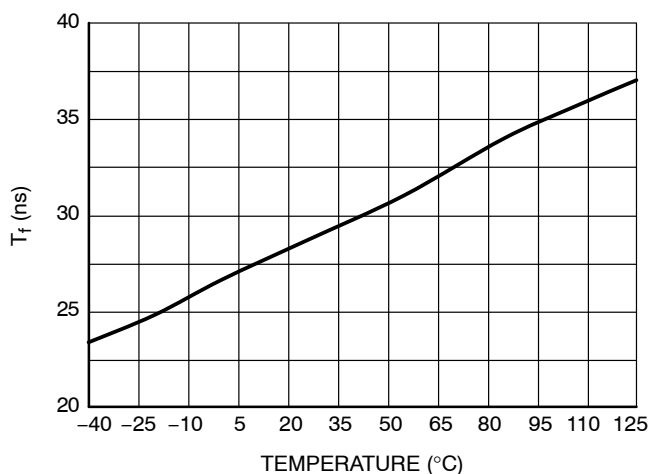


Figure 24. Output Voltage Fall-time, T_f

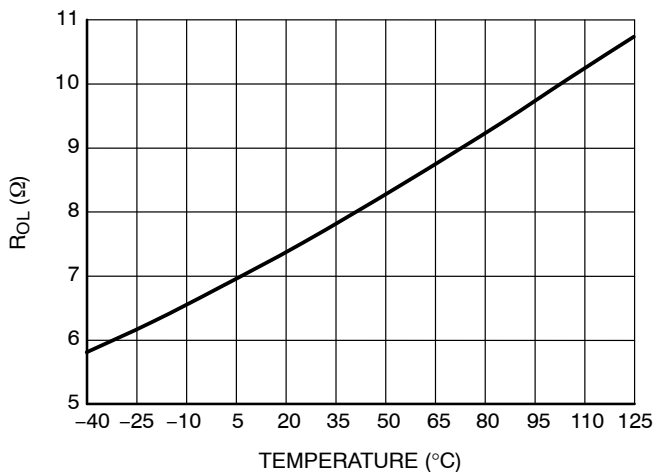


Figure 25. Source Resistance, R_{OL}

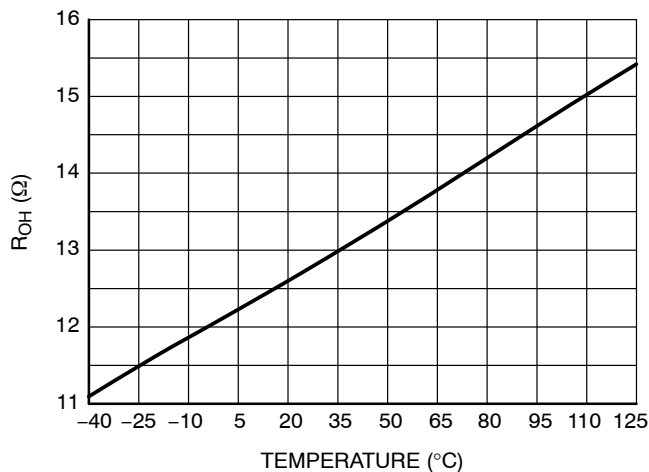


Figure 26. Sink Resistance, R_{OH}

NCP1249C, NCP1249D

TYPICAL CHARACTERISTICS

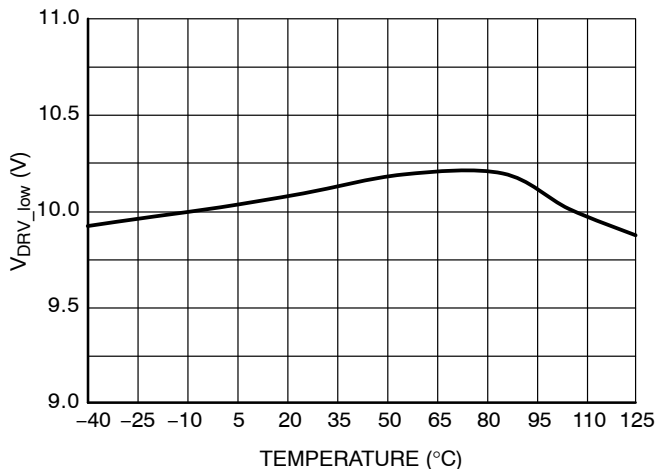


Figure 27. DRV Pin Level at V_{CC} Close to V_{CC_OFF} , V_{DRV_low}

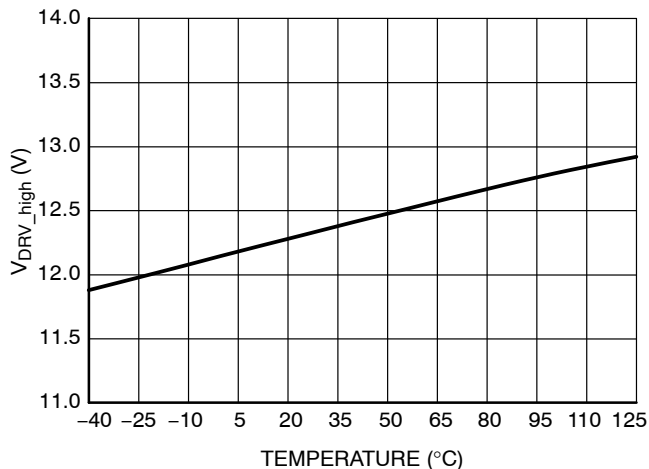


Figure 28. DRV Pin Level at V_{CC} Close to V_{OVP} , V_{DRV_high}

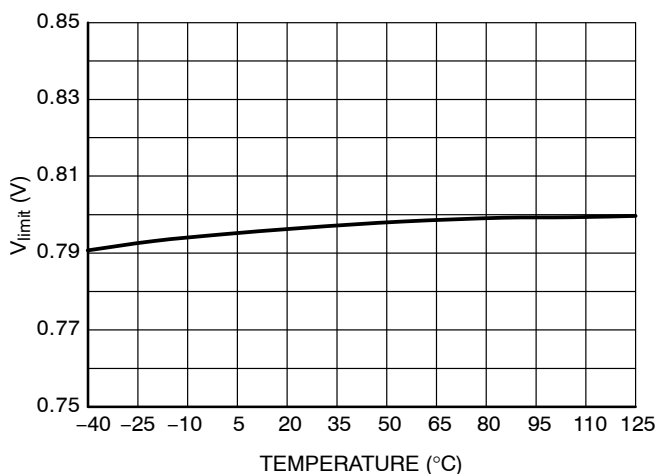


Figure 29. Maximum Internal Current Set-point, V_{limit}

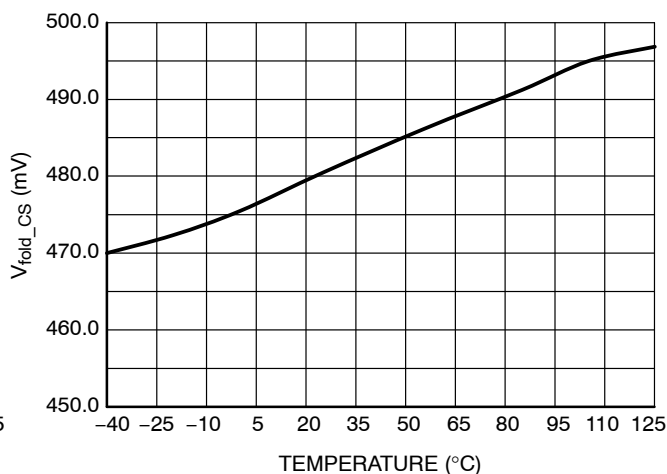


Figure 30. Default Internal Voltage Set Point for Frequency Foldback, V_{fold_CS}

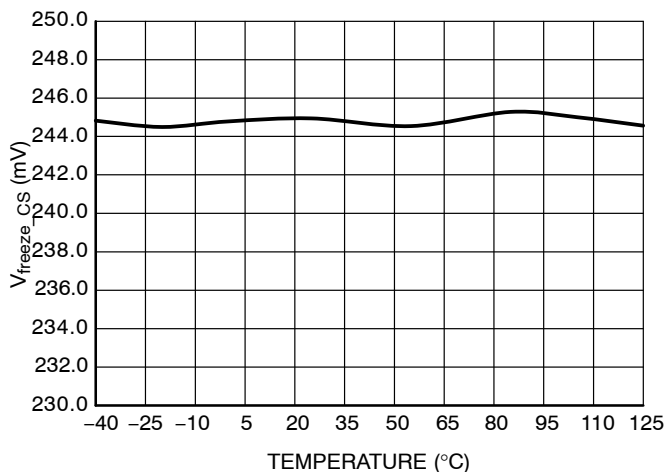


Figure 31. Internal Peak Current Set-point Freeze, V_{freeze_CS}

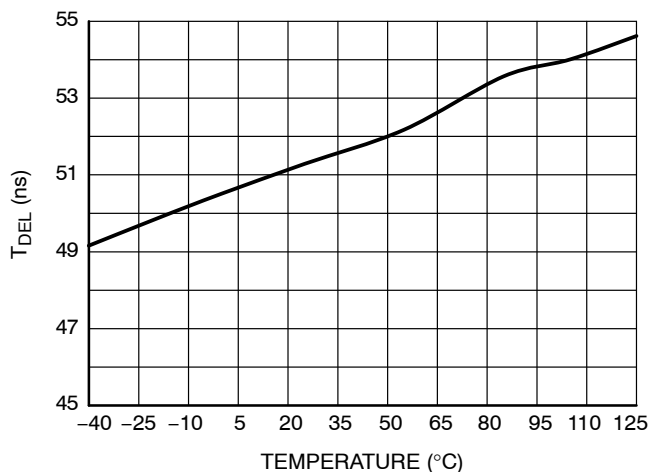


Figure 32. Propagation Delay from Current Detection to Gate Off-state, T_{DEL}

NCP1249C, NCP1249D

TYPICAL CHARACTERISTICS

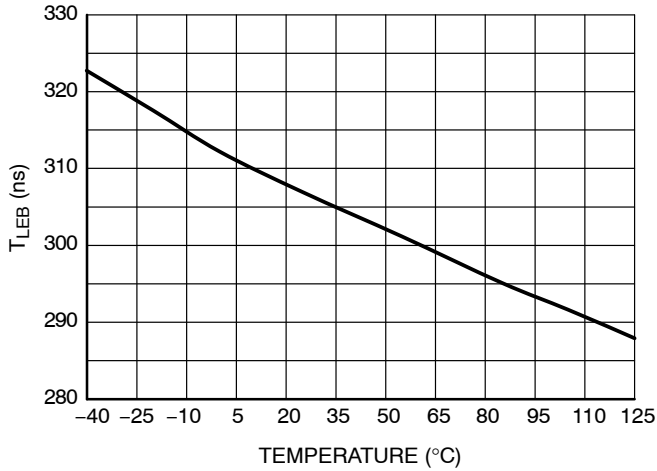


Figure 33. Leading Edge Blanking Duration, T_{LEB}

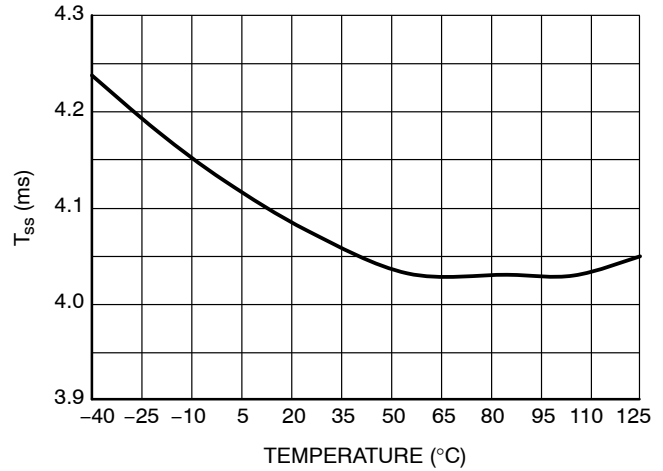


Figure 34. Internal Soft-start Duration, T_{SS}

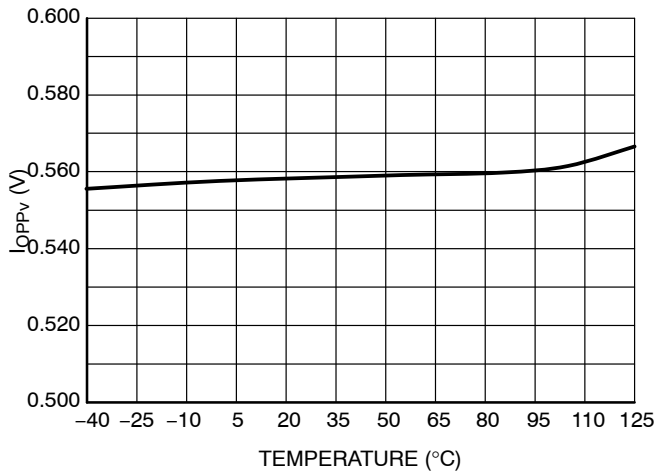


Figure 35. CS Voltage Setpoint for OPP, I_{OPPv}

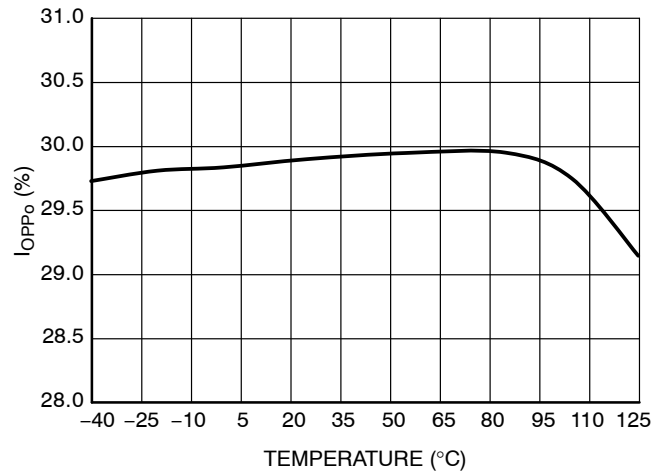


Figure 36. Set-point Decrease for OPP, I_{OPP0}

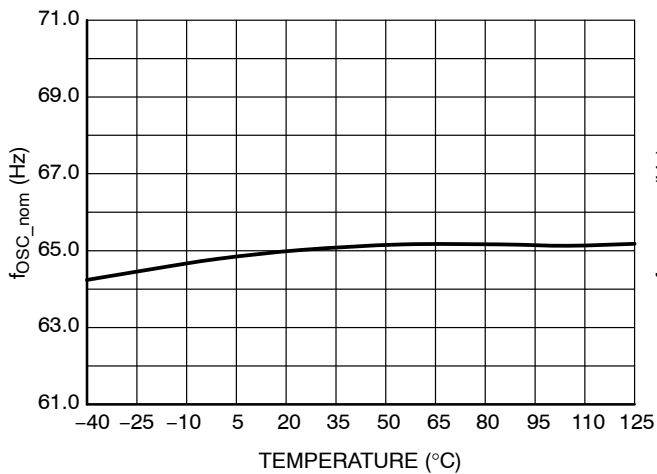


Figure 37. Oscillation Frequency, f_{OSC_nom}

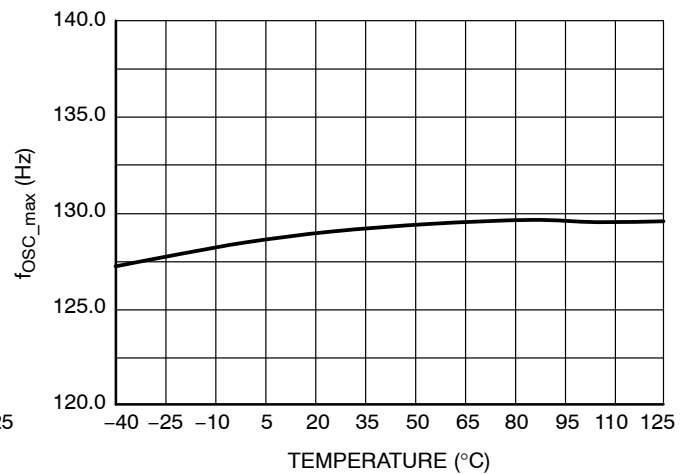


Figure 38. Maximum Oscillation Frequency, f_{OSC_max}

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TYPICAL CHARACTERISTICS

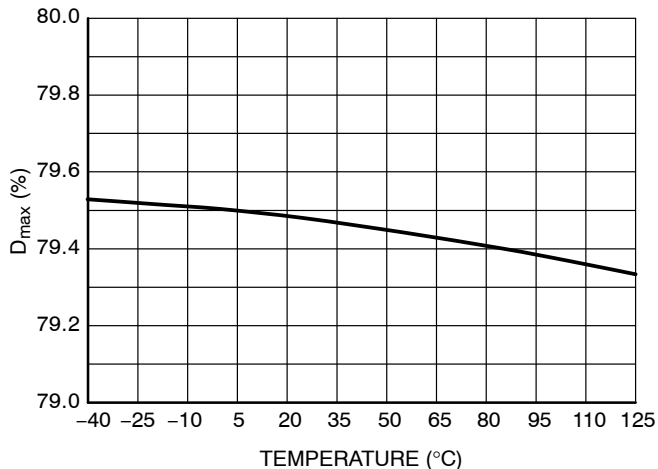


Figure 39. Maximum Duty-cycle, D_{max}

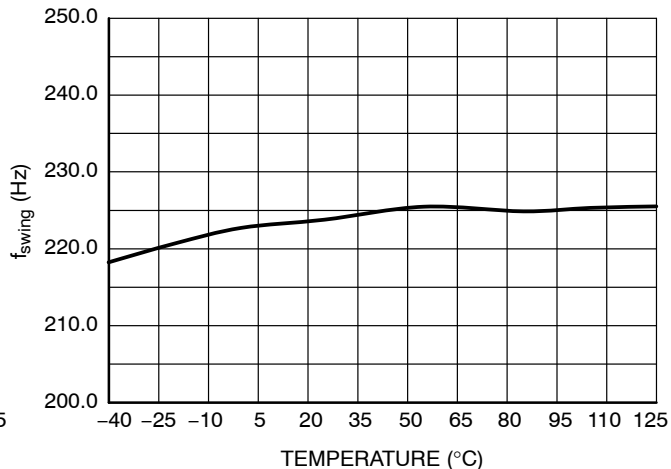


Figure 40. Swing Frequency, f_{swing}

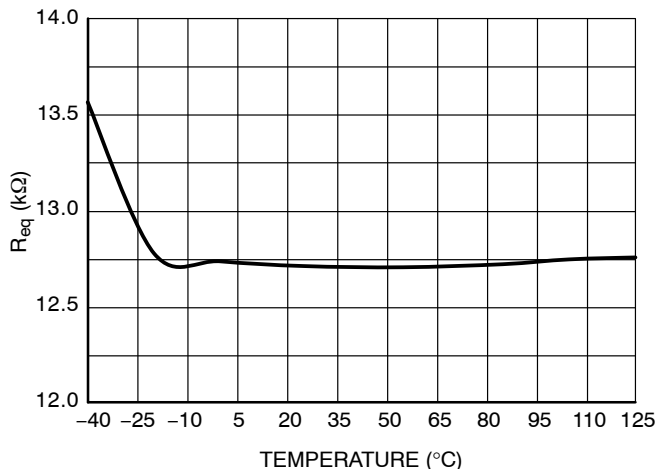


Figure 41. Equivalent ac Resistor from FB to GND, R_{eq}

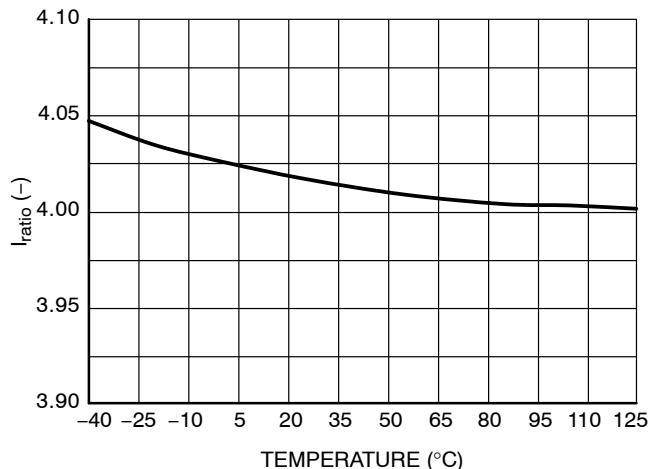


Figure 42. FB to Current Set-point Division Ratio, I_{ratio}

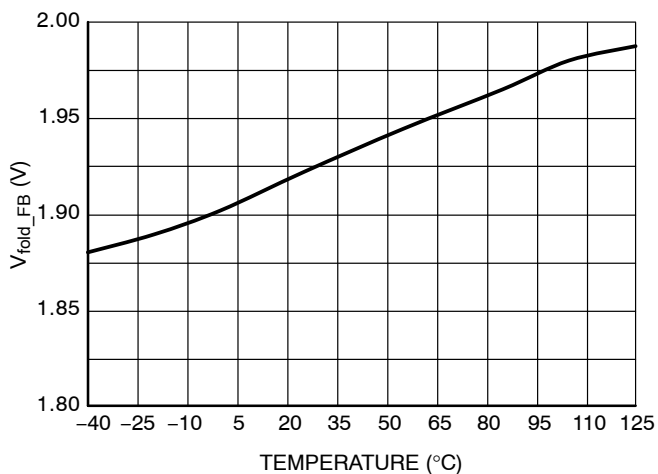


Figure 43. Frequency Foldback Level, V_{fold_FB}

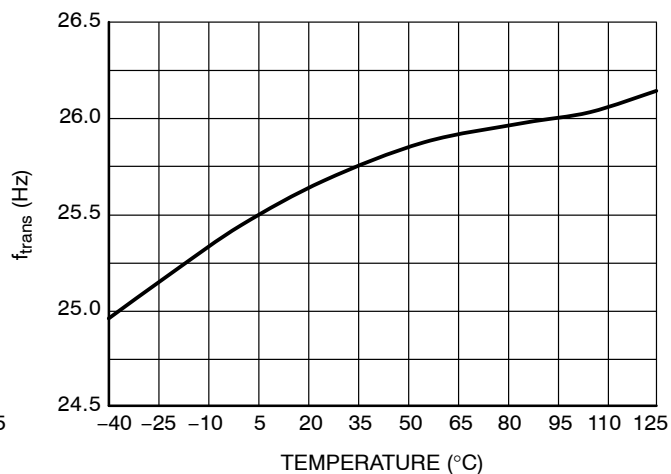


Figure 44. Transition Frequency Below Which Skip-cycle Occurs, f_{trans}

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TYPICAL CHARACTERISTICS

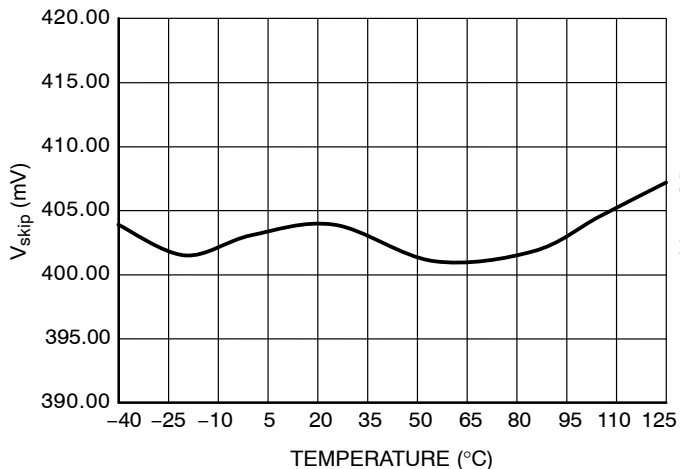


Figure 45. Skip-cycle Level Voltage on the Feedback Pin, V_{skip}

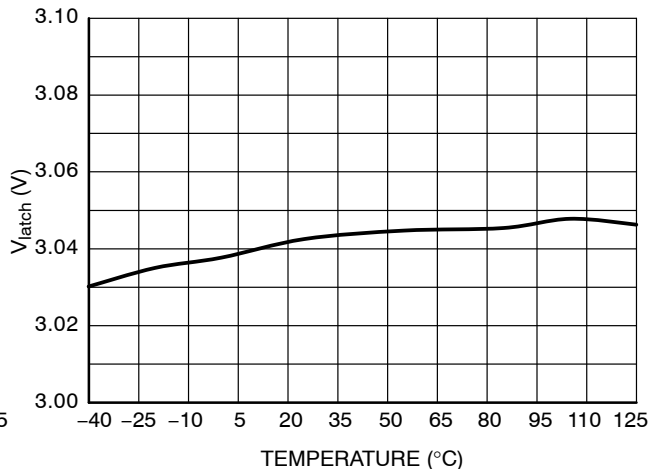


Figure 46. Latching Level Input, V_{latch}

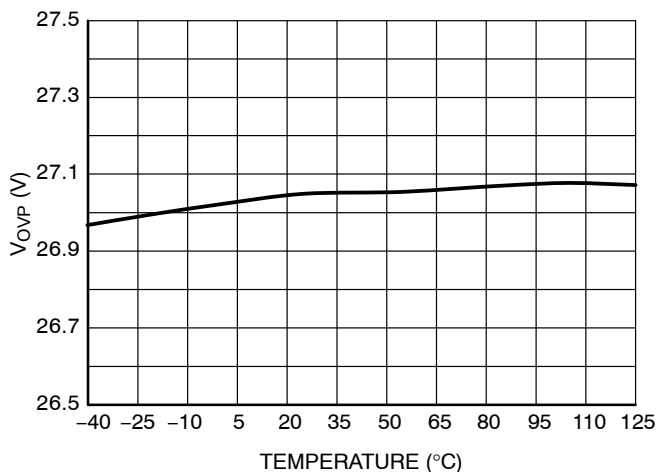


Figure 47. Over Voltage Protection on V_{CC} Rail, V_{OVP}

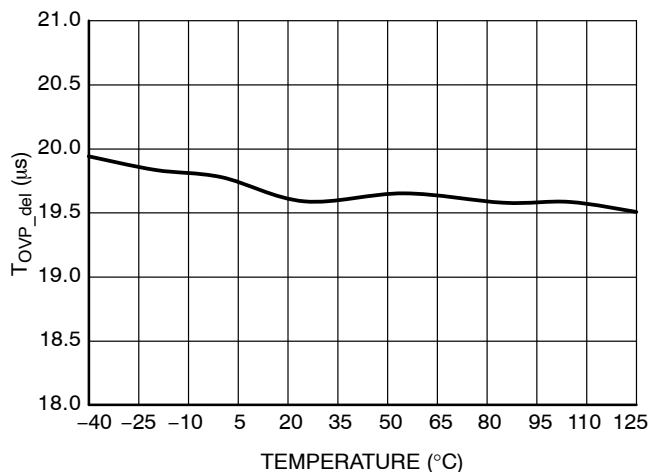


Figure 48. OVP Detection Time Constant, T_{OVP_del}

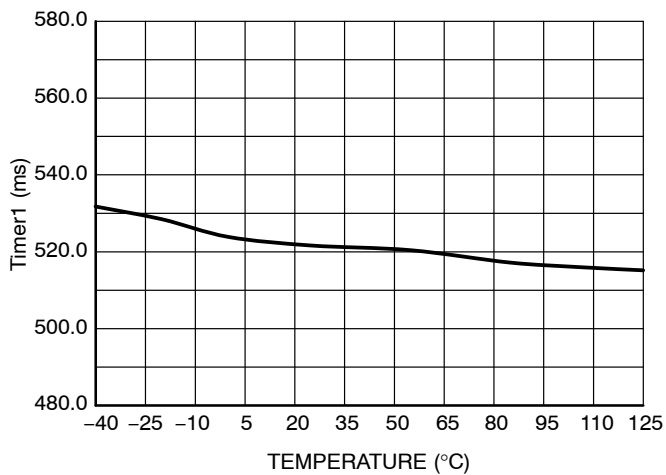


Figure 49. Fault Timer Duration - Overload, Timer1

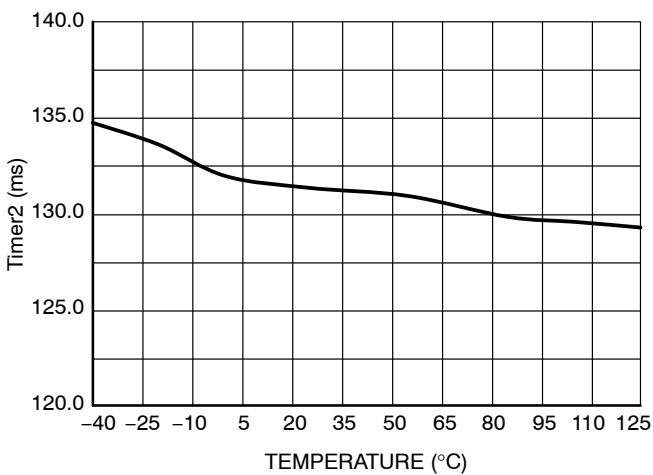


Figure 50. Fault Timer Duration - Short-circuit Condition, Timer2

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TYPICAL CHARACTERISTICS

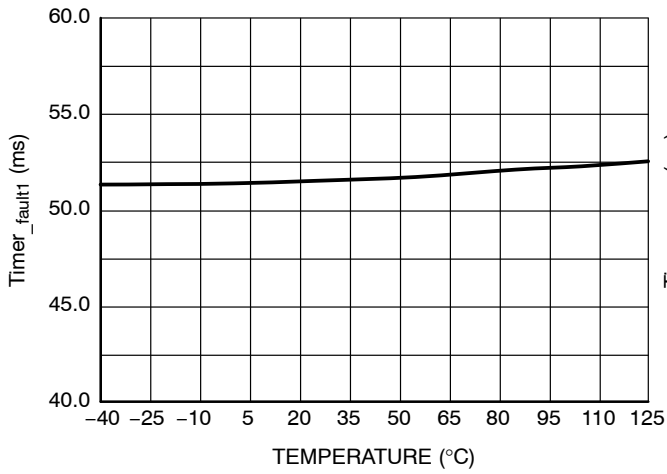


Figure 51. Fault Timer Duration when Pin 5 is Shorted to Ground – Fault Condition, Timer_fault1

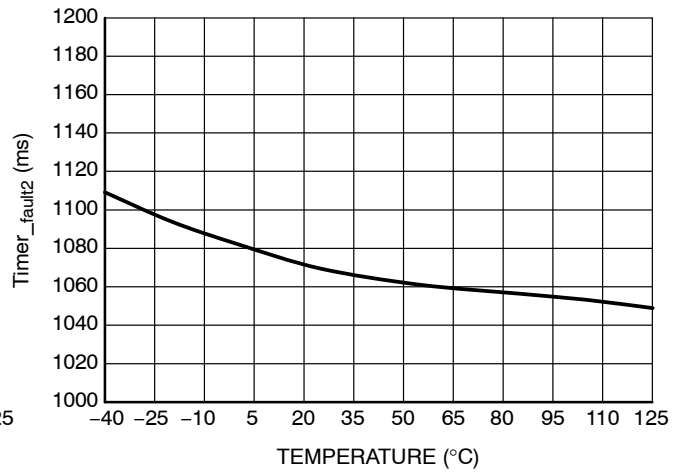


Figure 52. Fault Timer Duration when Pin 5 is Open – Fault Condition, Timer_fault2

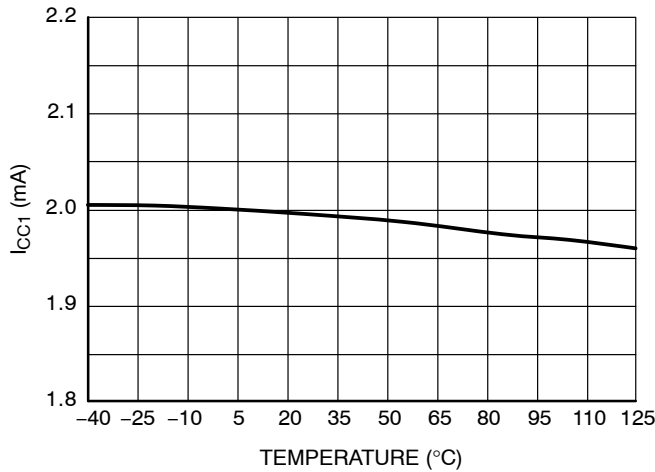


Figure 53. Internal IC Consumption, Icc1

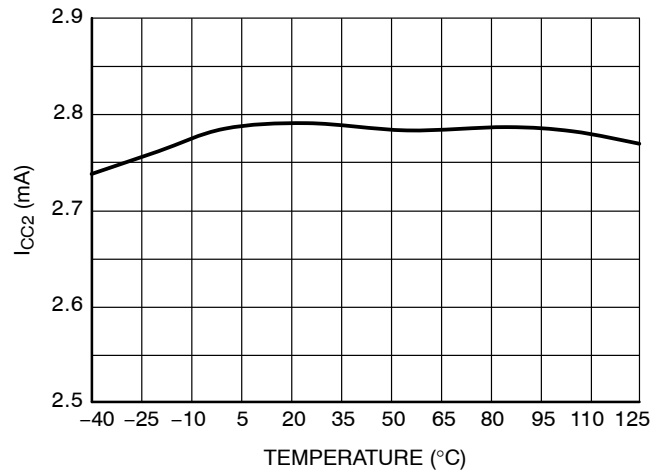


Figure 54. Internal IC Consumption, Icc2

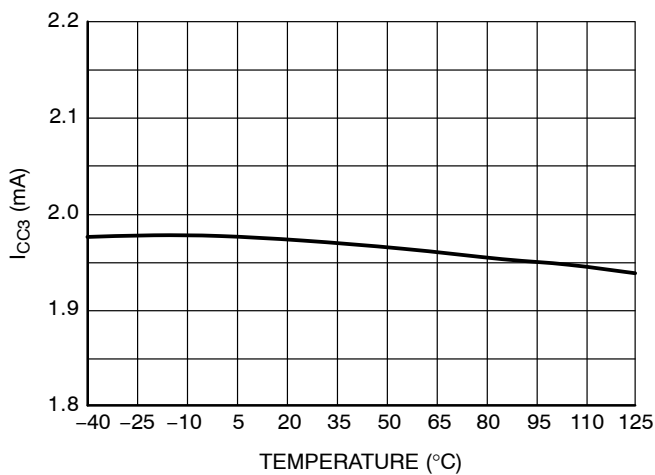


Figure 55. Internal IC Consumption, Icc3

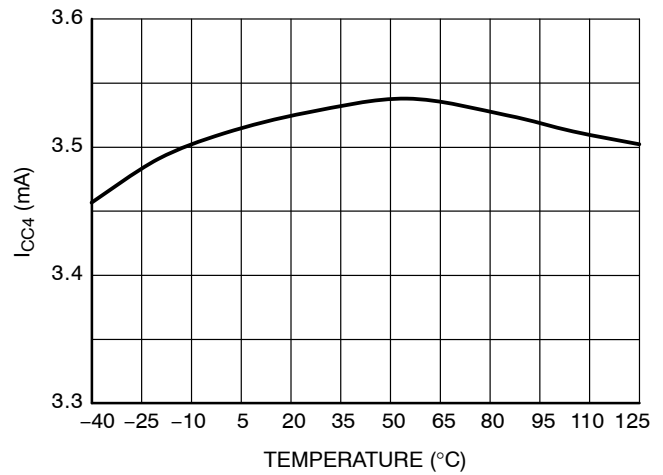


Figure 56. Internal IC Consumption, Icc4

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TYPICAL CHARACTERISTICS

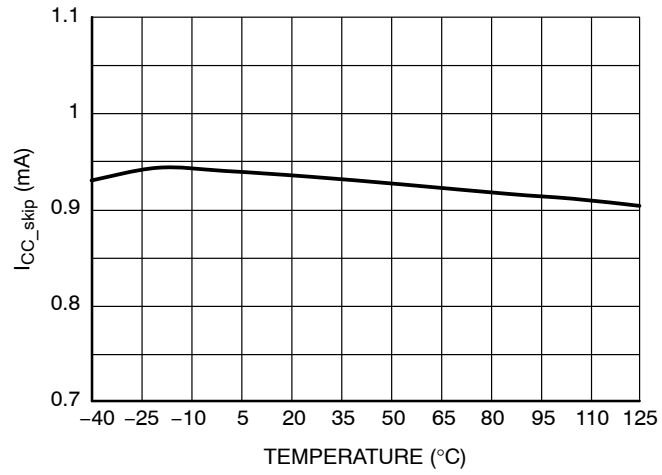


Figure 57. Internal IC Consumption during Skip Mode, I_{CC_skip}

APPLICATION INFORMATION

Introduction

The NCP1249 implements a standard current mode architecture where the switch-off event is dictated by the peak current setpoint. This component represents the ideal candidate where low part-count and cost effectiveness are the key parameters, particularly in low-cost ac-dc adapters, open-frame power supplies etc. The NCP1249 brings all the necessary components normally needed in today modern power supply designs, bringing several enhancements such as a non-dissipative OPP, a brown-out protection or peak power excursion for loads exhibiting variations over time. Accounting for the new needs of extremely low standby power requirements, the part includes an automatic X2-capacitor discharge circuitry that prevents the designer from installing power-consuming resistors across the front-end filtering capacitors. The controller is also able to enter a deep sleep mode via combined for feedback/remote pin.

- **High-Voltage start-up:** low standby power results cannot be obtained with the classical resistive start-up network. In this part, a high-voltage current-source provides the necessary current at start-up and turns off afterwards.
- **Internal Brown-Out protection:** a portion of the bulk voltage is internally sensed via the high-voltage pin monitoring (pin 10). When the voltage on this pin is too low, the part stops pulsing. No re-start attempt is made until the controller senses that the voltage is back within its normal range. When the brown-out comparator senses the voltage is acceptable, it sends a general reset to the controller (de-latch occurs) and authorizes to re-start.
- **X2-capacitors discharge capability:** per IEC-950 standard, the time constant of the front-end filter capacitors and their associated discharge resistors must be less than 1 s. This is to avoid electrical stress when the user unplugs the converter and inadvertently touches the power cord terminals. By providing an automatic means to discharge the X2 capacitors, the NCP1249 prevents the designer from installing the discharge resistors, helping to further save power.
- **Combined feedback/remote control pin:** the controller features a combined feedback/remote pin that forces the adapter to enter a deep off mode. When the FB pin is pulled down (slightly below the skip cycle mode), the part obviously stops all drive pulses. The auxiliary voltage disappears and IC goes into sleep mode. As the pull-down signal on the feedback pin is secondary-side driven, a wake-up signal releases the feedback pin and allows a fresh start-up sequence. If a dedicated circuitry is implemented on the secondary side, a self-relaxing mode can be implemented with very low standby power consumption.
- **Current-mode operation with internal slope compensation:** implementing peak current mode control at a fixed 65 kHz frequency, the NCP1249 offers an internal ramp compensation signal that can easily be summed up to the sensed current. Sub harmonic oscillations can thus be compensated via the inclusion of a simple resistor in series with the current-sense information.
- **Frequency excursion:** when the power demand forces the peak current setpoint to reach the internal limit ($0.8 \text{ V}/R_{\text{sense}}$ typically), the frequency is authorized to increase to let the converter deliver more power. The frequency excursion stops when 130 kHz are reached.
- **Internal OPP:** by routing a portion of the negative voltage present during the on-time on the auxiliary winding to the dedicated OPP pin (pin 5), the user has a simple and non-dissipative means to alter the maximum peak current setpoint as the bulk voltage increases. If the pin is grounded, no OPP compensation occurs. If the pin receives a negative voltage down to -250 mV , then a peak current reduction down to 31.3% typical can be achieved. For an improved performance, the maximum voltage excursion on the sense resistor is limited to 0.8 V.
- **EMI jittering:** an internal low-frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis. To improve the EMI signature at low power levels, the jittering will not be disabled in frequency foldback mode (light load conditions).
- **Frequency foldback capability:** a continuous flow of pulses is not compatible with no-load/light-load standby power requirements. To excel in this domain, the controller observes the feedback pin and when it reaches a level of 1.5 V, the oscillator then starts to reduce its switching frequency as the feedback level continues to decrease. When the feedback pin reaches 1 V, the peak current setpoint is internally frozen and the frequency continues to decrease. It can go down to 26 kHz (typical) reached for a feedback level of 450 mV roughly. At this point, if the power continues to drop to 400 mV, the controller enters classical skip-cycle mode.
- **Internal soft-start:** a soft-start precludes the main power switch from being stressed upon start-up. In this controller, the soft-start is internally fixed to 4 ms. Soft-start is activated when a new startup sequence occurs or during an auto-recovery hiccup.
- **Latch input:** the NCP1249 includes a latch input (pin 4) that can be used to sense an overvoltage condition on the adapter. If this pin is brought higher

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than the internal reference voltage V_{latch} , then the circuit permanently latches off. The VCC pin is pulled down to a fixed level, keeping the controller latched. The latch reset occurs when the user disconnects the adapter from the mains.

- **VCC OVP:** a latched OVP protects the circuit against VCC runaways. The fault must be present at least 20 μ s to be validated. Reset occurs when the user disconnects the adapter from the mains.
- **Short-circuit protection:** short-circuit and especially over-load protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the aux winding level does not properly collapse in presence of an output short). Here, every time the internal 0.8-V maximum peak current limit is activated (or less when OPP is used), an error flag is asserted and a time period starts, thanks to the programmable timer. The controller can distinguish between two faulty situations:
 - ◆ There is an extra demand of power, still within the power supply capabilities. In that case, the feedback level is in the vicinity of 3.2–4 V. It corresponds to 0.8 V as the maximum peak current setpoint without

OPP. The timer duration is then 100% of its normal value. If the fault disappears, e.g. the peak current setpoint no longer hits the maximum value (e.g. 0.8 V at no OPP), then the timer is reset.

- ◆ The output is frankly shorted. The feedback level is thus pushed to its upper stop (4.5 V) and the timer is reduced to 25% of its normal value.
- ◆ In either mode, when the fault is validated, all pulses are stopped and the controller enters an auto-recovery burst mode, with a soft-start sequence at the beginning of each cycle. Please note the presence of a divider by two which ignores one hiccup cycle over two (double hiccup type of burst).
- ◆ As soon as the fault disappears, the SMPS resumes operation. Please note that some version offers an auto-recovery mode as we just described, some do not and latch off in case of a short circuit.

Start-up Sequence

The start-up sequence of the NCP1249 involves a high-voltage current source whose input is in pin 10. As this start-up source also performs line sensing for brown-out operation, it is recommended to wire it according to Figure 58 sketch.

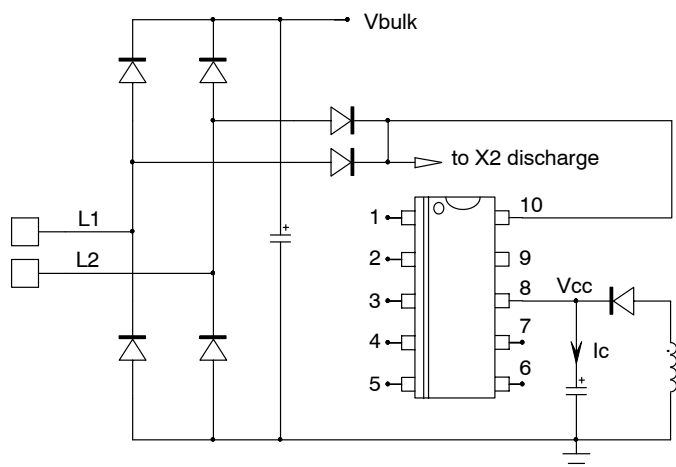


Figure 58. The Startup Resistor can be Connected to the Input Mains for Further Power Dissipation Reduction

In this drawing, the high-voltage pin is not connected to the bulk, but to the full-wave rectified ac input. It is important to keep this configuration as the X2 circuitry will also use it.

The first step starts with the calculation of the needed VCC capacitor which will supply the controller until the auxiliary winding takes over. Experience shows that this time t_1 can be between 5 and 20 ms. Considering that we need at least an energy reservoir for a t_1 time of 10 ms, the VCC capacitor must be larger than:

$$C_{VCC} \geq \frac{I_{CC4} \times t_1}{V_{CC_ON} - V_{CC_OFF}} \geq \frac{3 \text{ m} \times 10 \text{ m}}{18 - 10} \geq 3.75 \mu\text{F} \quad (\text{eq. 1})$$

In this calculation, we adopted the consumption at the highest switching frequency since this is the point at which

the IC will work in cold-start case. Let us select a 4.7 μ F capacitor at first and experiments in the laboratory will let us know if we were too optimistic for t_1 . The VCC capacitor being known, we can now evaluate the charging time to bring the VCC voltage from 0 to the V_{CC_ON} of the IC, 18 V typical. This time sequence can actually be split into two events: 0 V to $V_{CC_inhibit}$ and $V_{CC_inhibit}$ to V_{CC_ON} . This is because the HV source is protected from short-circuits on the VCC pin. In case this happens, the source detects that the VCC voltage is less than $V_{CC_inhibit}$ and only delivers I_{start1} which is below 1 mA: the die power consumption is maintained to the lowest value. In normal operation, when the voltage has normally reached $V_{CC_inhibit}$, the source toggles to the full current and charges the VCC capacitor at

a larger current, I_{start2} . The first time duration involves I_{start1} and $V_{CC_inhibit}$.

$$t_{start1} = \frac{V_{CC_inhibit} \times C_{VCC}}{I_{start1}} = \frac{1 \times 4.7 \mu}{700 \mu} \approx 6.7 \text{ ms} \quad (\text{eq. 2})$$

The second duration involves V_{CC_ON} and I_{start2} :

$$t_{start2} = \frac{(V_{CC_ON} - V_{CC_inhibit})C_{VCC}}{I_{start2}} = \frac{(18 - 1) \times 4.7 \mu}{10 \text{ m}} \approx 8 \text{ ms} \quad (\text{eq. 3})$$

The total start-up time is thus around 14–15 ms.

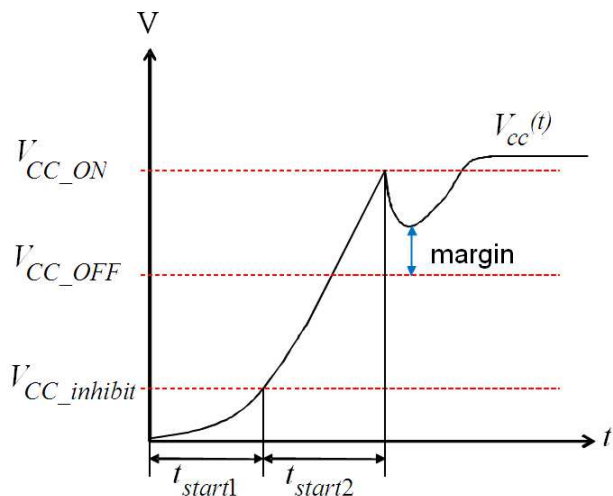


Figure 59. The VCC at Start-up is Made of Two Segments Given the Short-circuit Protection Implemented on the HV Source

In case the V_{CC} capacitor must be increased to cope with no-load standby requirements, there is plenty of margin to keep the total start-up sequence duration below 1 s. Assume the V_{CC} capacitor is 100 μF , then the total start-up time would be below 400 ms.

Brown-out Circuitry

The NCP1249 features, on its HV pin, a true AC line monitoring circuitry – refer to Figure 60. This system includes a minimum start-up threshold and auto-recovery brown-out protection; both of them independent of the input voltage ripple. The thresholds are fixed, but they are designed to fit most of the standard AC-DC converter applications. When the HV pin voltage drops below V_{BO_off} threshold for more than 50 ms, the brown-out condition is detected and confirmed. Thus the controller stops operation – refer to Figure 61. The V_{CC} capacitor is discharged to

V_{CC_bias} level. The HV current source maintains V_{CC} at V_{CC_bias} level until the input voltage is back above V_{BO_on} . The controller then fully discharges V_{CC} capacitor first to restart internal logic. Standard startup attempt is then placed by the controller.

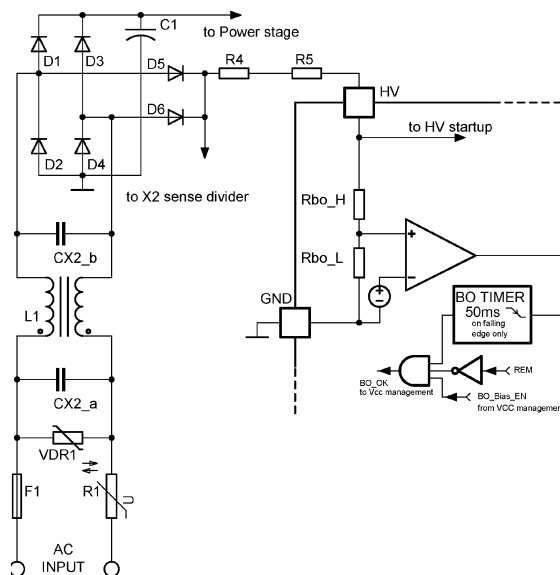


Figure 60. Simplified Block Diagram of Brown-out Detection Circuitry

The Internal HV BO sensing network is formed by high impedance resistor divider with minimum resistance of 20 M Ω . This solution reducing power losses during off-mode and thus helps to pass maximum standby power consumption limit. The internal BO network solution provides excellent noise and PCB leakage currents immunity that is hard to achieve when using external resistor divider built from SMT chip resistors.

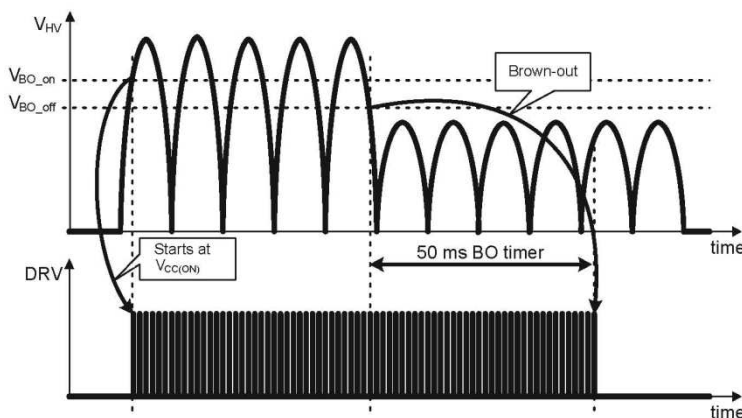


Figure 61. Brown-out Event Detection

X2 and V_{CC} Discharge Circuitry

The NCP1249 X2 discharge circuitry uses dedicated pin (X2) together with external charge pump sensing network to detect whether is application plugged into the mains or not. Advantage of this solution is that the internal IC consumption can be reduced to extremely low level by keeping all internal blocks unbiased except simple and low

consuming X2 timer disable circuitry. The internal X2 timer with typical duration of 100 ms is used to overcome unwanted activation of the X2 discharge switch in case of AC line dropout. The internal X2 discharge switch is activated once the X2 timer elapses. The HV startup current source is enabled in the same time thus the discharge path for X2 capacitor exists – refer to Figure 62.

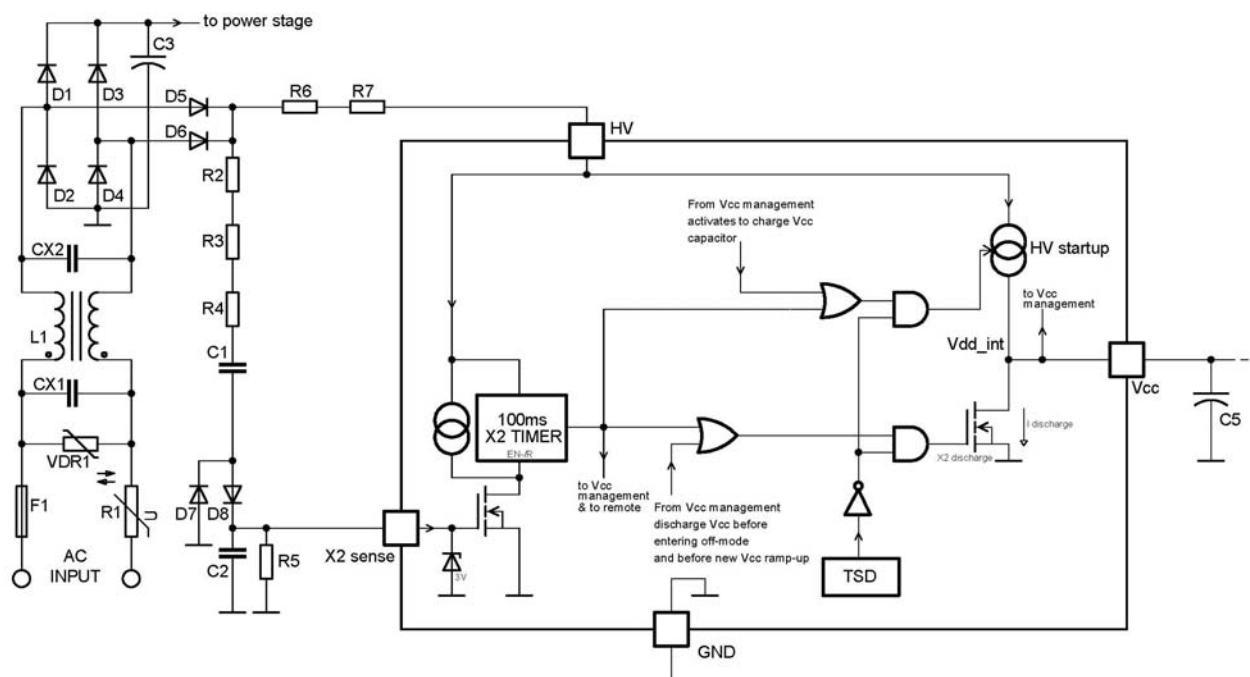


Figure 62. Simplified Block Diagram of X2 and V_{CC} Capacitor Discharge Circuitry

The time duration of X2 capacitors discharging could be calculated by:

$$t = \frac{U_{C_{X1,2}}}{I_{X2_dis}} \cdot C_{X1,2} \quad (\text{eq. 4})$$

The X2 capacitor discharging process can be interrupted by increasing voltage on X2 pin back above V_{th_X2} .

The over temperature protection controller is active during discharging process to protect controller chip against

unwanted overheat that could occur in case the X2 pin is opened and the high voltage is present on the HV pin (like during open – short pins testing for instance).

The X2 discharge switch is also activated to discharge V_{CC} capacitor when entering into fault mode (latch mode, auto-recovery mode or the HV pin voltage drops below V_{BO_off} threshold for more than 50 ms), off-mode and also before controller V_{CC} restart.

Feedback/Remote Input

The off mode is activated when the remote pin is low and V_{CC_OFF} threshold is crossed i.e. when the skip mode takes so long time that V_{CC} is lost. V_{CC} capacitor is then discharged by internal consumption. Maximum skip mode

duration before the NCP1249 enters off-mode is thus given by value of V_{CC} capacitor, total consumption during skip mode and voltage level on V_{CC} capacitor in the time when flyback controller enters skip mode.

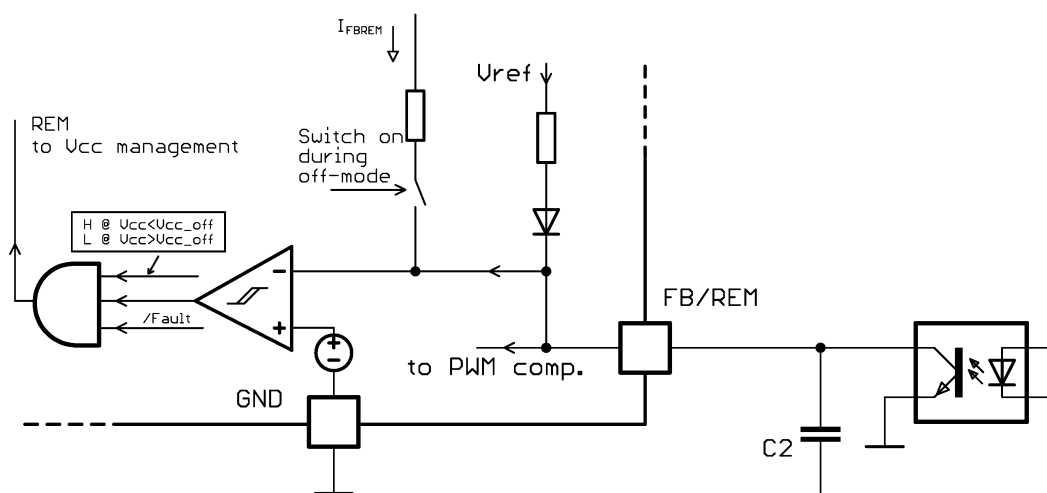


Figure 63. Simplified Block Diagram of FB/REM Control Input

To force the controller entering the off mode, the voltage on the feedback pin has to go below the skip cycle level, 400 mV typically. At this moment, all pulses are blocked and the auxiliary V_{CC} declines down to 0 V at a pace fixed by the V_{CC} capacitor and the controller consumption. When it passes below the V_{CC_OFF} threshold, because the FB pin is still maintained low, the controller does not reactivate the high-voltage start-up source and the circuit remains locked, consuming the least power. The circuit remains off as long as the feedback pin pulled to ground.

When the feedback pin is released, an internal current source (I_{FBREM}), pulls the feedback voltage up, above the

inhibition comparator. At this moment, the high-voltage source is good to go and it refuels the V_{CC} capacitor until a new start-up sequence occurs. If the feedback pin is driven by a dedicated off-mode controller, shortly after the new start-up sequence, the feedback pin will go down again, initiating another off cycle. The resulting output voltage exhibits a large low-frequency ripple, naturally decreasing the overall consumption budget of the converter. Typical V_{CC} and feedback signals while in this mode are drawn in Figure 64.

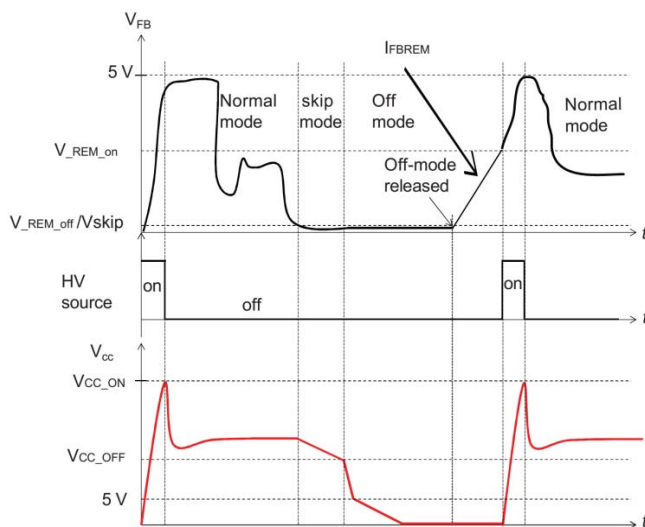


Figure 64. Combined FB/REM Pin Behavior

Operating Status Diagram

The NCP1249A/B V_{CC} management behavior is clearly described in status diagram on Figure 65.

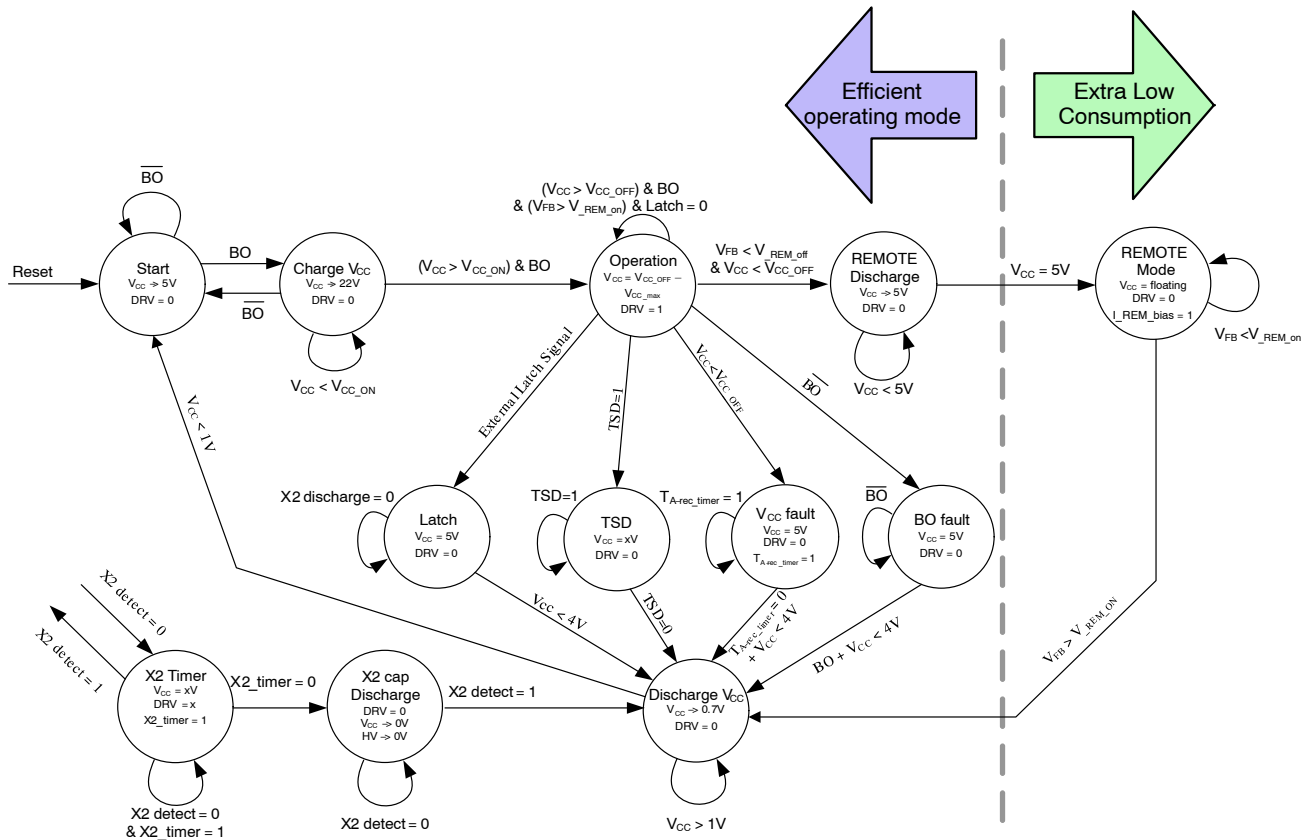


Figure 65. V_{CC} Management Status Diagram

Internal Over Power Protection

There are several known ways to implement Over Power Protection (OPP), all suffering from particular problems. These problems range from the added consumption burden on the converter or the skip-cycle disturbance brought by the current-sense offset. A way to reduce the power capability at high line is to capitalize on the negative voltage swing present on the auxiliary diode anode. During the turn-on time, this point dips to $-N V_{in}$, N being the turns ratio between the primary winding and the auxiliary winding. The negative plateau observed on Figure 66 will have amplitude depending on the input voltage. The idea implemented in this chip is to sum a portion of this negative swing with the 0.8 V internal reference level. For instance, if the voltage swings down to -150 mV during the on time, then the internal peak current set point will be fixed to $0.8 - 0.150 = 650$ mV. The adopted principle appears in Figure 67 and shows how the final peak current set point is constructed.

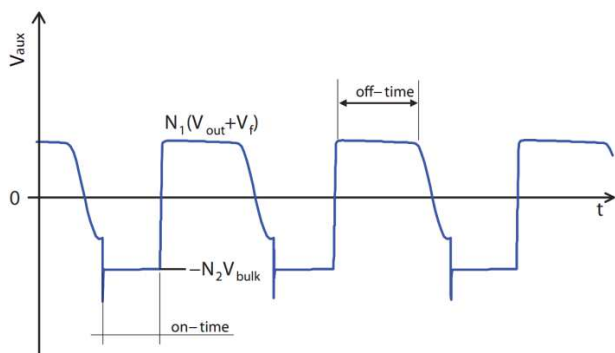


Figure 66. The Signal Obtained on the Auxiliary Winding Swings Negative During the On-Time

Let's assume we need to reduce the peak current from 2.5 A at low line, to 2 A at high line. This corresponds to a 20% reduction or a set point voltage of 640 mV. To reach this level, then the negative voltage developed on the OPP pin must reach:

$$V_{OPP} = 640 \text{ m} - 800 \text{ m} = -160 \text{ mV} \quad (\text{eq. 5})$$

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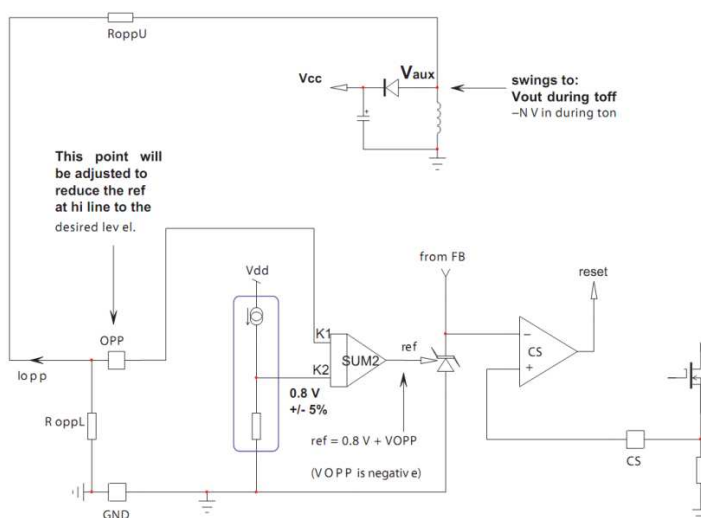


Figure 67. The OPP Circuitry Affects the Maximum Peak Current Set Point by Summing a Negative Voltage to the Internal Voltage Reference

Let us assume that we have the following converter characteristics:

$$V_{out} = 19 \text{ V}$$

$$V_{in} = 85 \text{ to } 265 \text{ V rms}$$

$$N_1 = N_p:N_s = 1:0.25$$

$$N_2 = N_p:N_{aux} = 1:0.18$$

Given the turns ratio between the primary and the auxiliary windings, the on-time voltage at high line (265 Vac) on the auxiliary winding swings down to:

$$V_{aux} = -N_2 V_{in,max} = -0.18 \times 375 = -67.5 \text{ V} \quad (\text{eq. 6})$$

To obtain a level as imposed by (Equation 5), we need to install a divider featuring the following ratio:

$$\text{Div} = \frac{0.16}{67.5} \approx 2.4 \text{ m} \quad (\text{eq. 7})$$

If we arbitrarily fix the pull-down resistor R_{OPPL} to 1 k Ω , then the upper resistor can be obtained by:

$$R_{OPPU} = \frac{67.5 - 0.16}{0.16/1 \text{ k}} \approx 421 \text{ k}\Omega \quad (\text{eq. 8})$$

If we now plot the peak current set point obtained by implementing the recommended resistor values, we obtain the following curve (Figure 68):

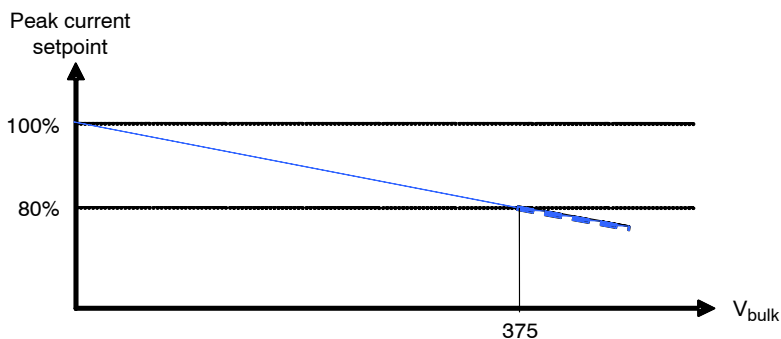


Figure 68. The peak current regularly reduces down to 20% at 375 V dc

The OPP pin is surrounded by Zener diodes stacked to protect the pin against ESD pulses. These diodes accept some peak current in the avalanche mode and are designed to sustain a certain amount of energy. On the other side, negative injection into these diodes (or forward bias) can cause substrate injection which can lead to an erratic circuit behavior. To avoid this problem, the pin is internal clamped slightly below -300 mV which means that if more current is injected before reaching the ESD forward drop, then the

maximum peak reduction is kept to 40%. If the voltage finally forward biases the internal zener diode, then care must be taken to avoid injecting a current beyond -2 mA. Given the value of R_{OPPU} , there is no risk in the present example. Finally, please note that another comparator internally fixes the maximum peak current set point to 0.8 V even if the OPP pin is adversely biased above 0 V.

For optimum performance over temperature, we recommend keeping the low-side OPP resistor below 3 k Ω .

Frequency Foldback

The reduction of no-load standby power associated with the need for improving the efficiency, requires a change in the traditional fixed-frequency type of operation. This controller implements a switching frequency foldback when the feedback voltage passes below a certain level, V_{fold_FB} , set around 1.9 V. At this point, the oscillator turns into a Voltage-Controlled Oscillator and reduces its switching frequency. The peak current setpoint is following the

feedback pin until its level reaches 1 V. Below this value, the peak current freezes to $V_{freeze_FB/4}$ (250 mV or $\approx 31\%$ of the maximum 0.8 V setpoint) and the only way to further reduce the transmitted power is to diminish the operating frequency down to 26 kHz. This value is reached at a voltage feedback level of 450 mV typically. Below this point, if the output power continues to decrease, the part enters skip cycle for the best noise-free performance in no-load conditions. Figure 69 depicts the adopted scheme for the part.

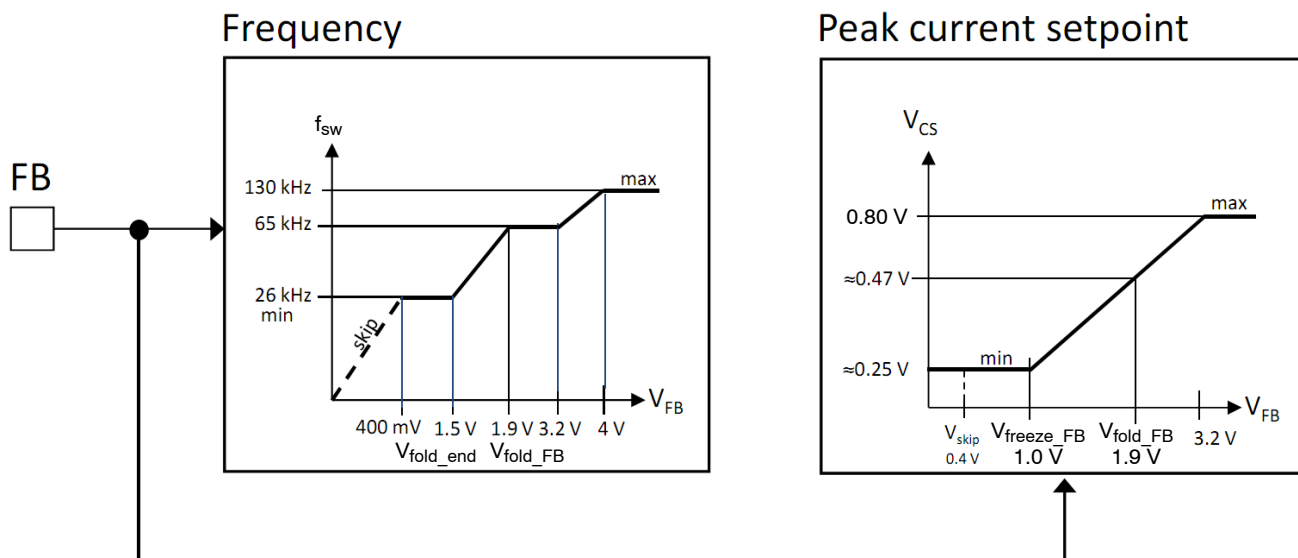


Figure 69. By Observing the Voltage on the Feedback Pin, the Controller Reduces its Switching Frequency for an Improved Performance at Light Load

Auto-recovery Short-circuit Protection

In case of output short-circuit or if the power supply experiences a severe overloading situation, an internal error flag is raised and starts a countdown timer. If the flag is asserted longer than fault timer duration, the driving pulses are stopped and the V_{CC} capacitor is discharged down to 10 V (V_{CC_OFF} threshold) by controller ICC consumption. At this point, the controller activates 2 s auto-recovery timer that starts to count down the time to new restart attempt. The total restart time from fault confirmation is thus given by sum of two times: V_{CC} capacitor discharge time from given V_{CC} level (present at fault confirmation event) to V_{CC_OFF} level and 2 s internal auto-recovery timer duration. The V_{CC} capacitor is discharged to V_{CC_bias} level when auto-recovery timer starts counting. The V_{CC} is maintained at V_{CC_bias} level during this operation to keep timer and other internal circuitry running.

The V_{CC} capacitor is fully discharged by X2 discharge switch before controller tries for restart from fault condition. The restart from fault condition is caused when auto-recovery timer elapses or V_{CC} is forced below 4 V externally. The HV startup current source is activated to charge the V_{CC} capacitor in fast manner to V_{CC_ON} level and

thus to restart converter operation in case the input line voltage is above V_{BO_on} threshold. The controller is then checking for the absence of the fault. If the fault is still there, the supply enters another cycle of so-called hiccup. If the fault has disappeared, the power supply resumes operations. Please note that the soft-start is activated during each of the re-start sequence.

Slope Compensation

The NCP1249 includes an internal ramp compensation signal. This is the buffered oscillator clock delivered during the on time only. Its amplitude is around 2.5 V at the maximum authorized duty-ratio. Ramp compensation is a known means used to cure sub harmonic oscillations in CCM-operated current-mode converters. These oscillations take place at half the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty-ratio greater than 50%. To lower the current loop gain, one usually mixes between 50% and 100% of the inductor downslope with the current-sense signal. Figure 70 depicts how internally the ramp is generated. Please note that the ramp signal will be disconnected from the CS pin, during the off-time.

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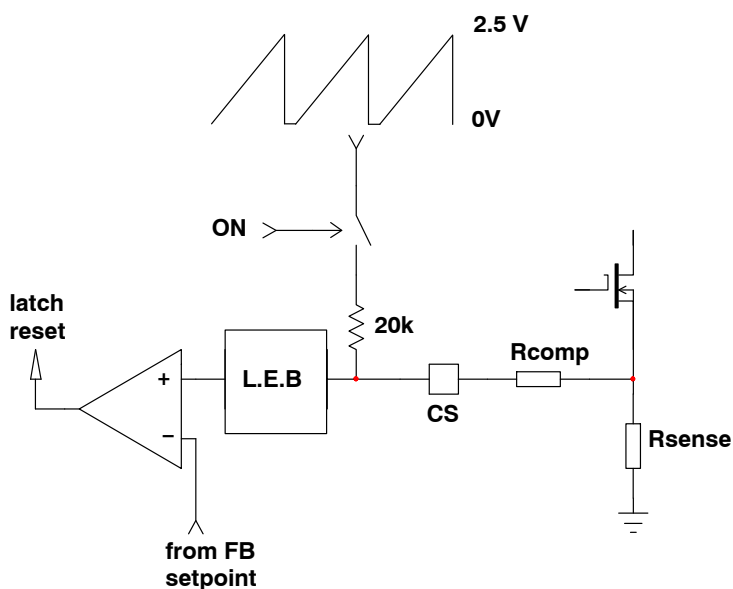


Figure 70. Inserting a Resistor in Series with the Current Sense Information Brings Slope Compensation and Stabilizes the Converter in CCM Operation

In the NCP1249 controller, the oscillator ramp exhibits a 2.5 V swing reached at a 80% duty-ratio. If the clock operates at a 65 kHz frequency, then the available oscillator slope corresponds to:

$$S_{\text{ramp}} = \frac{V_{\text{ramp}}}{D_{\text{max}} \times T_{\text{sw}}} = \frac{2.5}{0.8 \times 15 \mu} = 208 \text{ kV/s or } 208 \text{ mV}/\mu\text{s} \quad (\text{eq. 9})$$

In our flyback design, let's assume that our primary inductance L_p is 770 μH , and the SMPS delivers 19 V with a $N_p:N_s$ turns ratio of 1:0.25. The off-time primary current slope S_p is thus given by:

$$S_p = \frac{(V_{\text{out}} + V_f) \frac{N_p}{N_s}}{L_p} = \frac{(19 + 0.8) \times 4}{770 \mu} = 103 \text{ kA/s} \quad (\text{eq. 10})$$

Given a sense resistor of 330 m Ω , the above current ramp turns into a voltage ramp of the following amplitude:

$$S_{\text{sense}} = S_p R_{\text{sense}} = 103 \text{ k} \times 0.33 = 34 \text{ kV/s or } 34 \text{ mV}/\mu\text{s} \quad (\text{eq. 11})$$

If we select 50% of the downslope as the required amount of ramp compensation, then we shall inject a ramp whose slope is 17 mV/ μs . Our internal compensation being of 208 mV/ μs , the divider ratio (*divratio*) between R_{comp} and the internal 20 k Ω resistor is:

$$\text{divratio} = \frac{17 \text{ m}}{208 \text{ m}} = 0.082 \quad (\text{eq. 12})$$

The series compensation resistor value is thus:

$$R_{\text{comp}} = R_{\text{ramp}} \text{ divratio} = 20 \text{ k} \times 0.082 \approx 1.64 \text{ k}\Omega \quad (\text{eq. 13})$$

A resistor of the above value will then be inserted from the sense resistor to the current sense pin. We recommend adding a small 100 pF capacitor, from the current sense pin to the controller ground for improved noise immunity. Please make sure both components are located very close to the controller.

Latching Off the Controller

The OPP pin not only allows a reduction of the peak current set point in relationship to the line voltage, it also offers a means to permanently latch-off the part. When the part is latched-off, the VCC pin is internally pulled down to $V_{\text{CC_bias}}$ and the part stays in this state until the user un-plugs the converter from the mains outlet or V_{CC} is forced below 4 V externally. The latch detection is made by observing the OPP pin by a comparator featuring a 3 V reference voltage. However, for noise reasons and in particular to avoid the leakage inductance contribution at turn off, a 1 μs blanking delay is introduced before the output of the OVP comparator is checked. Then, the OVP comparator output is validated only if its high-state duration lasts a minimum of 600 ns. Below this value, the event is ignored. Then, a counter ensures that only four successive OVP events have occurred before actually latching the part. There are several possible implementations, depending on the needed precision and the parameters you want to control.

The first and easiest solution is the additional resistive divider on top of the OPP one. This solution is simple and inexpensive but requires the insertion of a diode to prevent disturbing the OPP divider during the on-time.