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NCP1652, NCP1652A

High-Efficiency Single Stage Power Factor Correction and Step-Down Controller

The NCP1652 is a highly integrated controller for implementing power factor correction (PFC) and isolated step down ac−dc power conversion in a single stage, resulting in a lower cost and reduced part count solution. This controller is ideal for notebook adapters, battery chargers and other off−line applications with power requirements between 75 W and 150 W. The single stage is based on the flyback converter and it is designed to operate in continuous conduction (CCM) or discontinuous conduction (DCM) modes.

The NCP1652 increases the system efficiency by incorporating a secondary driver with adjustable nonoverlap delay for controlling a synchronous rectifier switch in the secondary side, an active clamp switch in the primary or both. In addition, the controller features a proprietary Soft−Skip™ to reduce acoustic noise at light loads. Other features found in the NCP1652 include a high voltage startup circuit, voltage feedforward, brown out detector, internal overload timer, latch input and a high accuracy multiplier.

Features

- Dual Control Outputs with Adjustable Non Overlap Delay for Driving a Synchronous Rectifier Switch, an Active Clamp Switch or Both
- Voltage Feedforward Improves Loop Response
- Frequency Jittering Reduces EMI Signature
- Proprietary Soft−Skip™ at Light Loads Reduces Acoustic Noise
- Brown Out Detector
- Internal 150 ms Fault Timer
- Independent Latch−Off Input Facilitates Implementation of Overvoltage and Overtemperature Fault Detectors
- Single Stage PFC and Isolated Step Down Converter
- Continuous or Discontinuous Conduction Mode Operation
- Average Current Mode Control (ACMC), Fixed Frequency Operation
- High Accuracy Multiplier Reduces Input Line Harmonics
- Adjustable Operating Frequency from 20 kHz to 250 kHz
- These are Pb−Free Devices

Typical Applications

- Notebook Adapter
- High Current Battery Chargers
- Front Ends for Distributed Power Systems
- High Power Solid State Lighting

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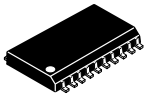
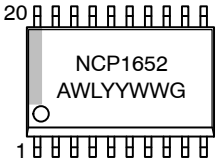
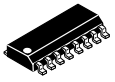
MARKING DIAGRAMS



SO−20 WB
DW SUFFIX
CASE 751D





SOIC−16
D SUFFIX
CASE 751B

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 32 of this data sheet.

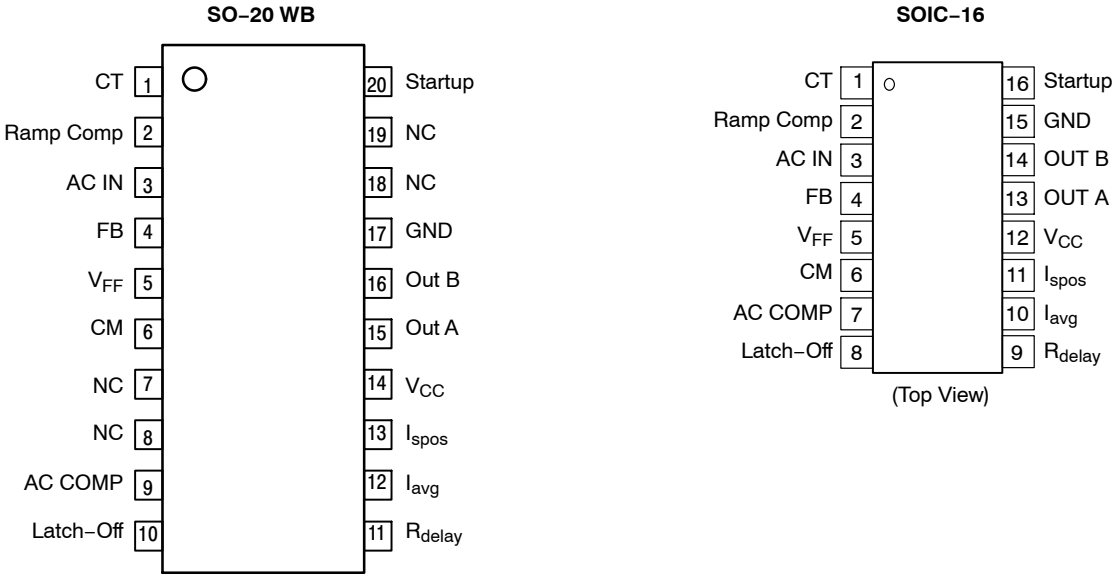


Figure 1. Pin Connections

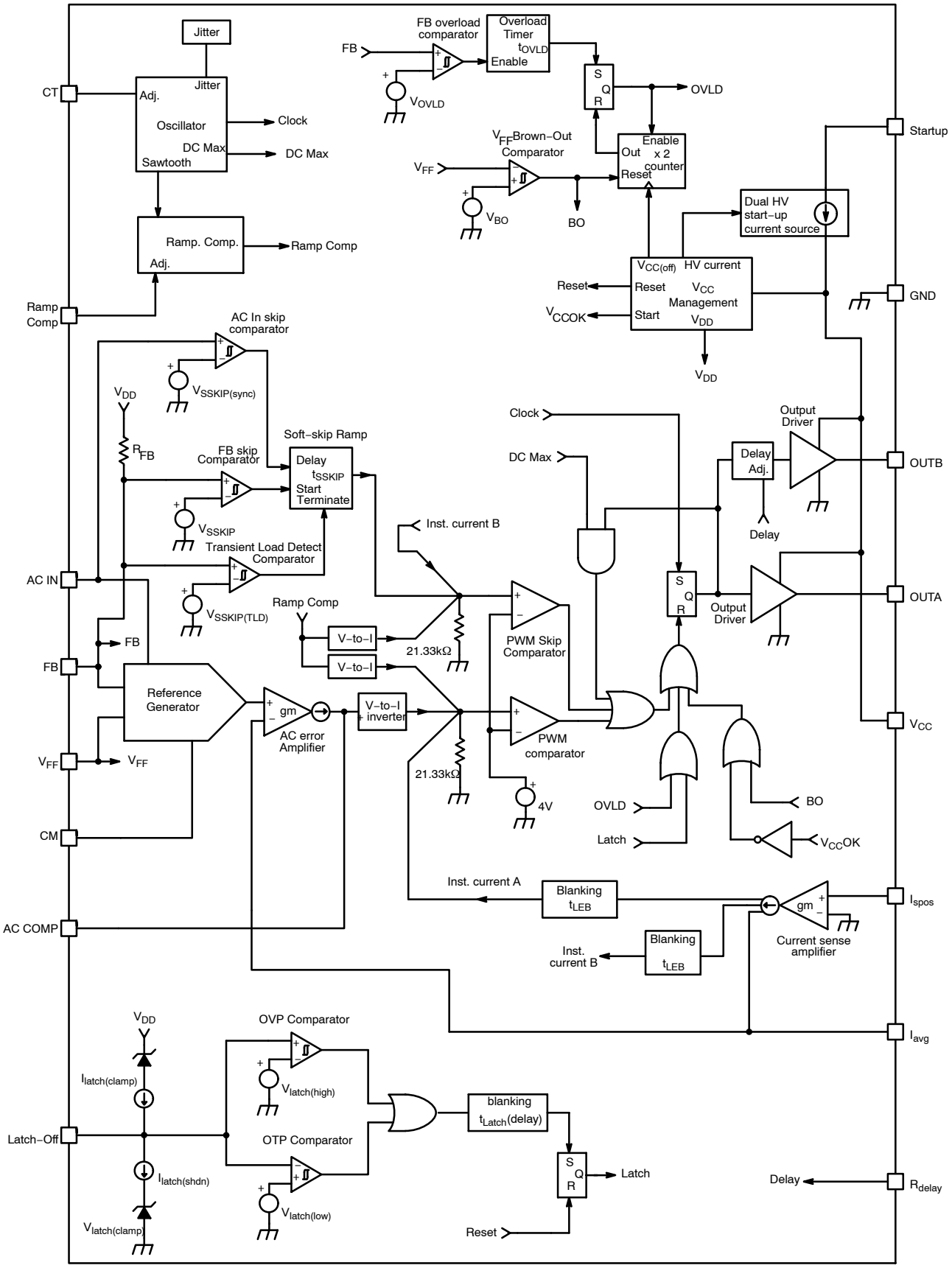


Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin		Symbol	Description
16 Pin	20 Pin		
1	1	C_T	An external timing capacitor (C_T) sets the oscillator frequency. A sawtooth between 0.2 V and 4 V sets the oscillator frequency and the gain of the multiplier.
2	2	RAMP COMP	A resistor (R_{RC}) between this pin and ground adjust the amount of ramp compensation that is added to the current signal. Ramp compensation is required to prevent subharmonic oscillations. This pin should not be left open.
3	3	AC IN	The scaled version of the full wave rectified input ac wave is connected to this pin by means of a resistive voltage divider. The line voltage information is used by the multiplier.
4	4	FB	An error signal from an external error amplifier circuit is fed to this pin via an optocoupler or other isolation circuit. The FB voltage is a proportional of the load of the converter. If the voltage on the FB pin drops below V_{SSKIP} the controller enters Soft−Skip™ to reduce acoustic noise.
5	5	VFF	Feedforward input. A scaled version of the filtered rectified line voltage is applied by means of a resistive divider and an averaging capacitor. The information is used by the Reference Generator to regulate the controller.
6	6	CM	Multiplier output. A capacitor is connected between this pin and ground to filter the modulated output of the multiplier.
	7	NC	
	8	NC	
7	9	AC COMP	Sets the pole for the ac reference amplifier. The reference amplifier compares the low frequency component of the input current to the ac reference signal. The response must be slow enough to filter out most of the high frequency content of the current signal that is injected from the current sense amplifier, but fast enough to cause minimal distortion to the line frequency information. The pin should not be left open.
8	10	Latch	Latch−Off input. Pulling this pin below 1.0 V (typical) or pulling it above 7.0 V (typical) latches the controller. This input can be used to implement an overvoltage detector, an overtemperature detector or both. Refer to Figure 69 for a typical implementation.
9	11	Rdelay	A resistor between this pin and ground sets the non−overlap time delay between OUTA and OUTB. The delay is adjusted to prevent cross conduction between the primary MOSFET and synchronous rectification MOSFET or optimize the resonant transition in an active clamp stage.
10	12	I_{AVG}	An external resistor and capacitor connected from this terminal to ground, to set and stabilizes the gain of the current sense amplifier output that drives the ac error amplifier.
11	13	I_{Spos}	Positive current sense input. Connects to the positive side of the current sense resistor.
12	14	V_{CC}	Positive input supply. This pin connects to an external capacitor for energy storage. An internal current source supplies current from the STARTUP pin V_{CC}. Once the voltage on V_{CC} reaches approximately 15.3 V, the current source turns off and the outputs are enabled. The drivers are disabled once V_{CC} reaches approximately 10.3 V. If V_{CC} drops below 0.85 V (typical), the startup current is reduced to less than 500 μA.
13	15	OUTA	Drive output for the main flyback power MOSFET or IGBT. OUTA has a source resistance of 13 Ω (typical) and a sink resistance of 8 Ω (typical).
14	16	OUTB	Secondary output of the PWM Controller. It can be used to drive synchronous rectifier, and active clamp switch, or both. OUTB has source and sink resistances of 22 Ω (typical) and 11 (typical), respectively.
15	17	GND	Ground reference for the circuit.
	18	NC	
	19	NC	
16	20	HV	Connect the rectified input line voltage directly to this pin to enable the internal startup regulator. A constant current source supplies current from this pin to the capacitor connected to the V_{CC} pin, eliminating the need for a startup resistor. The charge current is typically 5.5 mA. Maximum input voltage is 500 V.

MAXIMUM RATINGS (Notes 1 and 2)

Rating	Symbol	Value	Unit
Start_up Input Voltage Start_up Input Current	V_{HV} I_{HV}	−0.3 to 500 ±100	V mA
Power Supply Input Voltage Power Supply Input Current	V_{CC} I_{CC}	−0.3 to 20 ±100	V mA
Latch Input Voltage Latch Input Current	V_{Latch} I_{Latch}	−0.3 to 10 ±100	V mA
OUTA Pin Voltage OUTA Pin Current	V_{outA} I_{outA}	−0.3 to 20 ±1.0	V A
OUTB Pin Voltage OUTB Pin Current	V_{outB} I_{outB}	−0.3 to 20 ±600	V mA
All Other Pins Voltage All Other Pins Current		−0.3 to 6.5 ±100	V mA
Thermal Resistance, Junction−to−Air 0.1 in" Copper 0.5 in" Copper	θ_{JA}	 130 110	°C/W
Thermal Resistance, Junction−to−Lead	$R_{\Theta JL}$	50	°C/W
Maximum Power Dissipation @ T_A = 25°C	P_{MAX}	0.77	W
Operating Temperature Range	T_J	−40 to 125	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   16 pin package:
   Pin 1−15: Human Body Model 2000 V per JEDEC standard JESD22, Method A114.
   Machine Model 200 V per JEDEC standard JESD22, Method A115.
   Pin 16 is the high voltage startup of the device and is rated to the maximum rating of the part, 500 V.
   20 pin package:
   Pin 1−19: Human Body Model 2000 V per JEDEC standard JESD22, Method A114.
   Machine Model 200 V per JEDEC standard JESD22, Method A115.
   Pin 20 is the high voltage startup of the device and it is rated to the maximum rating of the part, or 500 V.
2. This device contains Latchup protection and exceeds ±100 mA per JEDEC Standard JESD78.

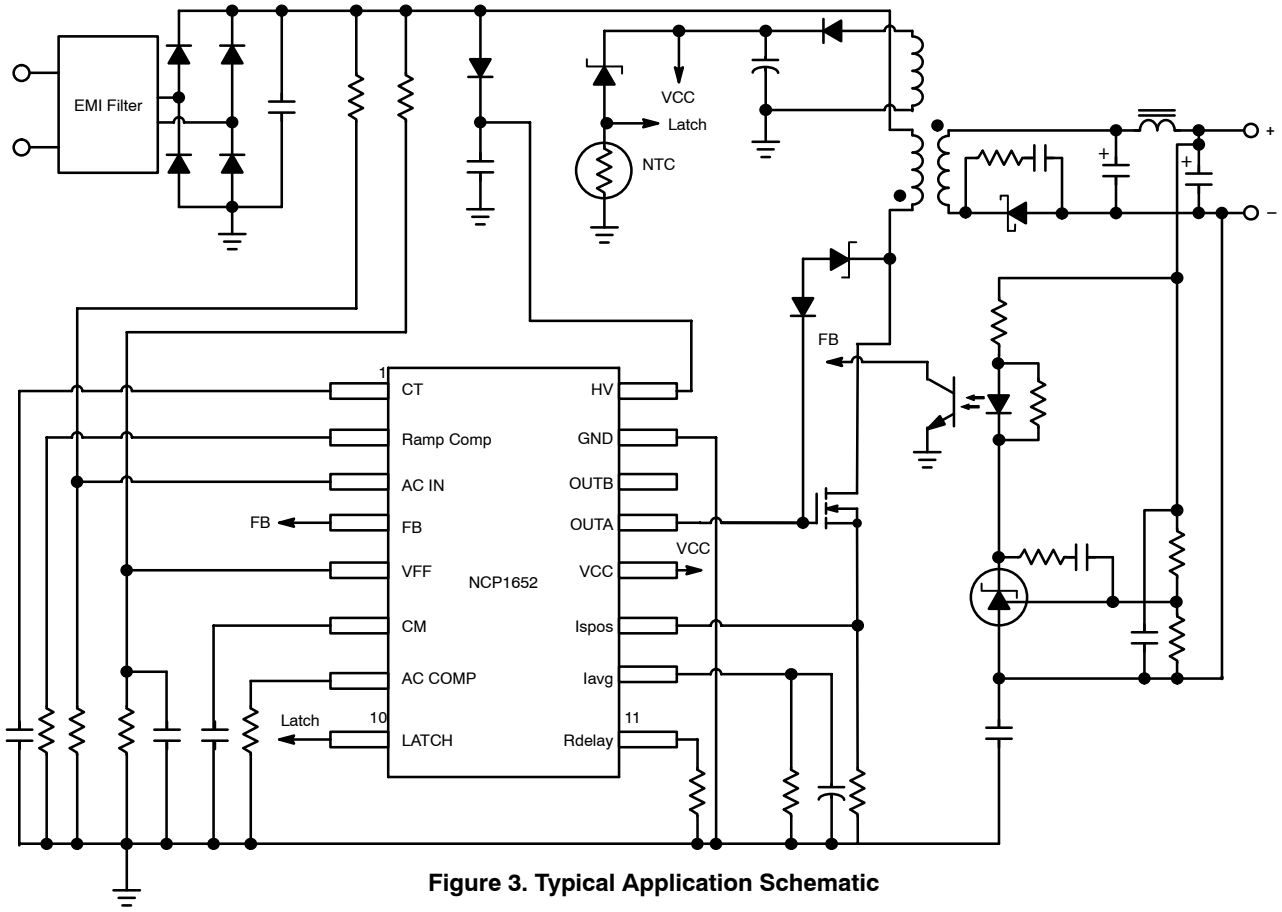


Figure 3. Typical Application Schematic

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, $V_{AC\ IN}$ = 3.8 V, V_{FB} = 2.0 V, V_{FF} = 2.4 V, V_{Latch} = open, V_{ISPOS} = −100 mV, C_{OUTA} = 1 nF, C_T = 470 pF, C_{IAVG} = 0.27 nF, C_{Latch} = 0.1 nF, C_M = 10 nF, R_{IAVG} = 76.8 kΩ, R_{delay} = 49.9 kΩ, C_{OUTB} = 330 pF, R_{RC} = 43 kΩ, For typical Value T_J = 25°C, for min/max values T_J = −40°C to 125°C, unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
OSCILLATOR						
Frequency		f_{osc}	90	100	110	kHz
Frequency Modulation in Percentage of f_{OSC}			–	6.8	–	%
Frequency Modulation Period			–	6.8	–	ms
Ramp Peak Voltage		$V_{CT(peak)}$	–	4.0	–	V
Ramp Valley Voltage		$V_{CT(valley)}$	–	0.10	–	V
Maximum Duty Ratio	R_{delay} = open	D	94	–	–	%
Ramp Compensation Peak Voltage		$V_{RCOMP(peak)}$	–	4	–	V
AC ERROR AMPLIFIER						
Input Offset Voltage (Note 3)	Ramp I_{AVG}, V_{FB} = 0 V	ACV_{IO}		40	–	mV
Error Amplifier Transconductance		g_m	–	100	–	μS
Source Current	$V_{AC\ COMP}$ = 2.0 V, $V_{AC\ IN}$ = 2.0 V, V_{FF} = 1.0 V	$I_{EA(source)}$	25	70	–	μA
Sink Current	$V_{AC\ COMP}$ = 2.0 V, $V_{A\ C\_IN}$ = 2.0 V, V_{FF} = 5.0 V	$I_{EA(sink)}$	−25	−70	–	μA
CURRENT AMPLIFIER						
Input Bias Current	V_{ISPOS} = 0 V	CAI_{bias}	40	53	80	μA
Input Offset Voltage	$V_{AC\ COMP}$ = 5.0 V, V_{ISpos} = 0 V	CAV_{IO}	−20	0	20	mV
Current Limit Threshold	force OUTA high, $V_{AC\ COMP}$ = 3.0 V, ramp V_{ISPOS}, V_{Ramp_Comp} = open	V_{ILIM}	0.695	0.74	0.77	V
Leading Edge Blanking Duration		t_{LEB}	–	200	–	ns
Bandwidth			–	1.5	–	MHz
PWM Output Voltage Gain	$PWMk = \frac{4}{(V_{ILIM} - C_{AVIO})}$	PWMk	4.0	5.3	6.0	V/V
Current Limit Voltage Gain (See Current Sense Section)	$ISVK = \frac{V_{(AVG)}}{VI_{SPOS}}$	ISVk	15.4	18.5	23	V/V
REFERENCE GENERATOR						
Reference Generator Gain	$k = \frac{V_{AC\_REF} \cdot V_{FF}^{\ 2}}{V_{FB} \cdot V_{AC\_IN}}$	k	–	0.55	–	V
Reference Generator output voltage (low input ac line and full load)	$V_{AC\ IN}$ = 1.2 V, V_{FF} = 0.765 V, V_{FB} = 4 V	RG_{out1}	3.61	4.36	4.94	Vpk
Reference Generator output voltage (high input ac line and full load)	$V_{AC\ IN}$ = 3.75 V, V_{FF} = 2.39 V, V_{FB} = 4.0 V	RG_{out2}	1.16	1.35	1.61	Vpk
Reference Generator output Voltage (low input as line and minimum load)	$V_{AC\ IN}$ = 1.2 V, V_{FF} = 0.765 V, V_{FB} = 2.0 V	RG_{out3}	1.85	2.18	2.58	Vpk
Reference Generator output voltage (high input ac line and minimum load)	$V_{AC\ IN}$ = 3.75 V, V_{FF} = 2.39 V, V_{FB} = 2.0 V	RG_{out4}	0.55	0.65	0.78	Vpk
Reference Generator output offset voltage		RG_{offset}	−100	–	100	mV

3. Guaranteed by Design

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, $V_{AC\ IN}$ = 3.8 V, V_{FB} = 2.0 V, V_{FF} = 2.4 V, V_{Latch} = open, V_{ISPOS} = −100 mV, C_{OUTA} = 1 nF, C_T = 470 pF, C_{IAVG} = 0.27 nF, C_{Latch} = 0.1 nF, C_M = 10 nF, R_{IAVG} = 76.8 kΩ, R_{delay} = 49.9 kΩ, C_{OUTB} = 330 pF, R_{RC} = 43 kΩ, For typical Value T_J = 25°C, for min/max values T_J = −40°C to 125°C, unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
AC INPUT						
Input Bias Current Into Reference Multiplier & Current Compensation Amplifier		$I_{AC\ IN(IB)}$	–	0.01	–	μA
DRIVE OUTPUTS A and B						
Drive Resistance (Thermally Limited) OUTA Sink OUTA Source OUTB Sink OUTB Source	 V_{OUTA} = 1 V I_{OUTA} = 100 mA V_{OUTB} = 1 V I_{OUTB} = 100 mA	 R_{SNK1} R_{SRC1} R_{SNK2} R_{SRC2}	 – – – –	 8 10.8 10 21	 18 24 22 44	Ω
Rise Time (10% to 90%) OUTA OUTB		 t_{r1} t_{r2}	 – –	 40 25	 – –	ns
Fall Time (90% to 10%) OUTA OUTB		 t_{f1} t_{f2}	 – –	 20 10	 – –	ns
DRV Low Voltage OUTA OUTB	 I_{OUTA} = 100 μA I_{OUTB} = 100 μA	 $V_{OUTA(low)}$ $V_{OUTB(low)}$	 – –	 1.0 1.0	 100 100	mV
Non−Overlap Adjustable Delay Range (Note 3)		$t_{delay(range)}$	0.08	–	2.8	μs
Non−Overlap Adjustable Delay Leading Trailing	Measured at 50% of V_{OUT}, C_{OUTA} = C_{OUTB} = 100 pF OUTA Rising to OUTB falling OUTB Rising to OUTA falling	 $t_{delay(lead)}$ $t_{delay(trail)}$	 250 250	 450 420	 550 550	ns
Non−Overlap Adjustable Delay Matching	OUTA Rising to OUTB Falling or OUTB Rising to OUTA Falling	$t_{delay(match)}$	–	–	55	%
Soft−Skip™						
Skip Synchronization to ac Line Voltage Threshold	V_{ACIN} Increasing, V_{FB} = 1.5 V	$V_{SSKIP(SYNC)}$	210	267	325	mV
Skip Synchronization to ac Line Voltage Threshold Hysteresis	V_{ACIN} Decreasing	$V_{SSKIP\ (SYNCHYS)}$	–	40	–	mV
Skip Ramp Period (Note 3)		t_{SSKIP}	–	2.5	–	ms
Skip Voltage Threshold NCP1652 NCP1652A		V_{SSKIP}	 1.04 0.36	 1.24 0.41	 1.56 0.46	V
Skip Voltage Hysteresis		$V_{SSKIP(HYS)}$	45	90	140	mV
Skip Transient Load Detect Threshold (Note 3)	$V_{SSKIP(TLD)}$ = V_{SSKIP} +0.55 V	$V_{SSKIP(TLD)}$	–	1.75	–	V
FEEDBACK INPUT						
Pull−Up Current Source	V_{FB}= 0.5 V	I_{FB}	600	750	920	μA
Pull−Up Resistor		R_{FB}	–	6.7	–	kΩ
Open Circuit Voltage		$V_{FB(open)}$	5.3	5.7	6.3	V
STARTUP AND SUPPLY CIRCUITS						
Supply Voltage Startup Threshold Minimum Operating Voltage Logic Reset Voltage	 V_{CC} Increasing V_{CC} Decreasing V_{CC} Decreasing	 $V_{CC(on)}$ $V_{CC(off)}$ $V_{CC(reset)}$	 14.3 9.3 –	 15.4 10.2 7.0	 16.3 11.3 –	V
Inhibit Threshold Voltage	V_{HV} = 40 V, $I_{inhibit}$ = 500 μA	$V_{inhibit}$	–	0.83	1.15	V

3. Guaranteed by Design

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, $V_{AC\ IN}$ = 3.8 V, V_{FB} = 2.0 V, V_{FF} = 2.4 V, V_{Latch} = open, V_{ISPOS} = −100 mV, C_{OUTA} = 1 nF, C_T = 470 pF, C_{IAVG} = 0.27 nF, C_{Latch} = 0.1 nF, C_M = 10 nF, R_{IAVG} = 76.8 kΩ, R_{delay} = 49.9 kΩ, C_{OUTB} = 330 pF, R_{RC} = 43 kΩ, For typical Value T_J = 25°C, for min/max values T_J = −40°C to 125°C, unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Inhibit Bias Current	V_{HV} = 40 V, V_{CC} = 0.8 * $V_{inhibit}$	$I_{inhibit}$	40	-	500	μA
Minimum Startup Voltage	I_{start} = 0.5 mA, V_{CC} = $V_{CC(on)}$ − 0.5 V	$V_{start(min)}$	–	–	40	V
Startup Current	V_{CC} = $V_{CC(on)}$ − 0.5 V, V_{FB} = Open	I_{start}	3.0	5.62	8.0	mA
Off−State Leakage Current	V_{HV} = 400 V, T_J = 25°C T_J = −40°C to 125°C	$I_{HV(off)}$	 – –	 17 15	 40 80	μA
Supply Current Device Disabled (Overload) Device Switching	 V_{FB} = Open f_{OSC} ≈ 100 kHz	 I_{CC1} I_{CC2}	 – –	 0.72 6.25	 1.2 7.2	mA
FAULT PROTECTION						
Overload Timer		t_{OVLD}	120	162	360	ms
Overload Detect Threshold		V_{OVLD}	4.7	4.9	5.2	V
Brown−Out Detect Threshold (entering fault mode)	V_{FF} Decreasing, V_{FB} = 2.5 V, $V_{AC\ IN}$ = 2.0 V	$V_{BO(low)}$	0.41	0.45	0.49	V
Brown−Out Exit Threshold (exiting fault mode)	V_{FF} Increasing, V_{FB} = 2.5 V, $V_{AC\ IN}$ = 2.0 V	$V_{BO(high)}$	0.57	0.63	0.69	V
Brown−Out Hysteresis		$V_{BO(HYS)}$	–	174	–	mV
LATCH INPUT						
Pull−Down Latch Voltage Threshold	V_{Latch} Decreasing	$V_{latch(low)}$	0.9	0.98	1.1	V
Pull−Up Latch Voltage Threshold	V_{Latch} Increasing	$V_{latch(high)}$	5.6	7.0	8.4	V
Latch Propagation Delay	V_{Latch} = $V_{latch(high)}$	$t_{latch(delay)}$	30	56	90	μs
Latch Clamp Current (Going Out)	V_{Latch} = 1.5 V	$I_{latch(clamp)}$	42	51	58	μA
Latch Clamp Voltage (I_{Latch} Going In)	I_{Latch} = 50 μA	$V_{latch(clamp)}$	2.5	3.27	4.5	V
Latch−Off Current Shutdown (Going In)	V_{Latch} Increasing	$I_{latch(shdn)}$	–	95	–	μA

3. Guaranteed by Design

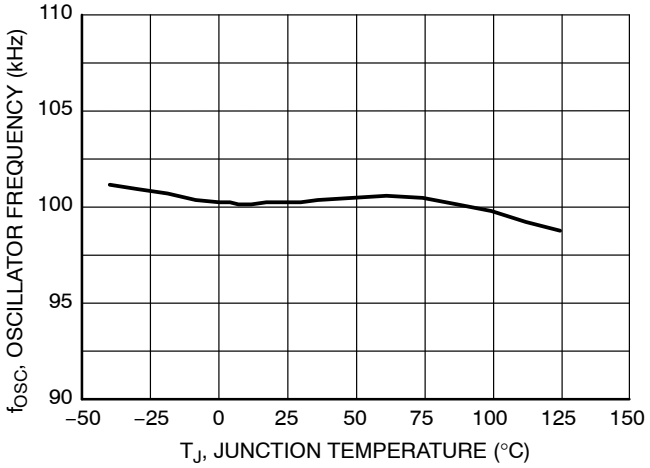


Figure 4. Oscillator Frequency (f_{OSC}) vs. Junction Temperature

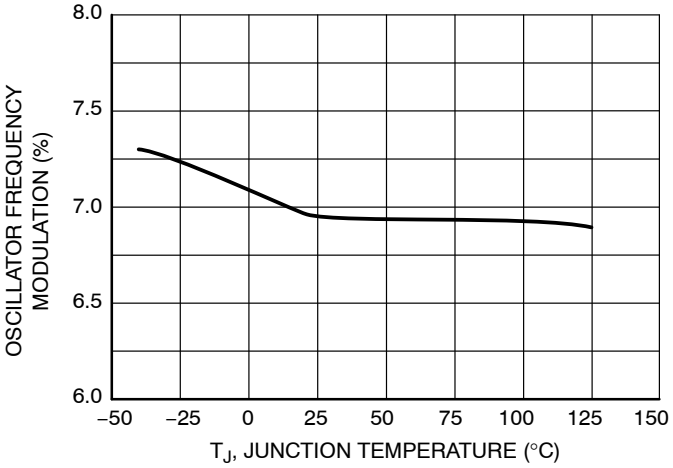


Figure 5. Oscillator Frequency Modulation in Percentage of f_{OSC} vs. Junction Temperature

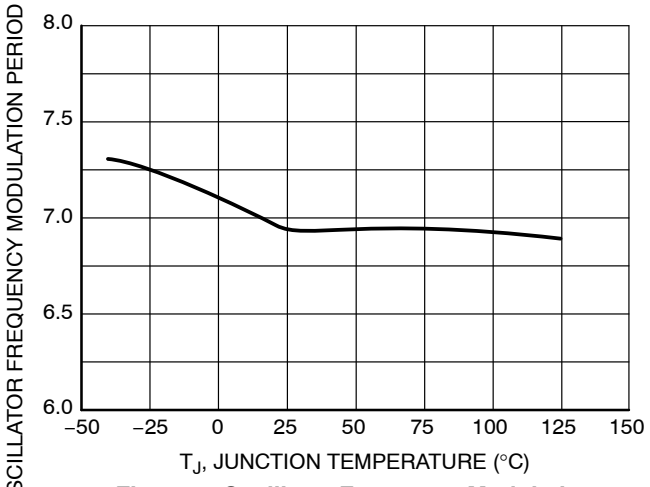


Figure 6. Oscillator Frequency Modulation Period vs. Junction Temperature

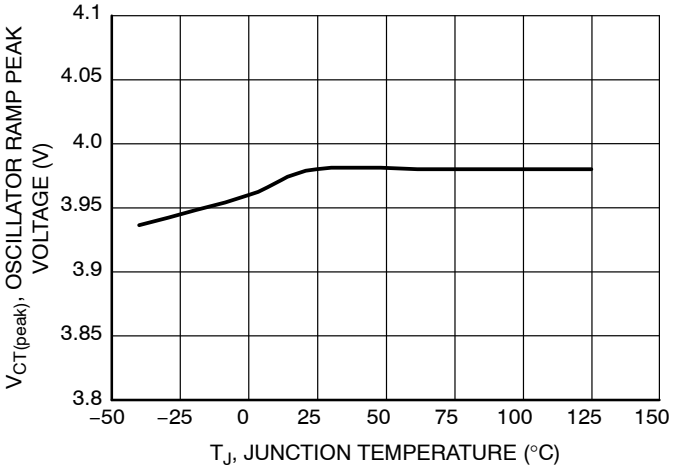


Figure 7. Ramp Peak Voltage vs. Junction Temperature

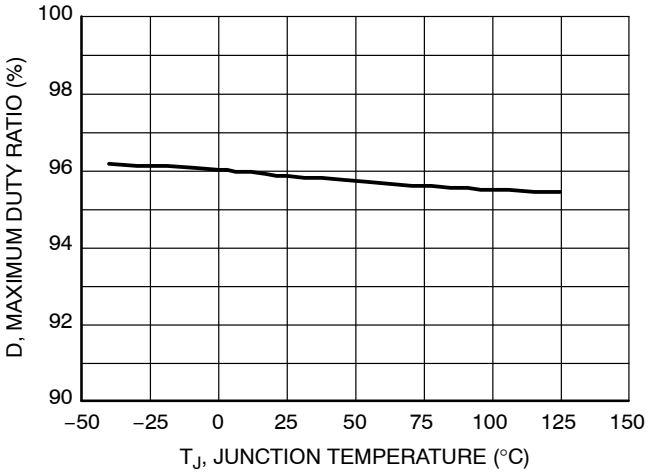


Figure 8. Maximum Duty Ratio vs. Junction Temperature

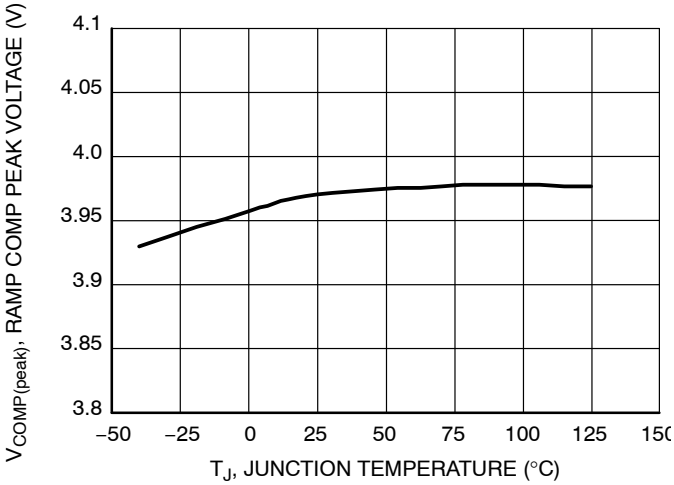


Figure 9. Ramp Compensation Peak Voltage vs. Junction Temperature

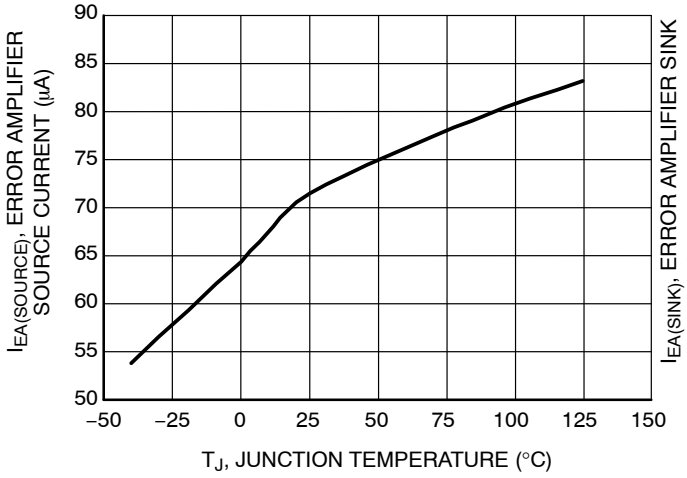


Figure 10. Error Amplifier Source Current vs. Junction Temperature

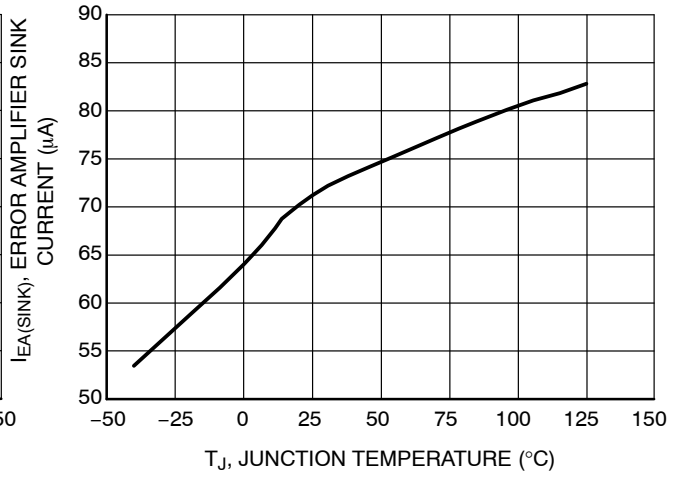


Figure 11. Error Amplifier Sink Current vs. Junction Temperature

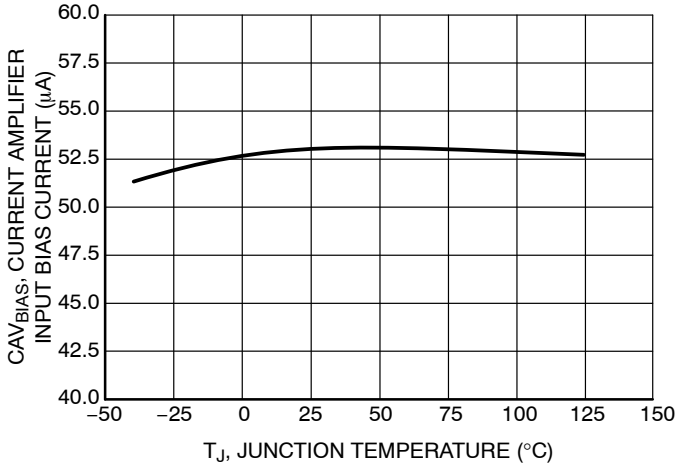


Figure 12. Current Amplifier Input Bias Current vs. Junction Temperature

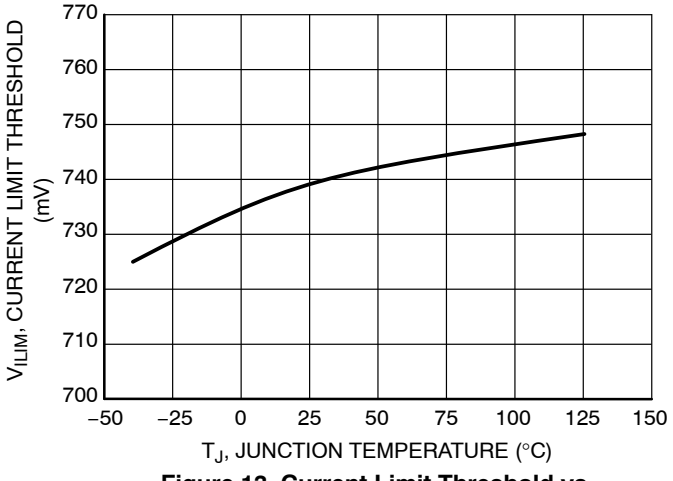


Figure 13. Current Limit Threshold vs. Junction Temperature

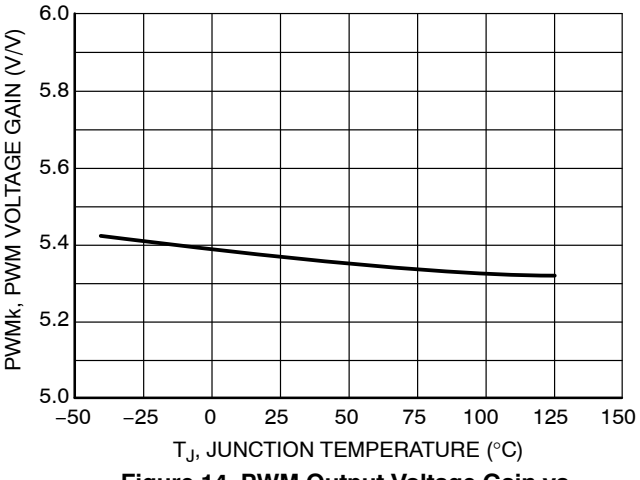


Figure 14. PWM Output Voltage Gain vs. Junction Temperature

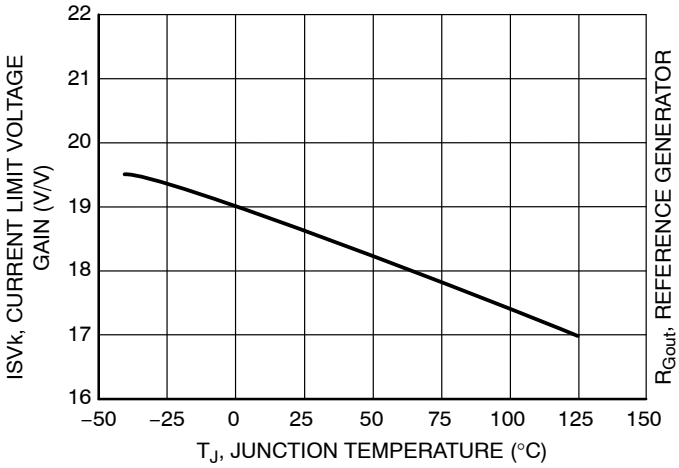


Figure 15. Oscillator CS Limit Voltage Gain vs. Junction Temperature

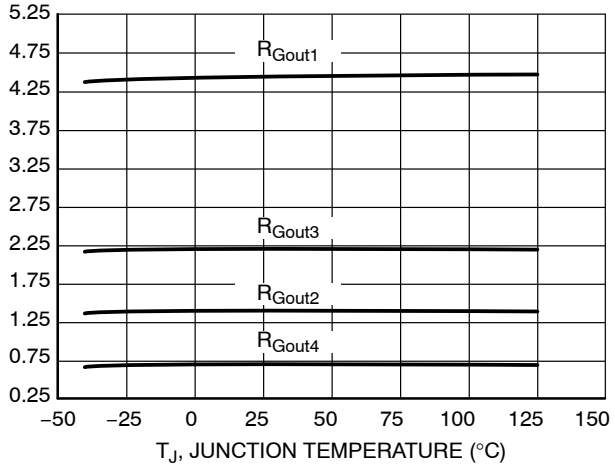


Figure 16. Oscillator Reference Generator Output Voltage vs. Junction Temperature

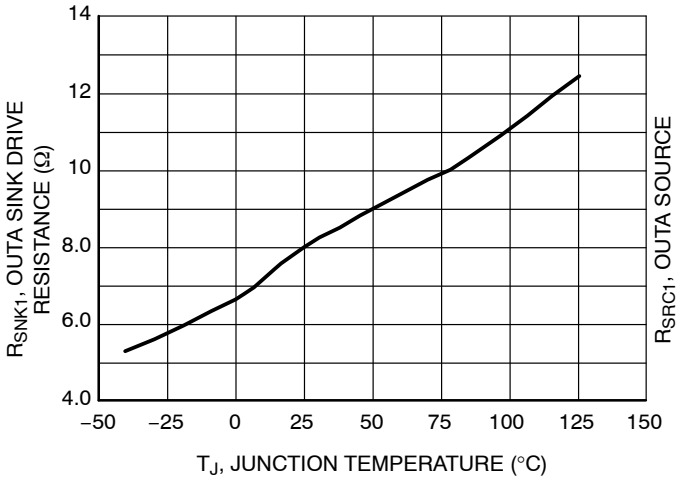


Figure 17. OUTA Sink Resistance vs. Junction Temperature

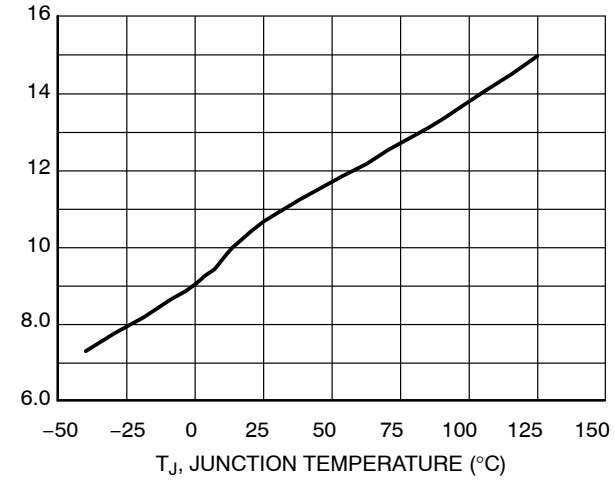


Figure 18. OUTA Source Drive Resistance vs. Junction Temperature

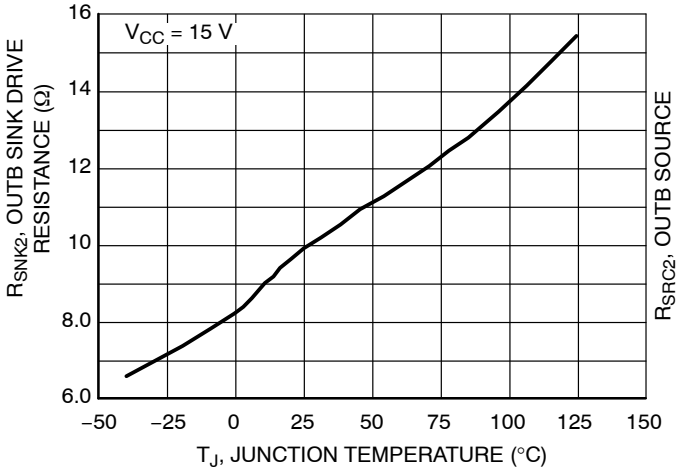


Figure 19. OUTB Sink Resistance vs. Junction Temperature

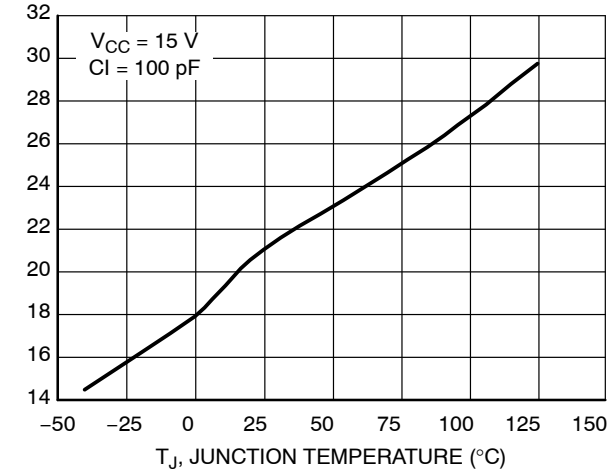


Figure 20. OUTB Source Drive Resistance vs. Junction Temperature

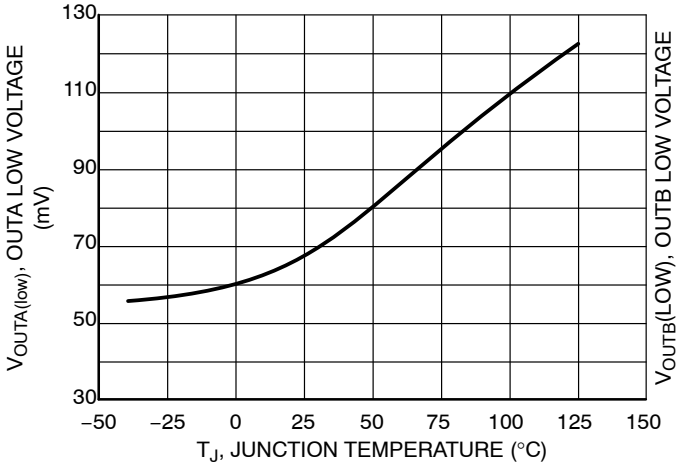


Figure 21. OUTA Low Voltage vs. Junction Temperature

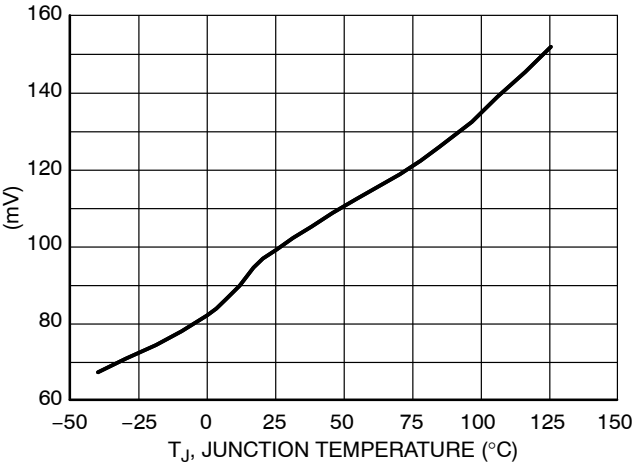


Figure 22. OUTB Low Voltage vs. Junction Temperature

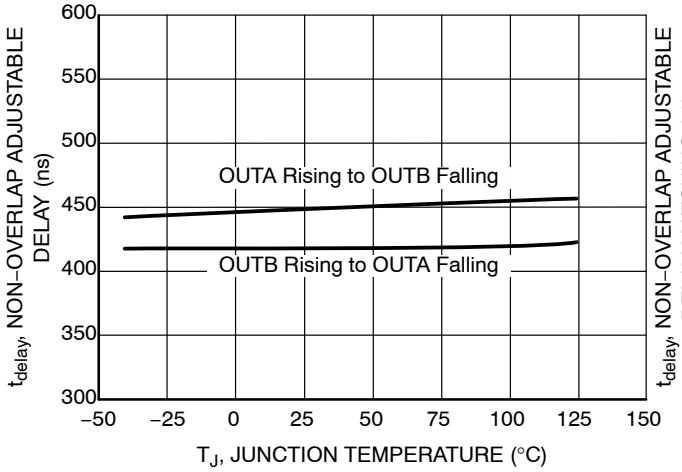


Figure 23. Non−Overlap Adjustable Delay vs. Junction Temperature

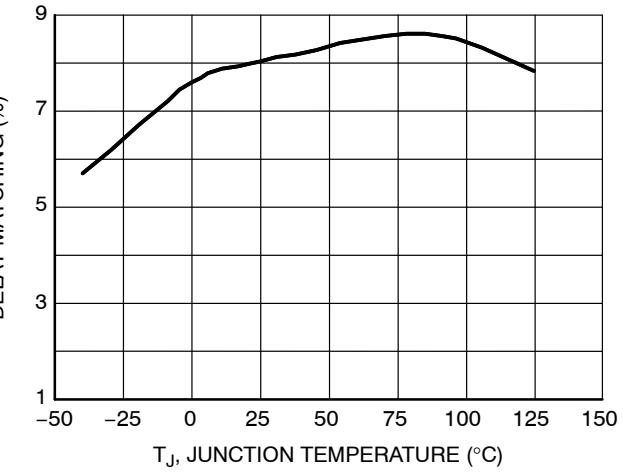


Figure 24. Non−Overlap Adjustable Delay Matching vs. Junction Temperature

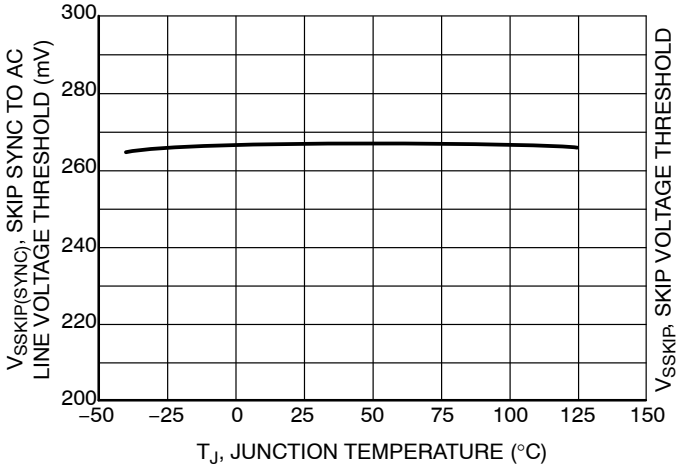


Figure 25. Skip Synchronization to ac Line Voltage Threshold vs. Junction Temperature

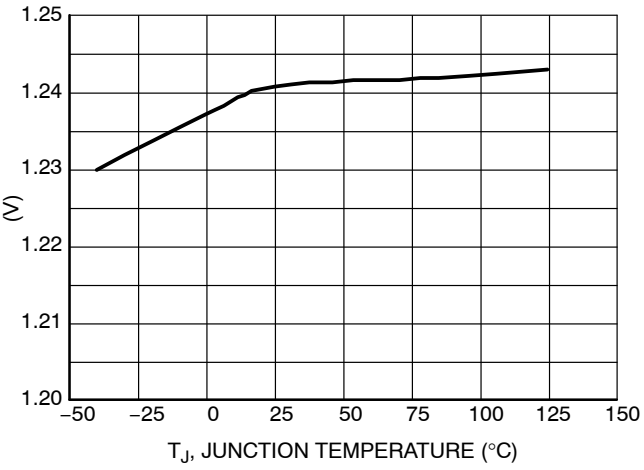


Figure 26. Skip Voltage Threshold vs. Junction Temperature

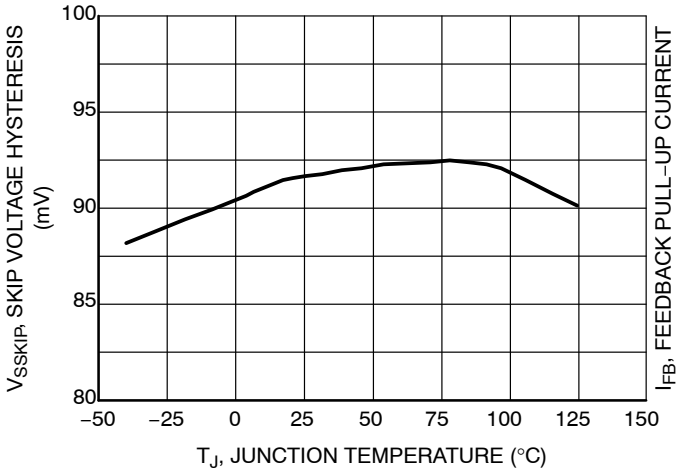


Figure 27. Skip Voltage Hysteresis vs. Junction Temperature

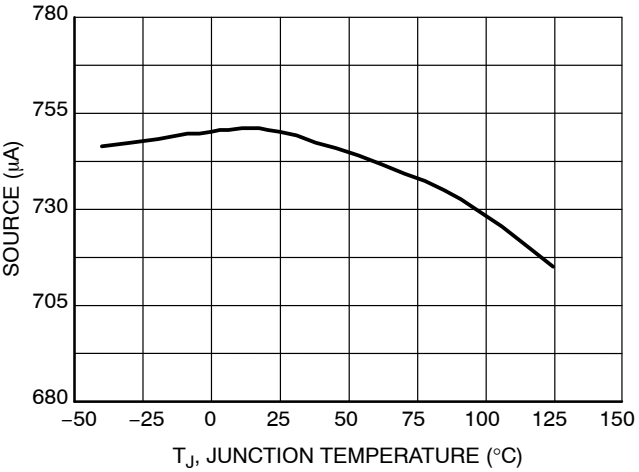


Figure 28. Feedback Pull−Up Current Source vs. Junction Temperature

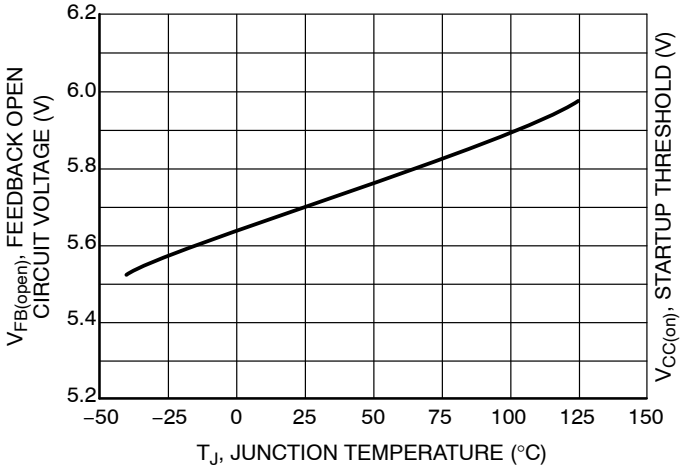


Figure 29. Feedback Open Circuit Voltage vs. Junction Temperature

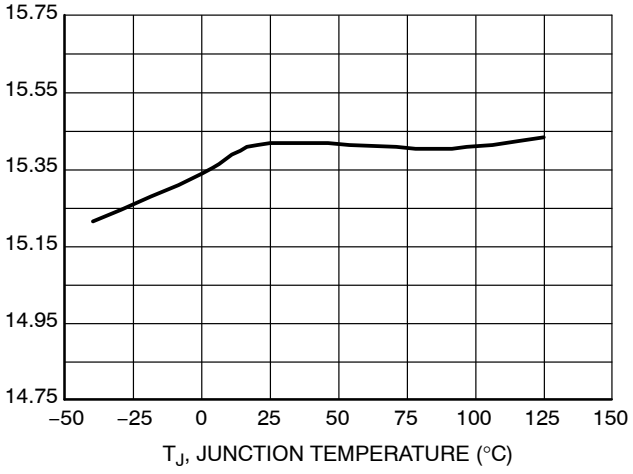


Figure 30. Startup Threshold vs. Junction Temperature

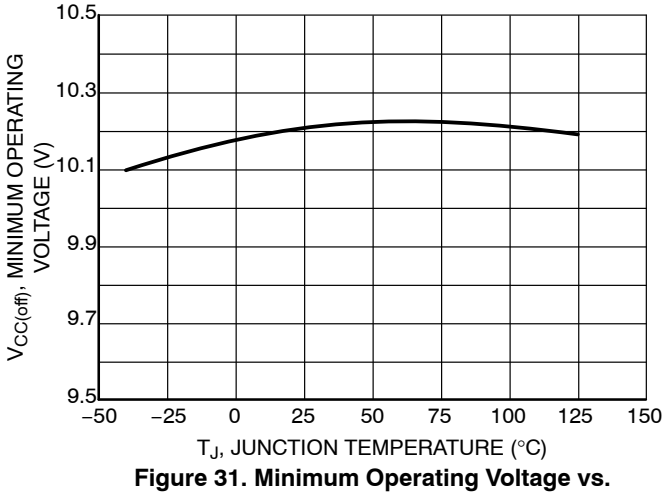


Figure 31. Minimum Operating Voltage vs. Junction Temperature

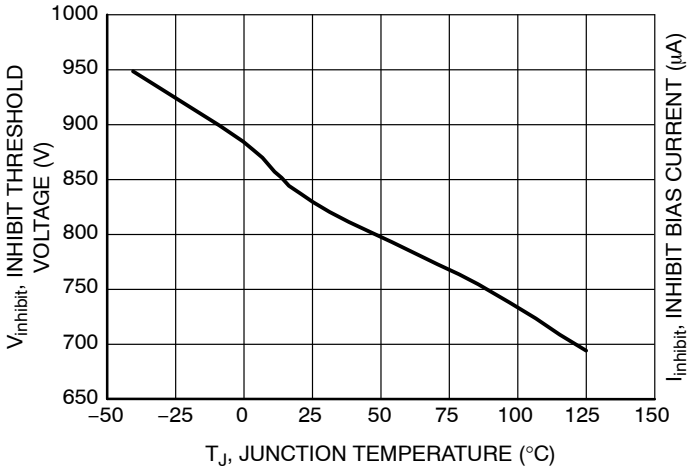


Figure 32. Inhibit Threshold Voltage vs. Junction Temperature

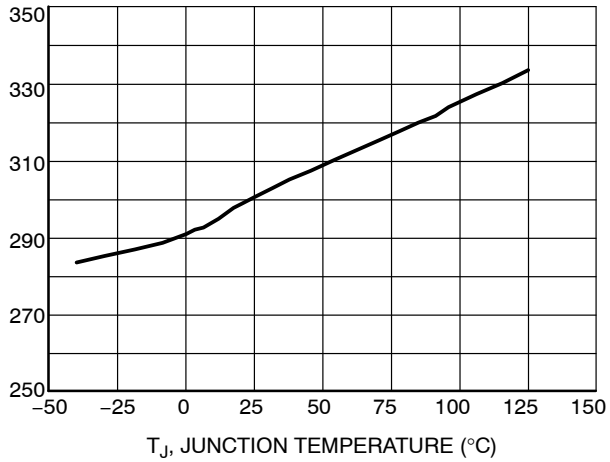


Figure 33. Inhibit Bias Current vs. Junction Temperature

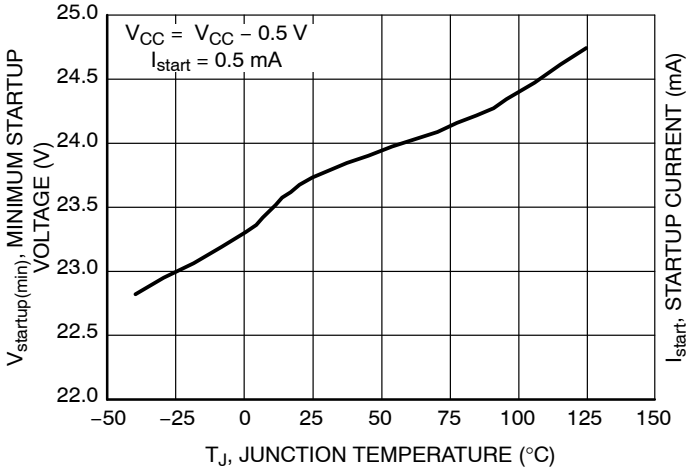


Figure 34. Minimum Startup Voltage vs. Junction Temperature

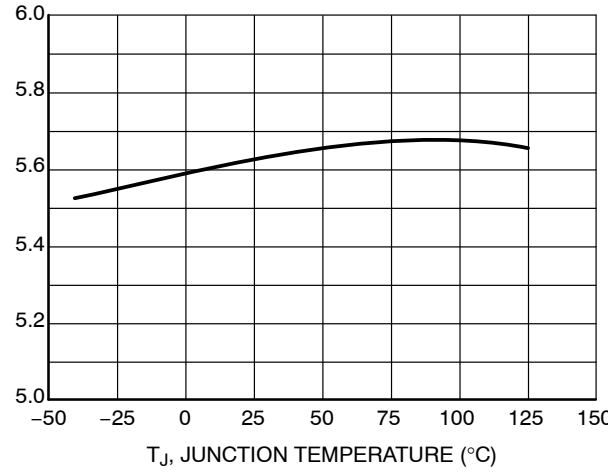


Figure 35. Startup Current vs. Junction Temperature

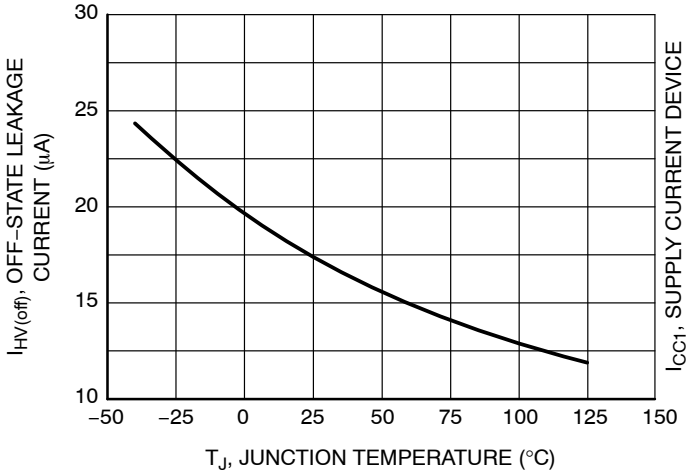


Figure 36. Off−State Leakage Current vs. Junction Temperature

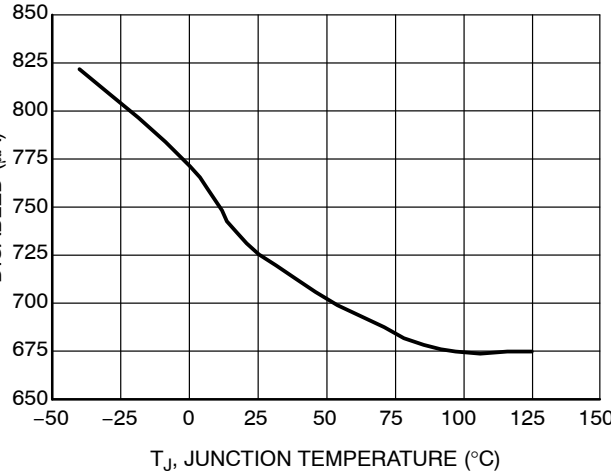


Figure 37. Supply Current Device Disabled (Overload) vs. Junction Temperature

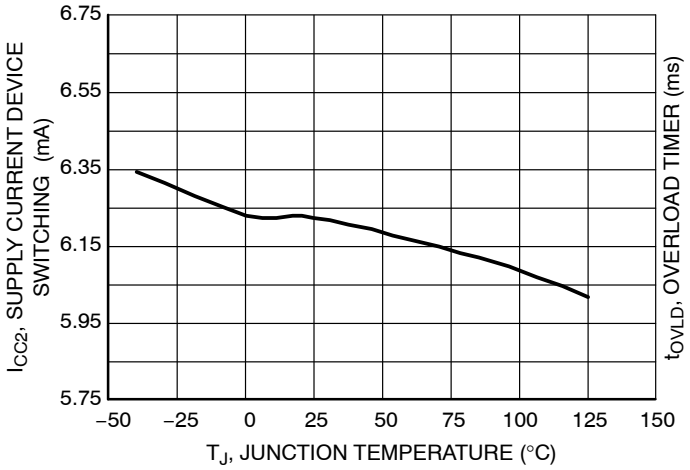


Figure 38. Supply Current Device Switching vs. Junction Temperature

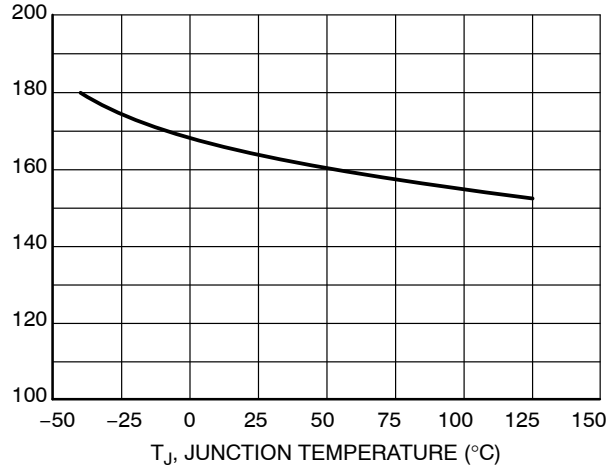


Figure 39. Overload Timer vs. Junction Temperature

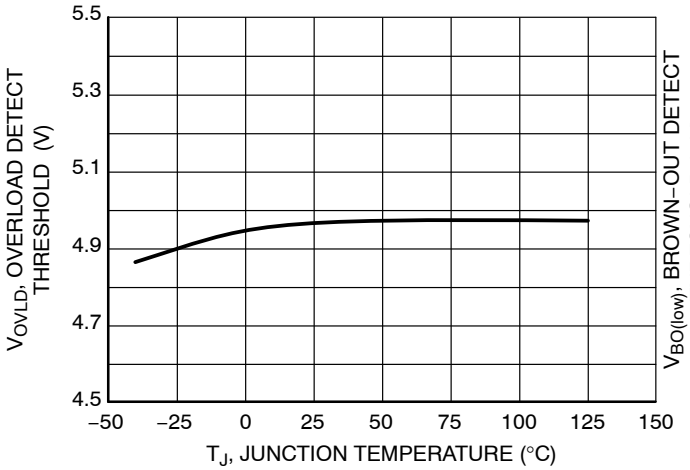


Figure 40. Overload Detect Threshold vs. Junction Temperature

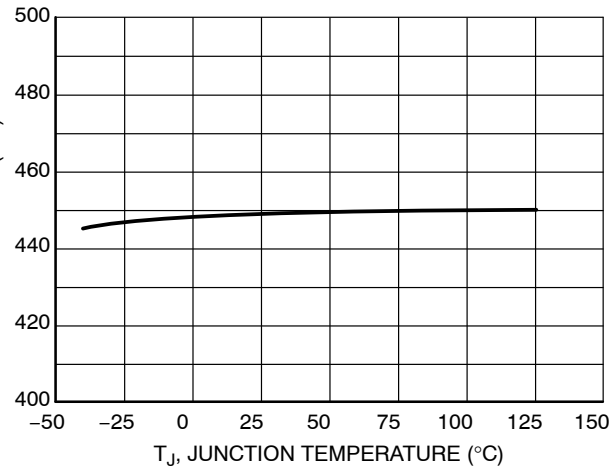


Figure 41. Brown−Out Detect Threshold vs. Junction Temperature

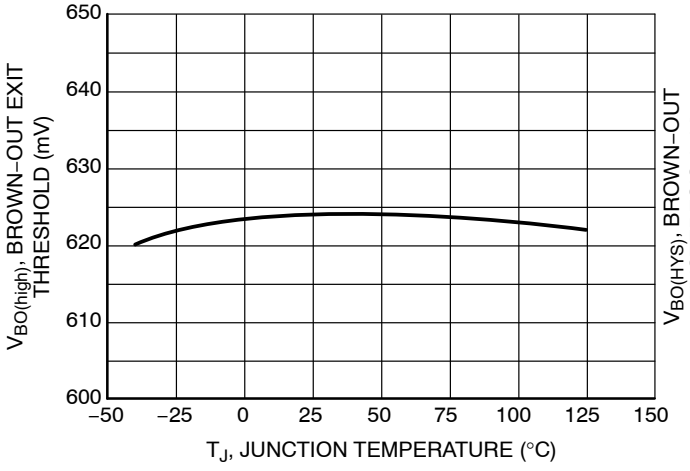


Figure 42. Brown−Out Exit Threshold vs. Junction Temperature

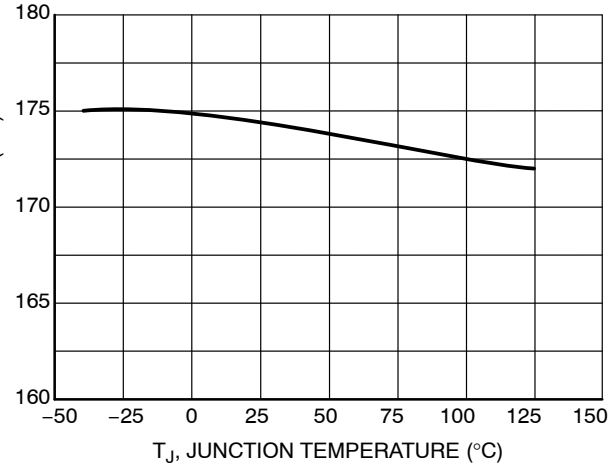


Figure 43. Brown−Out Hysteresis vs. Junction Temperature

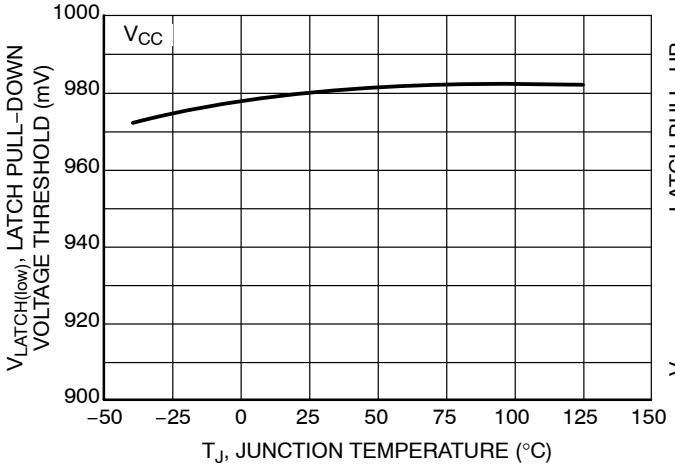


Figure 44. Latch Pull−Down Voltage Threshold vs. Junction Temperature

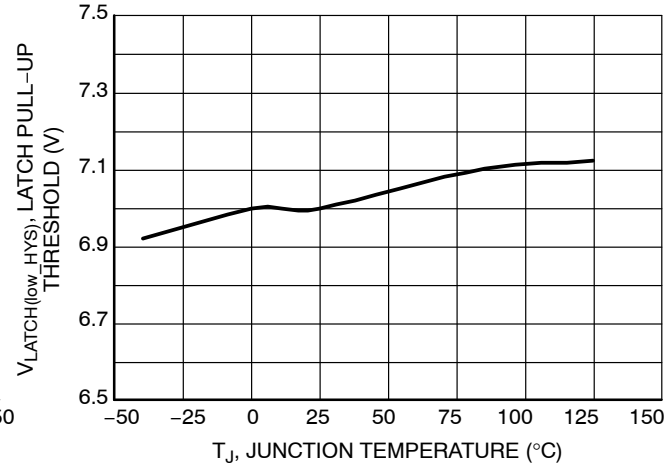


Figure 45. Latch Pull−Up Threshold vs. Junction Temperature

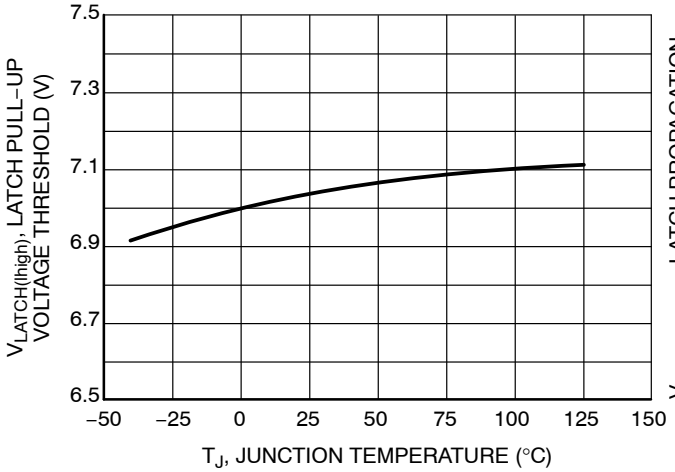


Figure 46. Latch Pull−Up Voltage Threshold vs. Junction Temperature

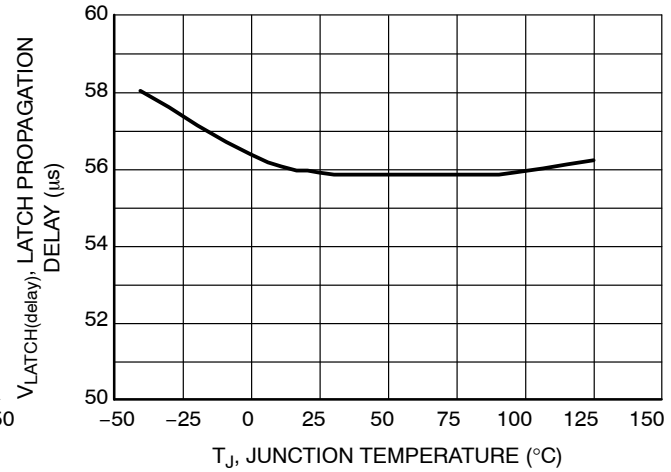


Figure 47. Latch Propagation Delay vs. Junction Temperature

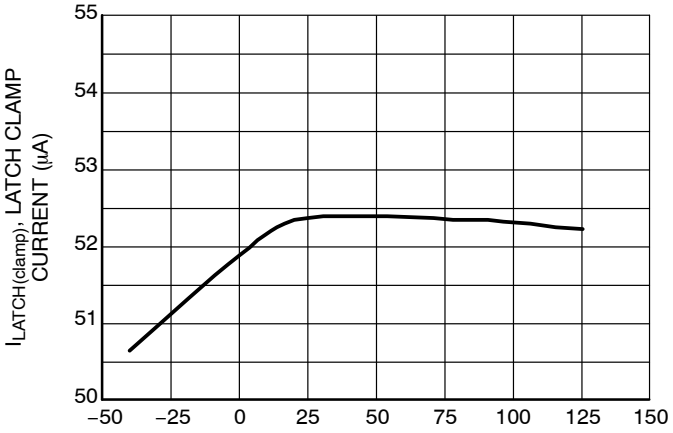


Figure 48. Latch Clamp Current vs. Junction Temperature

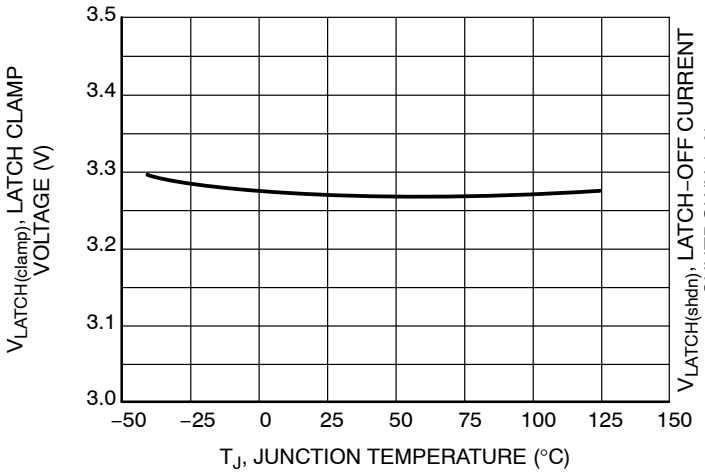


Figure 49. Latch Clamp Voltage vs. Junction Temperature

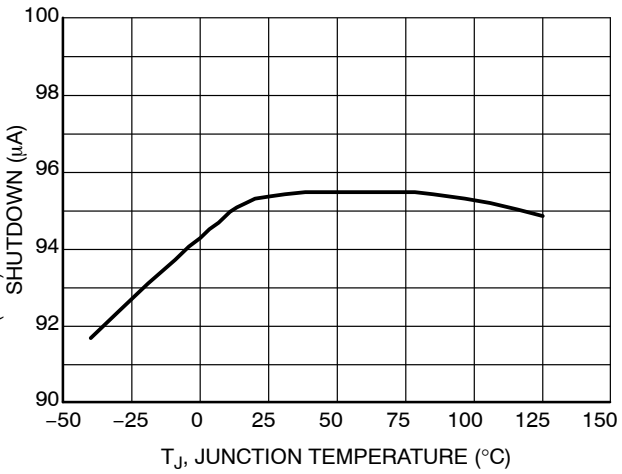


Figure 50. Latch−Off Current Shutdown vs. Junction Temperature

DETAILED DEVICE DESCRIPTION

Introduction

The NCP1652 is a highly integrated controller combining PFC and an isolated step down ac−dc power conversion in a single stage, resulting in a lower cost and reduced part count solution. This controller is ideal for notebook adapters, battery chargers and other off−line applications with power requirements between 75 W and 150 W with an output voltage greater than 12 V. The single stage is based on the flyback converter and it is designed to operate in CCM or DCM modes.

Power Factor Correction (PFC) Introduction

Power factor correction shapes the input current of off−line power supplies to maximize the real power available from the mains. Ideally, the electrical appliance should present a load that emulates a pure resistor, in which case the reactive power drawn by the device is zero. Inherent in this scenario is the freedom from input current harmonics. The current is a perfect replica of the input voltage (usually a sine wave) and is exactly in phase with it. In this case the current drawn from the mains is at a minimum for the real power required to perform the needed work, and this minimizes losses and costs associated not only with the distribution of the power, but also with the generation of the power and the capital equipment involved in the process. The freedom from harmonics also minimizes interference with other devices being powered from the same source.

Another reason to employ PFC in many of today's power supplies is to comply with regulatory requirements. Today, electrical equipment in Europe must comply with the European Norm EN61000−3−2. This requirement applies to most electrical appliances with input power of 75 W or greater, and it specifies the maximum amplitude of line−frequency harmonics up to and including the 39th harmonic. While this requirement is not yet in place in the US, power supply manufacturers attempting to sell products worldwide are designing for compliance with this requirement.

Typical Power Supply with PFC

A typical power supply consists of a boost PFC preregulator creating an intermediate ~400 V bus and an isolated dc−dc converter producing the desired output voltage as shown in Figure 51. This architecture has two power stages.

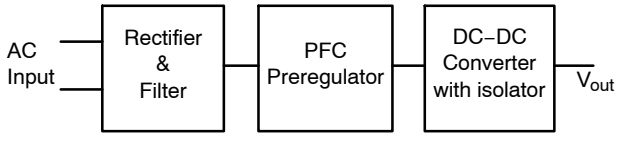


Figure 51. Typical Two Stage Power Converter

A two stage architecture allows optimization of each individual power stage. It is commonly used because of designer familiarity and a vast range of available components. But, because it processes the power twice, the search is always on for a more compact and power efficient solution.

The NCP1652 controller offers the convenience of shrinking the front−end converter (PFC preregulator) and the dc−dc converter into a single power processing stage as shown in Figure 52.

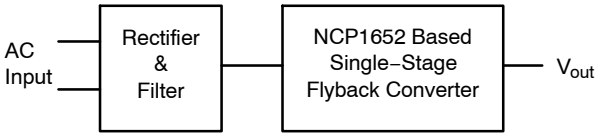


Figure 52. Single Stage Power Converter

This approach significantly reduces the component count. The NCP1652 based solution requires only one each of MOSFET, magnetic element, output rectifier (low voltage) and output capacitor (low voltage). In contrast, the 2−stage solution requires two or more of the above−listed components. Elimination of certain high−voltage components (e.g. high voltage capacitor and high voltage PFC diode) has significant impact on the system design. The resultant cost savings and reliability improvement are often worth the effort of designing a new converter.

Single PFC Stage

While the single stage offers certain benefits, it is important to recognize that it is not a recommended solution for all requirements. The following three limitations apply to the single stage approach:

- The output voltage ripple will have a 2x line frequency component (120 Hz for North American applications) that can not be eliminated easily. The cause of this ripple is the elimination of the energy storage element that is typically the boost output capacitor in the 2−stage solution. The only way to reduce the ripple is to increase the output filter capacitance. The required value of capacitance is inversely proportional to the output voltage – hence this approach is not recommended for low voltage outputs such as 3.3 V or 5 V. However, if there is a follow−on dc−dc converter stage or a battery after the single stage converter, the low frequency ripple should not cause any concerns.
- The hold−up time will not be as good as the 2−stage approach – again due to the lack of an intermediate energy storage element.
- In a single stage converter, one FET processes all the power – that is both a benefit and a limitation as the stress on that main MOSFET is relatively higher. Similarly, the magnetic component (flyback transformer/inductor) can not be optimized as well as in

the 2−stage solution. As a result, potentially higher leakage inductance induces higher voltage spikes (like the one shown in Figure 53) on the MOSFET drain. This may require a MOSFET with a higher voltage rating compared to similar dc−input flyback applications.

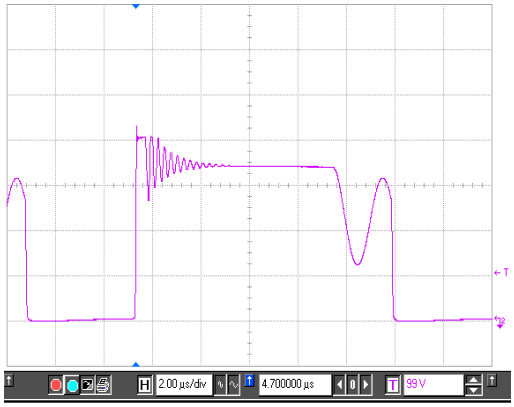


Figure 53. Typical Drain Voltage Waveform of a Flyback Main Switch

There are a few methods to clamp the voltage spike on the main switch, a resistor−capacitor−diode (RCD) clamp, a transient voltage suppressor (TVS) or an active clamp using a MOSFET and capacitor can be used as shown in Figures 54 to 56.

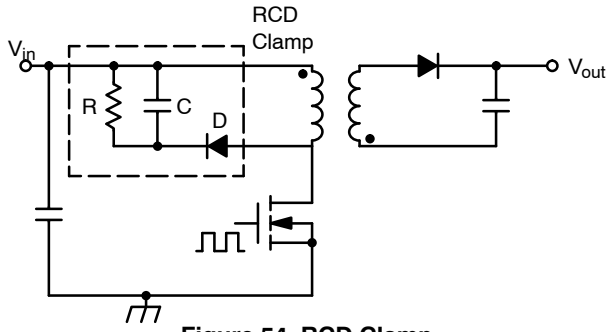


Figure 54. RCD Clamp

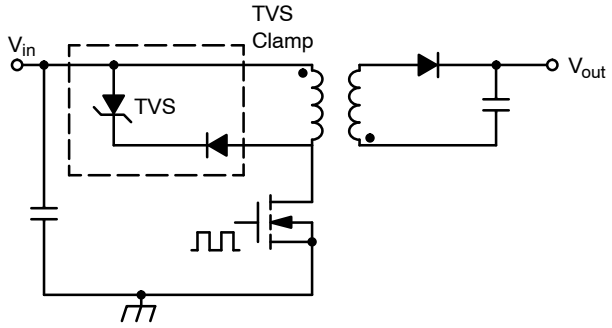


Figure 55. TVS Clamp

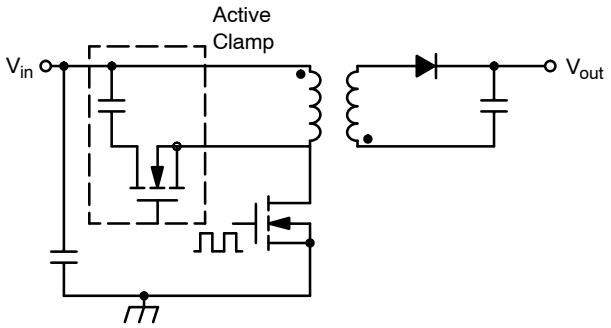


Figure 56. Active Clamp

The first two methods result in dissipation of the leakage energy in the clamping circuits – the dissipation is proportional to LI^2 where L is the leakage inductance of the transformer and I is the peak of the switch current at turn−off. An RDC snubber is simple and has the lowest cost, but constantly dissipates power. A TVS provides good voltage clamping at a slightly higher cost and dissipates power only when the drain voltage exceeds the voltage rating of the TVS.

The active clamp circuit provides an intriguing alternative to the other methods. It requires addition of a MOSFET and a high voltage capacitor as part of the active clamp circuit, thus adding complexity, but it results in a complete reuse of the leakage inductance energy. As a result, the transformer construction is no longer critical and one can use cheaper cost solution. Also, the active clamp circuit reduces the voltage stress on the primary switch and that can lead to usage of lower cost or lower on resistance ($R_{DS(on)}$) MOSFET. Finally, the turn−on switching losses are eliminated because the active clamp circuit allows the discharge of the MOSFET C_{OSS} capacitance prior to the turn−on. The energy stored in the leakage inductance is utilized for this transition.

In many applications, the added complexity of the active clamp circuit may not be justified. However, the OUTB of the NCP1652 is also usable for another purpose, synchronous rectification control. Synchronous rectification for flyback converters is an emerging requirement for flyback converters. The OUTB signal from NCP1652 is ideal for interfacing with a secondary side synchronous rectifier controller such as NCP4303 as shown in Figure 57. As shown in Figure 57, using the OUTB (coupled through pulse transformer or Y−capacitor) as a trigger for the NCP4303 allows guaranteed turn−off of the secondary side synchronous MOSFET prior to turn−on of the primary switch. In any CCM flyback converter, this is a critical requirement to prevent cross−conduction and NCP1652 and NCP4303 combination is the first such chipset that guarantees the operation without cross−conduction.

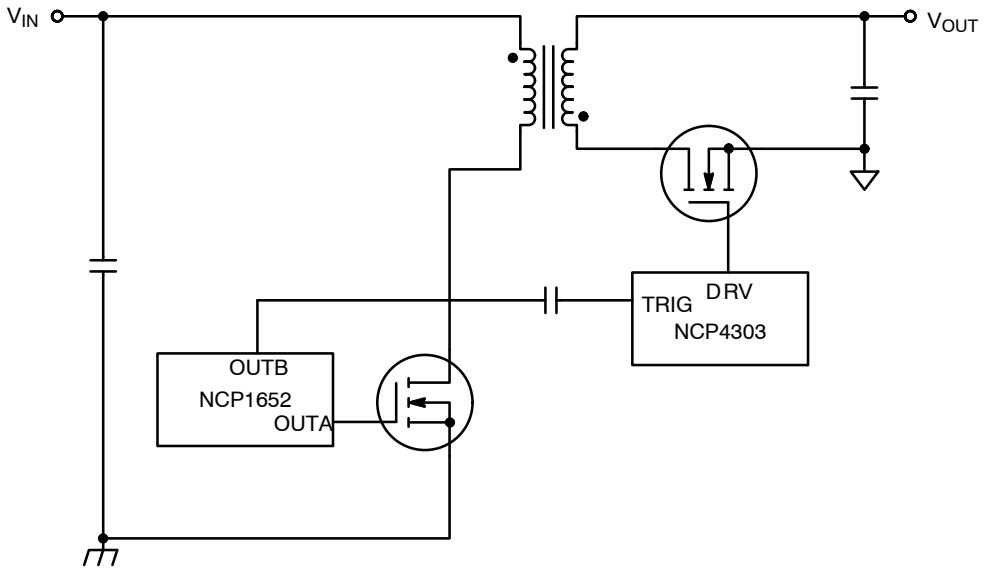


Figure 57. NCP1652 and NCP4302 based single stage PFC with synchronous rectification.

The NCP1652 incorporates a secondary driver, OUTB, with adjustable non overlap delay for controlling a synchronous rectifier switch in the secondary side, an active clamp switch in the primary or both. In addition, the controller features a proprietary Soft−Skip™ to reduce acoustic noise at light loads. Other features found in the NCP1652 include a high voltage startup circuit, voltage feedforward, brown out detector, internal overload timer, latch input and a high accuracy multiplier.

NCP1652 PFC Loop

The NCP1652 incorporates a modified version of average current mode control used for achieving the unity power factor. The PFC section includes a variable reference generator, a low frequency voltage regulation error amplifier (AC error AMP), ramp compensation (Ramp Comp) and current shaping network. These blocks are shown in the lower portion of the bock diagram (Figure 51).

The inputs to the reference generator include feedback signal (FB), scaled AC input signal (AC_IN) and feedforward input (V_{FF}). The output of the reference generator is a rectified version of the input sine−wave scaled by the FB and V_{FF} values. The reference amplitude is proportional to the FB and inversely proportional to the square of the V_{FF}. This, for higher load levels and/or lower input voltage, the signal would be higher.

The function of the AC error amp is to force the average current output of the current sense amplifier to match the reference generator output. The output of the AC error amplifier is compensated to prevent response to fast events. This output (V_{error}) is fed into the PWM comparator through a reference buffer. The PWM comparator sums the V_{error} and the instantaneous current and compares it to a 4.0 V threshold to provide the desired duty cycle control. Ramp compensation is also added to the input signal to allow CCM operation above 50% duty cycle.

High Voltage Startup Circuit

The NCP1652 internal high voltage startup circuit eliminates the need for external startup components and provides a faster startup time compared to an external startup resistor. The startup circuit consists of a constant current source that supplies current from the HV pin to the supply capacitor on the V_{CC} pin (C_{CC}). The startup current (I_{start}) is typically 5.5 mA.

The OUTA and OUTB drivers are enabled and the startup current source is disabled once the V_{CC} voltage reaches $V_{CC(on)}$, typically 15.3 V. The controller is then biased by the V_{CC} capacitor. The drivers are disabled if V_{CC} decays to its minimum operating threshold ($V_{CC(off)}$) typically 10.3 V. Upon reaching $V_{CC(off)}$ the gate drivers are disabled. The V_{CC} capacitor should be sized such V_{CC} is kept above $V_{CC(off)}$ while the auxiliary voltage is building up. Otherwise, the system will not start.

The controller operates in double hiccup mode while in overload or $V_{CC(off)}$. A double hiccup fault disables the drivers, sets the controller in a low current mode and allows V_{CC} to discharge to $V_{CC(off)}$. This cycle is repeated twice to minimize power dissipation in external components during a fault event. Figure 58 shows double hiccup mode operation. A soft−start sequence is initiated the second time V_{CC} reaches $V_{CC(on)}$. If the controller is latched upon reaching $V_{CC(on)}$, the controller stays in hiccup mode. During this mode, V_{CC} never drops below $V_{CC(reset)}$, the controller logic reset level. This prevents latched faults to be cleared unless power to the controller is completely removed (i.e. unplugging the supply from the AC line).

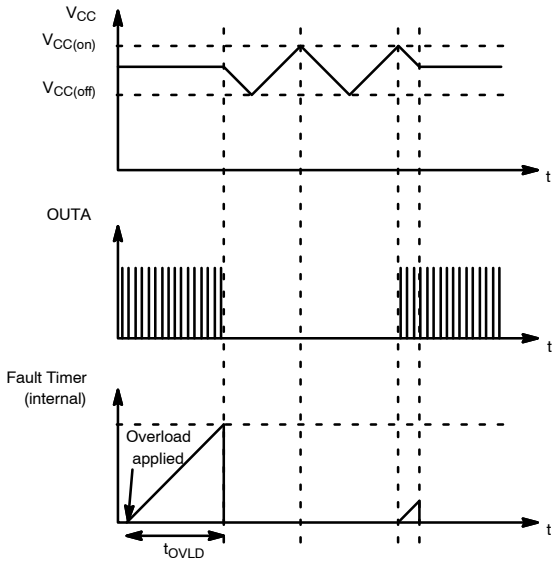


Figure 58. V_{CC} Double Hiccup Operation with a Fault Occurring while the Startup Circuit is Disabled

An internal supervisory circuit monitors the V_{CC} voltage to prevent the controller from dissipating excessive power if the V_{CC} pin is accidentally grounded. A lower level current source ($I_{inhibit}$) charges C_{CC} from 0 V to $V_{inhibit}$, typically 0.85 V. Once V_{CC} exceeds $V_{inhibit}$, the startup current source is enabled. This behavior is illustrated in Figure 59. This slightly increases the total time to charge V_{CC}, but it is generally not noticeable.

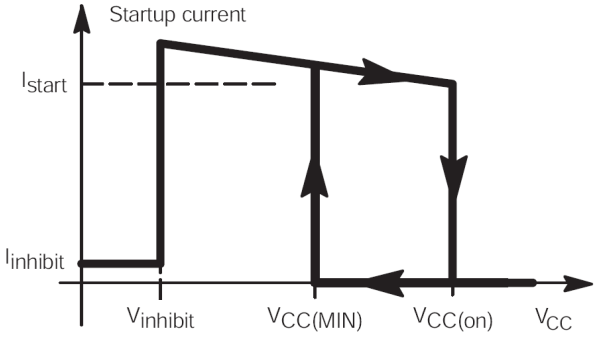


Figure 59. Startup Current at Various V_{CC} Levels

The rectified ac line voltage is provided to the power stage to achieve accurate PFC. Filtering the rectified ac line voltage with a large bulk capacitor distorts the PFC in a single stage PFC converter. A peak charger is needed to bias the HV pin as shown in Figure 60. Otherwise, the HV pin follows the ac line and the startup circuit is disabled every time the ac line voltage approaches 0 V. The V_{CC} capacitor is sized to bias the controller during power up.

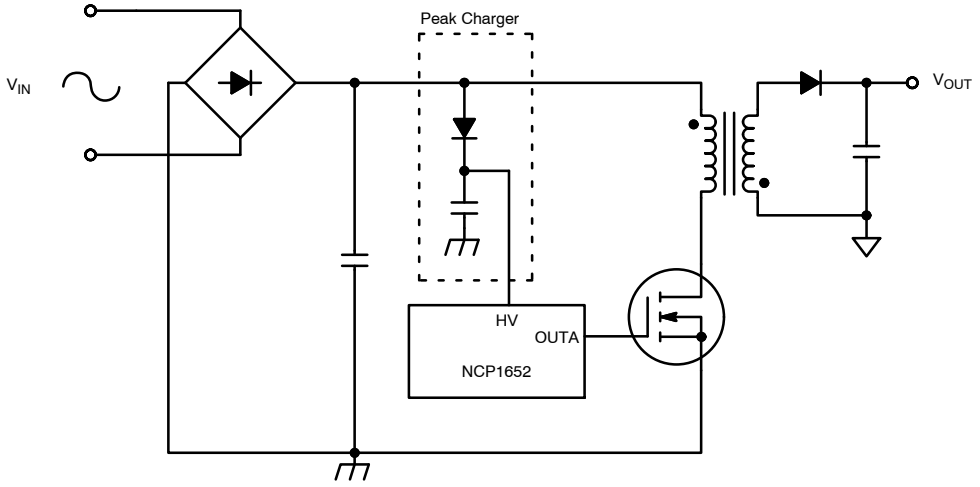


Figure 60. Peak charger

The startup circuit is rated at a maximum voltage of 500 V. Power dissipation should be controlled to avoid exceeding the maximum power dissipation of the controller. If dissipation on the controller is excessive, a resistor can be placed in series with the HV pin. This will reduce power dissipation on the controller and transfer it to the series resistor.

Drive Outputs

The NCP1652 has out off phase output drivers with an adjustable non−overlap delay (t_D). The main output, OUTA, drives the primary MOSFET. The secondary output, OUTB, is designed to provide a logic signal used to control a synchronous rectification switch in the secondary side, an active clamp switch in the primary or both. The outputs are biased directly from V_{CC} and their high state voltage is approximately V_{CC}.

OUTA has a source resistance of 13 Ω (typical) and a sink resistance of 8.0 Ω (typical) OUTB has a source resistance 22 Ω (typical) and a sink resistance of 10 Ω (typical). OUTB is a purposely sized smaller than OUTA because the gate charge of an active switch or logic used with synchronous rectification is usually less than that of the primary MOSFET. If a higher drive capability is required, an external discrete driver can be used.

The drivers are enabled once V_{CC} reaches $V_{CC(on)}$ and there are no faults present. They are disabled once V_{CC} discharges to $V_{CC(off)}$. OUTB is always the last pulse generated when the outputs are disabled due to a fault (latch−off, $V_{CC(off)}$, overload, or brown−out). The last pulse terminates at the end of the clock cycle. This ensures the active clamp capacitor is reset.

The high current drive capability of OUTA and OUTB may generate voltage spikes during switch transitions due to parasitic board inductance. Shortening the connection length between the drivers and their loads and using wider connections will reduce inductance−induce spikes.

Adjustable Dead Time

OUTA and OUTB have an adjustable dead time between transitions to prevent simultaneous conduction of the main and synchronous rectifier or active clamp MOSFETs. The delay is also used to optimize the turn−off transition of the active clamp switch to achieve zero−volt switching of the main switch in an active clamp topology. Figure 61 shows the timing relationship between OUTA and OUTB.

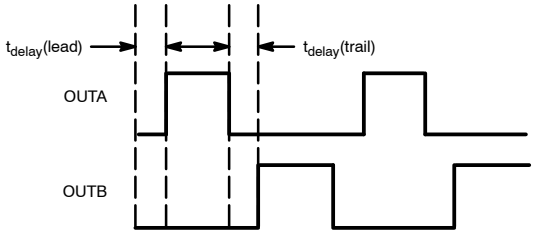


Figure 61. Timing relationship between OUTA and OUTB.

The dead time between OUTA and OUTB is adjusted by connecting a resistor, R_D, from the R_D pin to ground. The overlap delay is proportional to R_D. The delay time can be set between 80 ns and 1.8 μs using the formula:

$$t_{delay}(\text{in ns}) = 8.0 \times R_{delay}(\text{in k}\Omega) \text{ with}$$

$$R_{delay} \text{ varying between 10 k}\Omega \text{ and 230 k}\Omega$$

AC Error Amplifier and Buffer

The AC error amplifier (EA) shapes the input current into a high quality sine wave by forcing the filtered input current to follow the output of the reference generator. The output of the reference generator is a full wave rectified ac signal and it is applied to the non inverting input of the EA. The filtered input current, I_{in}, is the current sense signal at the

ISpos pin multiplied by the current sense amplifier gain. It is applied to the inverting input of the AC EA.

The AC EA is a transconductance amplifier. A transconductance amplifier generates an output current proportional to its differential input voltage. This amplifier has a nominal gain of 100 μS (or 0.0001 A/V). That is, an input voltage difference of 10 mV causes the output current to change by 1.0 μA. The AC EA has typical source and sink currents of 70 μA.

The filtered input current is a high frequency signal. A low frequency pole forces the average input current to follow the reference generator output. A pole-zero pair is created by placing a (R_{COMP}) and capacitor (C_{COMP}) series combination at the output of the AC EA. The AC COMP pin provides access to the AC EA output.

The output of the AC EA is inverted and converted into a current using a second transconductance amplifier. The output of the inverting transconductance amplifier is $V_{ACEA(buffer)}$. Figure 62 shows the circuit schematic of the AC EA buffer. The AC EA buffer output current, $I_{ACEA(out)}$, is given by Equation 1.

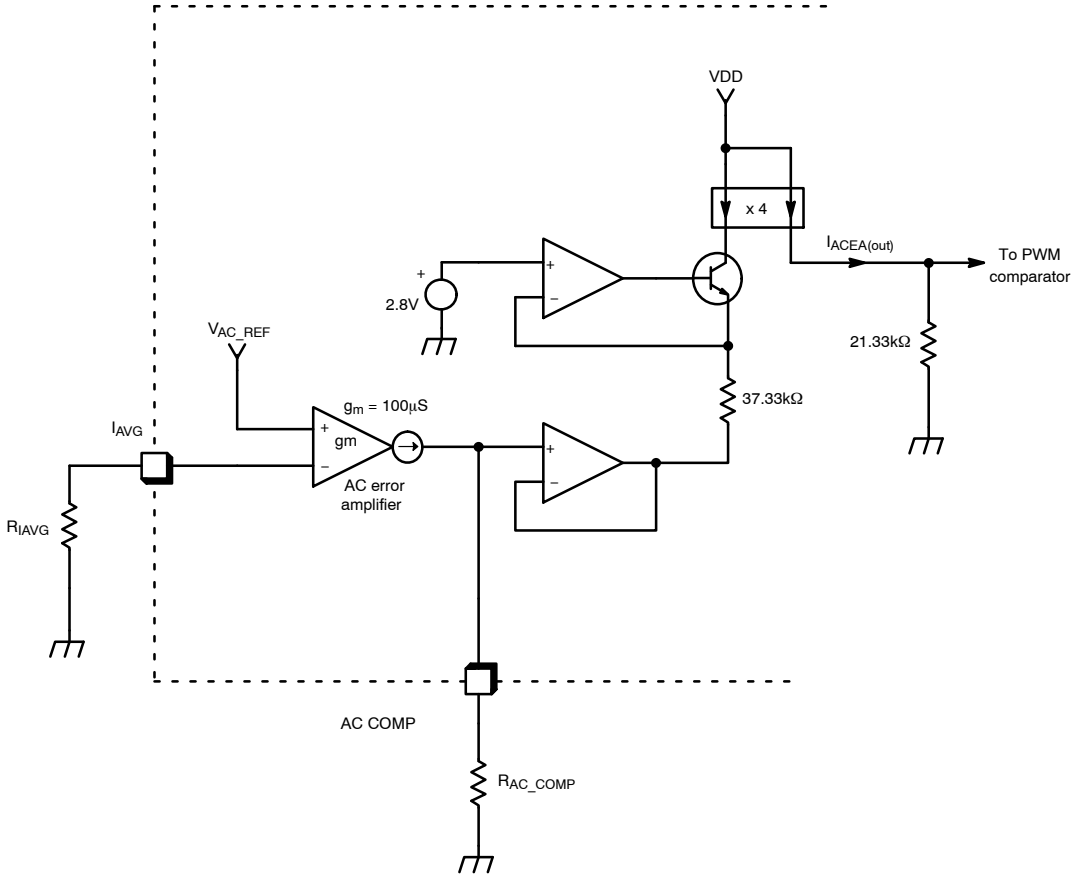


Figure 62. AC EA Buffer Amplifier

$$I_{ACEA(out)} = \left(\frac{2.8 - V_{ACEA}}{37.33k}\right) \cdot 4 \qquad \text{(eq. 1)}$$

The voltage at the PWN non-inverting input is determined by $I_{ACEA(out)}$, the instantaneous switch current along and the ramp compensation current. OUTA is terminated once the voltage at the PWM non-inverting input reaches 4 V.

Current Sense Amplifier

A voltage proportional to the main switch current is applied to the current sense input, IS_{POS}. The current sense amplifier is a wide bandwidth amplifier with a differential input. The current sense amplifier has two outputs, PWM Output and I_{AVG} Output. The PWM Output is the instantaneous switch current which is filtered by the internal leading edge blanking (LEB) circuitry prior to applying it to the PWM Comparator non inverting input. The second output is a filtered current signal resembling the average value of the input current. Figure 63 shows the internal architecture of the current sense amplifier.

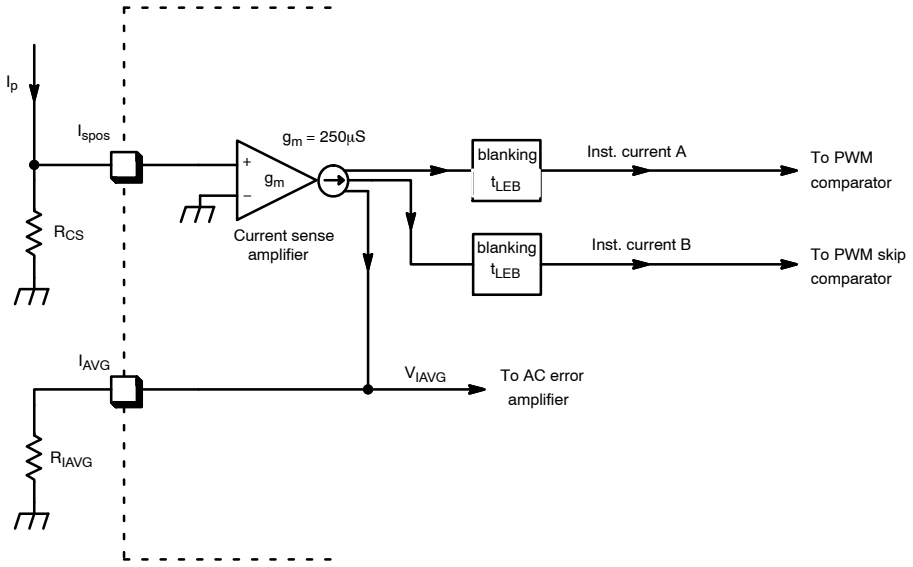


Figure 63. Current Sense Amplifier

Caution should be exercised when designing a filter between the current sense resistor and the IS_{POS} input, due to the low impedance of this amplifier. Any series resistance due to a filter creates a voltage offset (V_{OS}) due to its input bias current, CA_{Ibias}. The input bias current is typically 60 μA. The voltage offset is given by Equation 2.

$$V_{OS} = CA_{Ibias} \cdot R_{external} \quad \text{(eq. 2)}$$

The offset adds a positive offset to the current sense signal. The ac error amplifier will then try to compensate for the average output current which appears never to go to zero and cause additional zero crossing distortion.

A voltage proportional to the main switch current is applied to the IS_{POS} pin. The IS_{POS} pin voltage is converted into a current, i_1, and internally mirrored. Two internal currents are generated, I_{CS} and I_{AVG}. I_{CS} is a high frequency signal which is a replica of the instantaneous switch current. I_{AVG} is a low frequency signal. The relationship between V_{ISPOS} and I_{CS} and I_{AVG} is given by Equation 3.

$$I_{CS} = I_{IN} = \frac{V_{ISPOS}}{4k} \quad \text{(eq. 3)}$$

The PWM Output delivers current to the positive input of the PWM input where it is added to the AC EA and ramp compensation signal.

The I_{AVG} Output generates a voltage signal to a buffer amplifier. This voltage signal is the product of I_{AVG} and an external R_{IAVG} resistor filtered by the capacitor on the I_{AVG} pin, C_{IAVG}. The pole frequency, f_P, set by C_{IAVG} should be significantly below the switching frequency to remove the high frequency content. But, high enough to not to cause significant distortion to the input full wave rectified sinewave waveform. A properly filtered average current signal has twice the line frequency. Equation 4 shows the relationship between C_{IAVG} (in nF) and f_P (in kHz).

$$C_{IAVG} = \frac{1}{2 \cdot \pi \cdot R_{IAVG} \cdot f_P} \quad \text{(eq. 4)}$$