Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

NCP3101C

Wide Input Voltage Synchronous Buck Converter

The NCP3101C is a high efficiency, 6 A DC−DC buck converter designed to operate from a 5 V to 12 V supply. The device is capable of producing an output voltage as low as 0.8 V. The NCP3101C can continuously output 6 A through MOSFET switches driven by an internally set 275 kHz oscillator. The 40−pin device provides an optimal level of integration to reduce size and cost of the power supply. The NCP3101C also incorporates an externally compensated transconductance error amplifier and a capacitor programmable soft−start function. Protection features include programmable short circuit protection and input under voltage lockout (UVLO). The NCP3101C is available in a 40−pin QFN package.

Features

- Split Power Rail 2.7 V to 18 V on PWRVCC
- 275 kHz Internal Oscillator
- Greater Than 90% Max Efficiency
- Boost Pin Operates to 35 V
- Voltage Mode PWM Control
- 0.8 V ±1% Internal Reference Voltage
- Adjustable Output Voltage
- Capacitor Programmable Soft−Start
- 85% Max Duty Cycle
- Input Undervoltage Lockout
- Resistor Programmable Current Limit
- These are Pb−Free Devices

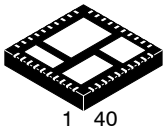
Applications

- Servers / Networking
- DSP and FPGA Power Supply
- DC−DC Regulator Modules

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM



QFN40, 6x6
CASE 485AK

NCP3101C
AWLYYWWG

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 24 of this data sheet.

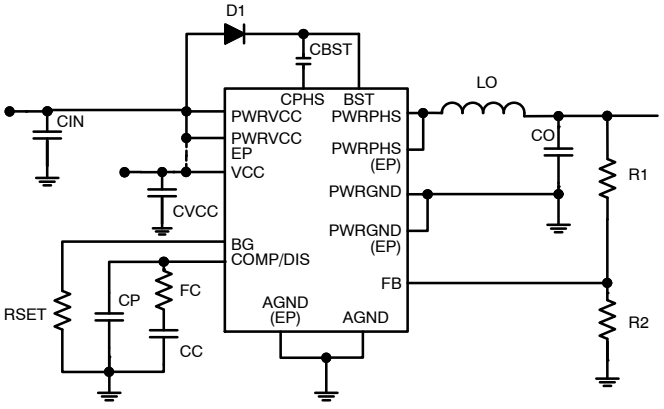


Figure 1. Typical Application Diagram

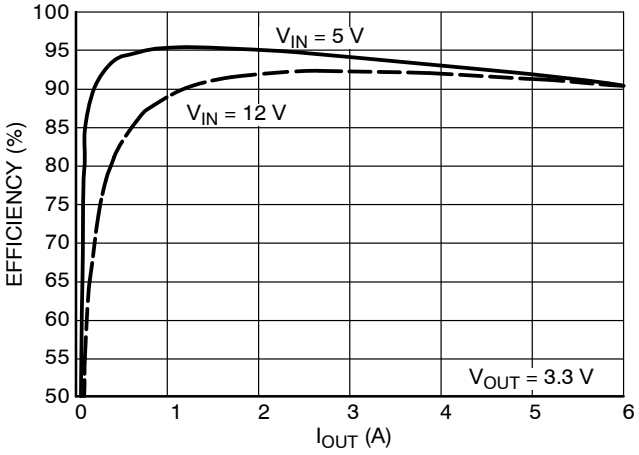


Figure 2. Efficiency

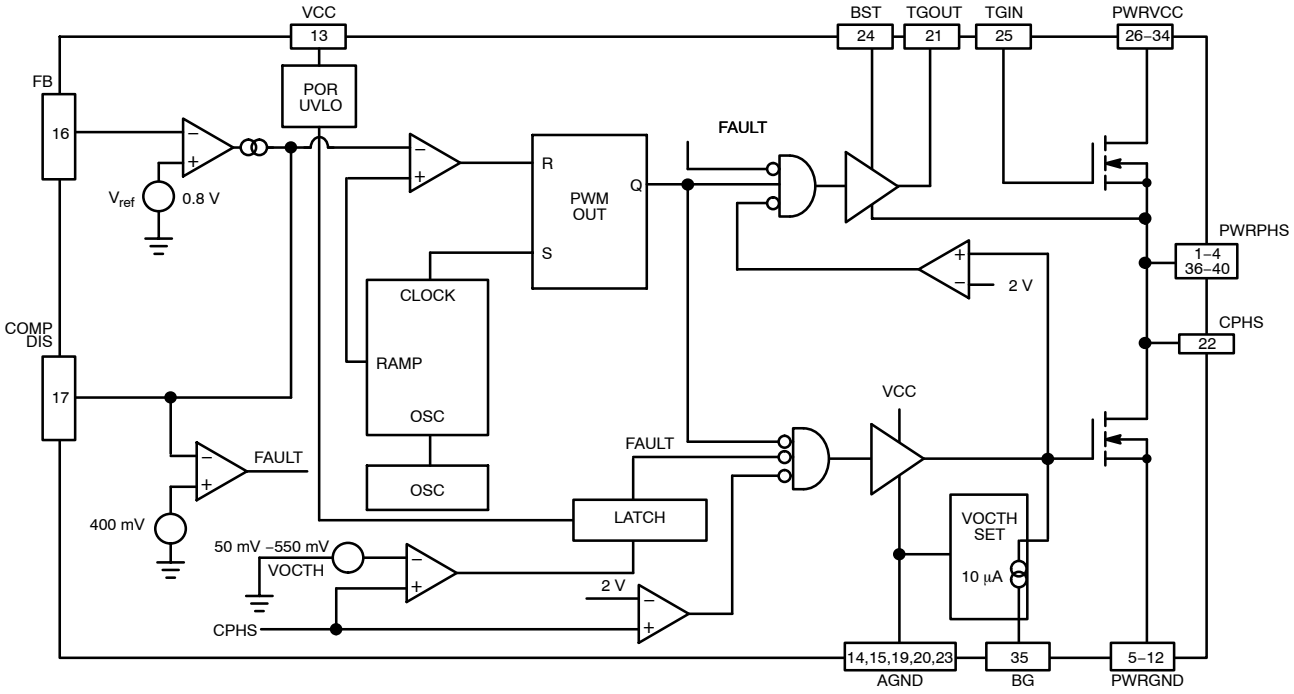


Figure 3. Detailed Block Diagram

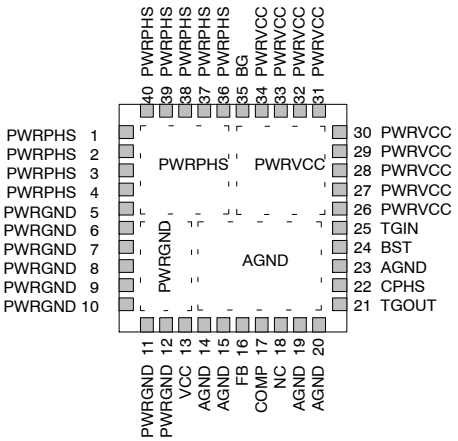


Figure 4. Pin Connections

Table 1. PIN FUNCTION DESCRIPTION

Pin No	Symbol	Description
1−4, 36−40	PWRPHS	Power phase node (PWRPHS). Drain of the low side power MOSFET.
5−12	PWRGND	Power ground. High current return for the low−side power MOSFET. Connect PWRGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors.
13	VCC	Supply rail for the internal circuitry. Operating supply range is 4.5 V to 13.2 V. Decouple with a 1 μF capacitor to GND. Ensure that this decoupling capacitor is placed near the IC.
14,15,19,20,23	AGND	IC ground reference. All control circuits are referenced to these pins.
16	FB	The inverting input pin to the error amplifier. Use this pin in conjunction with the COMP pin to compensate the voltage−control feedback loop. Connect this pin to the output resistor divider (if used) or directly to output voltage.
17	COMP/DIS	Compensation or disable pin. The output of the error amplifier (EA) and the non−inverting input of the PWM comparator. Use this pin in conjunction with the FB pin to compensate the voltage−control feedback loop. The compensation capacitor also acts as a soft start capacitor. Pull the pin below 400 mV to disable controller.
18	NC	Not Connected. The pin can be connected to AGND or not connected.
21	TGOUT	High side MOSFET driver output.
22	CPHS	The controller phase sensing for short circuit protection.
24	BST	Supply rail for the floating top gate driver. To form a boost circuit, use an external diode to bring the desired input voltage to this pin (cathode connected to BST pin). Connect a capacitor (C_{BST}) between this pin and the CPHS pin.
25	TGIN	High side MOSFET gate.
26−34	PWRVCC	Input supply pin for the high side MOSFET. Connect VCCPWR to the VCC pin or power separately for split rail application..
35	BG	The current limit set pin.

Table 2. ABSOLUTE MAXIMUM RATINGS

Pin Name	Symbol	Min	Max	Unit
Main Supply Voltage Control Input	V_{CC}	−0.3	15	V
Main Supply Voltage Power Input	PWRVCC	−0.3	30	V
Bootstrap Supply Voltage vs Ground	V_{BST}	−0.3	35	V
Bootstrap Supply Voltage vs Ground (spikes < = 50 ns)	V_{BST_spike}	−5.0	40	V

Table 2. ABSOLUTE MAXIMUM RATINGS

Pin Name	Symbol	Min	Max	Unit
Bootstrap Pin Voltage vs V_{PWRPHS}	$V_{BST}-V_{PWRPHS}$	−0.3	15	V
High Side Switch Max DC Current	I PHS	0	7.5	A
V_{PWRPHS} Pin Voltage	V_{PWRPHS}	−0.7	30	V
V_{PWRPHS} Pin Voltage (spikes < 50 ns)	$V_{PWRPHSSP}$	−5	40	V
CPHASE Pin Voltage	V_{CPHS}	−0.7	30	V
CPHASE Pin Voltage (spikes < 50 ns)	V_{CPHSTR}	−5	40	V
Current Limit Set and Bottom Gate	V_{BG}	−0.3	$V_{CC} < V_{BG} < 15$	V
Current Limit Set and Bottom Gate (spikes < 200 ns)	V_{BGSP}	−2.0	$V_{CC} < V_{BGSP} < 15$	V
Top Gate vs Ground	V_{TG}	−0.3	30	V
Top Gate vs Phase	V_{TG}	−0.3	$V_{CC} < V_{TG} < 15$	V
Top Gate vs Phase (spikes < 200 ns)	V_{TGSP}	−2.0	$V_{CC} < V_{TGSP} < 15$	V
FB Pin Voltage	V_{FB}	−0.3	$V_{CC} < V_{FB} < 6.0$	V
COMP/DISABLE	VCOMP/DIS	−0.3	$V_{CC} < V_{COMP/DIS} < 6.0$	V
Rating	**Symbol**	**Symbol**		**Unit**
Thermal Resistance, Junction−to−Ambient (Note 2)	$R_{\theta JA}$	35		°C/W
Thermal Resistance, Junction−to−Case (Note 2) at 85°C	$R_{\theta JC}$	5		°C/W
Continuous Power Distribution (T_A = +85°C)	P_D	1.8		W
Storage Temperature Range	T_{stg}	−55 to 150		°C
Junction Operating Temperature	T_J	−40 to 150		°C
Lead Temperature Soldering (10 sec): Reflow (SMD styles only) Pb−Free (Note 1)	RF	260 peak		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: These devices have limited built−in ESD protection. The devices should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the device.

1. 60−180 seconds minimum above 237°C
2. Based on 110 * 100 mm double layer PCB with 35 μm thick copper plating.

Table 3. ELECTRICAL CHARACTERISTICS (−40°C < T_J < 125°C; VCC =12 V, BST − PHS = 12 V, BST = 12 V, PHS = 24 V, for min/max values unless otherwise noted).

Characteristic	Conditions	Min	Typ	Max	Unit
Power Power Channel	$PWRV_{CC}$ − GND	2.7		18	V
Input Voltage Range	V_{CC} − GND	4.5		13.2	V
Boost Voltage Range	V_{BST} − GND	4.5		26.5	V
SUPPLY CURRENT					
Quiescent Supply Current	V_{FB} = 0.85 V V_{COMP} = 0.4 V, No Switching, V_{CC} = 13.2 V		4.1		mA
Quiescent Supply Current	V_{FB} = 0.85 V V_{COMP} = 0.4 V No Switching, V_{CC} = 5.0 V		3.2		mA
V_{CC} Supply Current	V_{FB} = V_{COMP} = 1 V, Switching, V_{CC} = 13.2 V		9.1	15	mA
V_{CC} Supply Current	V_{FB} = V_{COMP} = 1 V, Switching, V_{CC} = 5 V		4.8	8.0	mA
Boost Quiescent Current	V_{FB} = 0.85 V, No Switching, V_{CC} = 13.2 V		63		μA
Shutdown Supply Current	V_{FB} = 1 V, VCOMP= 0 V, No Switching, V_{CC} = 13.2 V	–	4.1	–	mA
UNDER VOLTAGE LOCKOUT					
V_{CC} UVLO Threshold	V_{CC} Rising Edge	3.8	–	4.3	V
V_{CC} UVLO Hysteresis	–	–	364	–	mV
BST UVLO Threshold Rising	BST Rising	–	3.82	–	V
BST UVLO Threshold Falling		–	3.71	–	V
SWITCHING REGULATOR					
VFB Feedback Voltage, Control Loop in Regulation	0°C < T_J < 70°C, 4.5 V < V_{CC} < 13.2 V −40°C < T_J < 125°C, 4.5 < V_{CC} < 13.2 V	0.792 0.788	0.800 0.800	0.808 0.812	V
Oscillator Frequency	0°C < T_J < 70°C, 4.5 V < V_{CC} < 13.2 V −40°C < T_J < 125°C, 4.5 < V_{CC} < 13.2 V	250 233	275 275	300 317	kHz
Ramp−Amplitude Voltage		0.8	1.1	1.4	V
Minimum Duty Cycle		–	7.0	–	%
Maximum Duty Cycle			88.5		%
TG Falling to BG Rising Delay	V_{CC} = 12 V, T_G < 2.0 V, B_G > 2.0 V		46		ns
BG Falling to TG Rising Delay	V_{CC} = 12 V, B_G < 2.0 V, T_G > 2.0 V		41		ns
PWM COMPENSATION					
Transconductance		3.1	–	3.5	mS
Open Loop DC Gain	Guaranteed by design	55	70	–	DB
Output Source Current Output Sink Current	V_{FB} < 0.8 V V_{FB} > 0.8 V	80 80	140 131	200 200	μA
Input Bias Current		–	0.160	1.0	μA
ENABLE					
Enable Threshold (Falling)		0.37	0.4	.43	V
SOFT−START					
Delay to Soft−Start		1	–	5	ms
SS Source Current	V_{FB} < 0.8 V	–	10.6	–	μA
Switch Over Threshold	V_{FB} = 0.8 V	–	100	–	% of Vref
OVER−CURRENT PROTECTION					
OCSET Current Source	Sourced from BG Pin before Soft−Start	–	10	–	μA
OC Threshold	R_{BG} = 5 kΩ	–	50	–	mV
OC Switch−Over Threshold		–	700	–	mV
Fixed OC Threshold		–	99	–	mV
PWM OUTPUT STAGE					
High−Side Switch On−Resistance	V_{CC} = 12 V I_D = 1 A	–	18	–	mΩ
Low−Side Switch On−Resistance	V_{CC} = 12 V I_D = 1 A	–	18	–	mΩ

TYPICAL OPERATING CHARACTERISTICS

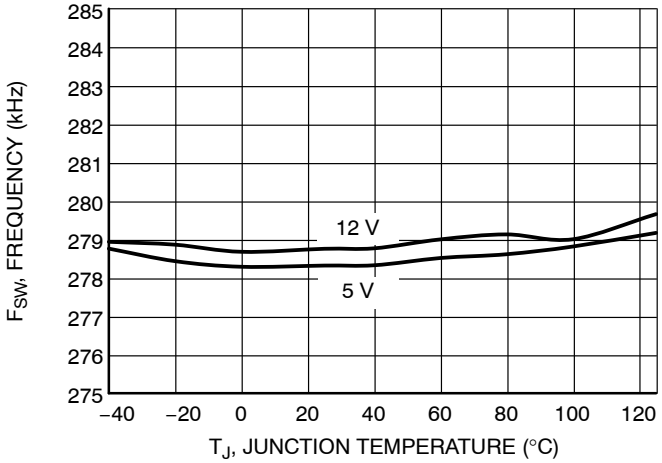


Figure 5. Frequency (F_{SW}) vs. Temperature

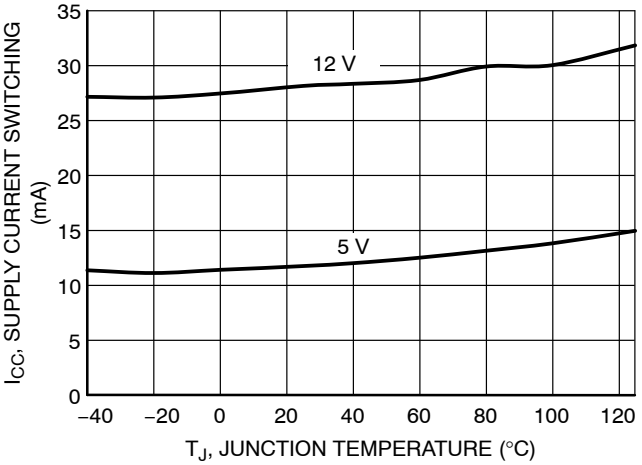


Figure 6. Switching Current vs. Temperature

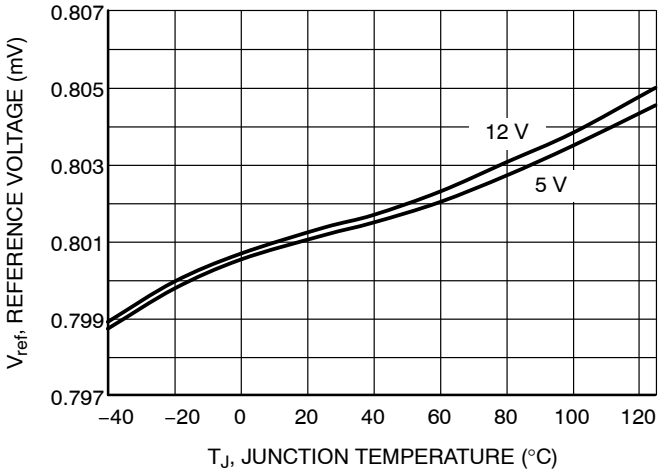


Figure 7. Reference Voltage (V_{ref}) vs. Temperature

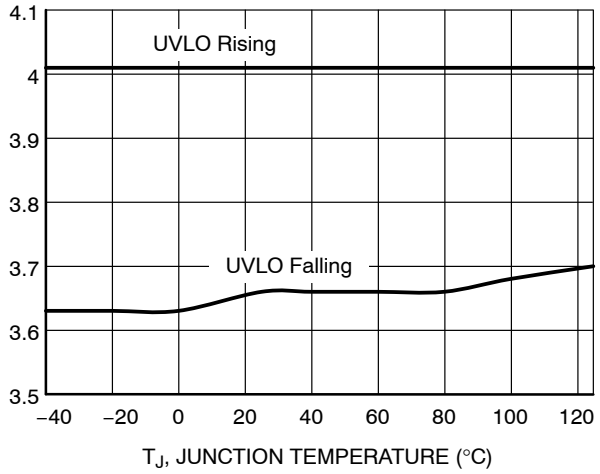


Figure 8. UVLO Threshold vs. Temperature

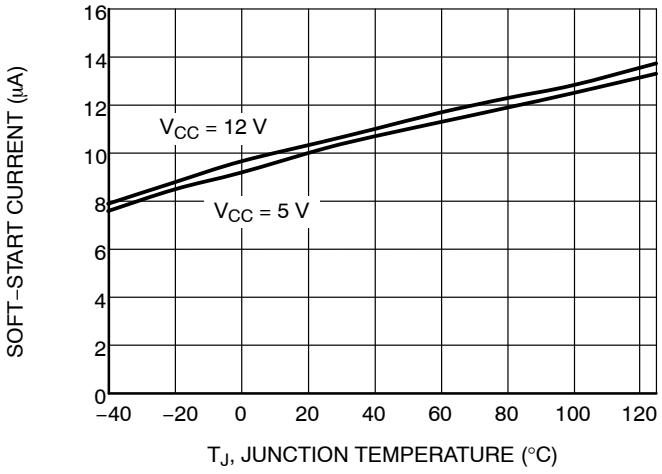


Figure 9. Soft−Start Sourcing vs. Temperature

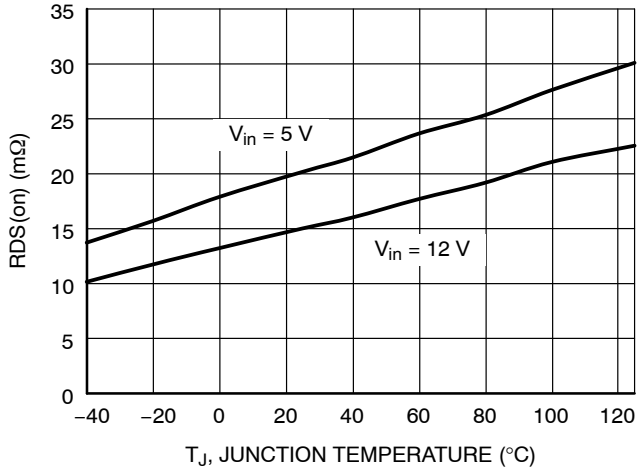


Figure 10. $R_{DS(on)}$ vs. Temperature

TYPICAL OPERATING CHARACTERISTICS

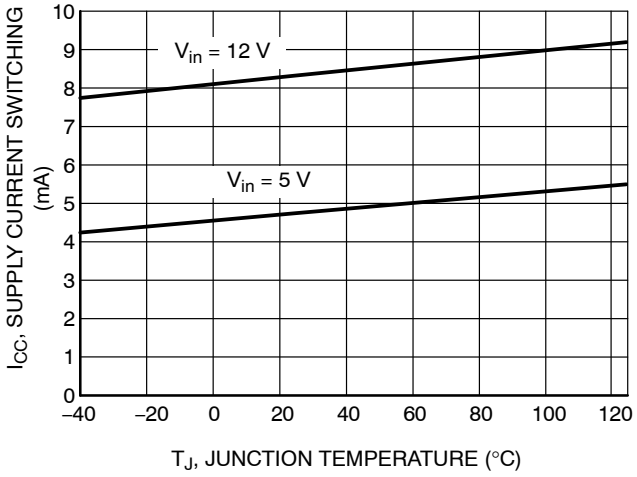


Figure 11. I_{CC} vs. Temperature

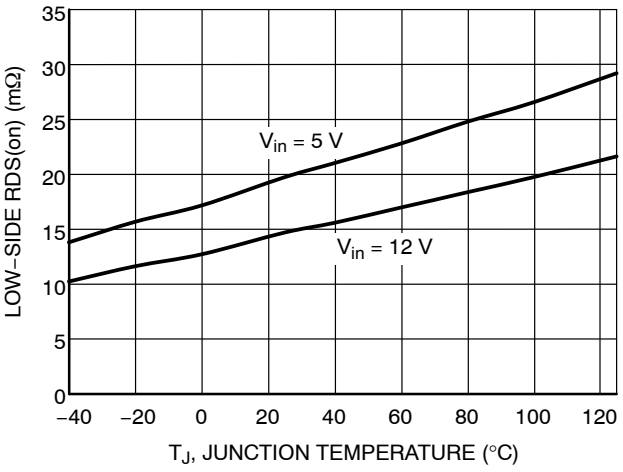


Figure 12. Low−Side $R_{DS(on)}$ vs. Temperature

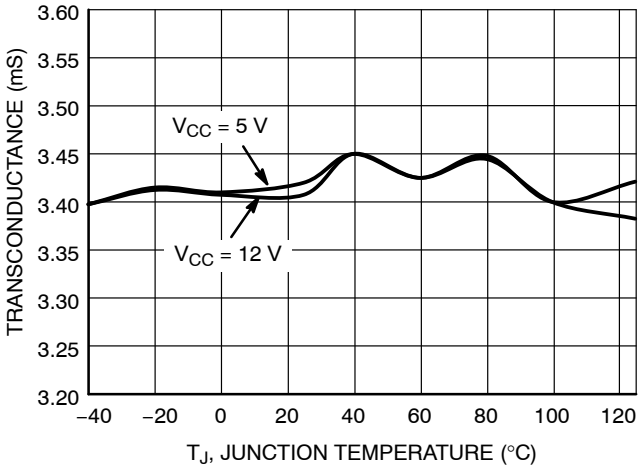


Figure 13. Transconductance vs. Temperature

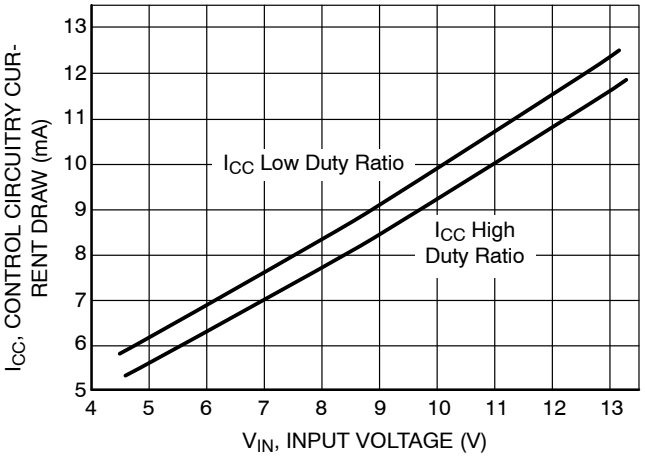


Figure 14. Maximum Duty Cycle vs. Input Voltage

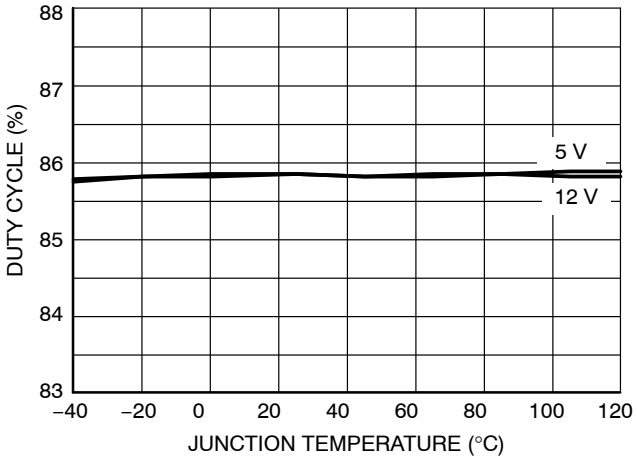


Figure 15. Controller Current vs. Input Voltage

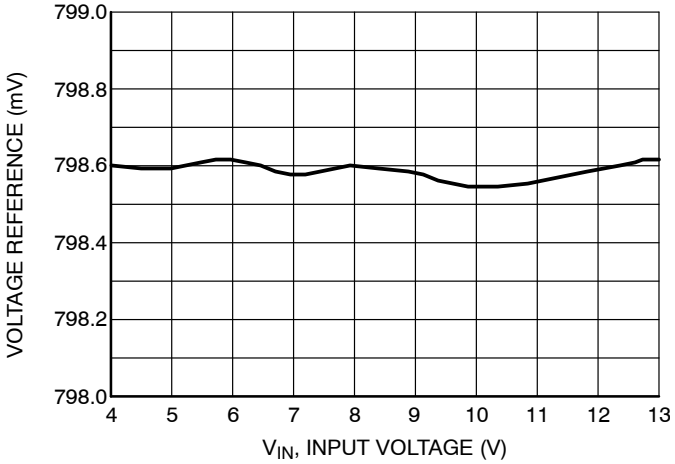


Figure 16. Reference Voltage vs. Input Voltage

TYPICAL OPERATING CHARACTERISTICS

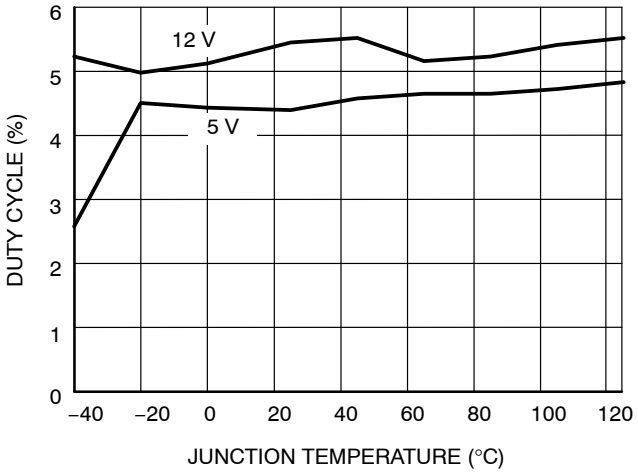


Figure 17. Minimum Duty Cycle vs. Temperature

DETAILED OPERATING DESCRIPTION

General

NCP3101C is a high efficiency integrated wide input voltage 6 A synchronous PWM buck converter designed to operate from a 4.5 V to 13.2 V supply. The output voltage of the converter can be precisely regulated down to 800 mV ±1.0% when the VFB pin is tied to the output voltage. The switching frequency is internally set to 275 kHz. A high gain Operational Transconductance Error Amplifier (OTEA) is used for feedback and stabilizing the loop.

Input Voltage

The NCP3101C can be used in many applications by using the V_{CC} and PWRVCC pins together or separately. The PWRVCC pin provides voltage to the switching MOSFETS. The V_{CC} pin provides voltage to the control circuitry and driver stage.

If the V_{CC} and the PWRVCC pin are not tied together, the input voltage of the PWRVCC pin can accept 2.7 V to 18 V. If the V_{CC} and PWRVCC pins are tied together the input voltage range is 4.5 V to 13.2 V.

Duty Cycle and Maximum Pulse Width Limits

In steady state DC operation, the duty cycle will stabilize at an operating point defined by the ratio of the input to the output voltage. The NCP3101C can achieve an 82% duty ratio. The part has a built in off−time which ensures that the bootstrap supply is charged every cycle. The NCP3101C is capable of a 100 ns pulse width (minimum) and allows a 12 V to 0.8 V conversion at 275 kHz. The duty cycle limit and the corresponding output voltage are shown below in graphical format in Figure 18. The green area represents the safe operating area for the lowest maximum operational duty cycle for 4.5 V and 13.2 V.

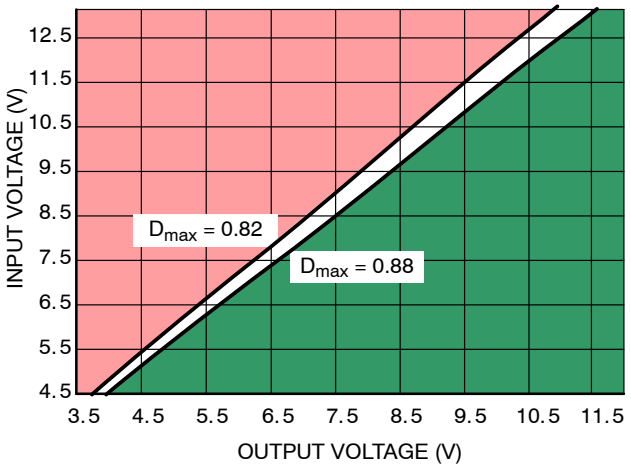


Figure 18. Maximum Input to Output Voltage

Input voltage range (VCC and BST)

The input voltage range for both VCC and BST is 4.5 V to 13.2 V with reference to GND and PHS, respectively. Although BST is rated at 13.2 V with reference to PHS, it can also tolerate 26.5 V with respect to GND.

External Enable/Disable

Once the input voltage has exceeded the boost and UVLO threshold at 3.82 V and V_{CC} threshold at 4 V, the COMP pin starts to rise. The PWRPHS node is tri−stated until the COMP voltage exceeds 830 mV. Once the 830 mV threshold is exceeded, the part starts to switch and is considered enabled. When the COMP pin voltage is pulled below the 400 mV threshold, it disables the PWM logic, the top MOSFET is driven off, and the bottom MOSFET is driven on as shown in Figure 19. In the disabled mode, the OTA output source current is reduced to 10 μA.

When disabling the NCP3101C using the COMP / Disable pin, an open collector or open drain drive should be used as shown in Figure 20.

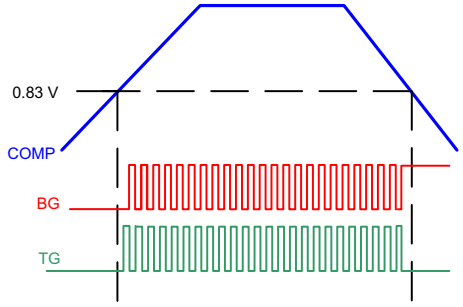


Figure 19. Enable/Disable Driver State Diagram

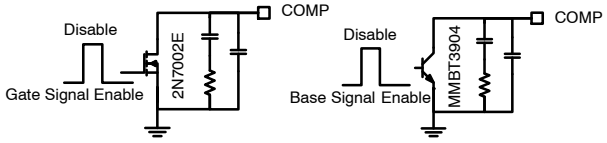


Figure 20. Recommended Disable Circuits

Power Sequencing

Power sequencing can be achieved with NCP3101C using two general purpose bipolar junction transistors or MOSFETs. An example of the power sequencing circuit using the external components is shown in Figure 21.

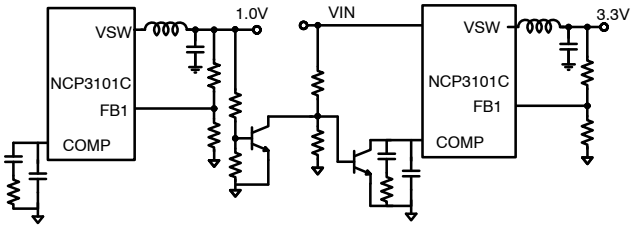


Figure 21. Power Sequencing

Normal Shutdown Behavior

Normal shutdown occurs when the IC stops switching because the input supply reaches UVLO threshold. In this case, switching stops, the internal soft start, SS, is discharged, and all gate pins go low. The switch node enters a high impedance state and the output capacitors discharge through the load with no ringing on the output voltage.

External Soft−Start

The NCP3101C features an external soft start function, which reduces inrush current and overshoot of the output voltage. Soft start is achieved by using the internal current source of 10 μA (typ), which charges the external integrator capacitor of the transconductance amplifier. Figures 22 and 23 are typical soft start sequences. The sequence begins once V_{CC} surpasses its UVLO threshold. During Soft Start as the Comp Pin rises through 400 mV, the PWM logic and gate drives are enabled. When the feedback voltage crosses 800 mV, the EOTA will be given control to switch to its higher regulation mode with the ability to source and sink 130 μA. In the event of an over current during the soft start, the overcurrent logic will override the soft start sequence and will shut down the PWM logic and both the high side and low side gates of the switching MOSFETS.

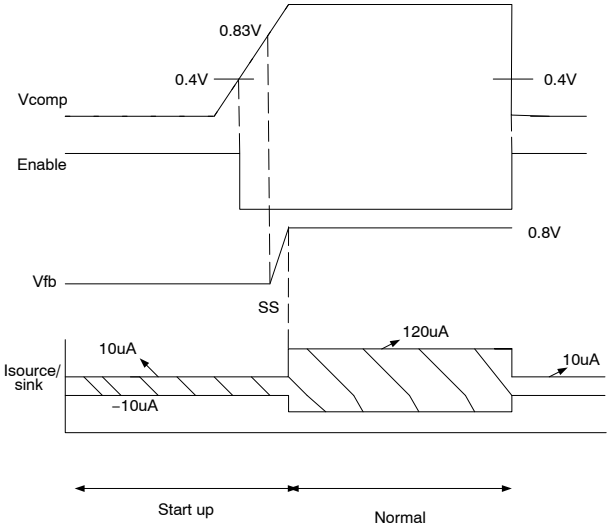


Figure 22. Soft−Start Implementation

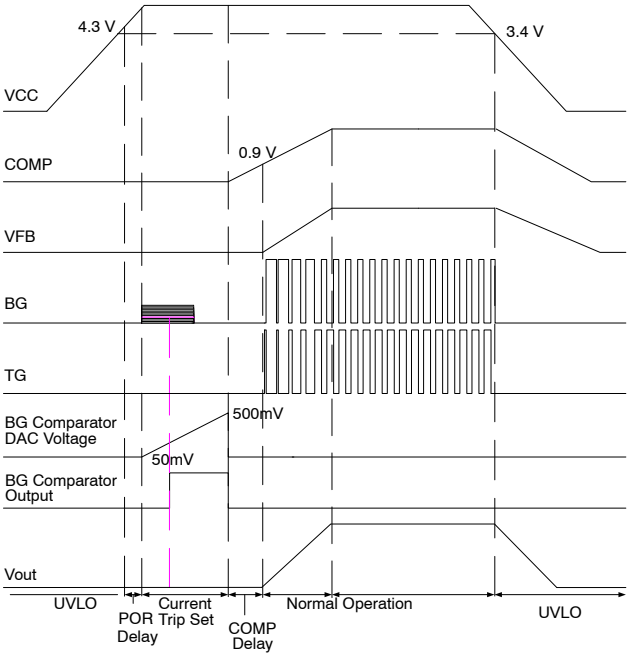


Figure 23. Soft−Start Sequence

UVLO

Under Voltage Lockout (UVLO) is provided to ensure that unexpected behavior does not occur when V_{CC} is too low to support the internal rails and power the converter. For the NCP3101C, the UVLO is set to ensure that the IC will start up when VCC reaches 4.0 V and shutdown when V_{CC} drops below 3.6 V. The UVLO feature permits smooth operation from a varying 5.0 V input source.

Current Limit Protection

In case of a short circuit or overload, the low−side (LS) FET will conduct large currents. The low−side $R_{DS(on)}$ sense is implemented to protect from over current by comparing the voltage at the phase node to AGND just prior to the low side MOSFET turnoff to an internally generated fixed voltage. If the differential phase node voltage is lower than OC trip voltage, an overcurrent condition occurs and a counter is initiated. If seven consecutive over current trips are counted, the PWM logic and both HS−FET and LS−FET are turned off. The converter will be latched off until input power drops below the UVLO threshold. The operation of key nodes are displayed in Figure 24 for both normal operation and during over current conditions.

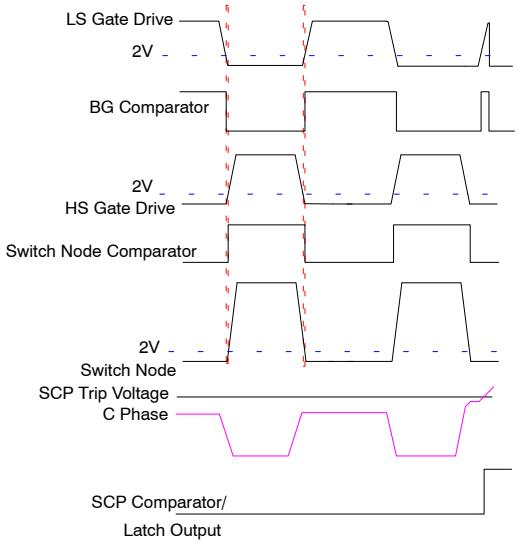


Figure 24. Switching and Current Limit Timing

Overcurrent Threshold Setting

The NCP3101C overcurrent threshold can be set from 50 mV to 450 mV by adding a resistor (RSET) between BG and GND. During a short period of time following V_{CC} rising above the UVLO threshold, an internal 10 μA current (IOCSET) is sourced from the BG pin, creating a voltage drop across RSET. The voltage drop is compared against a stepped internal voltage ramp. Once the internal stepped voltage reaches the RSET voltage, the value is stored internally until power is cycled. The overall time length for the OC setting procedure is approximately 3 ms. When connecting an RSET resistor between BG and GND, the programmed threshold will be:

$$I_{OCth} = \frac{I_{OCSET} * R_{SET}}{R_{DS(on)}} \rightarrow 7.2\ A = \frac{10\ \mu A * 13\ k\Omega}{18\ m\Omega} \quad \text{(eq. 1)}$$

I_{OCSET} = Sourced current
I_{OCTH} = Current trip threshold
$R_{DS(on)}$ = On resistance of the low side MOSFET
R_{SET} = Current set resistor

The RSET values range from 5 kΩ to 45 kΩ. If RSET is not connected or the RSET value is too high, the device switches the OCP threshold to a fixed 96 mV value (5.3 A) typical at 12 V. The internal safety clamp on BG is triggered as soon as BG voltage reaches 700 mV, enabling the 96 mV fixed threshold and ending the OC setting period. The current trip threshold tolerance is ± 25 mV. The accuracy is best at the highest set point (550 mV). The accuracy will decrease as the set point decreases.

Drivers

The NCP3101C drives the internal high and low side switching MOSFETS with 1 A gate drivers. The gate drivers also include adaptive non−overlap circuitry. The non−overlap circuitry increases efficiency which minimizes power dissipation by minimizing the low−side MOSFET body diode conduction time.

A block diagram of the non−overlap and gate drive circuitry used is shown in Figure 24.

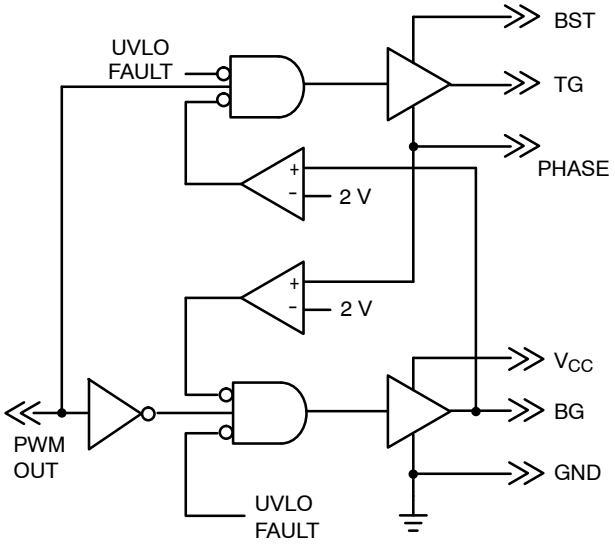


Figure 25. Block Diagram

Careful selection and layout of external components is required to realize the full benefit of the onboard drivers. The capacitors between V_{CC} and GND and between BST and CPHS must be placed as close as possible to the IC. A ground plane should be placed on the closest layer for return currents to GND in order to reduce loop area and inductance in the gate drive circuit.

APPLICATION SECTION

Design Procedure

When starting the design of a buck regulator, it is important to collect as much information as possible about the behavior of the input and output before starting the design.

ON Semiconductor has a Microsoft Excel® based design tool available online under the design tools section of the NCP3101C product page. The tool allows you to capture your design point and optimize the performance of your regulator based on your design criteria.

Table 4. DESIGN PARAMETERS

Design Parameter	Example Value
Input voltage (VCC)	10.8 V to 13.2 V
Output voltage (V_{OUT})	3.3 V
Input ripple voltage (VCC_{RIPPLE})	300 mV
Output ripple voltage ($V_{OUTRIPPLE}$)	40 mV
Output current rating (I_{OUT})	6 A
Operating frequency (F_{SW})	275 kHz

The buck converter produces input voltage V_{CC} pulses that are LC filtered to produce a lower DC output voltage V_{OUT}. The output voltage can be changed by modifying the on time relative to the switching period T or switching frequency. The ratio of high side switch on time to the switching period is called duty ratio D. Duty ratio can also be calculated using V_{OUT}, V_{CC}, Low Side Switch Voltage Drop V_{LSD}, and High Side Switch Voltage Drop V_{HSD}.

$$F_{SW} = \frac{1}{T} \quad \text{(eq. 2)}$$

$$D = \frac{T_{ON}}{T}(1 - D) = \frac{T_{OFF}}{T} \quad \text{(eq. 3)}$$

$$D = \frac{V_{OUT} + V_{LSD}}{V_{CC} - V_{HSD} + V_{LSD}} \approx D = \frac{V_{OUT}}{V_{CC}} \rightarrow \quad \text{(eq. 4)}$$

$$27.5\% = \frac{3.3\ V}{12\ V}$$

D = Duty cycle
F_{SW} = Switching frequency
T = Switching period
T_{OFF} = High side switch off time
T_{ON} = High side switch on time
V_{HSD} = High side switch voltage drop
VCC = Input voltage
V_{LSD} = Low side switch voltage drop
V_{OUT} = Output voltage

Inductor Selection

When selecting an inductor, the designer may employ a rule of thumb for the design where the percentage of ripple current in the inductor should be between 10% and 40%. When using ceramic output capacitors, the ripple current can be greater because the ESR of the output capacitor is small, thus a user might select a higher ripple current. However, when using electrolytic capacitors, a lower ripple current will result in lower output ripple due to the higher ESR of electrolytic capacitors. The ratio of ripple current to maximum output current is given in Equation 5.

$$ra = \frac{\Delta I}{I_{OUT}} \quad \text{(eq. 5)}$$

ΔI = Ripple current
I_{OUT} = Output current
ra = Ripple current ratio

Using the ripple current rule of thumb, the user can establish acceptable values of inductance for a design using Equation 6.

$$L_{OUT} = \frac{V_{OUT}}{I_{OUT} * ra * F_{SW}} * (1 - D) \rightarrow \quad \text{(eq. 6)}$$

$$5.6\ \mu H = \frac{12\ V}{6.0\ A * 26\% * 275\ kHz} * (1 - 27.5\%)$$

D = Duty ratio
F_{SW} = Switching frequency
I_{OUT} = Output current
L_{OUT} = Output inductance
ra = Ripple current ratio

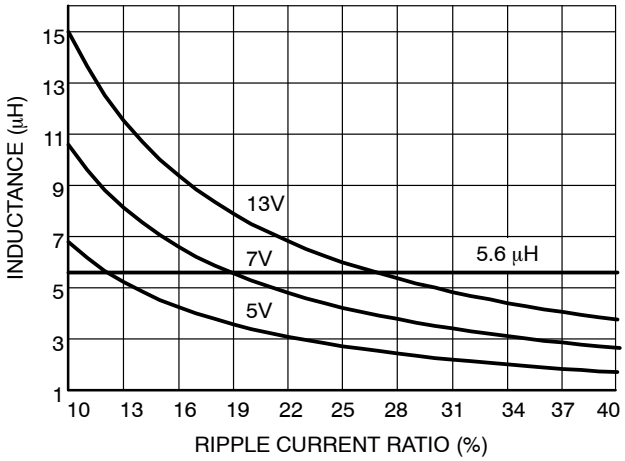


Figure 26. Inductance vs. Current Ripple Ratio

When selecting an inductor, the designer must not exceed the current rating of the part. To keep within the bounds of the part's maximum rating, a calculation of the RMS current and peak current are required.

$$I_{RMS} = I_{OUT} * \sqrt{1 + \frac{ra^2}{12}} \rightarrow$$
$$6.02\ A = 6\ A * \sqrt{1 + \frac{26\%^2}{12}} \quad \text{(eq. 7)}$$

I_{OUT} = Output current
I_{RMS} = Inductor RMS current
ra = Ripple current ratio

$$I_{PK} = I_{OUT} * \left(1 + \frac{ra}{2}\right) \rightarrow 6.78\ A = 6.0\ A * \left(1 + \frac{26\%}{2}\right) \quad \text{(eq. 8)}$$

I_{OUT} = Output current
I_{PK} = Inductor peak current
ra = Ripple current ratio

A standard inductor should be found so the inductor will be rounded to 5.6 μH. The inductor should support an RMS current of 6.02 A and a peak current of 6.78 A.

The final selection of an output inductor has both mechanical and electrical considerations. From a mechanical perspective, smaller inductor values generally correspond to smaller physical size. Since the inductor is often one of the largest components in the regulation system, a minimum inductor value is particularly important in space constrained applications. From an electrical perspective, the maximum current slew rate through the output inductor for a buck regulator is given by Equation 9.

$$SlewRate_{LOUT} = \frac{V_{CC} - V_{OUT}}{L_{OUT}} \rightarrow 1.56\ A = \frac{12\ V - 3.3\ V}{5.6\ \mu H} \quad \text{(eq. 9)}$$

L_{OUT} = Output inductance
V_{CC} = Input voltage
V_{OUT} = Output voltage

Equation 9 implies that larger inductor values limit the regulator's ability to slew current through the output inductor in response to output load transients. Consequently, output capacitors must supply the load current until the inductor current reaches the output load current level. Reduced inductance to increase slew rates results in larger values of output capacitance to maintain tight output voltage regulation. In contrast, smaller values of inductance increase the regulator's maximum achievable slew rate and decrease the necessary capacitance at the expense of higher ripple current. The peak−to−peak ripple current is given by the following equation:

$$I_{PP} = \frac{V_{OUT}(1 - D)}{L_{OUT} * F_{SW}} \rightarrow$$
$$1.56\ A = \frac{3.3\ V(1 - 27.5\%)}{5.6\ \mu H * 275\ kHz} \quad \text{(eq. 10)}$$

D = Duty ratio
F_{SW} = Switching frequency
I_{PP} = Peak−to−peak current of the inductor
L_{OUT} = Output inductance
V_{OUT} = Output voltage

From Equation 10 it is clear that the ripple current increases as L_{OUT} decreases, emphasizing the trade−off between dynamic response and ripple current.

The power dissipation of an inductor falls into two categories: copper and core losses. Copper losses can be further categorized into DC losses and AC losses. A good first order approximation of the inductor losses can be made using the DC resistance as shown below:

$$LP_{CU\_DC} = I_{RMS}^{\ 2} * DCR \rightarrow 199\ mW = 6.02^2 * 5.5\ m\Omega \quad \text{(eq. 11)}$$

I_{RMS} = Inductor RMS current
DCR = Inductor DC resistance
LP_{CU_DC} = Inductor DC power dissipation

The core losses and AC copper losses will depend on the geometry of the selected core, core material, and wire used. Most vendors will provide the appropriate information to make accurate calculations of the power dissipation, at which point the total inductor losses can be captured by the equation below:

$$LP_{tot} = LP_{CU\_DC} + LP_{CU\_AC} + LP_{Core} \rightarrow$$
$$204\ mW = 199\ mW + 2\ mW + 3\ mW \quad \text{(eq. 12)}$$

LP_{CU_DC} = Inductor DC power dissipation
LP_{CU_AC} = Inductor AC power dissipation
LP_{Core} = Inductor core power dissipation

Output Capacitor Selection

The important factors to consider when selecting an output capacitor are DC voltage rating, ripple current rating, output ripple voltage requirements, and transient response requirements.

The output capacitor must be rated to handle the ripple current at full load with proper derating. The RMS ratings given in datasheets are generally for lower switching frequency than used in switch mode power supplies, but a multiplier is usually given for higher frequency operation. The RMS current for the output capacitor can be calculated below:

$$CO_{RMS} = I_{OUT}\frac{ra}{\sqrt{12}} \rightarrow 0.45\ A = 6.0\ A\frac{26\%}{\sqrt{12}} \quad \text{(eq. 13)}$$

Co_{RMS} = Output capacitor RMS current
I_{OUT} = Output current
ra = Ripple current ratio

The maximum allowable output voltage ripple is a combination of the ripple current selected, the output capacitance selected, the Equivalent Series Inductance (ESL), and Equivalent Series Resistance (ESR).

The main component of the ripple voltage is usually due to the ESR of the output capacitor and the capacitance selected, which can be calculated as shown in Equation 14:

$$V_{ESR\_C} = I_{OUT} * ra\left(CO_{ESR} + \frac{1}{8 * F_{SW} * C_{OUT}}\right) \quad \text{(eq. 14)}$$

$$19.6\ mV = 6 * 26\%\left(12\ m\Omega + \frac{1}{8 * 275\ kHz * 820\ \mu F}\right)$$

Co_{ESR} = Output capacitor ESR
C_{OUT} = Output capacitance
F_{SW} = Switching frequency
I_{OUT} = Output current
ra = Ripple current ratio

The ESL of capacitors depends on the technology chosen, but tends to range from 1 nH to 20 nH, where ceramic capacitors have the lowest inductance and electrolytic capacitors have the highest. The calculated contributing voltage ripple from ESL is shown for the switch on and switch off below:

$$V_{ESLON} = \frac{ESL * I_{PP} * F_{SW}}{D} \rightarrow \quad \text{(eq. 15)}$$

$$15.6\ mV = \frac{10\ nH * 1.56\ A * 275\ kHz}{27.5\%}$$

$$V_{ESLOFF} = \frac{ESL * I_{PP} * F_{SW}}{(1 - D)} \rightarrow \quad \text{(eq. 16)}$$

$$5.92\ mV = \frac{10\ nH * 1.56\ A * 275\ kHz}{(1 - 27.5\%)}$$

D = Duty ratio
ESL = Capacitor inductance
F_{SW} = Switching frequency
Ipp = Peak−to−peak current

The output capacitor is a basic component for fast response of the power supply. For the first few microseconds of a load transient, the output capacitor supplies current to the load. Once the regulator recognizes a load transient, it adjusts the duty ratio, but the current slope is limited by the inductor value.

During a load step transient, the output voltage initially drops due to the current variation inside the capacitor and the ESR (neglecting the effect of the ESL). The user must also consider the resistance added due to PCB traces and any connections to the load. The additional resistance must be added to the ESR of the output capacitor.

$$\Delta V_{OUT-ESR} = I_{TRAN} \times \left(CO_{ESR} + RCON\right) \rightarrow$$

$$111\ mV = 3\ A \times (12\ m\Omega + 25 m\Omega) \quad \text{(eq. 17)}$$

Co_{ESR} = Output capacitor Equivalent Series Resistance
I_{TRAN} = Output transient current
ΔV_{OUT_ESR} = Voltage deviation of V_{OUT} due to the effects of ESR

A minimum capacitor value is required to sustain the current during the load transient without discharging it. The voltage drop due to output capacitor discharge is given by the following equation:

$$\Delta V_{OUT-DIS} = \frac{(I_{TRAN})^2 \times L_{OUT}}{2 * D_{MAX} * C_{OUT} \times (V_{CC} - V_{OUT})} \rightarrow \text{(eq. 18)}$$

$$4.16\ mV = \frac{(3\ A)^2 \times 5.6\ \mu H}{2 * 82\% * 820\ \mu F \times (12\ V - 3.3\ V)}$$

C_{OUT} = Output capacitance
D_{MAX} = Maximum duty ratio
I_{TRAN} = Output transient current
L_{OUT} = Output inductor value
VCC = Input voltage
V_{OUT} = Output voltage
ΔV_{OUT_DIS} = Voltage deviation of V_{OUT} due to the effects of capacitor discharge

In a typical converter design, the ESR of the output capacitor bank dominates the transient response. Please note that ΔV_{OUT_DIS} and ΔV_{OUT_ESR} are out of phase with each other, and the larger of these two voltages will determine the maximum deviation of the output voltage (neglecting the effect of the ESL).

Table 5 shows values of voltage drop and recovery time of the NCP3101C demo board with the configuration shown in Figure 27. The transient response was measured for the load current step from 3 A to 6 A (50% to 100% load).

Input capacitors are 2 x 47 μF ceramic and 1 x 270 μF OS−CON, output capacitors are 2 x 100 μF ceramic and OS−CON as mentioned in Table 5. Typical transient response waveforms are shown in Figure 27.

More information about OS−CON capacitors is available at http://www.edc.sanyo.com.

Table 5. TRANSIENT RESPONSE VERSUS OUTPUT CAPACITANCE (50% to 100% Load Step)

COUT OS−CON (μF)	Drop (mV)	Recovery Time (μs)
0	384	336
100	224	298
150	192	278
220	164	238
270	156	212
560	128	198
820	112	118
1000	112	116

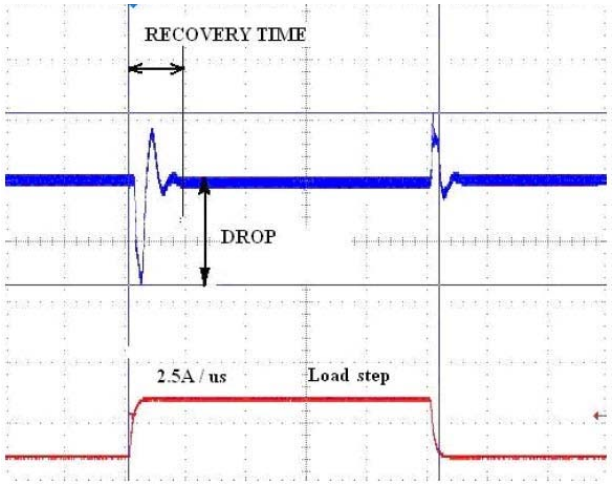


Figure 27. Typical Waveform of Transient Response

Input Capacitor Selection

The input capacitor has to sustain the ripple current produced during the on time of the upper MOSFET, therefore must have a low ESR to minimize losses. The RMS value of the input ripple current is:

$$IIN_{RMS} = I_{OUT} \times \sqrt{D \times (1 - D)} \rightarrow$$
$$2.68\ A = 6.0\ A \sqrt{27.5\% \times (1 - 27.5\%)} \quad \text{(eq. 19)}$$

D = Duty ratio
IIN_{RMS} = Input capacitance RMS current
I_{OUT} = Load current

The equation reaches its maximum value with D = 0.5. Loss in the input capacitors can be calculated with the following equation:

$$P_{CIN} = CIN_{ESR} \times \left(IIN_{RMS}\right)^2$$
$$71.8\ mW = 10\ m\Omega \times (2.68\ A)^2 \quad \text{(eq. 20)}$$

CIN_{ESR} = Input capacitance Equivalent Series Resistance
IIN_{RMS} = Input capacitance RMS current
P_{CIN} = Power loss in the input capacitor

Due to large di/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum capacitor must be used, it must be surge protected, otherwise capacitor failure could occur.

Power MOSFET Dissipation

Power dissipation, package size, and the thermal environment drive power supply design. Once the dissipation is known, the thermal impedance can be calculated to prevent the specified maximum junction temperatures from being exceeded at the highest ambient temperature.

Power dissipation has two primary contributors: conduction losses and switching losses. The high−side MOSFET will display both switching and conduction losses. The switching losses of the low side MOSFET will not be calculated as it switches into nearly zero voltage and the losses are insignificant. However, the body diode in the low−side MOSFET will suffer diode losses during the non−overlap time of the gate drivers.

Starting with the high−side MOSFET, the power dissipation can be approximated from:

$$P_{D\_HS} = P_{COND} + P_{SW\_TOT} \quad \text{(eq. 21)}$$

P_{COND} = Conduction losses
P_{D_HS} = Power losses in the high side MOSFET
P_{SW_TOT} = Total switching losses

The first term in Equation 21 is the conduction loss of the high−side MOSFET while it is on.

$$P_{COND} = \left(I_{RMS\_HS}\right)^2 \cdot R_{DS(on)\_HS} \quad \text{(eq. 22)}$$

I_{RMS_HS} = RMS current in the high side MOSFET
$R_{DS(ON)\_HS}$ = On resistance of the high side MOSFET
P_{COND} = Conduction power losses

Using the ra term from Equation 5, I_{RMS} becomes:

$$I_{RMS\_HS} = I_{OUT} \cdot \sqrt{D \cdot \left(1 + \frac{ra^2}{12}\right)} \quad \text{(eq. 23)}$$

D = Duty ratio
ra = Ripple current ratio
I_{OUT} = Output current
I_{RMS_HS} = High side MOSFET RMS current

The second term from Equation 21 is the total switching loss and can be approximated from the following equations.

$$P_{SW\_TOT} = P_{SW} + P_{DS} + P_{RR} \quad \text{(eq. 24)}$$

P_{DS} = High side MOSFET drain to source losses
P_{RR} = High side MOSFET reverse recovery losses
P_{SW} = High side MOSFET switching losses

P_{SW_TOT} = High side MOSFET total switching losses

The first term for total switching losses from Equation 24 are the losses associated with turning the high−side MOSFET on and off and the corresponding overlap in drain voltage and current.

$$P_{SW} = P_{TON} + P_{TOFF} = \frac{1}{2} \cdot \left(I_{OUT} \cdot V_{IN} \cdot F_{SW}\right) \cdot \left(t_{RISE} + t_{FALL}\right) \quad \text{(eq. 25)}$$

F_{SW} = Switching frequency
I_{OUT} = Load current
P_{SW} = High side MOSFET switching losses
P_{TON} = Turn on power losses
P_{TOFF} = Turn off power losses
t_{FALL} = MOSFET fall time
t_{RISE} = MOSFET rise time
VCC = Input voltage

When calculating the rise time and fall time of the high side MOSFET it is important to know the charge characteristic shown in Figure 28.

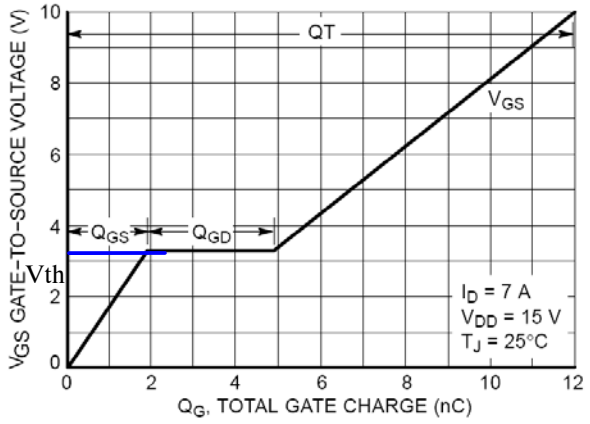


Figure 28. High Side MOSFET Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

$$t_{RISE} = \frac{Q_{GD}}{I_{G1}} = \frac{Q_{GD}}{\left(V_{BST} - V_{TH}\right) / \left(R_{HSPU} + R_G\right)} \quad \text{(eq. 26)}$$

I_{G1} = Output current from the high−side gate drive
Q_{GD} = MOSFET gate to drain gate charge
R_{HSPU} = Drive pull up resistance
R_G = MOSFET gate resistance
t_{RISE} = MOSFET rise time
V_{BST} = Boost voltage
V_{TH} = MOSFET gate threshold voltage

$$t_{FALL} = \frac{Q_{GD}}{I_{G2}} = \frac{Q_{GD}}{\left(V_{BST} - V_{TH}\right) / \left(R_{HSPD} + R_G\right)} \quad \text{(eq. 27)}$$

I_{G2} = Output current from the low−side gate drive
Q_{GD} = MOSFET gate to drain gate charge
R_G = MOSFET gate resistance
R_{HSPD} = Drive pull down resistance
t_{FALL} = MOSFET fall time
V_{BST} = Boost voltage
V_{TH} = MOSFET gate threshold voltage

Next, the MOSFET output capacitance losses are caused by both the high−side and low−side MOSFETs, but are dissipated only in the high−side MOSFET.

$$P_{DS} = \frac{1}{2} \cdot C_{OSS} \cdot V_{IN}{}^2 \cdot F_{SW} \quad \text{(eq. 28)}$$

C_{OSS} = MOSFET output capacitance at 0 V
F_{SW} = Switching frequency
P_{DS} = MOSFET drain to source charge losses
VCC = Input voltage

Finally, the loss due to the reverse recovery time of the body diode in the low−side MOSFET is shown as follows:

$$P_{RR} = Q_{RR} \cdot V_{IN} \cdot F_{SW} \quad \text{(eq. 29)}$$

F_{SW} = Switching frequency
P_{RR} = High side MOSFET reverse recovery losses
Q_{RR} = Reverse recovery charge
V_{CC} = Input voltage

The low−side MOSFET turns on into small negative voltages so switching losses are negligible. The low−side MOSFET's power dissipation only consists of conduction loss due to $R_{DS(on)}$ and body diode loss during non−overlap periods.

$$P_{D\_LS} = P_{COND} + P_{BODY} \quad \text{(eq. 30)}$$

P_{BODY} = Low side MOSFET body diode losses
P_{COND} = Low side MOSFET conduction losses
P_{D_LS} = Low side MOSFET losses

Conduction loss in the low−side MOSFET is described as follows:

$$P_{COND} = \left(I_{RMS\_LS}\right)^2 \cdot R_{DS(on)\_LS} \quad \text{(eq. 31)}$$

I_{RMS_LS} = RMS current in the low side
$R_{DS(ON)\_LS}$ = Low−side MOSFET on resistance
P_{COND} = High side MOSFET conduction losses

$$I_{RMS\_LS} = I_{OUT} \cdot \sqrt{(1 - D) \cdot \left(1 + \frac{ra^2}{12}\right)} \quad \text{(eq. 32)}$$

D = Duty ratio
I_{OUT} = Load current
I_{RMS_LS} = RMS current in the low side
ra = Ripple current ratio

The body diode losses can be approximated as:

$$P_{BODY} = V_{FD} \cdot I_{OUT} \cdot F_{SW} \cdot \left(NOL_{LH} + NOL_{HL}\right) \quad \text{(eq. 33)}$$

F_{SW} = Switching frequency
I_{OUT} = Load current
NOL_{HL} = Dead time between the high−side MOSFET turning off and the low−side MOSFET turning on, typically 46 ns
NOL_{LH} = Dead time between the low−side

MOSFET turning off and the high−side MOSFET turning on, typically 42 ns

P_{BODY} = Low−side MOSFET body diode losses

V_{FD} = Body diode forward voltage drop

Control Dissipation

The control portion of the IC power dissipation is determined by the formula below:

$$P_C = I_{CC} * V_{CC} \quad \text{(eq. 34)}$$

I_{CC} = Control circuitry current draw

P_C = Control power dissipation

V_{CC} = Input voltage

Once the IC power dissipations are determined, the designer can calculate the required thermal impedance to maintain a specified junction temperature at the worst case ambient temperature. The formula for calculating the junction temperature with the package in free air is:

$$T_J = T_A + P_D \cdot R_{\theta JC} \quad \text{(eq. 35)}$$

P_D = Power dissipation of the IC

$R_{\theta JC}$ = Thermal resistance junction−to−case of the regulator package

T_A = Ambient temperature

T_J = Junction temperature

As with any power design, proper laboratory testing should be performed to ensure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading, and component variations (i.e., worst case MOSFET $R_{DS(on)}$).

Compensation Network

To create a stable power supply, the compensation network around the transconductance amplifier must be used in conjunction with the PWM generator and the power stage. Since the power stage design criteria is set by the application, the compensation network must correct the overall output to ensure stability. The output inductor and capacitor of the power stage form a double pole at the frequency shown in Equation 36:

$$F_{LC} = \frac{1}{2\pi * \sqrt{L_{OUT} * C_{OUT}}} \rightarrow \quad \text{(eq. 36)}$$

$$2.35\ \text{kHz} = \frac{1}{2\pi * \sqrt{5.6\ \mu\text{H} * 820\ \mu\text{F}}}$$

C_{OUT} = Output capacitor

F_{LC} = Double pole inductor and capacitor frequency

L_{OUT} = Output inductor value

The ESR of the output capacitor creates a “zero” at the frequency a shown in Equation 37:

$$F_{ESR} = \frac{1}{2\pi * CO_{ESR} * C_{OUT}} \rightarrow \quad \text{(eq. 37)}$$

$$16.2\ \text{kHz} = \frac{1}{2\pi * 12\ \text{m}\Omega * 820\ \mu\text{F}} \rightarrow$$

CO_{ESR} = Output capacitor ESR

C_{OUT} = Output capacitor

F_{LC} = Output capacitor ESR frequency

The two equations above define the bode plot that the power stage has created or open loop response of the system. The next step is to close the loop by considering the feedback values. The closed loop crossover frequency should be greater then the F_{LC} and less than 1/5 of the switching frequency, which would place the maximum crossover frequency at 55 kHz. Further, the calculated F_{ESR} frequency should meet the following:

$$F_{ESR} = < \frac{F_{SW}}{5} \quad \text{(eq. 38)}$$

F_{SW} = Switching frequency

F_{ESR} = Output capacitor ESR zero frequency

If the criteria is not met, the compensation network may not provide stability, and the output power stage must be modified.

Figure 29 shows a pseudo Type III transconductance error amplifier.

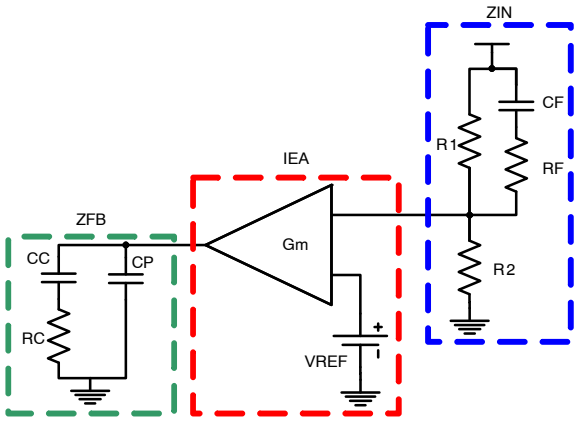


Figure 29. Pseudo Type III Transconductance Error Amplifier

The compensation network consists of the internal error amplifier and the impedance networks Z_{IN} (R_1, R_2, R_F, and C_F) and external Z_{FB} (R_C, C_C, and C_P). The compensation network has to provide a closed loop transfer function with the highest 0 dB crossing frequency to have fast response and the highest gain in DC conditions to minimize the load regulation issues. A stable control loop has a gain crossing with −20 dB/decade slope and a phase margin greater than 45°. Include worst−case component variations when

determining phase margin. To start the design, a resistor value should be chosen for R_2 from which all other components can be chosen. A good starting value is 10 kΩ.

The NCP3101C allows the output of the DC−DC regulator to be adjusted down to 0.8 V via an external resistor divider network. The regulator will maintain 0.8 V at the feedback pin. Thus, if a resistor divider circuit was placed across the feedback pin to V_{OUT}, the regulator will regulate the output voltage proportional to the resistor divider network in order to maintain 0.8 V at the FB pin.

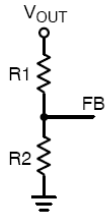


Figure 30. Feedback Resistor Divider

The relationship between the resistor divider network above and the output voltage is shown in Equation 39:

$$R_2 = R_1 \cdot \left(\frac{V_{REF}}{V_{OUT} - V_{REF}} \right) \quad \text{(eq. 39)}$$

R_1 = Top resistor divider
R_2 = Bottom resistor divider
V_{OUT} = Output voltage
V_{REF} = Regulator reference voltage

The most frequently used output voltages and their associated standard R_1 and R_2 values are listed in Table 6.

Table 6. OUTPUT VOLTAGE SETTINGS

V_O (V)	R_1 (kΩ)	R_2 (kΩ)
0.8	1.0	Open
1.0	2.55	10
1.1	3.83	10.2
1.2	4.99	10
1.5	10	11.5
1.8	12.7	10.2
2.5	21.5	10
3.3	31.6	10
5.0	52.3	10

The compensation components for the Pseudo Type III Transconductance Error Amplifier can be calculated using the method described below. The method serves to provide a good starting place for compensation of a power supply. The values can be adjusted in real time using the compensation tool comp calc, available for download at ON Semiconductor's website.

The poles of the compensation network are calculated as follows if RF is reduced to zero.

The first pole is set at the ESR zero.

$$F_{P1} = \frac{1}{2\pi \cdot R_C \cdot C_P} \quad \text{(eq. 40)}$$

The second pole is set at zero crossover frequency.

$$F_{P2} = \frac{1}{2\pi \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C_F} \quad \text{(eq. 41)}$$

The first zero should be set at the LC pole frequency.

$$F_{z1} = \frac{1}{2\pi \cdot R_C \cdot C_C} \quad \text{(eq. 42)}$$

The second zero is determined automatically by F_{P2}.

$$F_{z2} = \frac{1}{2\pi \cdot R_1 \cdot C_F} \quad \text{(eq. 43)}$$

In practical design, the feed through resistor should be at 2X the value of R_2 to minimize error from high frequency feed through noise. Using the 2X assumption, R_F will be set to 20 kΩ and the feed through capacitor can be calculated as shown below:

$$C_F = \frac{(R_1 + R_2)}{2\pi * (R_1 * R_F + R_2 * R_F + R_2 * R_1) * f_{cross}} \rightarrow 214\ pF = \frac{(31.6\ k\Omega + 10\ k\Omega)}{2 * \pi * (31.6\ k\Omega * 20\ k\Omega + 10\ k\Omega * 20\ k\Omega + 10\ k\Omega * 31.6\ k\Omega) * 27\ kHz} \quad \text{(eq. 44)}$$

C_F = Feed through capacitor
f_{cross} = Crossover frequency
R_1 = Top resistor divider
R_2 = Bottom resistor divider
R_F = Feed through resistor

The crossover of the overall feedback occurs at F_{PO}:

$$F_{PO} = \frac{(R_1 + R_F)}{(2\pi)^2 * C_F{}^2 [(R_1 + R_F) * R_2 + R_1 * R_F] * (R_F + R_1)} * \frac{V_{ramp}}{F_{LC} * V_{IN}} \quad \text{(eq. 45)}$$

$$18.9\ kHz = \frac{(31.6\ k\Omega + 20\ k\Omega)}{(2\pi)^2 * (214\ pF)^2 [(31.6\ k\Omega + 20\ k\Omega) * 10\ k\Omega + 31.6\ k\Omega * 20\ k\Omega](20\ k\Omega + 31.6\ k\Omega)} * \frac{1.1\ V}{2.35\ kHz * 12\ V}$$

C_F = Feed through capacitor
f_{cross} = Crossover frequency
F_{LC} = Frequency of the output inductor and capacitor
F_{PO} = Pole frequency
R_1 = Top of resistor divider
R_2 = Bottom of resistor divider
R_F = Feed through resistor
VCC = Input voltage
V_{ramp} = Peak−to−peak voltage of the ramp

The cross over combined compensation network can be used to calculate the transconductance output compensation network as follows:

$$C_C = \frac{1}{F_{PO}} * \frac{R_2}{R_2 * R_1} * gm \rightarrow \quad \text{(eq. 46)}$$

$$43.3\ nF = \frac{1}{18.9\ kHz} * \frac{10\ k\Omega}{10\ k\Omega + 31.6\ k\Omega} * 3.4\ mS$$

C_C = Compensation capacitor
F_{PO} = Pole frequency
gm = Transconductance of amplifier
R_1 = Top of resistor divider
R_2 = Bottom of resistor divider

$$R_C = \frac{1}{2 * F_{LC} * C_C * \left(\frac{\sqrt{2}}{2} + f_{cross} * CO_{ESR} * C_{OUT}\right)} \rightarrow \quad \text{(eq. 47)}$$

$$5.05\ k\Omega = \frac{1}{2 * 2.35\ kHz * 43.3\ nF * \left(\frac{\sqrt{2}}{2} + 27\ kHz * 12\ m\Omega * 820\ \mu F\right)}$$

C_C = Compensation capacitance
CO_{ESR} = Output capacitor ESR
C_{OUT} = Output capacitance
f_{cross} = Crossover frequency
F_{LC} = Output inductor and capacitor frequency
R_C = Compensation resistor

$$C_P = C_{OUT} * \frac{CO_{ESR}}{R_C * 2 * \pi} \rightarrow \quad \text{(eq. 48)}$$

$$309\ pF = 820\ \mu F * \frac{12\ m\Omega}{5.05\ k\Omega * 2 * \pi}$$

CO_{ESR} = Output capacitor ESR
C_{OUT} = Output capacitor
C_P = Compensation pole capacitor
R_C = Compensation resistor

Calculating Soft−Start Time

To calculate the soft start delay and soft start time, the following equations can be used.

$$t_{SSdelay} = \frac{\left(C_P + C_C\right) * 0.9\ V}{I_{SS}} \quad \text{(eq. 49)}$$

$$3.59\ ms = \frac{(0.309\ nF + 43\ nF) * 0.83\ V}{10\ \mu A}$$

C_P = Compensation pole capacitor
C_C = Compensation capacitor
I_{SS} = Soft start current

The time the output voltage takes to increase from 0 V to a regulated output voltage is t_{ss} as shown in Equation 50:

$$t_{SS} = \frac{\left(C_P + C_C\right) * D * V_{ramp}}{I_{SS}} \rightarrow \quad \text{(eq. 50)}$$

$$1.31\ ms = \frac{(0.309\ nF + 43\ nF) * 27.5\% * 1.1\ V}{10\ \mu A}$$

C_P = Compensation pole capacitor
C_C = Compensation capacitor
D = Duty ratio
I_{SS} = Soft−start current
t_{SS} = Soft−start interval
V_{ramp} = Peak−to−peak voltage of the ramp

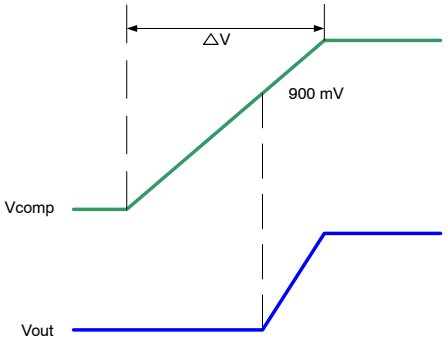


Figure 31. Soft Start Ramp

The delay from the charging of the compensation network to the bottom of the ramp is considered $t_{SSdelay}$. The total delay time is the addition of the current set delay and $t_{SSdelay}$, which in this case is 3.2 ms and 3.59 ms respectively, for a total of 6.79 ms.

Calculating Input Inrush Current

The input inrush current has two distinct stages: input charging and output charging. The input charging of a buck stage is usually not controlled, and is limited only by the input RC network and the output impedance of the upstream power stage. If the upstream power stage is a perfect voltage source, then the input charge inrush current can be depicted as shown in Figure 32 and calculated as:

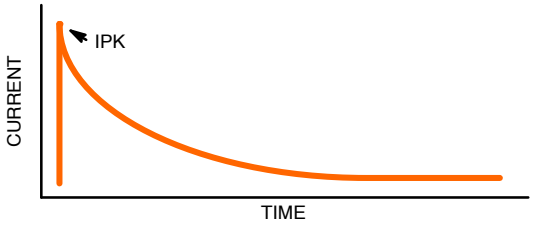


Figure 32. Input Charge Inrush Current

$$I_{ICinrush\_PK} = \frac{V_{IN}}{CIN_{ESR}} \quad \text{(eq. 51)}$$

$$120\ A = \frac{12}{0.1}$$

$$I_{ICin\_RMS} = \frac{V_{IN}}{CINESR} * \quad 0.316 * \sqrt{\frac{5 * CIN_{ESR} * C_{IN}}{t_{DELAY\_TOTAL}}} \quad \text{(eq. 52)}$$

$$5.92\ A = \frac{12\ V}{0.1\ \Omega} \quad * 0.316 * \sqrt{\frac{5 * 0.1\ \Omega * 330\ \mu F}{6.76\ ms}}$$

C_{IN} = Input capacitor
CIN_{ESR} = Input capacitor ESR
t_{DELAY_TOTAL} = Total delay interval
V_{CC} = Input voltage

Once the t_{DELAY_TOTAL} has expired, the buck converter starts to switch and a second inrush current can be calculated:

$$I_{OCinrush\_RMS} = \frac{\left(C_{OUT} + C_{LOAD}\right) * V_{OUT}}{t_{SS}} * \frac{D}{\sqrt{3}} + I_{CL} * D \quad \text{(eq. 53)}$$

C_{OUT} = Total converter output capacitance
C_{LOAD} = Total load capacitance
D = Duty ratio of the load
I_{CL} = Applied load at the output
$I_{OCinrush\_RMS}$ = RMS inrush current during start−up
t_{SS} = Soft start interval
V_{OUT} = Output voltage

From the above equation, it is clear that the inrush current is dependant on the type of load that is connected to the output. Two types of load are considered in Figure 33: a resistive load and a stepped current load.

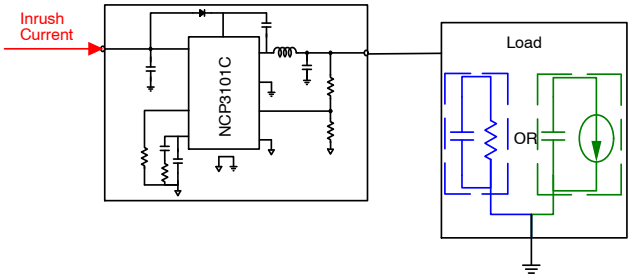


Figure 33. Load Connected to the Output Stage

If the load is resistive in nature, the output current will increase with soft start linearly which can be quantified in Equation 54.

$$I_{CLR\_RMS} = \frac{1}{\sqrt{3}} * \frac{V_{OUT}}{R_{OUT}} \qquad I_{CR\_PK} = \frac{V_{OUT}}{R_{OUT}} \quad \text{(eq. 54)}$$

$$191\ mA = \frac{1}{\sqrt{3}} * \frac{3.3\ V}{10\ \Omega} \qquad 330\ mA = \frac{3.3\ V}{10\ \Omega}$$

R_{OUT} = Output resistance
V_{OUT} = Output voltage
I_{CLR_RMS} = RMS resistor current
I_{CR_PK} = Peak resistor current

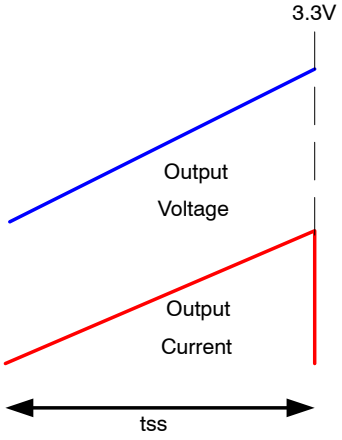


Figure 34. Resistive Load Current

Alternatively, if the output has an under voltage lockout, turns on at a defined voltage level, and draws a consistent current, then the RMS connected load current is:

$$I_{CLKI} = \sqrt{\frac{V_{OUT} - V_{OUT\_TO}}{V_{OUT}}} * I_{OUT} \quad \text{(eq. 55)}$$

$$835\ mA = \sqrt{\frac{3.3\ V - 1.0\ V}{3.3\ V}} * 1\ A$$

I_{OUT} = Output current
V_{OUT} = Output voltage
V_{OUT_TO} = Output voltage load turn on

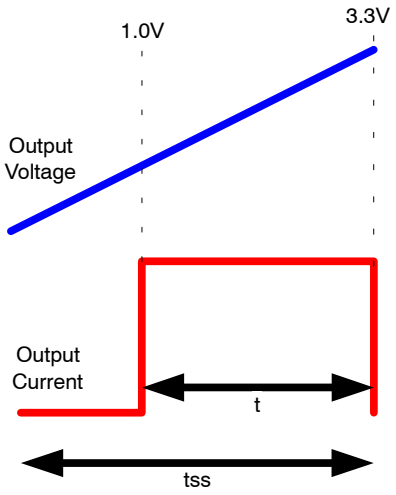


Figure 35. Voltage Enable Load Current

If the inrush current is higher than the steady state input current during max load, then an input fuse should be rated accordingly using I^2t methodology.

Layout Considerations

When designing a high frequency switching converter, layout is very important. Using a good layout can solve many problems associated with these types of power supplies as transients occur.

External compensation components (R1, C9) are needed for converter stability. They should be placed close to the NCP3101C. The feedback trace is recommended to be kept as far from the inductor and noisy power traces as possible. The resistor divider and feedback acceleration circuit (R2, R3, R6, C13) are recommended to be placed near output feedback (Pin 16, NCP3101C).

Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. The interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located together as close as possible using ground plane construction or single point grounding. The inductor and output capacitors should be located together as close as possible to the NCP3101C.

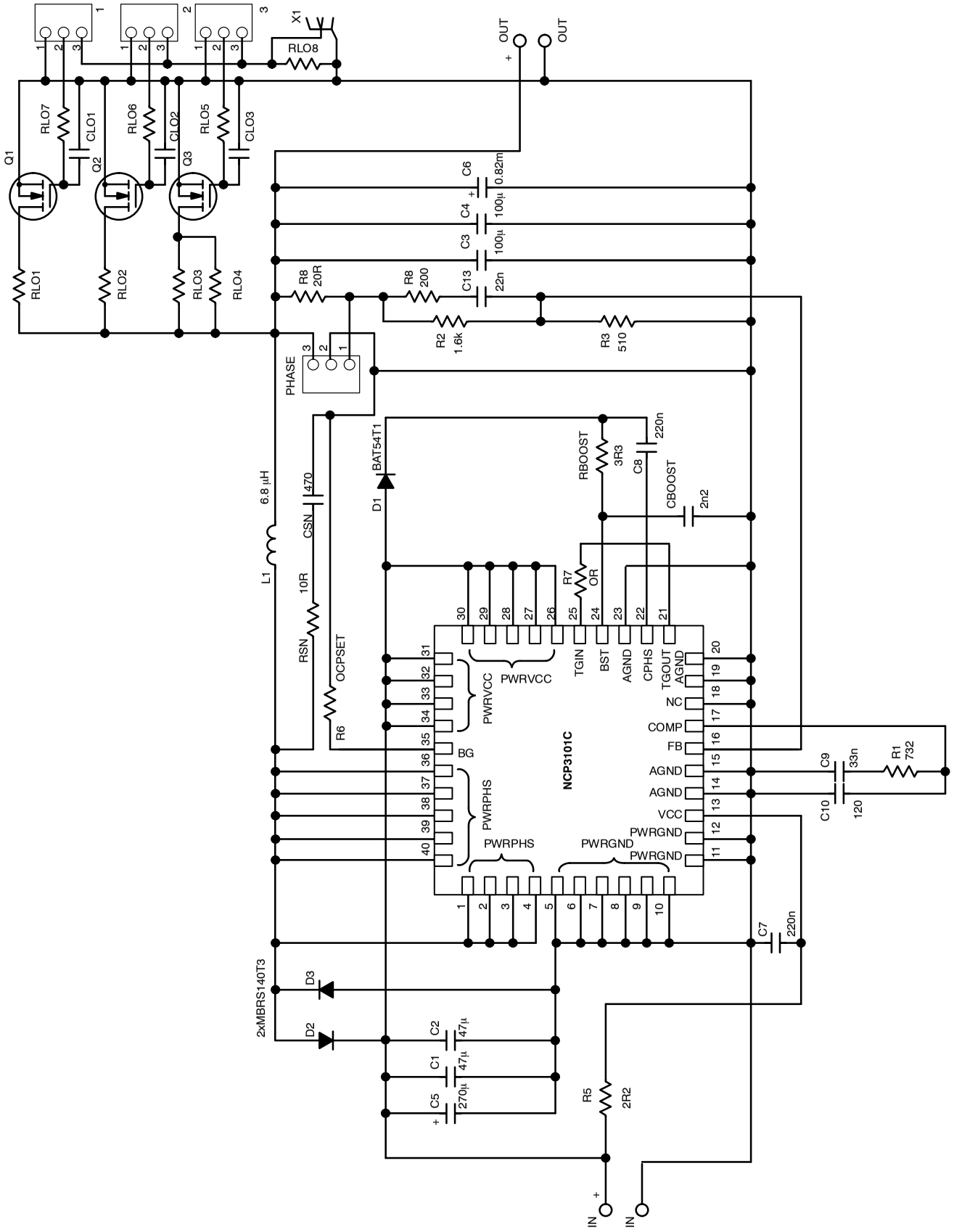


Figure 36. Schematic Diagram of NCP3101C Evaluation Board

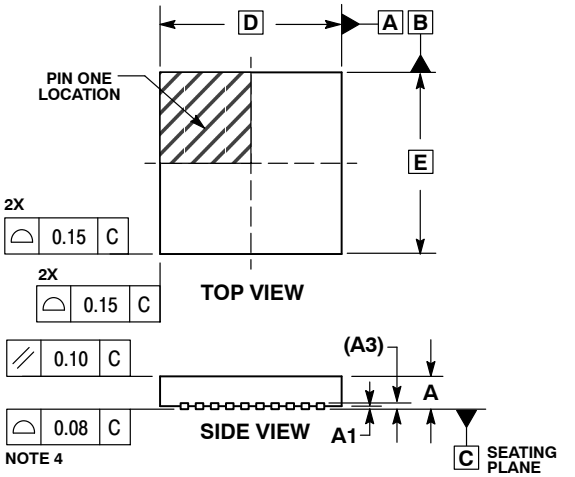
ORDERING INFORMATION

Device	Temperature Grade	Package	Shipping†
NCP3101CMNTXG	For −40°C to +125°C	QFN40 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

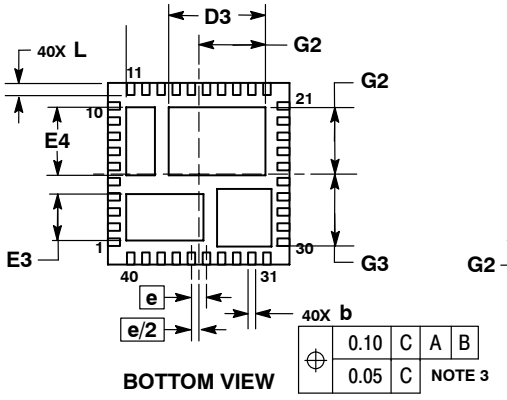
PACKAGE DIMENSIONS

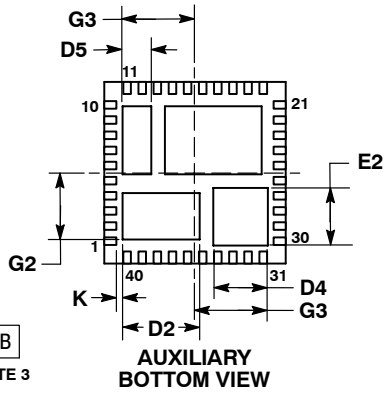
QFN40 6x6, 0.5P
CASE 485AK−01
ISSUE A



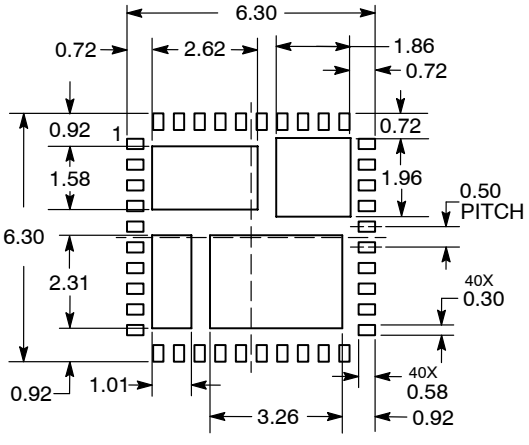
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	−−−	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	2.45	2.65
D3	3.10	3.30
D4	1.70	1.90
D5	0.85	1.05
E	6.00 BSC	
E2	1.80	2.00
E3	1.43	1.63
E4	2.15	2.35
e	0.50 BSC	
G2	2.10	2.30
G3	2.30	2.50
K	0.20	−−−
L	0.30	0.50





SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.