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# Adjustable Front End Overvoltage Protection Controller with Protected Vbus Output

The NCP392C is an overvoltage front end protection controller and is able to disconnect the systems from its output pin in case wrong input operating conditions are detected, up to +28 V. Thanks to this device using internal NMOS, no external device is necessary, reducing the system cost and the PCB area of the application board.

Internal OVLO threshold is available, or can be adjusted if an external resistor bridge is used.

At power up  $(\overline{EN} \text{ pin} = \text{low level})$ , the Vout turns on tstart time after internal timer elapsed.

The NCP392C features an  $\overline{ACOK}$  pin that indicates faulty condition.

#### **Features**

- Over-voltage Protection Up to + 28 V
- On-chip Low  $R_{DS(on)}$  NMOS Transistors: Typical 34 m $\Omega$
- Over-voltage Lockout (OVLO)
- Externally Adjustable OVLO
- Internal 15 ms Startup Delay
- Shutdown EN Input
- ACOK Status Pin
- + 100 V Surge Capability, in Compliance with IEC61000-4-5 Standard
- Compliance to IEC61000-4-2 (Level 4) Standard 8 kV (Contact) 15 kV (Air)
- ESD Ratings:

Machine Model = B (200 V) Human Body Model = 2 (2 kV)

- CSP-12 Package 1.3 x 2.0 mm, 0.4 mm Pitch
- This is a Pb-Free Device

#### **Typical Applications**

- Cell Phones
- Tablets
- Camera Phones
- Digital Still Cameras
- Personal Digital Applications



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#### WLCSP 12 FCC SUFFIX CASE 567JM





392Cx = Specific Device Number (x = R or S)

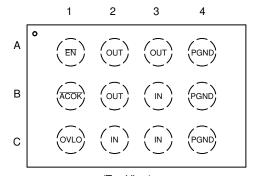
A = Assembly Location

Y = Year

WW = Work Week

= Pb-Free Package

#### **PIN CONNECTION**



(Top View)

#### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 9 of this data sheet.

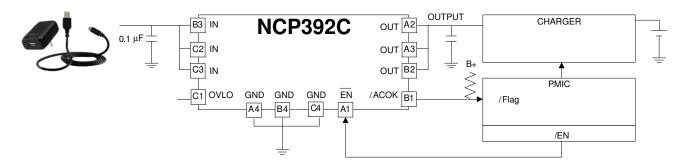


Figure 1. Typical Application Circuit

# **FUNCTIONAL BLOCK DIAGRAM**

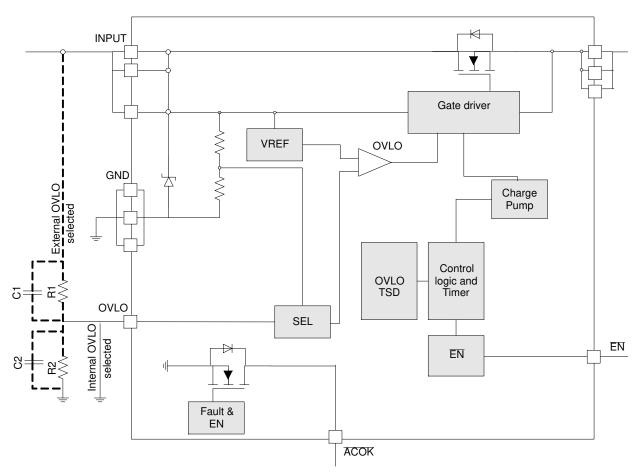


Figure 2. Functional Block Diagram

# **PIN FUNCTION DESCRIPTION**

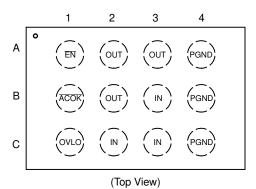


Figure 3. Pinout

**Table 1. NCP392 PIN DESCRIPTION** 

Pin	Pin Name	Туре	Description			
A1	EN	I/O	Enable pin bar. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input.			
A2, A3, B2	OUT	OUTPUT	Output voltage pins. These pins follow IN pins, with debounce time, when "no fault" are detected. The outputs are disconnected from the Vin power supply when the input voltage is below UVLO, above OVLO threshold or internal thermal protection is exceeded. The three OUT pins must be hardwired together and used for power dissipation.			
A4, B4, C4	PGND	POWER	Ground. The three GND pins must be hardwired together and connect to the system GND.			
B1	ACOK	OUTPUT	ACOK pin: fault indication pin. Open drain. This pied in tied	1	$V_{IN} < V_{UVLO}$ or $V_{IN} \ge V_{OVLO}$	
			low if Vin is within UVLO and OVLO range.	0	Voltage stable	
B3, C2, C3	IN	POWER	Input voltage pins. These pins are connected to the power supply. The three IN pins must be hardwired together.			
C1	OVLO	INPUT	External OVLO Adjustment. Connect external resistor bridge to OVLO pin to select a different OVLO threshold. Connect OVLO pin to GND if not used. In this case internal OVLO will be selected.			

**Table 2. MAXIMUM RATINGS** 

Rating	Symbol	Value	Unit
Minimum Voltage (IN, OVLO to GND)	Vmin <sub>IN</sub>	-0.3	V
Minimum Voltage (All others to GND)	Vmin	-0.3	V
Maximum Voltage (IN to GND)	Vmax <sub>IN</sub>	29	V
Maximum Voltage (OVLO to GND)	Vmax <sub>OVLO</sub>	14	V
Maximum Voltage (OUT to GND)	Vmax <sub>OUT</sub>	22	V
Maximum Voltage (All others to GND)	Vmax	7	V
Maximum DC current	Imax	4.5	Α
Peak input current	lpeak	8	Α
Thermal Resistance, Junction-to-Air	$R_{ heta JA}$	70	°C/W
Operating Ambient Temperature Range	T <sub>A</sub>	-40 to +85	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Junction Operating temperature	T <sub>J</sub>	+ 125	°C
ESD Withstand Voltage (IEC 61000–4–2) Human Body Model (HBM), model = 2 (Note 1) Machine Model (MM) model = B (Note 2)	V <sub>esd</sub>	15 kV air, 8 kV contact 2000 V 200 V	kV V V
Moisture Sensitivity	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.

2. Machine Model, 200 pF discharged through all pins following specification JESD22/A115

# **Table 3. ELECTRICAL CHARACTERISTICS**

Min / Max limits values ( $-40^{\circ}C < T_A < +85^{\circ}C$ ) and  $V_{in} = +5$  V (Unless otherwise noted). Typical values are  $T_A = +25^{\circ}C$ .

Imput Voltage Range   V <sub>sin</sub> V <sub>OVLO</sub>   V <sub>sin</sub> rising   V <sub>sin</sub> V <sub>oVlo</sub>   V <sub>sin</sub> rising   V <sub>sin</sub> toltage Lockout   UVLO   V <sub>sin</sub> rising   V <sub>sin</sub> falling   V <sub></sub>	Characteristics	Symbols	Conditions		Min	Тур	Max	Unit
United	Input Voltage Range	$V_{in}, V_{OVLO}$			2.8		28	V
Internal Over voltage   OVLO   OVLO   OVLO   Pin tied to GND − 25° C   13.4   13.8   14.2   14.2   15.5   16.5	Under voltage Lockout	UVLO	V <sub>in</sub> rising				2.8	V
Cockout threshold   Covide   Continued to GND   Copin tied tied to GND   Copin tied tied to GND   Copin tied to GND   Copin tied tied to GND   Copin tied tied to GND   Copin tied to GND   Copin tied tied		UVLO <sub>hyst</sub>	V <sub>in</sub> falling		-	60	-	mV
NCP392CS   15   15.5   16   15.5   16   15.5   16   15.5   16   15.5   16   15.5   16   15.5   16   15.5   16   15.5   16   15.5   16   15.5   16   15.5   16   15.5   16   15.5   15   15.5   16   15.5   15   15.5   16   15.5   15   15.5   16   15.5   15   15.5   15   15.5   15   1		OVLO		NCP392CR	13.4	13.8	14.2	V
hysteresis   OVLO pin tied to GND - 25°C	Lockout threshold		OVLO pin tied to GND = 25°C	NCP392CS	15	15.5	16	
External Adjustable OVLO   Cover-Voltage Lockout   Au   Au   Au   Au   Au   Au   Au		OVLO <sub>hyst</sub>			1.5		2.5	%
External Adjustable OVLO   Cover—Voltage Lockout Hysteresis   OVLOEXThyst Hysteresis   Vin falling   Cover—Voltage Lockout Hysteresis   OVLOSEL   Vin falling   Cover—Voltage Lockout Hysteresis   OVLOSEL   Vin falling   Cover—Voltage Lockout Hysteresis   OvloseL   OVLOSEL   Over—Voltage Lockout Hysteresis   OvloseL   Over—Voltage Cover—Voltage Lockout Hysteresis   OvloseLect tereshold   OvloseLect Lockout Hysteresis   OvloseLect Lockout Hysteresis   OvloseLect Lockout Hybrid Hysteresis   OvloseLect Lockout Hybrid	External OVLO Reference	OVLO_EXT		NCP392CR	1.12	1.20	1.24	V
Over-Voltage Lockout Hysteresis         OVLOEXThyst Vin falling         2         %           External OVLO select threshold         OVLOSEL Vin versus Vout Resistance         R <sub>DSon</sub> V <sub>in</sub> = 5 V, EN = GND, -40°C < T <sub>J</sub> < 125°C				NCP392CS	1.18	1.221	1.26	
Hysteresis   External OVLO select threshold   OVLO SEL   OVER SENSE OVER SENSE OVER SENSE OVLO SEL   OVLO S	External Adjustable OVLO				4		20	V
threshold         Vin versus Vout Resistance         R <sub>DSon</sub> V <sub>in</sub> = 5 V, EN = GND, −40°C < T <sub>J</sub> < 125°C         34         50         mΩ           Supply Quiescent Current         I <sub>DD</sub> No load, EN = 0.4 V         58         100         μA           Standby Current         I <sub>STB</sub> No load, EN = 1.2 V,         6         μA           OVLO Supply current         I <sub>IN_OVLO</sub> V <sub>OVLO</sub> = 3 V, V <sub>IN</sub> = 5 V, V <sub>OUT</sub> = 0 V         60         100         μA           VLO select leakage         I <sub>OVLO</sub> V <sub>OVLO</sub> = 3 V, V <sub>IN</sub> = 5 V, V <sub>OUT</sub> = 0 V         60         100         μA           LOGIC           EN Voltage High         V <sub>IH</sub> 1.2         V         V           EN Voltage Low         V <sub>IL</sub> V         V		OVLO <sub>EXThyst</sub>	V <sub>in</sub> falling			2		%
Supply Quiescent Current         IDD         No load, EN = 0.4 V         58         100         μA           Standby Current         IsTB         No load, EN = 1.2 V,         6         μA           OVLO Supply current         In_OVLO         VOLO = 3 V, VIN = 5 V, VOUT = 0 V         60         100         μA           OVLO select leakage         IoVLO         VOLO = 3 V, VIN = 5 V, VOUT = 0 V         60         100         μA           LOGIC           EN Voltage High         VIH         1.2         V         V           EN Voltage Low         VIL         0.4         V           ACOK Output Low Voltage         VoL         IsINK = 1 mA         0.4         V           TIMINGS         TIMINGS         15         ms           Start up time         ItSTART         From Vin > 2.8 V to 10% Vout, EN low         15         ms           Enable time         ItEN         Vin present, From EN high to low, 10% Vout         15         ms           Soft Start         ItalisE         From 10% to 90% of Vout, C load 100 μF, Rload, 100 Ω, EN low         1         ms           ACOK Start up time         ItalisE         From Vin Valid to ACOK tied low, EN low or high         30         ms           Turn off time         Ital		OVLO <sub>SEL</sub>			0.2		0.3	V
Standby Current   ISTB   No load, EN = 1.2 V,   60   μA     OVLO Supply current   I <sub>IN_OVLO</sub>   V <sub>OVLO</sub> = 3 V, V <sub>IN</sub> = 5 V, V <sub>OUT</sub> = 0 V   60   100   μA     OVLO select leakage   I <sub>OVLO</sub>   100   nA     LOGIC     EN Voltage High   V <sub>IH</sub>   1.2   V     EN Voltage Low   V <sub>IL</sub>   0.4   V     ACOK Output Low Voltage   V <sub>OL</sub>   I <sub>SINK</sub> = 1 mA   0.4   V     TIMINGS     Start up time   I <sub>START</sub>   From V <sub>In</sub> > 2.8 V to 10% V <sub>Out</sub> , EN low   15   ms     Enable time   I <sub>START</sub>   From 10% to 90% of V <sub>Out</sub> , C load 100 μF, Rload, 100 Ω, EN low   1   ms     ACOK Start up time   I <sub>START2</sub>   From Vin Valid to ACOK tied low, EN low or high   30   ms     Turn off time   I <sub>OFF</sub>   Surge off time   100   ns     Disable time   I <sub>OIS</sub>   From EN > 1.2 V to 90% V <sub>Out</sub> , No load   20   μS     TSD   TSD   140   °C     Thermal shutdown   TSD   140   °C     Thermal shutdown   TSD   140   °C     Tour off time   Tou	Vin versus Vout Resistance	R <sub>DSon</sub>	V <sub>in</sub> = 5 V, <del>EN</del> = GND, -40°C <	T <sub>J</sub> < 125°C		34	50	mΩ
OVLO Supply current         I <sub>IN_OVLO</sub> V <sub>OVLO</sub> = 3 V, V <sub>IN</sub> = 5 V, V <sub>OUT</sub> = 0 V         60         100         μA           OVLO select leakage         I <sub>OVLO</sub> 100 InA	Supply Quiescent Current	I <sub>DD</sub>	No load, EN = 0.4 \	/		58	100	μΑ
OVLO select leakage   IoVLO	Standby Current	I <sub>STB</sub>	No load, EN = 1.2 V	<b>'</b> ,			6	μΑ
LOGIC           EN Voltage High         V <sub>IH</sub> 1.2         V           EN Voltage Low         V <sub>IL</sub> 0.4         V           ACOK Output Low Voltage         V <sub>OL</sub> I <sub>SINK</sub> = 1 mA         0.4         V           TIMINGS           Start up time         t <sub>START</sub> From V <sub>in</sub> > 2.8 V to 10% V <sub>out</sub> , EN low         15         ms           Enable time         t <sub>EN</sub> V <sub>in</sub> present, From EN high to low, 10% V <sub>out</sub> 15         ms           Soft Start         t <sub>RISE</sub> From 10% to 90% of V <sub>out</sub> , C load 100 μF, Rload, 100 Ω, EN low         1         ms           ACOK Start up time         t <sub>START2</sub> From Vin Valid to ACOK tied low, EN low or high         30         ms           Turn off time         t <sub>OFF</sub> Surge off time         100         ns           Disable time         t <sub>DIS</sub> From EN >1.2 V to 90% V <sub>out</sub> , No load         20         μs           OVLO Turn off time         t <sub>OVLO</sub> V <sub>in</sub> rising 2 V/μs         1.5         μs           TSD	OVLO Supply current	I <sub>IN_OVLO</sub>	$V_{OVLO} = 3 \text{ V}, V_{IN} = 5 \text{ V}, V_{O}$	<sub>UT</sub> = 0 V		60	100	μΑ
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	OVLO select leakage	l <sub>OVLO</sub>					100	nA
	LOGIC							
ACOK Output Low VoltageVOL $I_{SINK} = 1 \text{ mA}$ 0.4VTIMINGSStart up time $t_{START}$ $From V_{in} > 2.8 \text{ V to } 10\% V_{out}$ , $EN low$ 15msEnable time $t_{EN}$ $V_{in}$ present, $From EN$ high to low, $10\% V_{out}$ 15msSoft Start $t_{RISE}$ $From 10\%$ to $90\%$ of $V_{out}$ , $C load 100 \mu F$ , $Rload$ , $100 \Omega$ , $EN low$ 1msACOK Start up time $t_{START2}$ $From Vin Valid to ACOK tied low, EN low or high30msTurn off timet_{OFF}Surge off time100nsDisable timet_{DIS}From EN > 1.2 \text{ V to } 90\% V_{out}. No load20\musOVLO Turn off timet_{OVLO}V_{in} rising 2 V/\mu s1.5\musTSDThermal shutdownTSD140°C$	EN Voltage High	V <sub>IH</sub>			1.2			V
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	EN Voltage Low	V <sub>IL</sub>					0.4	V
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	ACOK Output Low Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 1 mA			0.4		V
Enable time $t_{EN}$ $V_{in}$ present, From EN high to low, 10% $V_{out}$ 15       ms         Soft Start $t_{RISE}$ From 10% to 90% of $V_{out}$ , C load 100 μF, Rload, 100 Ω, EN low       1       ms         ACOK Start up time $t_{START2}$ From Vin Valid to $\overline{ACOK}$ tied low, $\overline{EN}$ low or high       30       ms         Turn off time $t_{OFF}$ Surge off time       100       ns         Disable time $t_{DIS}$ From EN >1.2 V to 90% $V_{out}$ . No load       20       μs         OVLO Turn off time $t_{OVLO}$ $V_{in}$ rising 2 $V/\mu$ s       1.5       μs         TSD       140       °C	TIMINGS							
Soft Start $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Start up time	t <sub>START</sub>	From V <sub>in</sub> > 2.8 V to 10% V <sub>ou</sub>	<sub>it,</sub> EN low		15		ms
Rload, 100 Ω, EN low       Rload, 100 Ω, EN low       30       ms         ACOK Start up time $t_{START2}$ From Vin Valid to $\overline{ACOK}$ tied low, $\overline{EN}$ low or high       30       ms         Turn off time $t_{OFF}$ Surge off time       100       ns         Disable time $t_{DIS}$ From EN >1.2 V to 90% $V_{out}$ . No load       20 $\mu$ s         OVLO Turn off time $t_{OVLO}$ $V_{in}$ rising 2 V/ $\mu$ s       1.5 $\mu$ s         TSD       140 $^{\circ}$ C	Enable time	t <sub>EN</sub>	V <sub>in</sub> present, From EN high to low, 10% V <sub>out</sub>			15		ms
Turn off time $t_{OFF}$ Surge off time 100 ns Disable time $t_{DIS}$ From EN >1.2 V to 90% $V_{out}$ . No load 20 $\mu_S$ OVLO Turn off time $t_{OVLO}$ $V_{in}$ rising 2 $V/\mu_S$ 1.5 $\mu_S$ TSD 140 °C	Soft Start	t <sub>RISE</sub>	From 10% to 90% of $V_{out}$ , C load 100 $\mu$ F, Rload, 100 $\Omega$ , $\overline{EN}$ low			1		ms
Disable time $t_{DIS}$ From EN >1.2 V to 90% $V_{out}$ . No load 20 $\mu s$ OVLO Turn off time $t_{OVLO}$ $V_{in}$ rising 2 V/ $\mu s$ 1.5 $\mu s$ TSD Thermal shutdown TSD 140 $^{\circ}C$	ACOK Start up time	tSTART2	From Vin Valid to ACOK tied low, EN low or high			30		ms
OVLO Turn off time $t_{OVLO}$ $V_{in}$ rising 2 V/ $\mu$ s 1.5 $\mu$ s TSD Thermal shutdown TSD 140 °C	Turn off time	t <sub>OFF</sub>	Surge off time			100		ns
TSD  Thermal shutdown TSD 140 °C	Disable time	t <sub>DIS</sub>	From EN >1.2 V to 90% V <sub>out.</sub> No load			20		μS
Thermal shutdown TSD 140 °C	OVLO Turn off time	t <sub>OVLO</sub>	V <sub>in</sub> rising 2 V/μs			1.5		μS
	TSD							
Thermal shutdown rearming TSD rearm 115 °C	Thermal shutdown	TSD				140		°C
	Thermal shutdown rearming TSD rearm			115		°C		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Please contact your ON Semiconductor representative for additional OVLO threshold.

Electrical parameters are guaranteed by correlation across the full range of temperature.

#### Operation

The NCP392C provides over-voltage protection for positive voltage surge, up to + 28 V. An additional clamp, between IN and GND, protects the part against surge test, in compliance with IEC 61000-4-5 standard.

A ACOK open drain fault indicator is provided. This signal indicates whether input voltage is within the valid range.

#### Under-voltage Lockout (UVLO)

To ensure proper operation under any conditions, the device has a built—in under—voltage lock out (UVLO) circuit. This circuit has a built—in hysteresis to provide noise immunity to transient conditions.

#### Over-voltage Lockout (OVLO)

To protect connected systems on Vout pin from over-voltage, the device has a built-in over-voltage lock out (OVLO) circuit. During over-voltage condition, the output remains disabled until the input voltage is above OVLO – hysteresis.

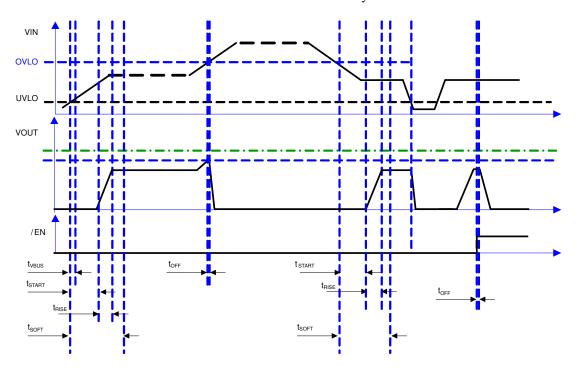


Figure 4. UVLO, OVLO and EN Functionality

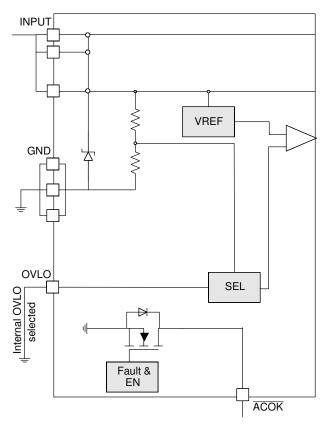


Figure 5. External Connection to GND of OVLO

If OVLO pin is not grounded, and by adding external bridge resistor on OVLO pin, between IN and GND, overvoltage protection can be adjusted as following:

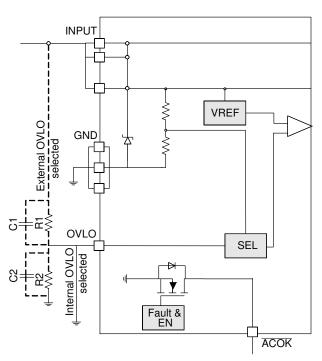


Figure 6. External Connection to Resistor Bridge of OVLO

$$NEW\_OVLO_{TH} = \frac{OVLO_{EXT} \times (R_1 + R_2)}{R_2} \text{ (eq. 1)}$$

With: OVLO<sub>EXT</sub> = 1.221 V Typical (OVLO External Reference)

Example:

NEW\_OVLO<sub>TH</sub> target 12 V.

(eq. 2)  
R1 = R2 × 
$$\left(\frac{\text{OVLO}}{1.221} - 1\right)$$
 = R2 ×  $\left(\frac{12}{1.221} - 1\right)$  = 8.828 × R2

Taking into account external input bridge doesn't have excessive current consumption, and 1% is recommended:

R2 arbitrarilly fixed at 1.05 M $\Omega$ .

 $R1 = 9.269 \text{ M}\Omega \text{ (9.31 M}\Omega \text{ standard value)}$ 

Obtained typical OVLO = 12.04 V

 $C_1$  and  $C_2$  should be selected in such a way that the time constant  $R_1C_1 = R_2C_2$ .

# **EN** Input

To enable normal operation, the  $\overline{EN}$  pin has to be at low level. There is neither internal pull up, nor internal pull down connected to  $\overline{EN}$  pin. If not externally driven, this pin and so NCP392C switch are undefined state.

A high level on the pin, disconnects OUT pin from IN pin.

**Table 4. CONTROL LOGIC MODES** 

OVP	State	OVLO EXT		
_	92Cx	Low	High	
ĒN	Low	ON T <sub>start</sub> 15 ms	OFF	
	High	OFF	OFF	

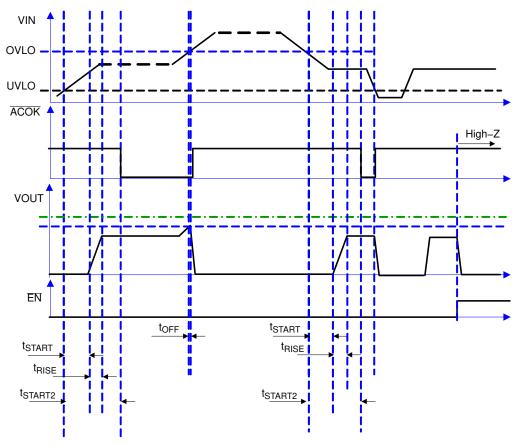


Figure 7. EN and ACOK Associated Timers

## **ACOK** Pin

The NCP392C version integrates a  $\overline{\text{ACOK}}$  status indicator. This is a drain pin tied low when no fault is present (no TSd, no under voltage, no over voltage).

When disabled, the  $\overline{ACOK}$  feature is disabled too and the output pin is in high impedance mode.

#### **Thermal Shutdown Protection**

In case of internal overheating, the integrated thermal shutdown (TSD) protection allows to open the internal MOSFET in order to instantaneously decrease the device temperature.

Embedded hysteresis allows to reengage the MOSFET when the junction temperature decreases.

If the fault event is still present, the temperature increases again and engages the thermal shutdown one more time until fault event disappeared.

## **PCB Recommendations**

To limit internal power dissipation, PCB routing must be carefully done to improve current capability.

The NCP392C is declined in a CSP package. So power dissipation can be decreased on each pin connection but main thermal area must be as large as possible around IN and OUT pins. Taking into account and respectively, four IN and OUT pins must be hardwired together on the PCB.

Maximum power dissipation can be calculated with the following formula:

$$T_J - T_A = R_{\theta JA} \times P_d$$
 (eq. 3)

T<sub>I</sub>: junction temperature

T<sub>A</sub>: ambient temperature

 $R_{\theta JA}\!\!:$  thermal resistance of the junction to air through the case and board.

 $P_d$ : power dissipation =  $R_{DS(on)} \times I^2$ 

#### **ESD Tests**

The NCP392C fully supports the IEC61000–4–2, level 4 (Input pin, 1  $\mu$ F mounted on board).

That means, in Air condition,  $V_{in}$  has a  $\pm 15$  kV ESD protected input. In Contact condition,  $V_{in}$  has  $\pm 8$  kV ESD protected input.

Please refer to Figure 8 to see the IEC 61000-4-2 electrostatic discharge waveform.

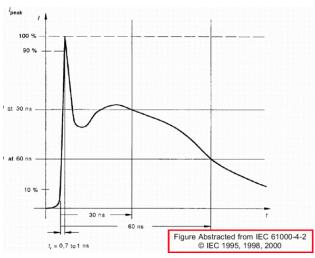


Figure 8.  $I_{peak} = f(t) / IEC61000-4-2$ 

# **USB OTG Support**

When used in an application that has to supply voltage to an external accessory (i.e. USB OTG), the part is able to supply 1.8 A to the accessory. If  $V_{\rm IN}=0$  V when +5.0 V OTG is applied to the OUT pin, current will flow through the MOSFET body diode and, as soon as the output voltage will be higher than the  $V_{\rm UVLO}$  voltage (2.8 V) plus Body diode forward voltage, the part will turn fully ON and current will be supplied to the accessory with minimum drop.

In that case, the ACOK pin will keep High-Z state.

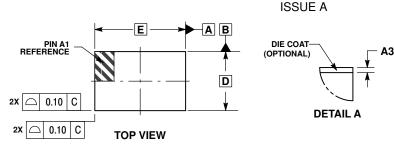
#### **ORDERING INFORMATION**

Device	Marking	Option	Package	Shipping <sup>†</sup>
NCP392CRFCCT1G	392CR	OVLO 13.8 V	WLCSP	3000 / Tape & Reel
NCP392CSFCCT1G	392CS	OVLO 15.5 V	(Pb-Free)	Jooo / Tape & neer

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

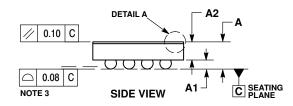
# WLCSP12, 1.3x2.0 CASE 567JM



#### NOTES:

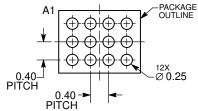
- DIMENSIONING AND TOLERANCING PER
  ASME V14 5M 1994
- ASME Y14.5M, 1994. 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

CROWING OF SOLDER E				
	MILLIMETERS			
DIM	MIN MAX			
Α		0.60		
A1	0.17	0.23		
A2	0.36 REF			
A3	0.04 REF			
b	0.24	0.30		
D	1.26	1.31		
E	2.01	2.04		
е	0.40 BSC			



# 12X Ø b 0.05 C A B C B A BOTTOM VIEW

#### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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