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NCP4305

Secondary Side Synchronous Rectification Driver for High Efficiency SMPS Topologies

The NCP4305 is high performance driver tailored to control a synchronous rectification MOSFET in switch mode power supplies. Thanks to its high performance drivers and versatility, it can be used in various topologies such as DCM or CCM flyback, quasi resonant flyback, forward and half bridge resonant LLC.

The combination of externally adjustable minimum off-time and on-time blanking periods helps to fight the ringing induced by the PCB layout and other parasitic elements. A reliable and noise less operation of the SR system is insured due to the Self Synchronization feature. The NCP4305 also utilizes Kelvin connection of the driver to the MOSFET to achieve high efficiency operation at full load and utilizes a light load detection architecture to achieve high efficiency at light load.

The precise turn−off threshold, extremely low turn−off delay time and high sink current capability of the driver allow the maximum synchronous rectification MOSFET conduction time and enables maximum SMPS efficiency. The high accuracy driver and 5 V gate clamp enables the use of GaN FETs.

Features

- Self−Contained Control of Synchronous Rectifier in CCM, DCM and QR for Flyback, Forward or LLC Applications
- Precise True Secondary Zero Current Detection
- Typically 12 ns Turn off Delay from Current Sense Input to Driver
- Rugged Current Sense Pin (up to 200 V)
- Ultrafast Turn−off Trigger Interface/Disable Input (7.5 ns)
- Adjustable Minimum ON−Time
- Adjustable Minimum OFF-Time with Ringing Detection
- Adjustable Maximum ON−Time for CCM Controlling of Primary QR Controller
- Improved Robust Self Synchronization Capability
- 8 A / 4 A Peak Current Sink / Source Drive Capability
- Operating Voltage Range up to V_{CC} = 35 V
- Automatic Light−load & Disable Mode
- Adaptive Gate Drive Clamp
- GaN Transistor Driving Capability (options A and C)
- Low Startup and Disable Current Consumption
- Maximum Operation Frequency up to 1 MHz
- SOIC-8 and DFN−8 (4x4) and WDFN8 (2x2) Packages
- These are Pb−Free Devices

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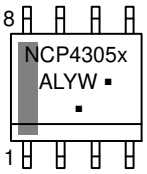
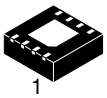
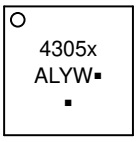
MARKING DIAGRAMS

SOIC−8
D SUFFIX
CASE 751

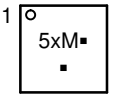




DFN8
MN SUFFIX
CASE 488AF



WDFN8
MT SUFFIX
CASE 511AT



4305x	= Specific Device Code x = A, B, C, D or Q
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
M	= Date Code
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 49 of this data sheet.

Typical Applications

- Notebook Adapters
- High Power Density AC/DC Power Supplies (Cell Phone Chargers)
- LCD TVs
- All SMPS with High Efficiency Requirements

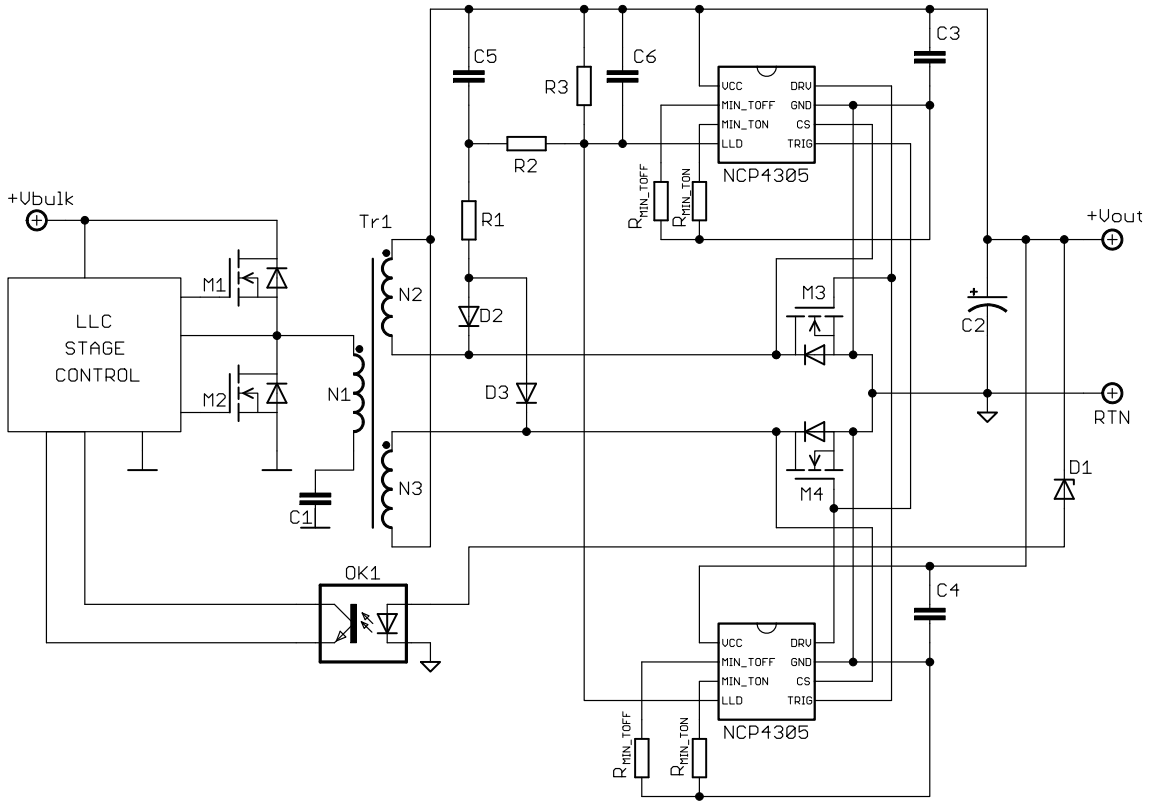


Figure 1. Typical Application Example – LLC Converter with Optional LLD and Trigger Utilization

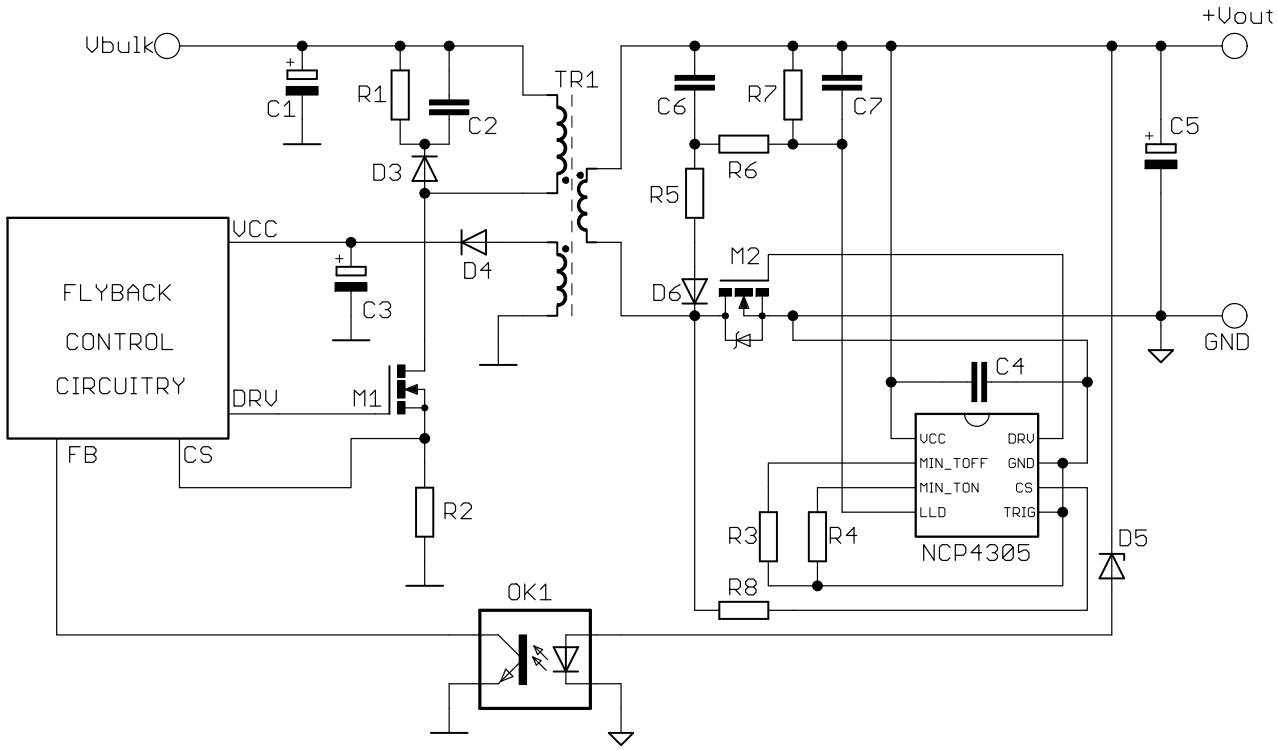


Figure 2. Typical Application Example – DCM, CCM or QR Flyback Converter with optional LLD and Disabled TRIG

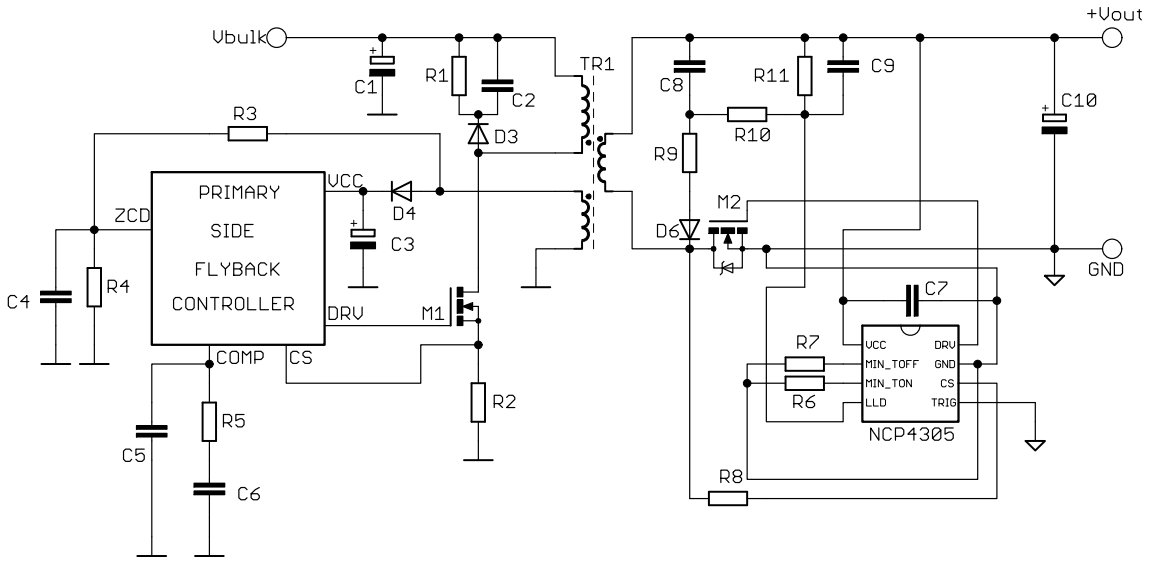


Figure 3. Typical Application Example – Primary Side Flyback Converter with optional LLD and Disabled TRIG

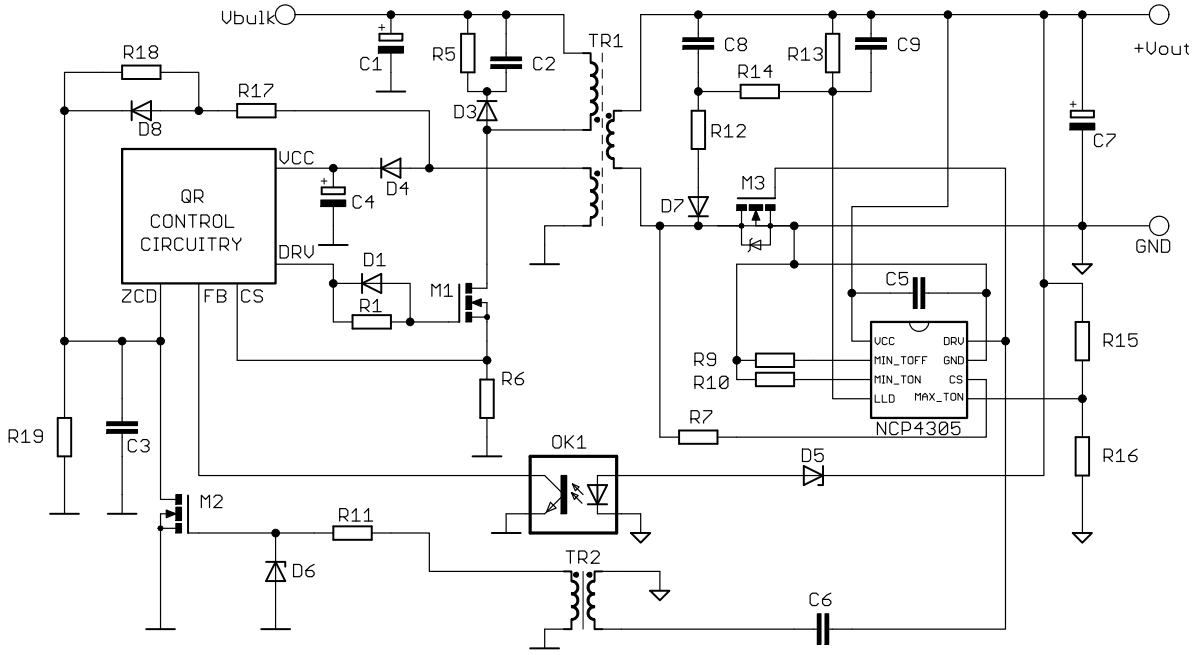


Figure 4. Typical Application Example – QR Converter – Capability to Force Primary into CCM Under Heavy Loads utilizing MAX–TON

PIN FUNCTION DESCRIPTION

ver. A, B, C, D	ver. Q	Pin Name	Description
1	1	VCC	Supply voltage pin
2	2	MIN_TOFF	Adjust the minimum off time period by connecting resistor to ground.
3	3	MIN_TON	Adjust the minimum on time period by connecting resistor to ground.
4	4	LLD	This input modulates the driver clamp level and/or turns the driver off during light load conditions.
5	–	TRIG/DIS	Ultrafast turn−off input that can be used to turn off the SR MOSFET in CCM applications in order to improve efficiency. Activates disable mode if pulled−up for more than 100 μs.
6	6	CS	Current sense pin detects if the current flows through the SR MOSFET and/or its body diode. Basic turn−off detection threshold is 0 mV. A resistor in series with this pin can decrease the turn off threshold if needed.
7	7	GND	Ground connection for the SR MOSFET driver and V_{CC} decoupling capacitor. Ground connection for minimum on and off time adjust resistors, LLD and trigger inputs. GND pin should be wired directly to the SR MOSFET source terminal/soldering point using Kelvin connection. DFN8 exposed flag should be connected to GND
8	8	DRV	Driver output for the SR MOSFET
–	5	MAX_TON	Adjust the maximum on time period by connecting resistor to ground.

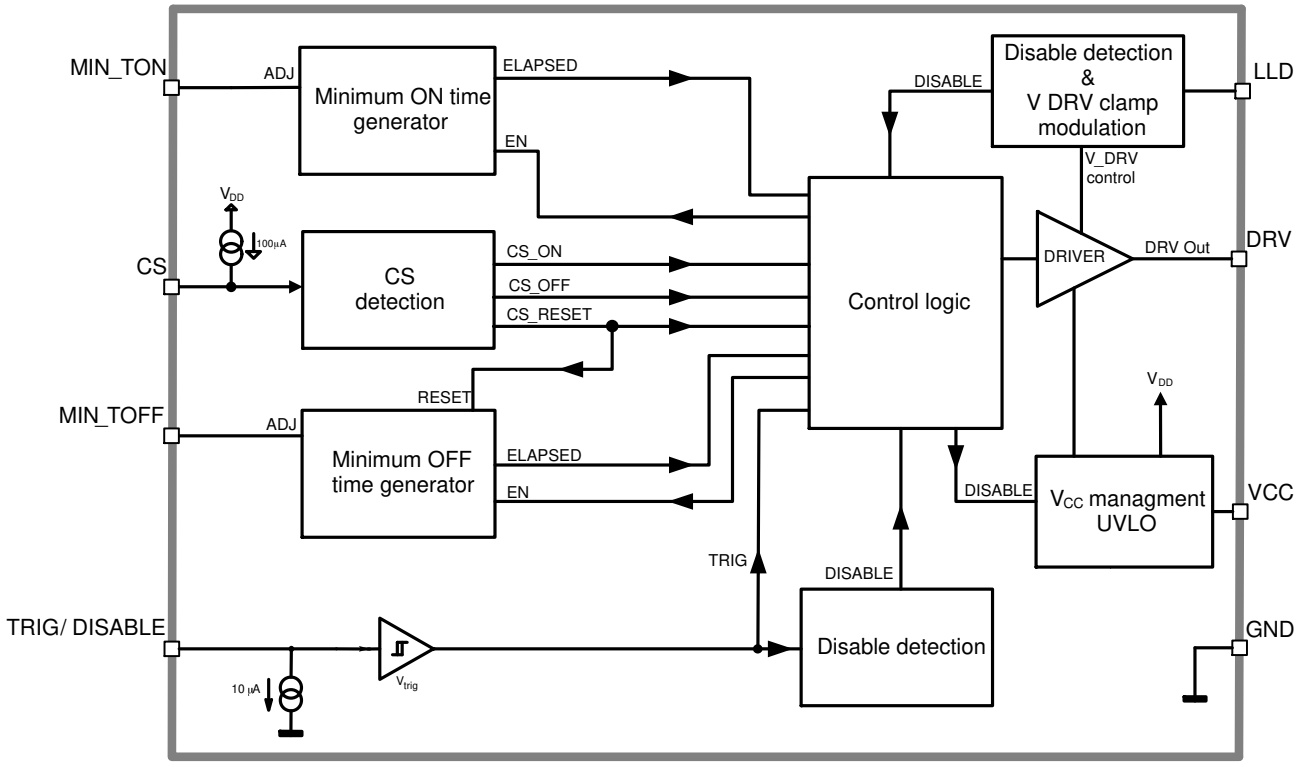


Figure 5. Internal Circuit Architecture – NCP4305A, B, C, D

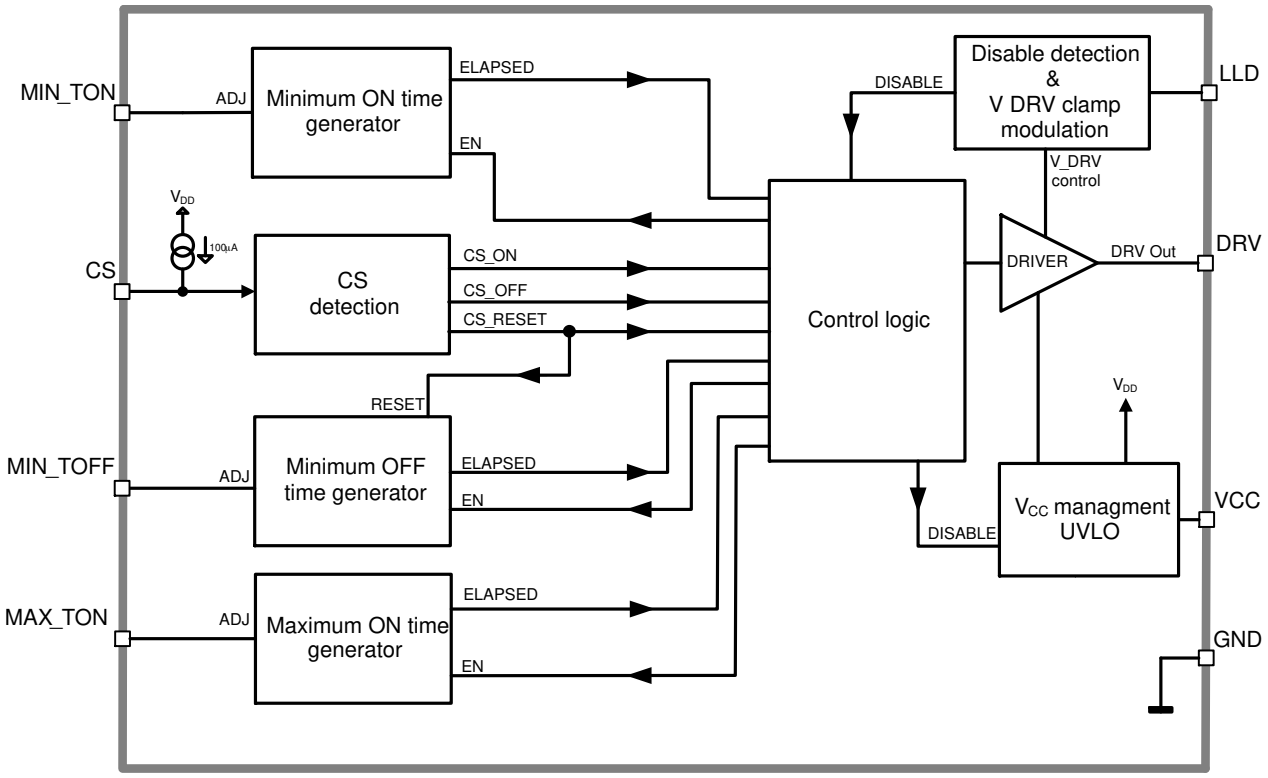


Figure 6. Internal Circuit Architecture – NCP4305Q (CCM QR) with MAX_TON

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to 37.0	V
TRIG/DIS, MIN_TON, MIN_TOFF, MAX_TON, LLD Input Voltage	$V_{TRIG/DIS}$, V_{MIN_TON}, V_{MIN_TOFF}, V_{MAX_TON}, V_{LLD}	–0.3 to V_{CC}	V
Driver Output Voltage	V_{DRV}	–0.3 to 17.0	V
Current Sense Input Voltage	V_{CS}	–4 to 200	V
Current Sense Dynamic Input Voltage (t_{PW} = 200 ns)	V_{CS_DYN}	–10 to 200	V
MIN_TON, MIN_TOFF, MAX_TON, LLD, TRIG Input Current	I_{MIN_TON}, I_{MIN_TOFF}, I_{MAX_TON}, I_{LLD}, I_{TRIG}	–10 to 10	mA
Junction to Air Thermal Resistance, 1 oz 1 in^2 Copper Area, SOIC8	$R_{\theta J-A\_SOIC8}$	160	°C/W
Junction to Air Thermal Resistance, 1 oz 1 in^2 Copper Area, DFN8	$R_{\theta J-A\_DFN8}$	80	°C/W
Junction to Air Thermal Resistance, 1 oz 1 in^2 Copper Area, WDFN8	$R_{\theta J-A\_WDFN8}$	160	°C/W
Maximum Junction Temperature	T_{JMAX}	150	°C
Storage Temperature	T_{STG}	–60 to 150	°C
ESD Capability, Human Body Model, Except Pin 6, per JESD22–A114E	ESD_{HBM}	2000	V
ESD Capability, Human Body Model, Pin 6, per JESD22–A114E	ESD_{HBM}	1000	V
ESD Capability, Machine Model, per JESD22–A115–A	ESD_{MM}	200	V
ESD Capability, Charged Device Model, Except Pin 6, per JESD22–C101F	ESD_{CDM}	750	V
ESD Capability, Charged Device Model, Pin 6, per JESD22–C101F	ESD_{CDM}	250	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device meets latch–up tests defined by JEDEC Standard JESD78D Class I.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Maximum Operating Input Voltage	V_{CC}		35	V
Operating Junction Temperature	T_J	–40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

$-40°C \le T_J \le 125°C$; V_{CC} = 12 V; C_{DRV} = 0 nF; $R_{MIN\_TON} = R_{MIN\_TOFF}$ = 10 kΩ; $V_{TRIG/DIS}$ = 0 V; V_{LLD} = 0 V; V_{CS} = –1 to +4 V; f_{CS} = 100 kHz, DC_{CS} = 50%, unless otherwise noted. Typical values are at T_J = +25°C

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
SUPPLY SECTION							
VCC UVLO (ver. B & C)	V_{CC} rising		V_{CCON}	8.3	8.8	9.4	V
	V_{CC} falling		V_{CCOFF}	7.3	7.8	8.3	
VCC UVLO Hysteresis (ver. B & C)			V_{CCHYS}		1.0		V
VCC UVLO (ver. A, D & Q)	V_{CC} rising		V_{CCON}	4.20	4.45	4.80	V
	V_{CC} falling		V_{CCOFF}	3.70	3.95	4.20	
VCC UVLO Hysteresis (ver. A, D & Q)			V_{CCHYS}		0.5		V
Start–up Delay	V_{CC} rising from 0 to V_{CCON} + 1 V @ tr = 10 μs		t_{START_DEL}		75	125	μs
Current Consumption, $R_{MIN\_TON} = R_{MIN\_TOFF}$ = 0 kΩ	C_{LOAD} = 0 nF, f_{SW} = 500 kHz	A, C	I_{CC}	3.3	4.0	5.6	mA
		B, D, Q		3.8	4.5	6.0	
	C_{LOAD} = 0 nF, f_{SW} = 500 kHz, WDFN	A, C		3.0	4.0	5.6	
		B, D, Q		3.5	4.5	6.0	
	C_{LOAD} = 1 nF, f_{SW} = 500 kHz	A, C		4.5	6.0	7.5	
		B, D, Q		7.7	9.0	10.7	
	C_{LOAD} = 10 nF, f_{SW} = 500 kHz	A, C		20	25	30	
		B, D, Q		40	50	60	
Current Consumption	No switching, V_{CS} = 0 V, $R_{MIN\_TON} = R_{MIN\_TOFF}$ = 0 k		I_{CC}	1.5	2.0	2.5	mA
Current Consumption below UVLO	No switching, $V_{CC} = V_{CCOFF}$ – 0.1 V, V_{CS} = 0 V		I_{CC_UVLO}		75	125	μA
Current Consumption in Disable Mode	$V_{LLD} = V_{CC}$ – 0.1 V, V_{CS} = 0 V		I_{CC_DIS}	40	55	70	μA
	V_{TRIG} = 5 V, $V_{LLD} = V_{CC}$ – 3 V, V_{CS} = 0 V			45	65	80	
DRIVER OUTPUT							
Output Voltage Rise–Time	C_{LOAD} = 10 nF, 10% to 90% V_{DRVMAX}		t_r		40	55	ns
Output Voltage Fall–Time	C_{LOAD} = 10 nF, 90% to 10% V_{DRVMAX}		t_f		20	35	ns
Driver Source Resistance			R_{DRV_SOURCE}		1.2		Ω
Driver Sink Resistance			R_{DRV_SINK}		0.5		Ω
Output Peak Source Current			I_{DRV_SOURCE}		4		A
Output Peak Sink Current			I_{DRV_SINK}		8		A
Maximum Driver Output Voltage	V_{CC} = 35 V, C_{LOAD} > 1 nF, V_{LLD} = 0 V, (ver. B, D and Q)		V_{DRVMAX}	9.0	9.5	10.5	V
	V_{CC} = 35 V, C_{LOAD} > 1 nF, V_{LLD} = 0 V, (ver. A, C)			4.3	4.7	5.5	
Minimum Driver Output Voltage	$V_{CC} = V_{CCOFF}$ + 200 mV, V_{LLD} = 0 V, (ver. B)		V_{DRVMIN}	7.2	7.8	8.5	V
	$V_{CC} = V_{CCOFF}$ + 200 mV, V_{LLD} = 0 V, (ver. C)			4.2	4.7	5.3	
	$V_{CC} = V_{CCOFF}$ + 200 mV, V_{LLD} = 0 V, (ver. A, D, Q)			3.6	4.0	4.4	
Minimum Driver Output Voltage	$V_{LLD} = V_{CC} - V_{LLDREC}$ V		$V_{DRVLLDMIN}$	0.0	0.4	1.2	V

ELECTRICAL CHARACTERISTICS

$-40°C \le T_J \le 125°C$; V_{CC} = 12 V; C_{DRV} = 0 nF; $R_{MIN\_TON} = R_{MIN\_TOFF}$ = 10 kΩ; $V_{TRIG/DIS}$ = 0 V; V_{LLD} = 0 V; V_{CS} = −1 to +4 V; f_{CS} = 100 kHz, DC_{CS} = 50%, unless otherwise noted. Typical values are at T_J = +25°C

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
CS INPUT						
Total Propagation Delay From CS to DRV Output On	V_{CS} goes down from 4 to −1 V, t_{f_CS} = 5 ns	t_{PD_ON}		35	60	ns
Total Propagation Delay From CS to DRV Output Off	V_{CS} goes up from −1 to 4 V, t_{r_CS} = 5 ns	t_{PD_OFF}		12	23	ns
CS Bias Current	V_{CS} = −20 mV	I_{CS}	−105	−100	−95	μA
Turn On CS Threshold Voltage		$V_{TH\_CS\_ON}$	−120	−75	−40	mV
Turn Off CS Threshold Voltage	Guaranteed by Design	$V_{TH\_CS\_OFF}$	−1		0	mV
Turn Off Timer Reset Threshold Voltage		$V_{TH\_CS\_RESET}$	0.42	0.48	0.54	V
CS Leakage Current	V_{CS} = 200 V	$I_{CS\_LEAKAGE}$			0.4	μA
TRIGGER DISABLE INPUT						
Minimum Trigger Pulse Duration	V_{TRIG} = 5 V; Shorter pulses may not be proceeded	$t_{TRIG\_PW\_MIN}$			10	ns
Trigger Threshold Voltage		V_{TRIG_TH}	1.87	2.02	2.18	V
Trigger to DRV Propagation Delay	V_{TRIG} goes from 0 to 5 V, t_{r_TRIG} = 5 ns	t_{PD_TRIG}		7.5	12.5	ns
Trigger Blank Time After DRV Turn−on Event	V_{CS} drops below $V_{TH\_CS\_ON}$	t_{TRIG_BLANK}	35	50	65	ns
Delay to Disable Mode	V_{TRIG} = 5 V	t_{DIS_TIM}	75	100	125	μs
Disable Recovery Timer	V_{TRIG} goes down from 5 to 0 V	t_{DIS_REC}	5	8	13	μs
Minimum Pulse Duration to Disable Mode End	V_{TRIG} = 0 V; Shorter pulses may not be proceeded	$t_{DIS\_END\_MIN}$			200	ns
Pull Down Current	V_{TRIG} = 5 V	I_{TRIG}	9	13	16	μA
MINIMUM t_{ON} and t_{OFF} ADJUST						
Minimum t_{ON} time	R_{MIN_TON} = 0 Ω	t_{ON_MIN}	35	55	75	ns
Minimum t_{OFF} time	R_{MIN_TOFF} = 0 Ω	t_{OFF_MIN}	190	245	290	ns
Minimum t_{ON} time	R_{MIN_TON} = 10 kΩ	t_{ON_MIN}	0.92	1.00	1.08	μs
Minimum t_{OFF} time	R_{MIN_TOFF} = 10 kΩ	t_{OFF_MIN}	0.92	1.00	1.08	μs
Minimum t_{ON} time	R_{MIN_TON} = 50 kΩ	t_{ON_MIN}	4.62	5.00	5.38	μs
Minimum t_{OFF} time	R_{MIN_TOFF} = 50 kΩ	t_{OFF_MIN}	4.62	5.00	5.38	μs
MAXIMUM t_{ON} ADJUST						
Maximum t_{ON} Time	V_{MAX_TON} = 3 V	t_{ON_MAX}	4.3	4.8	5.3	μs
Maximum t_{ON} Time	V_{MAX_TON} = 0.3 V	t_{ON_MAX}	41	48	55	μs
Maximum t_{ON} Output Current	V_{MAX_TON} = 0.3 V	I_{MAX_TON}	−105	−100	−95	μA
LLD INPUT						
Disable Threshold	$V_{LLD\_DIS} = V_{CC} - V_{LLD}$	V_{LLD_DIS}	0.8	0.9	1.0	V
Recovery Threshold	$V_{LLD\_REC} = V_{CC} - V_{LLD}$	V_{LLD_REC}	0.9	1.0	1.1	V
Disable Hysteresis		V_{LLD_DISH}		0.1		V
Disable Time Hysteresis	Disable to Normal, Normal to Disable	t_{LLD_DISH}		45		μs
Disable Recovery Time		$t_{LLD\_DIS\_REC}$	7.0	12.5	16.0	μs
Low Pass Filter Frequency		f_{LPLLD}	6	10	13	kHz
Driver Voltage Clamp Threshold	$V_{DRV} = V_{DRVMAX}$, $V_{LLDMAX} = V_{CC} - V_{LLD}$	V_{LLDMAX}		2.0		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

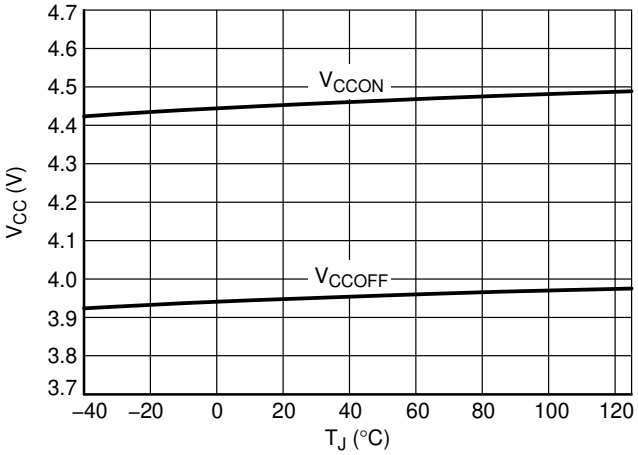


Figure 7. V_{CCON} and V_{CCOFF} Levels, ver. A, D, Q

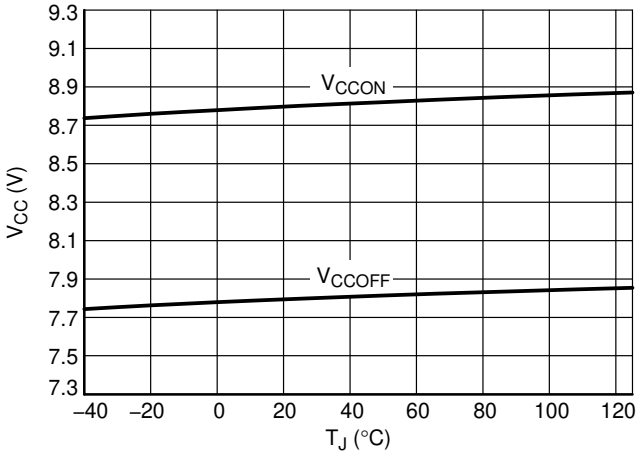


Figure 8. V_{CCON} and V_{CCOFF} Levels, ver. B, C

TYPICAL CHARACTERISTICS

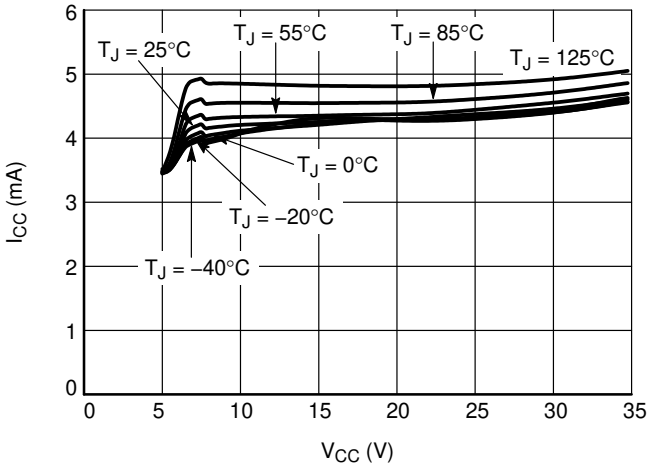


Figure 9. Current Consumption, C_{DRV} = 0 nF, f_{CS} = 500 kHz, ver. D

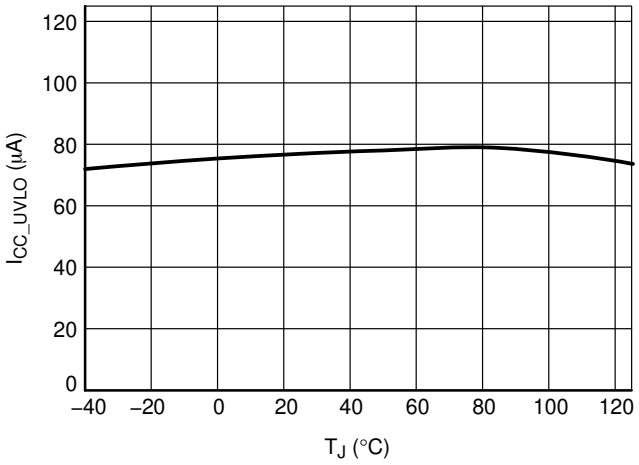


Figure 10. Current Consumption, V_{CC} = V_{CCOFF} − 0.1 V, V_{CS} = 0 V, ver. D

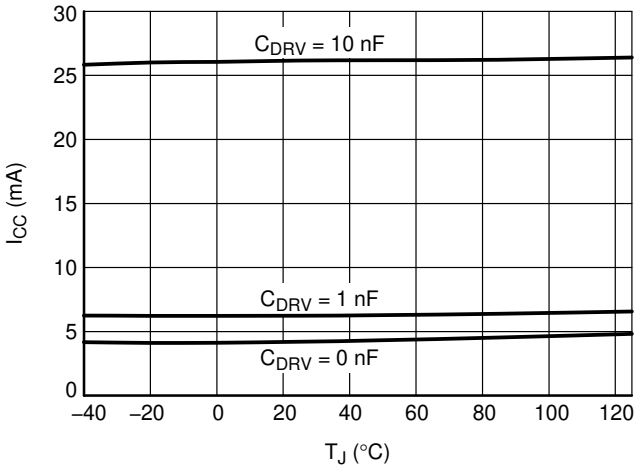


Figure 11. Current Consumption, V_{CC} = 12 V, V_{CS} = −1 to 4 V, f_{CS} = 500 kHz, ver. A

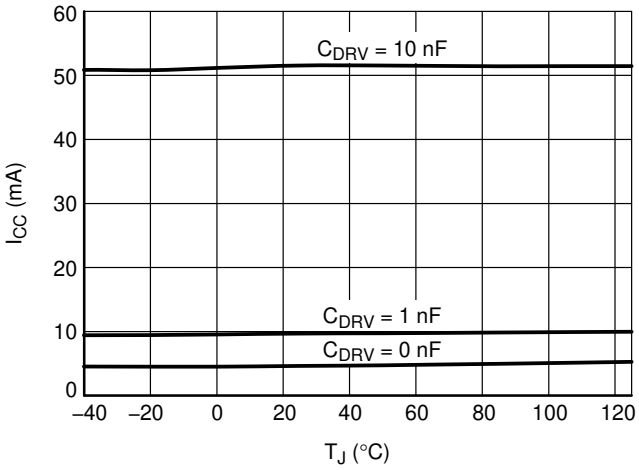


Figure 12. Current Consumption, V_{CC} = 12 V, V_{CS} = −1 to 4 V, f_{CS} = 500 kHz, ver. D

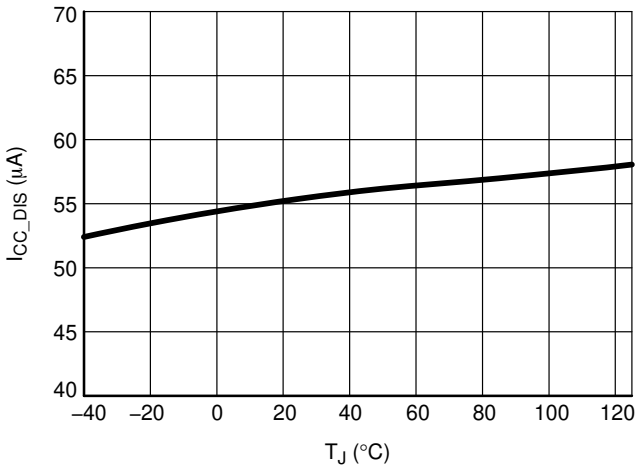


Figure 13. Current Consumption in Disable, V_{CC} = 12 V, V_{CS} = 0 V, V_{LLD} = V_{CC} − 0.1 V

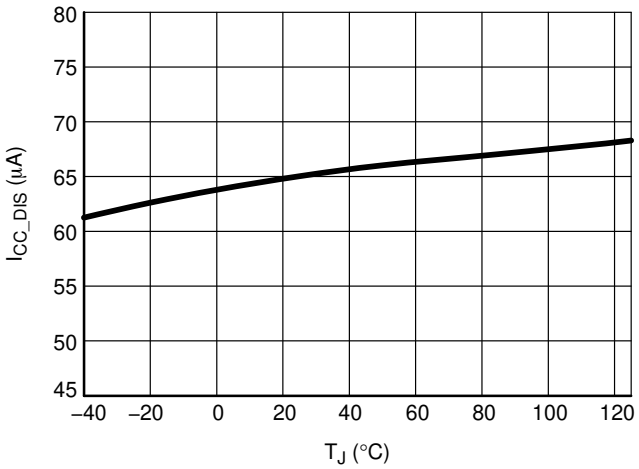


Figure 14. Current Consumption in Disable, V_{CC} = 12 V, V_{CS} = 0 V, V_{LLD} = V_{CC} − 3 V, V_{TRIG} = 5 V

TYPICAL CHARACTERISTICS

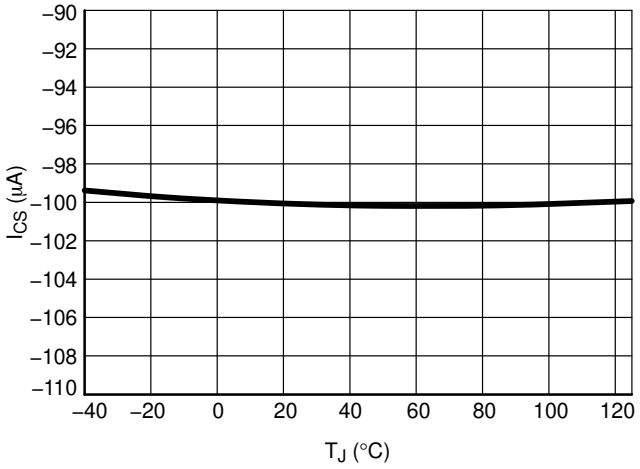


Figure 15. CS Current, V_{CS} = −20 mV

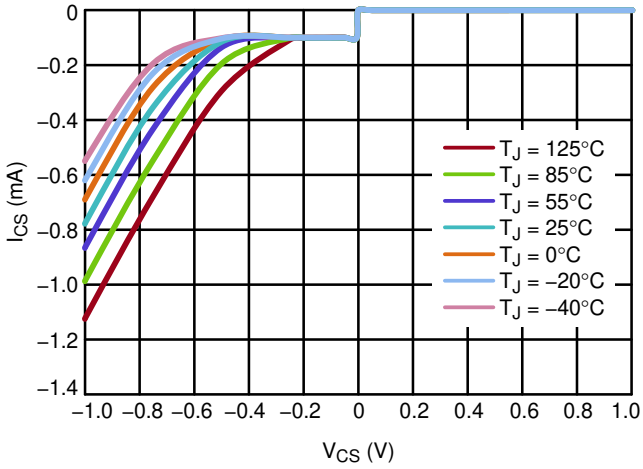


Figure 16. CS Current, V_{CC} = 12 V

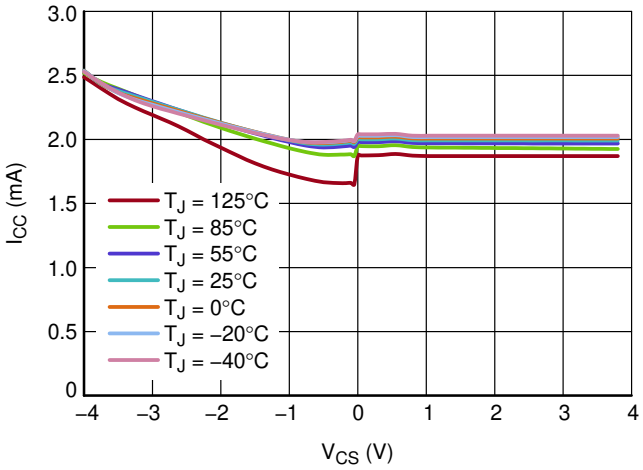


Figure 17. Supply Current vs. CS Voltage, V_{CC} = 12 V

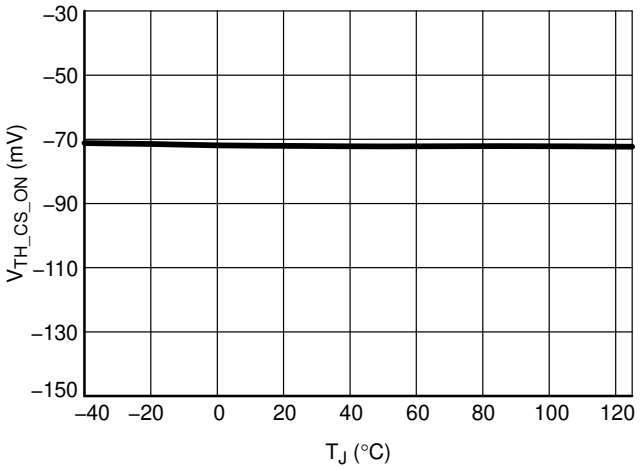


Figure 18. CS Turn−on Threshold

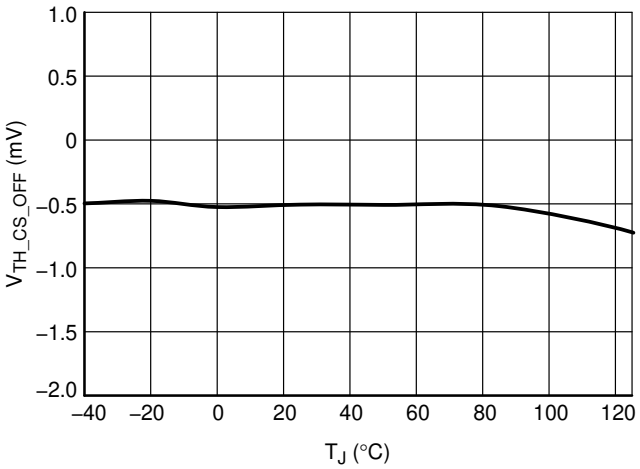


Figure 19. CS Turn−off Threshold

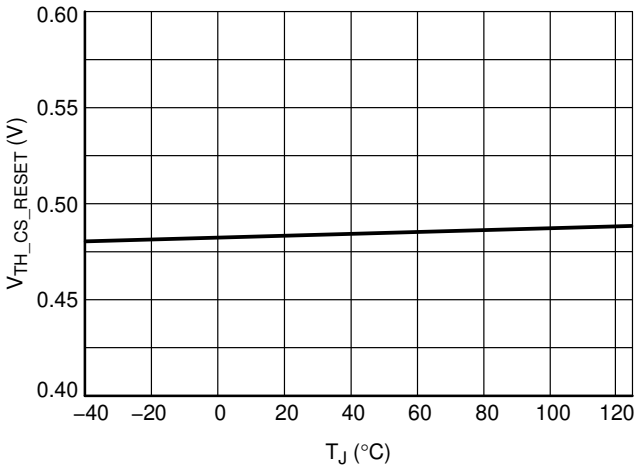


Figure 20. CS Reset Threshold

TYPICAL CHARACTERISTICS

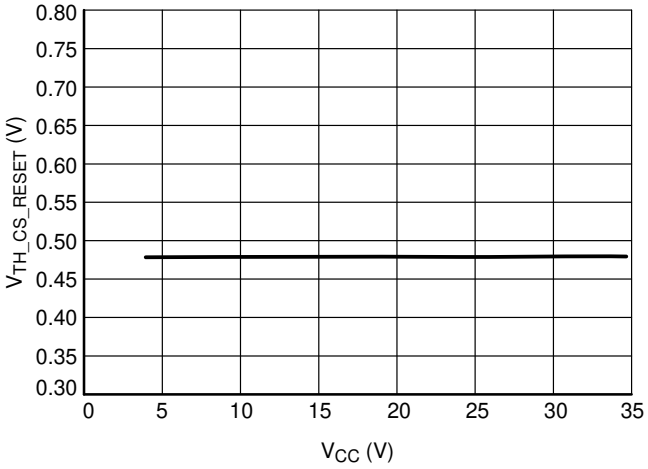


Figure 21. CS Reset Threshold

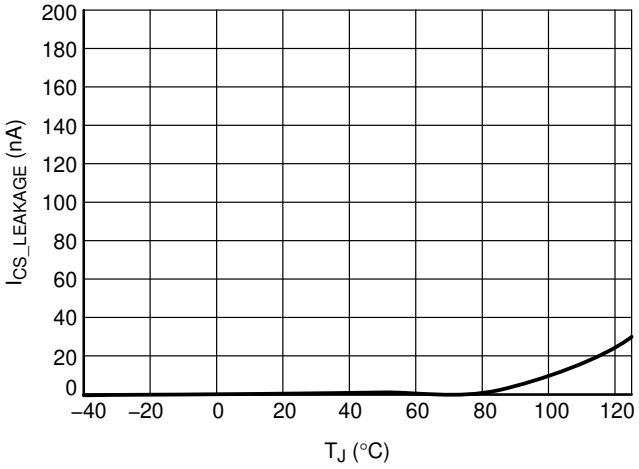


Figure 22. CS Leakage, V_{CS} = 200 V

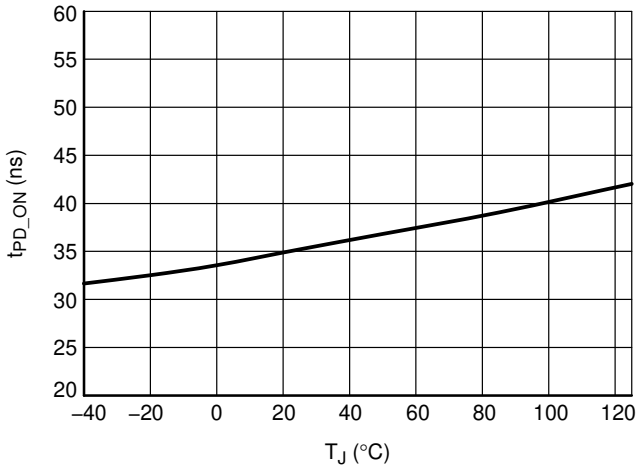


Figure 23. Propagation Delay from CS to DRV Output On

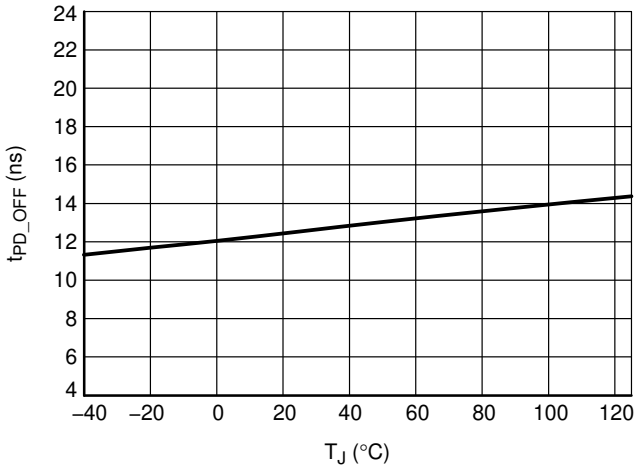


Figure 24. Propagation Delay from CS to DRV Output Off

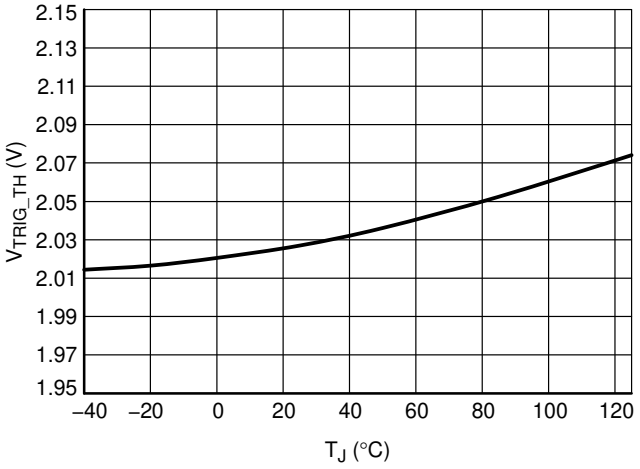


Figure 25. Trigger Threshold, V_{CC} = 12 V

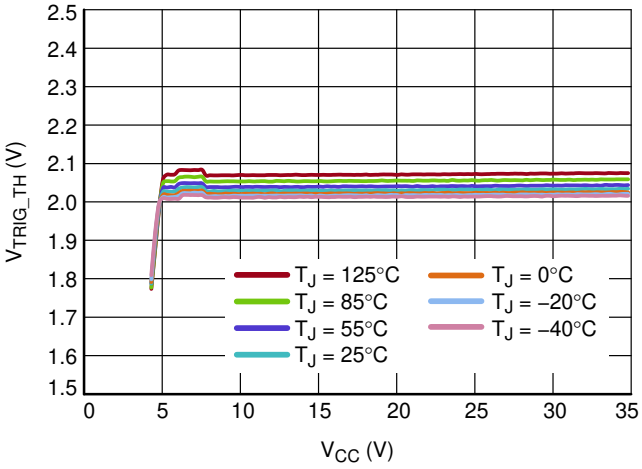


Figure 26. Trigger Threshold

TYPICAL CHARACTERISTICS

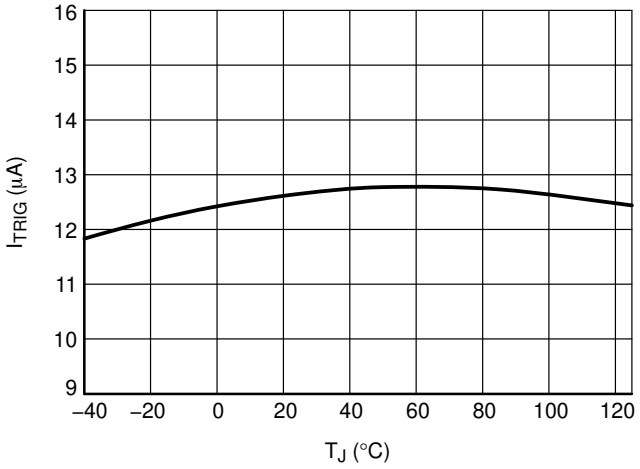


Figure 27. Trigger Pull Down Current

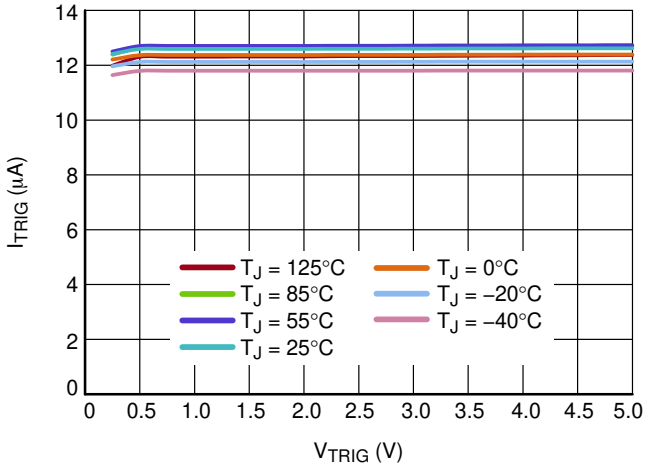


Figure 28. Trigger Pull Down Current, V_{CC} = 12 V

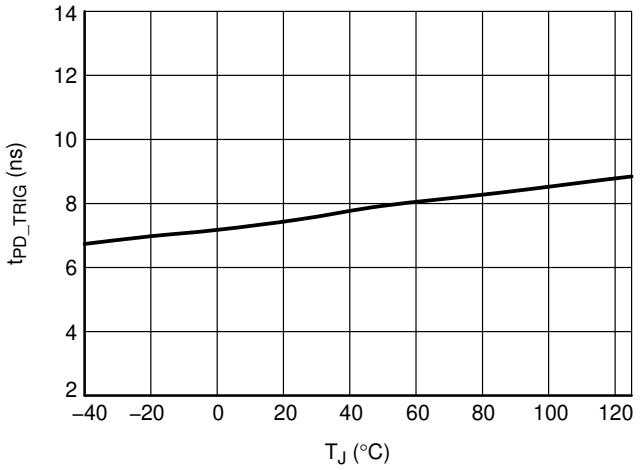


Figure 29. Propagation Delay from Trigger to Driver Output Off

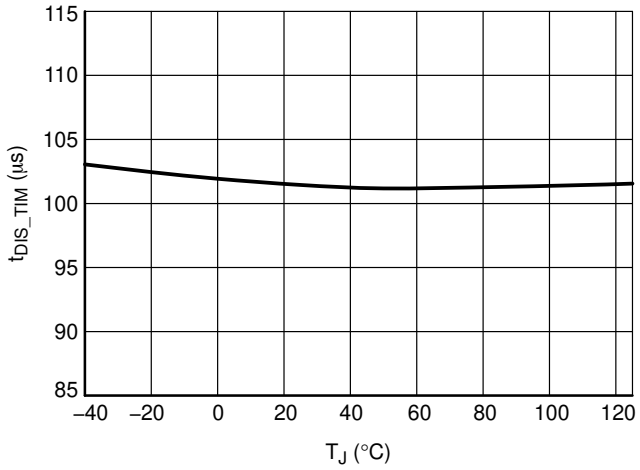


Figure 30. Delay to Disable Mode, V_{TRIG} = 5 V

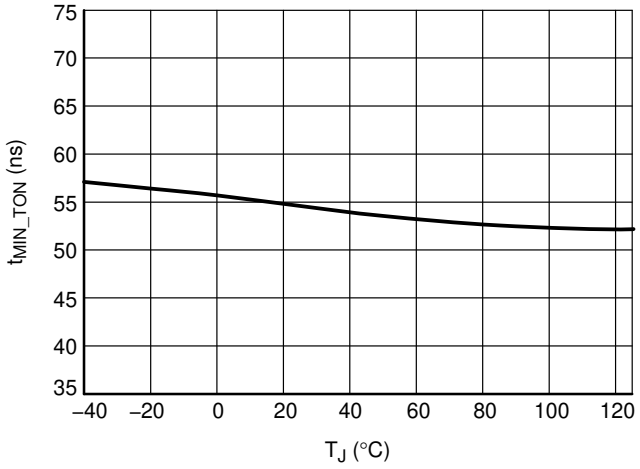


Figure 31. Minimum On−time R_{MIN_TON} = 0 Ω

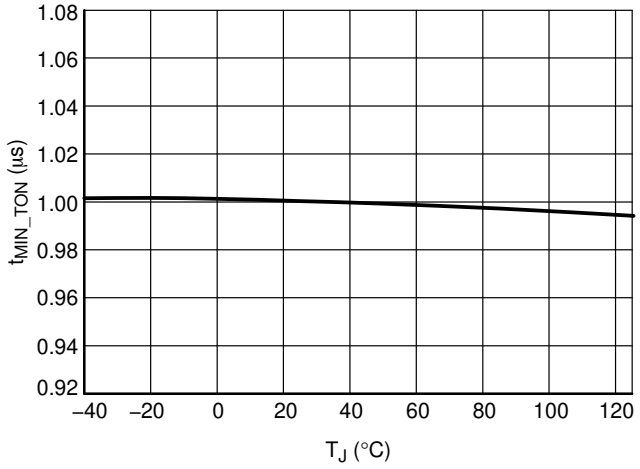


Figure 32. Minimum On−time R_{MIN_TON} = 10 kΩ

TYPICAL CHARACTERISTICS

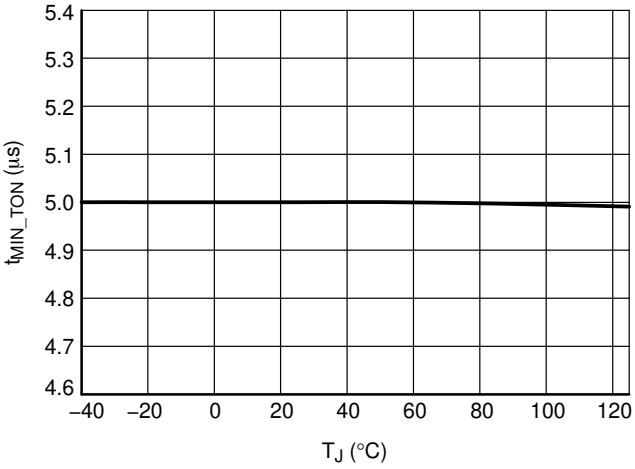


Figure 33. Minimum On−time R_{MIN_TON} = 50 kΩ

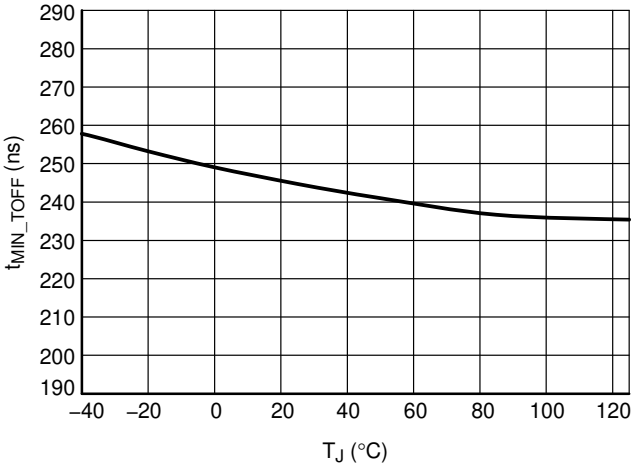


Figure 34. Minimum Off−time R_{MIN_TOFF} = 0 Ω

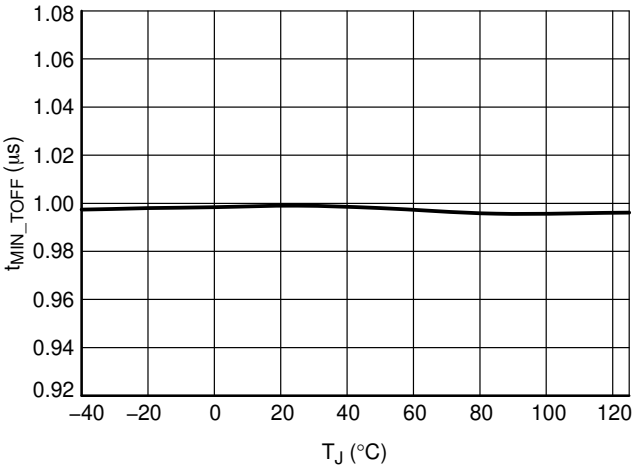


Figure 35. Minimum Off−time R_{MIN_TOFF} = 10 kΩ

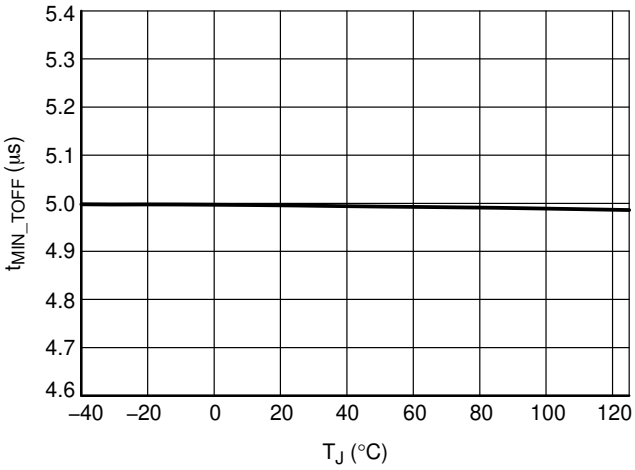


Figure 36. Minimum Off−time R_{MIN_TOFF} = 50 kΩ

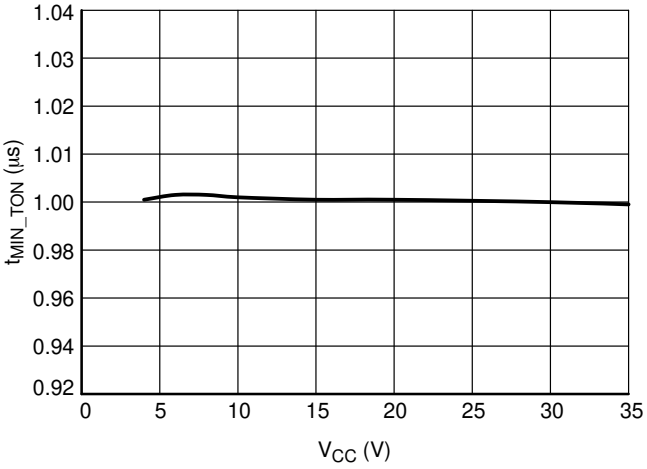


Figure 37. Minimum On−time R_{MIN_TON} = 10 kΩ

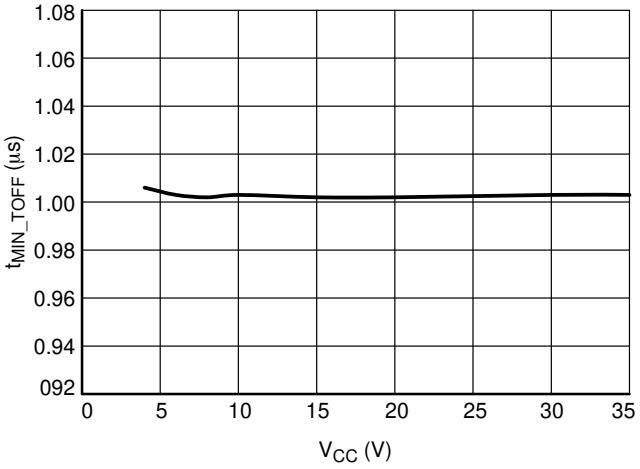


Figure 38. Minimum Off−time R_{MIN_TOFF} = 10 kΩ

TYPICAL CHARACTERISTICS

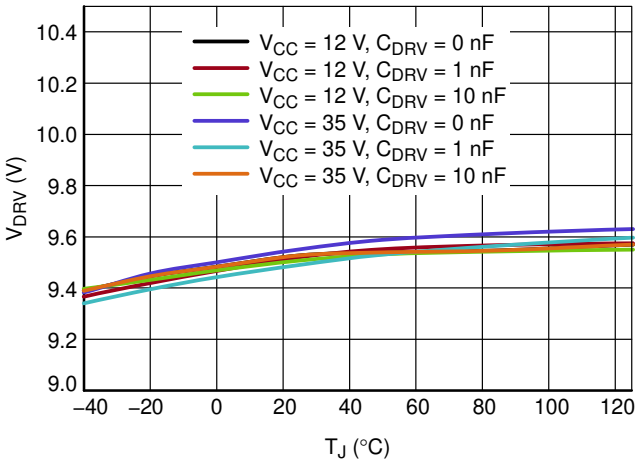


Figure 39. Driver and Output Voltage, ver. B, D and Q

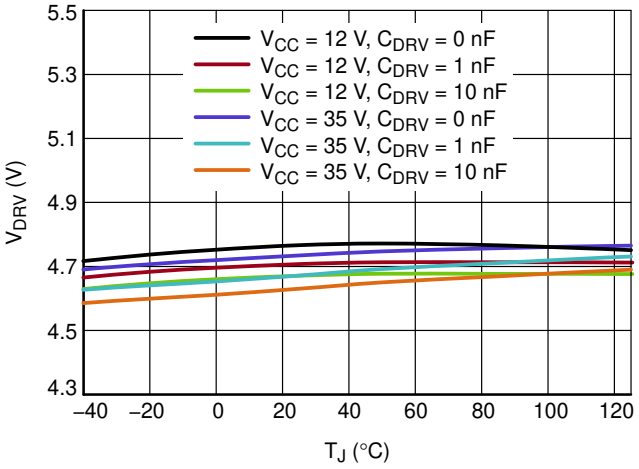


Figure 40. Driver Output Voltage, ver. A and C

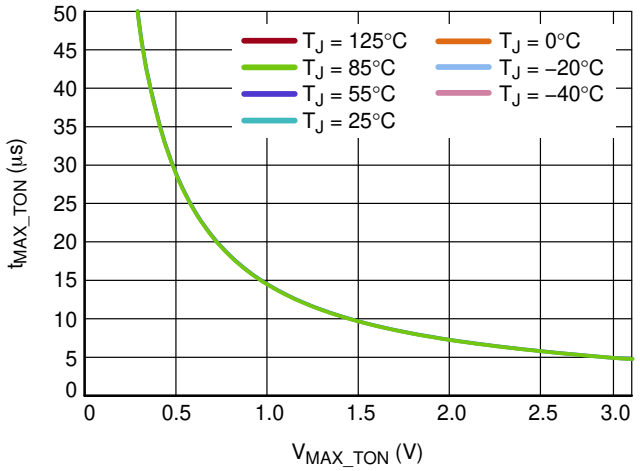


Figure 41. Maximum On−time, ver. Q

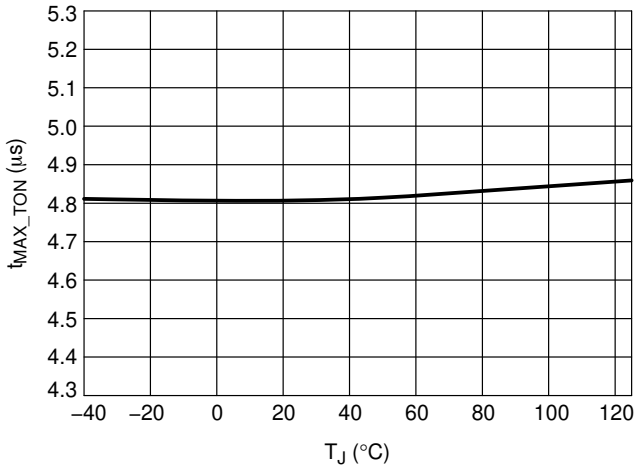


Figure 42. Maximum On−time, V_{MAX_TON} = 3 V, ver. Q

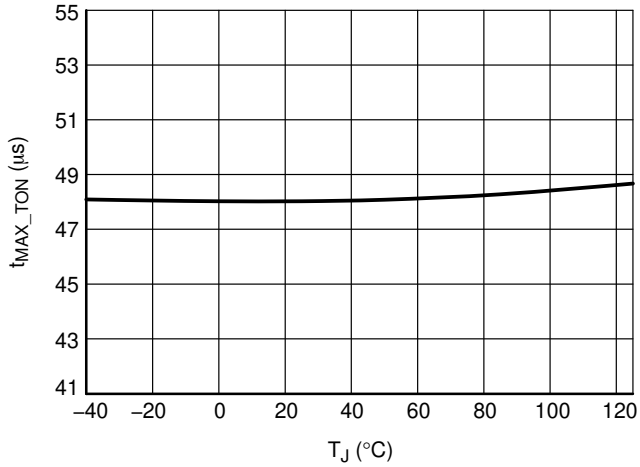


Figure 43. Maximum On−time, V_{MAX_TON} = 0.3 V, ver. Q

APPLICATION INFORMATION

General description

The NCP4305 is designed to operate either as a standalone IC or as a companion IC to a primary side controller to help achieve efficient synchronous rectification in switch mode power supplies. This controller features a high current gate driver along with high−speed logic circuitry to provide appropriately timed drive signals to a synchronous rectification MOSFET. With its novel architecture, the NCP4305 has enough versatility to keep the synchronous rectification system efficient under any operating mode.

The NCP4305 works from an available voltage with range from 4 V (A, D & Q options) or 8 V (B & C options) to 35 V (typical). The wide V_{CC} range allows direct connection to the SMPS output voltage of most adapters such as notebooks, cell phone chargers and LCD TV adapters.

Precise turn-off threshold of the current sense comparator together with an accurate offset current source allows the user to adjust for any required turn-off current threshold of the SR MOSFET switch using a single resistor. Compared to other SR controllers that provide turn-off thresholds in the range of −10 mV to −5 mV, the NCP4305 offers a turn-off threshold of 0 mV. When using a low $R_{DS(on)}$ SR (1 mΩ) MOSFET our competition, with a −10 mV turn off, will turn off with 10 A still flowing through the SR FET, while our 0 mV turn off turns off the FET at 0 A; significantly reducing the turn-off current threshold and improving efficiency. Many of the competitor parts maintain a drain source voltage across the MOSFET causing the SR MOSFET to operate in the linear region to reduce turn−off time. Thanks to the 8 A sink current of the NCP4305 significantly reduces turn off time allowing for a minimal drain source voltage to be utilized and efficiency maximized.

To overcome false triggering issues after turn-on and turn−off events, the NCP4305 provides adjustable minimum on-time and off-time blanking periods. Blanking times can be adjusted independently of IC VCC using external resistors connected to GND. If needed, blanking periods can be modulated using additional components.

An extremely fast turn−off comparator, implemented on the current sense pin, allows for NCP4305 implementation in CCM applications without any additional components or external triggering.

An ultrafast trigger input offers the possibility to further increase efficiency of synchronous rectification systems operated in CCM mode (for example, CCM flyback or forward). The time delay from trigger input to driver turn off event is t_{PD_TRIG}. Additionally, the trigger input can be used to disable the IC and activate a low consumption standby mode. This feature can be used to decrease standby consumption of an SMPS. If the trigger input is not wanted than the trigger pin can be tied to GND or an option can be chosen to replace this pin with a MAX_TON input.

An output driver features capability to keep SR transistor closed even when there is no supply voltage for NCP4305. SR transistor drain voltage goes up and down during SMPS operation and this is transferred through drain gate capacitance to gate and may turn on transistor. NCP4305 uses this pulsing voltage at SR transistor gate (DRV pin) and uses it internally to provide enough supply to activate internal driver sink transistor. DRV voltage is pulled low (not to zero) thanks to this feature and eliminate the risk of turned on SR transistor before enough V_{CC} is applied to NCP4305.

Some IC versions include a MAX_TON circuit that helps a quasi resonant (QR) controller to work in CCM mode when a heavy load is present like in the example of a printer's motor starting up.

Finally, the NCP4305 features a special pin (LLD) that can be used to reduce gate driver voltage clamp according to application load conditions. This feature helps to reduce issues with transition from disabled driver to full driver output voltage and back. Disable state can be also activated through this pin to decrease power consumption in no load conditions. If the LLD feature is not wanted then the LLD pin can be tied to GND.

Current Sense Input

Figure 44 shows the internal connection of the CS circuitry on the current sense input. When the voltage on the secondary winding of the SMPS reverses, the body diode of M1 starts to conduct current and the voltage of M1's drain drops approximately to −1 V. The CS pin sources current of 100 μA that creates a voltage drop on the R_{SHIFT_CS} resistor (resistor is optional, we recommend shorting this resistor). Once the voltage on the CS pin is lower than $V_{TH\_CS\_ON}$ threshold, M1 is turned−on. Because of parasitic impedances, significant ringing can occur in the application. To overcome false sudden turn−off due to mentioned ringing, the minimum conduction time of the SR MOSFET is activated. Minimum conduction time can be adjusted using the R_{MIN_TON} resistor.

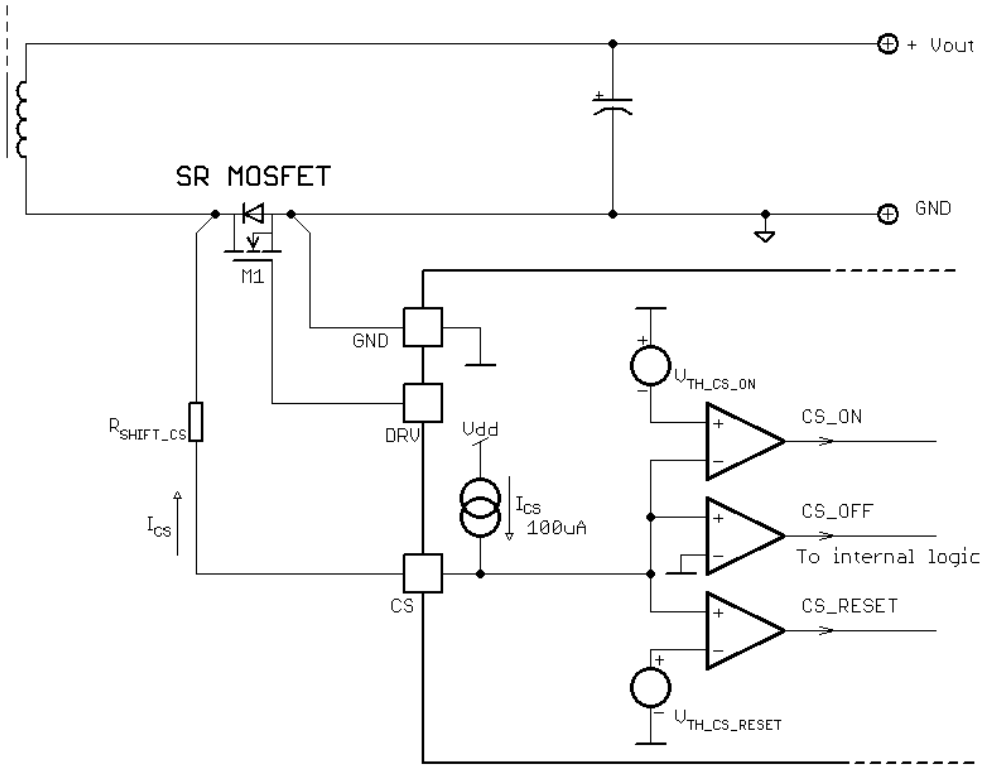


Figure 44. Current Sensing Circuitry Functionality

The SR MOSFET is turned-off as soon as the voltage on the CS pin is higher than $V_{TH\_CS\_OFF}$ (typically −0.5 mV minus any voltage dropped on the optional R_{SHIFT_CS}). For the same ringing reason, a minimum off-time timer is asserted once the V_{CS} goes above $V_{TH\_CS\_RESET}$. The minimum off-time can be externally adjusted using R_{MIN_TOFF} resistor. The minimum off−time generator can be re−triggered by MIN_TOFF reset comparator if some spurious ringing occurs on the CS input after SR MOSFET turn−off event. This feature significantly simplifies SR system implementation in flyback converters.

In an LLC converter the SR MOSFET M1 channel conducts while secondary side current is decreasing (refer to Figure 45). Therefore the turn−off current depends on MOSFET R_{DSON}. The −0.5 mV threshold provides an optimum switching period usage while keeping enough time margin for the gate turn-off. The R_{SHIFT_CS} resistor provides the designer with the possibility to modify (increase) the actual turn−on and turn−off secondary current thresholds. To ensure proper switching, the min_t_{OFF} timer is reset, when the V_{DS} of the MOSFET rings and falls down past the $V_{TH\_CS\_RESET}$. The minimum off−time needs to expire before another drive pulse can be initiated. Minimum off−time timer is started again when V_{DS} rises above $V_{TH\_CS\_RESET}$.

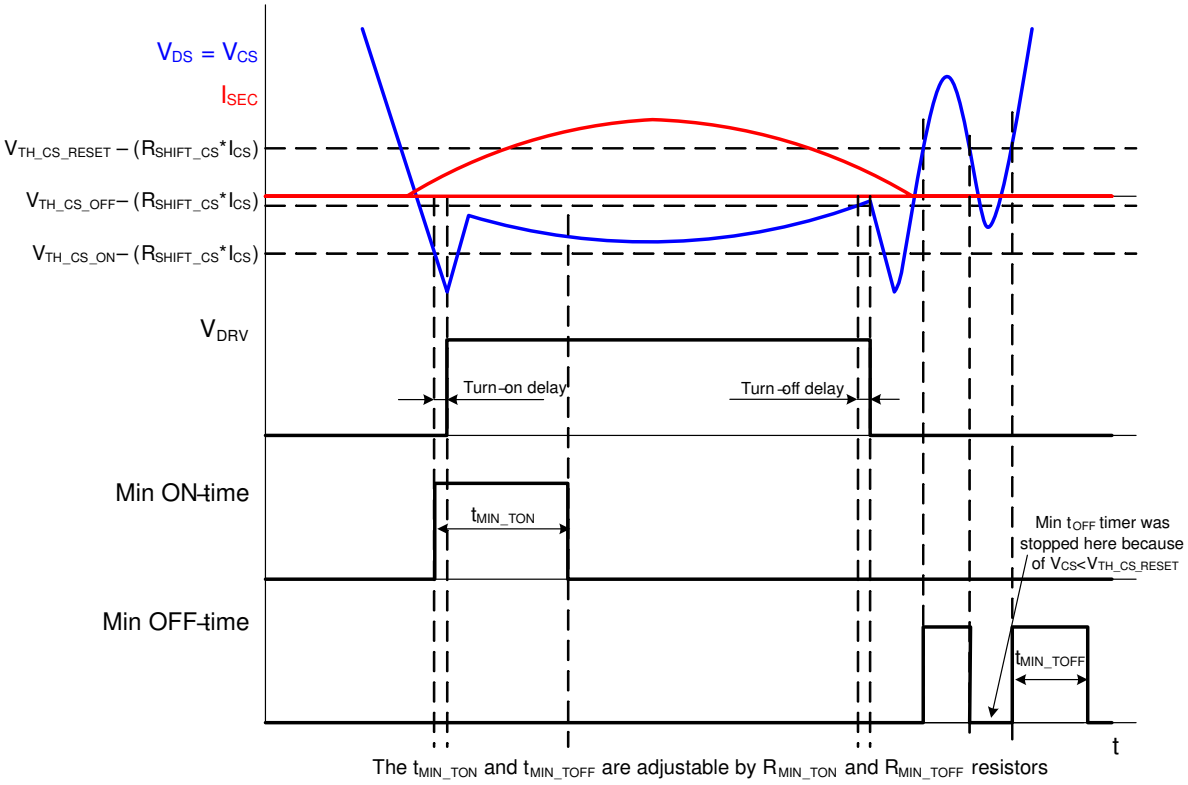


Figure 45. CS Input Comparators Thresholds and Blanking Periods Timing in LLC

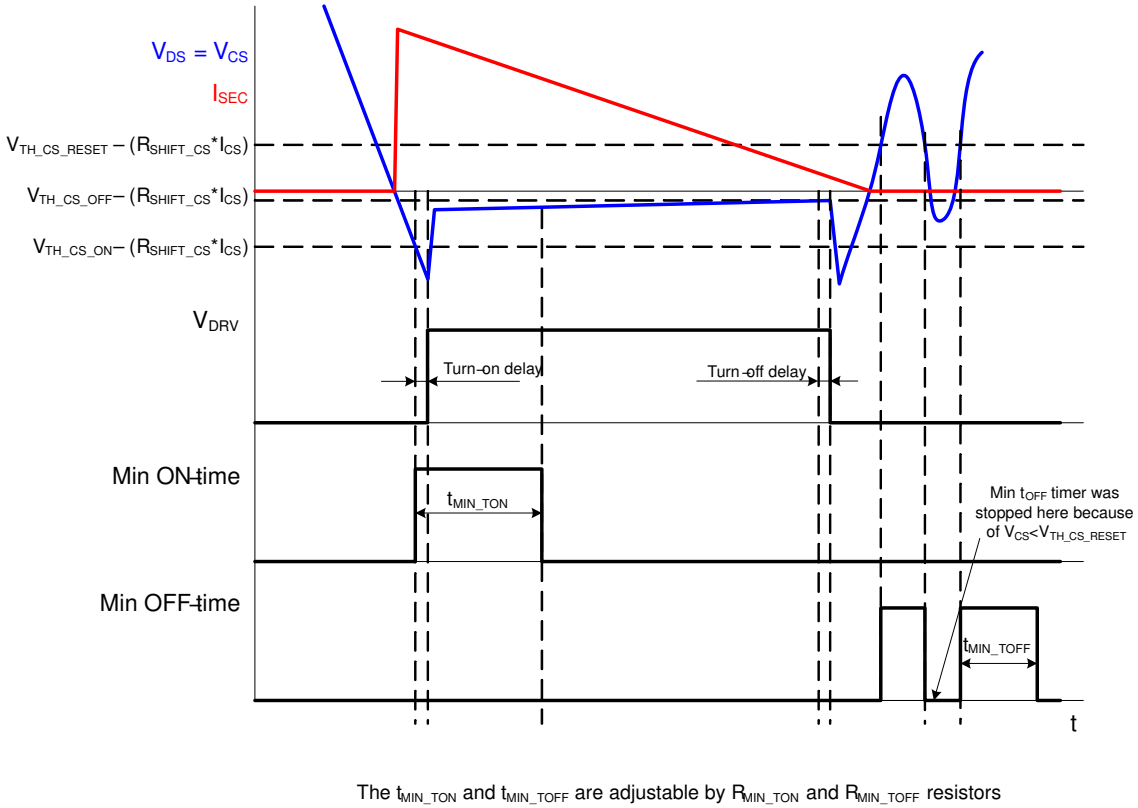


Figure 46. CS Input Comparators Thresholds and Blanking Periods Timing in Flyback

If no R_{SHIFT_CS} resistor is used, the turn-on, turn-off and $V_{TH\_CS\_RESET}$ thresholds are fully given by the CS input specification (please refer to electrical characteristics table). The CS pin offset current causes a voltage drop that is equal to:

$$V_{RSHIFT\_CS} = R_{SHIFT\_CS} * I_{CS} \quad \text{(eq. 1)}$$

Final turn−on and turn off thresholds can be then calculated as:

$$V_{CS\_TURN\_ON} = V_{TH\_CS\_ON} - \left(R_{SHIFT\_CS} * I_{CS}\right) \quad \text{(eq. 2)}$$

$$V_{CS\_TURN\_OFF} = V_{TH\_CS\_OFF} - \left(R_{SHIFT\_CS} * I_{CS}\right) \quad \text{(eq. 3)}$$

$$V_{CS\_RESET} = V_{TH\_CS\_RESET} - \left(R_{SHIFT\_CS} * I_{CS}\right) \quad \text{(eq. 4)}$$

Note that R_{SHIFT_CS} impact on turn-on and $V_{TH\_CS\_RESET}$ thresholds is less critical than its effect on the turn−off threshold.

It should be noted that when using a SR MOSFET in a through hole package the parasitic inductance of the MOSFET package leads (refer to Figure 47) causes a turn−off current threshold increase. The current that flows through the SR MOSFET experiences a high $\Delta i(t)/\Delta t$ that induces an error voltage on the SR MOSFET leads due to their parasitic inductance. This error voltage is proportional to the derivative of the SR MOSFET current; and shifts the CS input voltage to zero when significant current still flows through the MOSFET channel. As a result, the SR MOSFET is turned−off prematurely and the efficiency of the SMPS is not optimized – refer to Figure 48 for a better understanding.

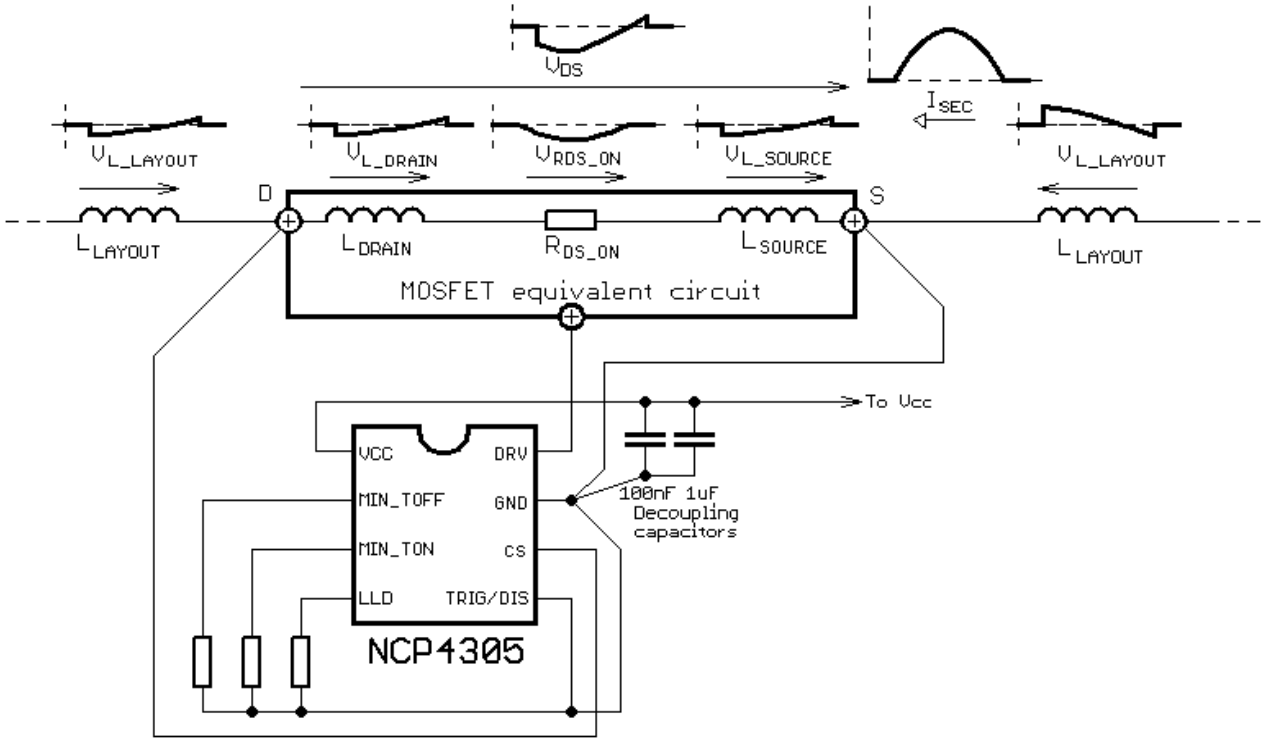


Figure 47. SR System Connection Including MOSFET and Layout Parasitic Inductances in LLC Application

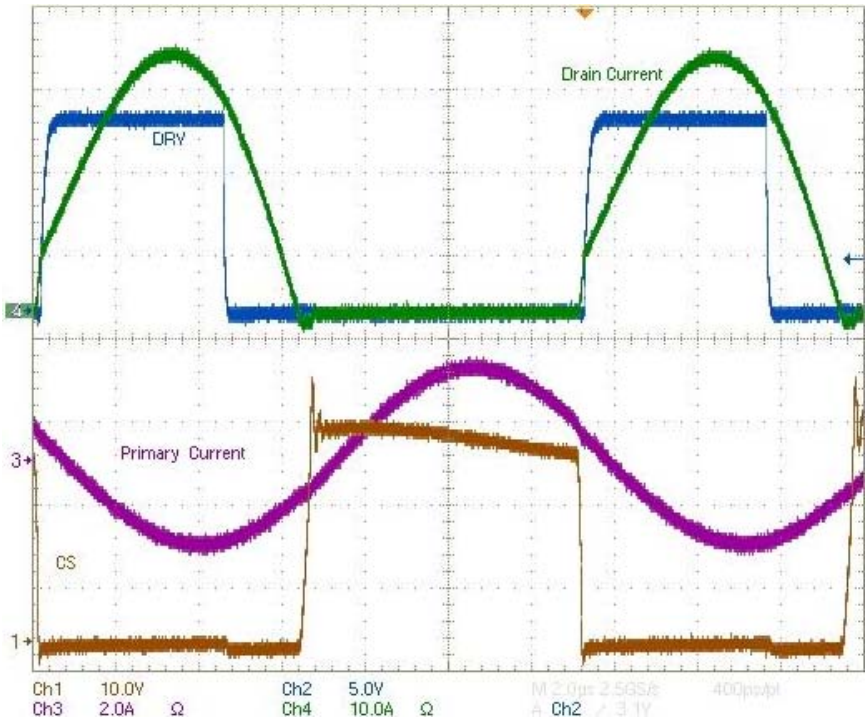


Figure 48. Waveforms From SR System Implemented in LLC Application and Using MOSFET in TO220 Package With Long Leads – SR MOSFET channel Conduction Time is Reduced

Note that the efficiency impact caused by the error voltage due to the parasitic inductance increases with lower MOSFETs $R_{DS(on)}$ and/or higher operating frequency.

It is thus beneficial to minimize SR MOSFET package leads length in order to maximize application efficiency. The optimum solution for applications with high secondary current $\Delta i/\Delta t$ and high operating frequency is to use lead−less SR MOSFET i.e. SR MOSFET in SMT package. The parasitic inductance of a SMT package is negligible causing insignificant CS turn−off threshold shift and thus minimum impact to efficiency (refer to Figure 49).

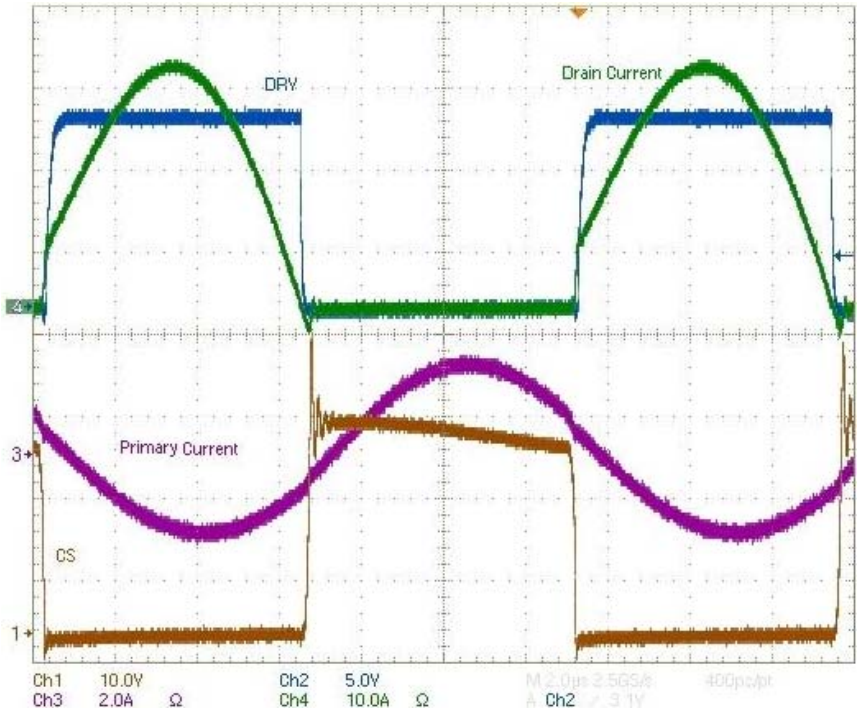


Figure 49. Waveforms from SR System Implemented in LLC Application and Using MOSFET in SMT Package with Minimized Parasitic Inductance – SR MOSFET Channel Conduction Time is Optimized

It can be deduced from the above paragraphs on the induced error voltage and parameter tables that turn−off threshold precision is quite critical. If we consider a SR MOSFET with $R_{DS(on)}$ of 1 mΩ, the 1 mV error voltage on the CS pin results in a 1 A turn-off current threshold difference; thus the PCB layout is very critical when implementing the SR system. Note that the CS turn-off comparator is referred to the GND pin. Any parasitic impedance (resistive or inductive − even on the magnitude of mΩ and nH values) can cause a high error voltage that is then evaluated by the CS comparator. Ideally the CS turn−off comparator should detect voltage that is caused by secondary current directly on the SR MOSFET channel resistance. In reality there will be small parasitic impedance on the CS path due to the bonding wires, leads and soldering. To assure the best efficiency results, a Kelvin connection of the SR controller to the power circuitry should be implemented. The GND pin should be connected to the SR MOSFET source soldering point and current sense pin should be connected to the SR MOSFET drain soldering point − refer to Figure 47. Using a Kelvin connection will avoid any impact of PCB layout parasitic elements on the SR controller functionality; SR MOSFET parasitic elements will still play a role in attaining an error voltage. Figure 50 and Figure 51 show examples of SR system layouts using MOSFETs in TO220 and SMT packages. It is evident that the MOSFET leads should be as short as possible to minimize parasitic inductances when using packages with leads (like TO220). Figure 51 shows how to layout design with two SR MOSFETs in parallel. It has to be noted that it is not easy task and designer has to paid lot of attention to do symmetric Kelvin connection.

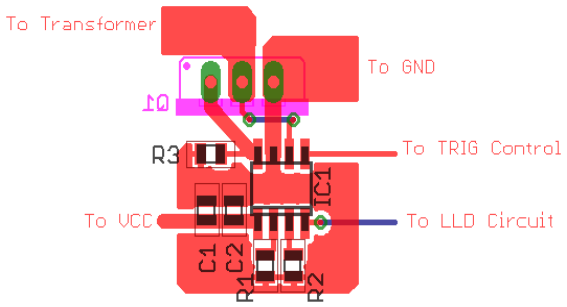


Figure 50. Recommended Layout When Using SR MOSFET in TO220 Package

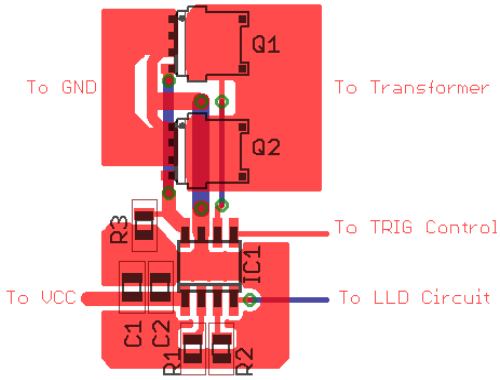


Figure 51. Recommended Layout When Using SR MOSFET in SMT Package (2x SO8 FL)

Trigger/Disable input

The NCP4305 features an ultrafast trigger input that exhibits a maximum of t_{PD_TRIG} delay from its activation to the start of SR MOSFET turn−off of process. This input can be used in applications operated in deep Continues Conduction Mode (CCM) to further increase efficiency and/or to activate disable mode of the SR driver in which the consumption of the NCP4305 is reduced to maximum of I_{CC_DIS}.

NCP4305 is capable to turn−off the SR MOSFET reliably in CCM applications just based on CS pin information only, without using the trigger input. However, natural delay of the ZCD comparator and DRV turn−off delay increase overlap between primary and secondary MOSFETs switching (also known as cross conduction). If one wants to achieve absolutely maximum efficiency with deep CCM applications, then the trigger signal coming from the primary side should be applied to the trigger pin. The trigger input then turns the SR MOSFET off slightly before the secondary winding voltage reverses. There are several possibilities for transferring the trigger signal from the primary to the secondary side – refer to Figures 66 and 67.

The trigger signal is blanked for $t_{TRIGBLANK}$ after the DRV turn−on process has begun. The blanking technique is used to increase trigger input noise immunity against the parasitic ringing that is present during the turn on process due to the SMPS layout. The trigger input is supersedes the CS input except trigger blanking period. TRIG/DIS signal turns the SR MOSFET off or prohibits its turn−on when the Trigger/Disable pin is pulled above V_{TRIG_TH}.

The SR controller enters disable mode when the trigger pin is pulled−up for more than t_{DIS_TIM}. In disable mode the IC consumption is significantly reduced. To recover from disable mode and enter normal operation, the TRIG/DIS pin is pulled low at least for t_{DIS_END}.

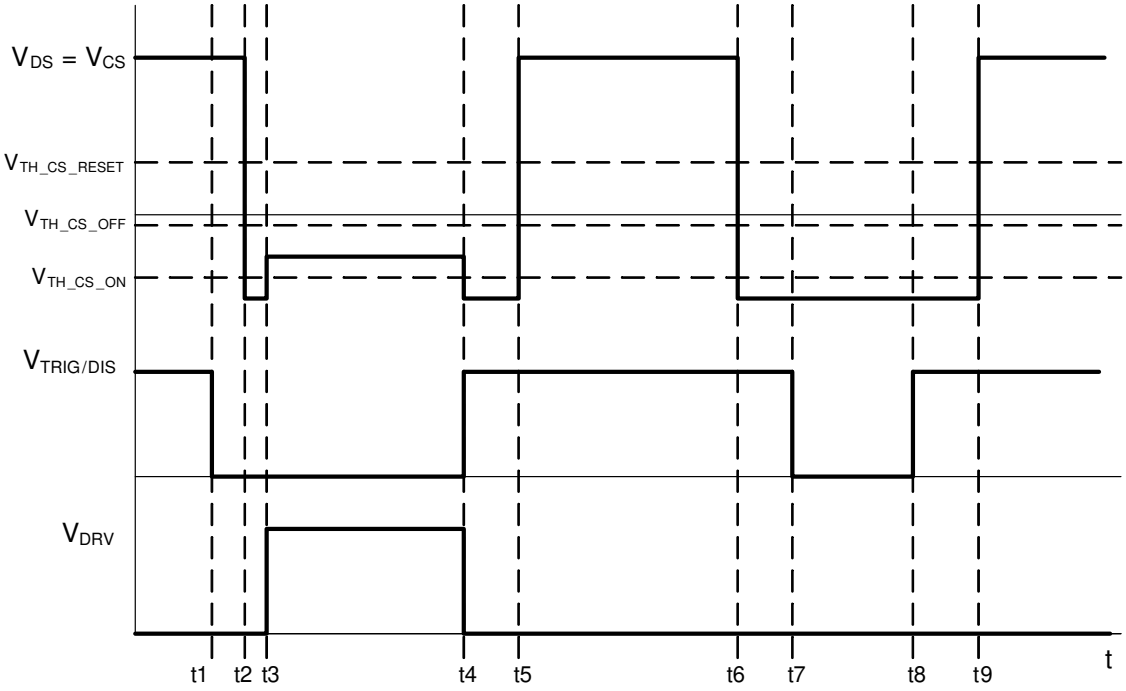


Figure 52. Trigger Input Functionality Waveforms Using the Trigger to Turn−off and Block the DRV Signal

Figure 52 shows basic Trigger/Disable input functionality. At t1 the Trigger/Disable pin is pulled low to enter into normal operation. At t2 the CS pin is dropped below the $V_{TH\_CS\_ON}$, signaling to the NCP4305 to start to turn the SR MOSFET on. At t3 the NCP4305 begins to drive the MOSFET. At t4, the SR MOSFET is conducting and the Trigger/Disable pin is pulled high. This high signal on the Trigger/Disable pin almost immediately turns off the drive to the SR MOSFET, turning off the MOSFET. The DRV is not turned−on in other case (t6) because the trigger pin is high in the time when CS pin signal crosses turn−on threshold. This figure clearly shows that the DRV can be asserted only on falling edge of the CS pin signal in case the trigger input is at low level (t2).

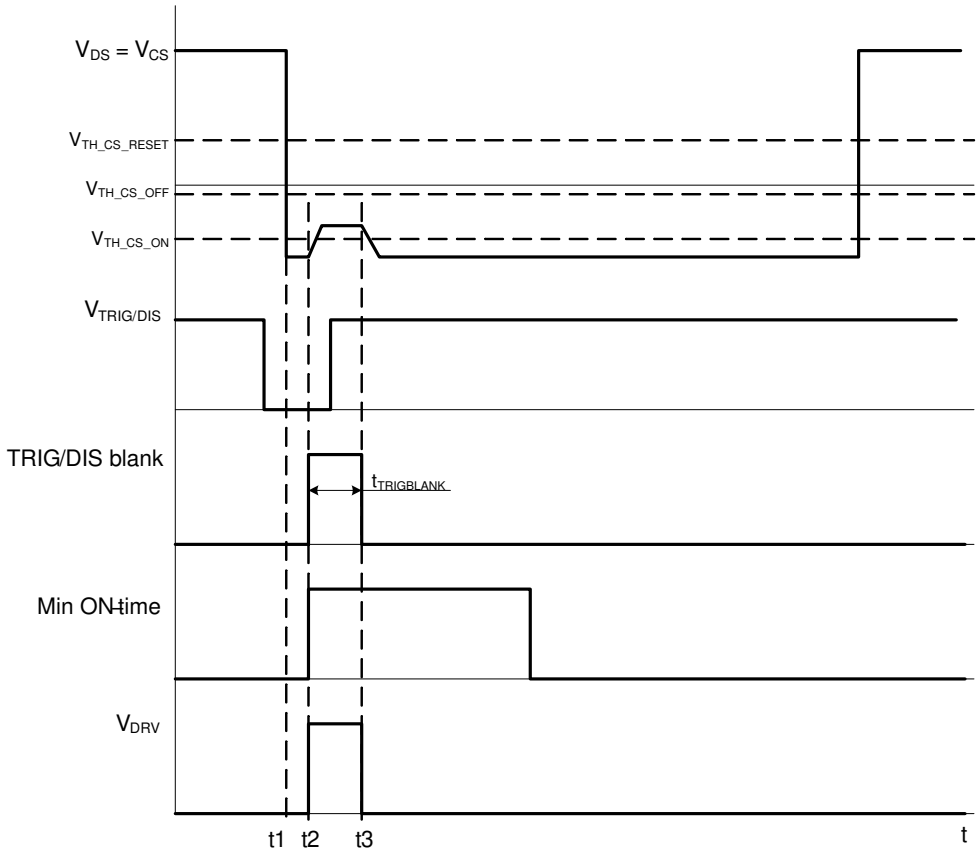


Figure 53. Trigger Input Functionality Waveforms – Trigger Blanking

In Figure 53 above, at time t1 the CS pin falls below the $V_{TH\_CS\_ON}$ while the Trigger is low setting in motion the DRV signal that appears at t2. At time t2 the DRV signal and Trigger blanking clock begin. Trigger/Disable signal goes high shortly after time t2. Due to the Trigger blanking clock (t_{TRIG_BLANK}) the Trigger's high signal does not affect the DRV signal until the $t_{TRIGBLANK}$ timer has expired. At time t3 the Trigger/Disable signal is re evaluated and the DRV signal is turned off. The TRIG/DIS input is blanked for $t_{TRIGBLANK}$ after DRV set signal to avoid undesirable behavior during SR MOSFET turn−on event. The blanking time in combination with high threshold voltage (V_{TRIG_TH}) prevent triggering on ringing and spikes that are present on the TRIG/DIS input pin during the SR MOSFET turn−on process. Controller's response to the narrow pulse on the Trigger/Disable pin is depicted in Figure 53 − this short trigger pulse enables to turn the DRV on for t_{TRIG_BLANK}. Note that this case is valid only if device not entered disable mode before.

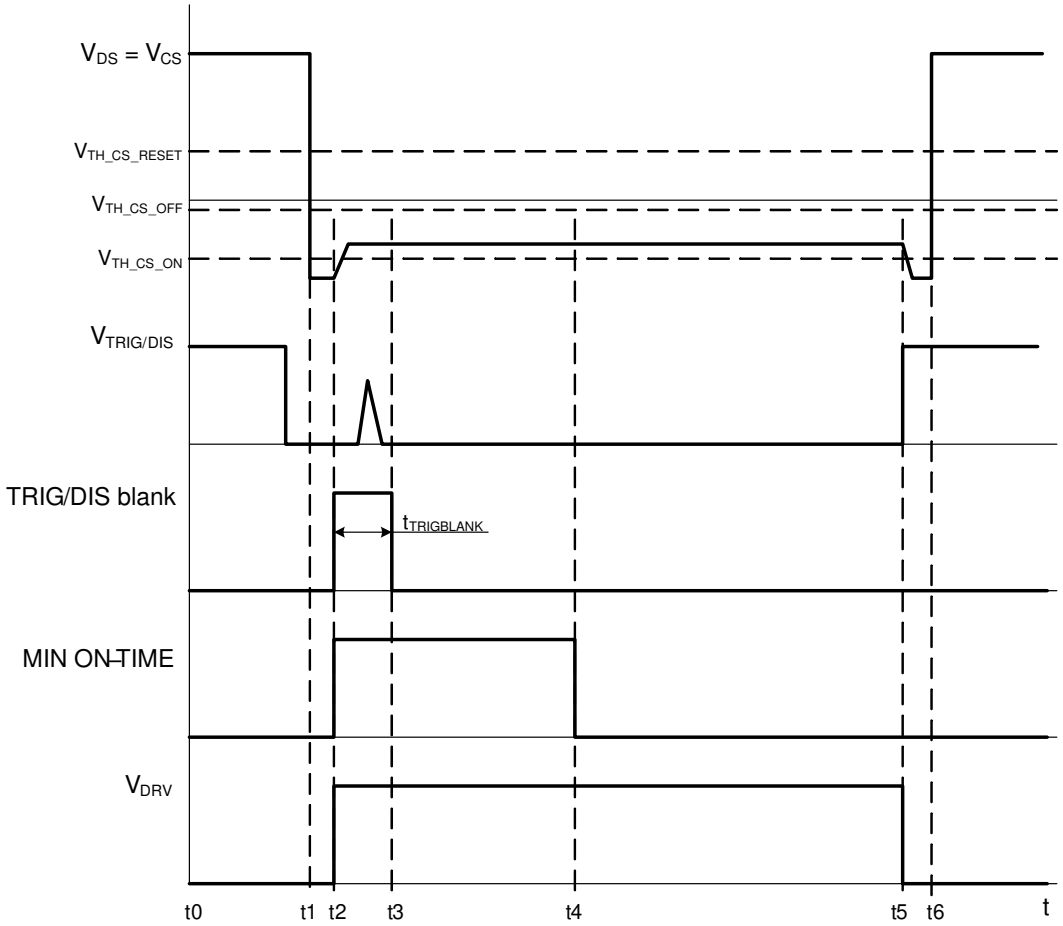


Figure 54. Trigger Input Functionality Waveforms – Trigger Blanking Acts Like a Filter

Figure 54 above shows almost the same situation as in Figure 53 with one main exception; the TRIG/DIS signal was not high after trigger blanking timer expired so the DRV signal remains high. The advantage of the trigger blanking time during DRV turn−on is evident from Figure 54 since it acts like a filter on the Trigger/Disable pin. Rising edge of the DRV signal may cause spikes on the trigger input. If it wasn't for the TRIG/DIS blanking these spikes, in combination with ultra−fast performance of the trigger logic, could turn the SR MOSFET off in an inappropriate time.

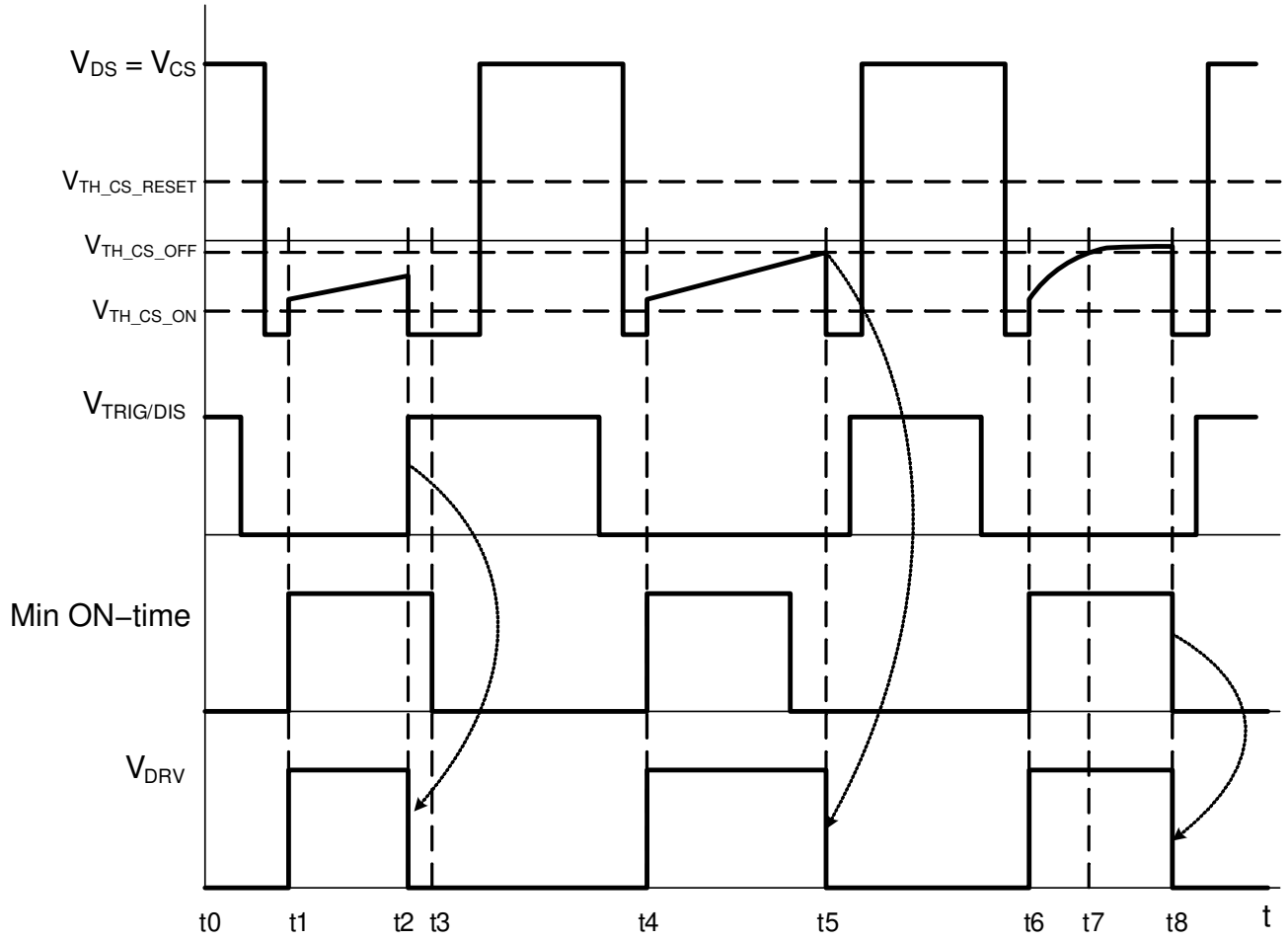


Figure 55. Trigger Input Functionality Waveforms – Trigger Over Ride, CS Turn Off and Min On−time

Figure 55 depicts all possible driver turn−off events in details when correct V_{CC} is applied. Controller driver is disabled based on trigger input signal in time t2; the trigger input overrides the minimum on−time period.

Driver is turned−off according to the CS (V_{DS}) signal (t5 marker) and when minimum on−time period elapsed already. TRIG/DIS signal needs to be LOW during this event.

If the CS (V_{DS}) voltage reaches $V_{TH\_CS\_OFF}$ threshold before minimum on−time period ends (t7) and the Trigger/Disable pin is low the DRV is turned−off on the falling edge of the minimum on−time period (t8 time marker in Figure 55). This demonstrates the fact that the Trigger over rides the minimum on−time. Minimum on−time has higher priority than the CS signal.

In Figure 56 the trigger input is low the whole time and the DRV pulses are purely a function of the CS signal and the minimum on−time. The first DRV pulse terminated based on the CS signal and another two DRV pulses are prolonged till the minimum on−time period end despite the CS signal crosses the $V_{TH\_CS\_OFF}$ threshold earlier.

If a minimum on−time is too long the situation that occurs after time marker t6 Figure 56 can occur, is not correct and should be avoided. The minimum t_{ON} period should be selected shorter to overcome situation that the SR MOSFET is turned−on for too long time. The secondary current then changes direction and energy flows back to the transformer that result in reduced application efficiency and also in excessive ringing on the primary and secondary MOSFETs.